

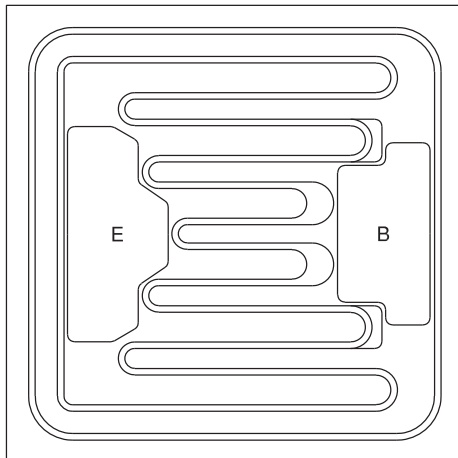
**PROCESS CP305**  
**Small Signal Transistor**  
NPN - High Current Transistor Chip



**PROCESS DETAILS**

Process	EPITAXIAL PLANAR
Die Size	31 x 31 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	5.9 x 11.8 MILS
Emitter Bonding Pad Area	6.5 x 13.8 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

**GEOMETRY**



BACKSIDE COLLECTOR R2

**GROSS DIE PER 4 INCH WAFER**

11,212

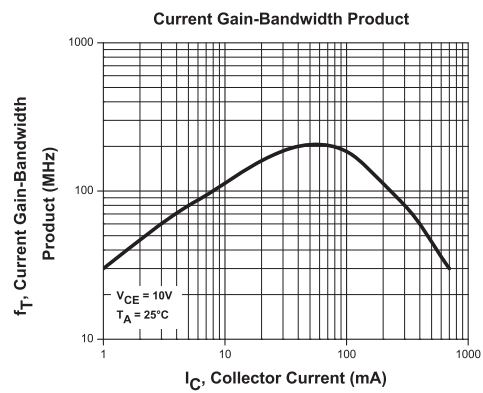
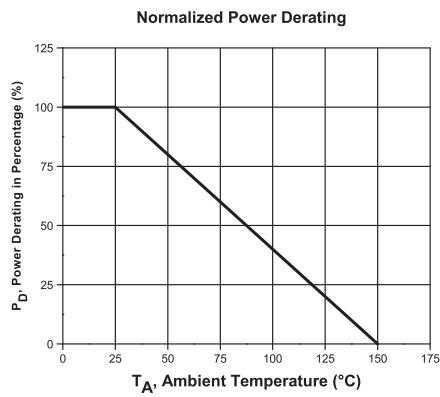
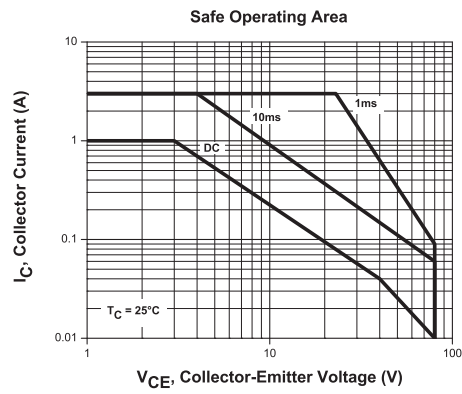
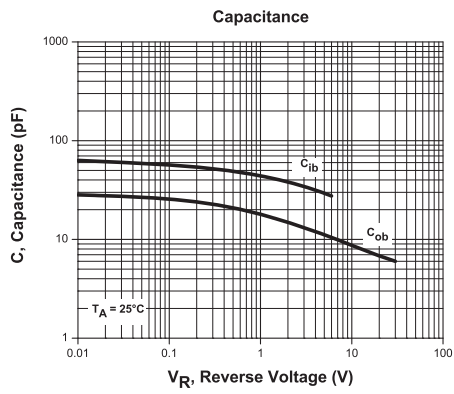
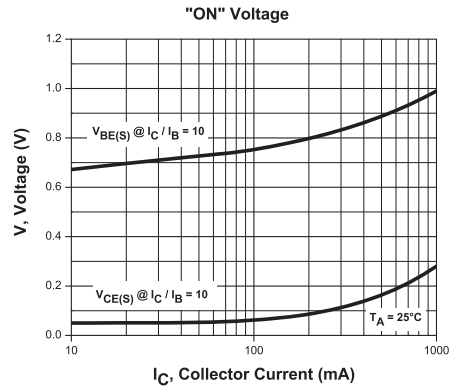
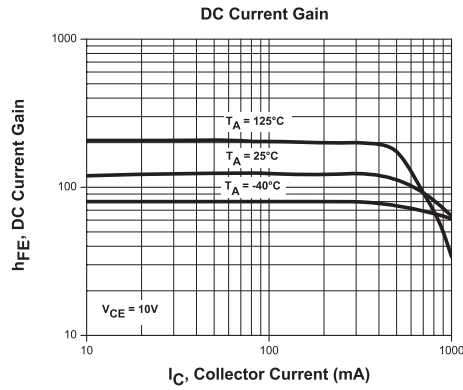
**PRINCIPAL DEVICE TYPES**

2N3019  
CMPT3019  
CXT3019  
CZT3019

R3 (22-March 2010)

# PROCESS CP305

## Typical Electrical Characteristics



R3 (22-March 2010)