

2.5 V or 3.3 V, 200 MHz, 11 Output Zero Delay Buffer

Features

■ Output frequency range: 16.67 MHz to 200 MHz

■ Input frequency range: 16.67 MHz to 200 MHz

■ 2.5 V or 3.3 V operation

■ Split 2.5 V and 3.3 V outputs

■ ±2% maximum output duty cycle variation

■ 11 clock outputs: drive up to 22 clock lines

■ LVCMOS reference clock input

■ 125 ps maximum output-output skew

■ PLL bypass mode

■ Spread Aware[™]

■ Output enable and disable

■ Pin compatible with MPC9352 and MPC952

■ Industrial temperature range: -40 °C to +85 °C

■ 32-pin 1.4 mm TQFP package

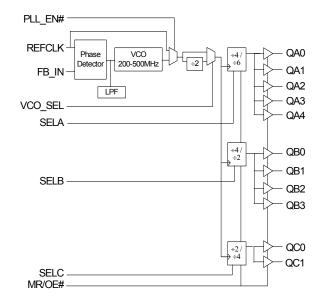
Description

The CY29352 is a low voltage high performance 200 MHz PLL based zero delay buffer designed for high speed clock distribution applications.

The CY29352 features an LVCMOS reference clock input and provides 11 outputs partitioned in three banks of five, four, and two outputs. Bank A divides the VCO output by four and six while bank B divides by four and two, and bank C divides by two and four per SEL(A:C) settings, see Table 3 on page 3. These dividers allow output to input ratios of 3:1, 2:1, 3:2, 1:1, 2:3, 1:2, and 1:3. Each LVCMOS compatible output drives 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output drives one or two traces, giving the device an effective fanout of 1:22.

The PLL is stable if the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies from 16.67 MHz to 200 MHz. For normal operation, the external feedback input, FB_IN, is connected to one of the outputs. The internal VCO runs at multiples of the input reference clock set by the feedback divider, see Table 2 on page 3. When PLL_EN# is HIGH, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

Block Diagram





Pinouts

Figure 1. Pin Diagram - 32-pin 1.4 mm TQFP package

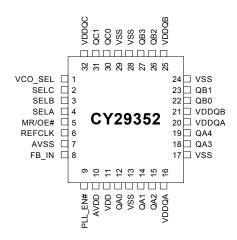


Table 1. Pin Definition - 32-pin 1.4 mm TQFP package

Pin	Name	IO ^[1]	Туре	Description	
6	REFCLK	I, PD	LVCMOS	Reference clock input	
12, 14, 15, 18, 19	QA(0:4)	0	LVCMOS	Clock output bank A	
22, 23, 26, 27	QB(0:3)	0	LVCMOS	Clock output bank B	
30, 31	QC(0,1)	0	LVCMOS	Clock output bank C	
8	FB_IN	I, PD	LVCMOS	Feedback clock input. Connect to an output for normal operation input must be at the same voltage rail as input reference clock, s Table 2 on page 3.	
1	VCO_SEL	I, PD	LVCMOS	VCO divider select input, see Table 3 on page 3.	
5	MR/OE#	I, PD	LVCMOS	Master reset or output enable and disable input, see Table 3 on page 3.	
9	PLL_EN#	I, PD	LVCMOS	PLL enable and disable input, see Table 3 on page 3.	
2, 3, 4	SEL(A:C)	I, PD	LVCMOS	Frequency select input, bank (A:C), see Table 3 on page 3.	
16, 20	V_{DDQA}	Supply	V_{DD}	2.5 V or 3.3 V power supply for bank A output clocks [2,3]	
21, 25	V_{DDQB}	Supply	V_{DD}	2.5 V or 3.3 V power supply for bank B output clocks [2,3]	
32	V_{DDQC}	Supply	V_{DD}	2.5 V or 3.3 V power supply for bank C output clocks [2,3]	
10	AV_{DD}	Supply	V_{DD}	2.5 V or 3.3 V power supply for PLL [2,3]	
11	V_{DD}	Supply	V_{DD}	2.5 V or 3.3 V power supply for core and inputs [2,3]	
7	AV _{SS}	Supply	Ground	Analog ground	
13, 17, 24, 28, 29	V_{SS}	Supply	Ground	Common ground	

Notes

- 1. PD = Internal pull down.
- 2. A 0.1-μF bypass capacitor must be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins, the high frequency filtering characteristics are cancelled by the lead inductance of the traces.</p>
- 3. AV_{DD} and V_{DD} pins must be connected to a power supply level that is at least equal or higher than that of V_{DDQA} , V_{DDQB} , and V_{DDQC} power supply pins.



Table 2. Frequency Table

VCO_SEL	Feedback Output Divider	vco	Input Frequency Range (AVDD = 3.3 V)	Input Frequency Range (AVDD = 2.5 V)
0	÷2	Input clock * 2	100 MHz to 200 MHz	100 MHz to 200 MHz
0	÷4	Input clock * 4	50 MHz to 125 MHz	50 MHz to 100 MHz
0	÷6	Input clock * 6	33.33 MHz to 83.33 MHz	33.33 MHz to 66.67 MHz
1	÷2	Input clock * 4	50 MHz to 125 MHz	50 MHz to 100 MHz
1	÷4	Input clock * 8	25 MHz to 62.5 MHz	25 MHz to 50 MHz
1	÷6	Input clock * 12	16.67 MHz to 41.67 MHz	16.67 MHz to 33.33 MHz

Table 3. Function Table

Control	Default	0	1
VCO_SEL	0	VCO	VCO ÷ 2
PLL_EN#	0	PLL enabled, the VCO output connects to the output dividers	Bypass mode, PLL disabled, the input clock connects to the output dividers
MR/OE#	0	Outputs enabled	Outputs disabled (three-state), VCO runs at its minimum frequency
SELA	0	QA = VCO ÷ 4	QA = VCO ÷ 6
SELB	0	QB = VCO ÷ 4	QB = VCO ÷ 2
SELC	0	QC = VCO ÷ 2	QC = VCO ÷ 4

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	DC supply voltage		-0.3	5.5	V
V_{DD}	DC operating voltage	Functional	2.375	3.465	V
V _{IN}	DC input voltage	Relative to V _{SS}	-0.3	V _{DD} + 0.3	V
V _{OUT}	DC output voltage	Relative to V _{SS}	-0.3	V _{DD} + 0.3	V
V _{TT}	Output termination voltage		_	$V_{DD} \div 2$	V
LU	Latch up immunity	Functional	200	-	mA
R _{PS}	Power supply ripple	Ripple frequency < 100 kHz	_	150	mVp-p
T _S	Temperature, storage	Non functional	-65	+150	°C
T _A	Temperature, operating ambient	Functional	-40	+85	°C
TJ	Temperature, junction	Functional	_	155	°C
\emptyset_{JC}	Dissipation, junction to case	Functional	_	42	°C/W
Ø _{JA}	Dissipation, junction to ambient	Functional	_	105	°C/W
ESD _H	ESD protection (human body model)		2000	_	Volts
FIT	Failure in time	Manufacturing test		10	ppm

Document Number: 38-07476 Rev. *C Page 3 of 10



DC Parameters

 $(V_{DD} = 2.5 \text{ V} \pm 5\%, T_{A} = -40 \text{ °C to } +85 \text{ °C})$

Parameter	Description	Condition	Min	Тур	Max	Unit
V _{IL}	Input voltage, low	LVCMOS	-	-	0.7	V
V _{IH}	Input voltage, high	LVCMOS	1.7	-	V _{DD} + 0.3	V
V _{OL}	Output voltage, low ^[4]	I _{OL} = 15 mA		-	0.6	V
V _{OH}	Output voltage, high ^[4]	I _{OH} = –15 mA	1.8	-		V
I _{IL}	Input current, low	V _{IL} = V _{SS}	-	-	-10	μА
I _{IH}	Input current, high ^[5]	$V_{IL} = V_{DD}$	_	_	100	μА
I _{DDA}	PLL supply current	AV _{DD} only	_	5	10	mA
I_{DDQ}	Quiescent supply current	All V _{DD} pins except AV _{DD}	_	3	5	mA
I _{DD}	Dynamic supply current		-	170		mA
C _{IN}	Input pin capacitance		-	4		pF
Z _{OUT}	Output impedance		-	17–20		Ω

DC Parameters

(V_{DD} = 3.3 V \pm 5%, T_A = -40 °C to +85 °C)

Parameter	Description	Condition	Min	Тур	Max	Unit
V_{IL}	Input voltage, low	LVCMOS	_	_	0.8	V
V _{IH}	Input voltage, high	LVCMOS	2.0	_	V _{DD} + 0.3	V
V_{OL}	Output voltage, low ^[4]	I _{OL} = 24 mA	_	_	0.55	V
		I _{OL} = 12 mA	_	_	0.30	
V _{OH}	Output voltage, high ^[4]	I _{OH} = -24 mA	2.4	_	_	V
I _{IL}	Input current, low	$V_{IL} = V_{SS}$	-	_	-10	μΑ
I _{IH}	Input current, high ^[5]	$V_{IL} = V_{DD}$	_	_	100	μА
I _{DDA}	PLL supply current	AV _{DD} only	_	5	10	mA
V _{IL}	Input voltage, low	LVCMOS	_	_	0.8	V
V _{IH}	Input voltage, high	LVCMOS	2.0	_	V _{DD} + 0.3	V
V _{OL}	Output voltage, low ^[4]	I _{OL} = 24 mA	_	_	0.55	V
		I _{OL} = 12 mA	-	_	0.30	
V _{OH}	Output voltage, high ^[4]	I _{OH} = -24 mA	2.4	_	-	V
I _{IL}	Input current, low	V _{IL} = V _{SS}	_	_	-10	μА
I _{IH}	Input current, high ^[5]	V _{IL} = V _{DD}	_	_	100	μА
I _{DDA}	PLL supply current	AV _{DD} only	_	5	10	mA
I _{DDQ}	Quiescent supply current	All V _{DD} pins except AV _{DD}	_	3	5	mA
I _{DD}	Dynamic supply current		_	240	_	mA
C _{IN}	Input pin capacitance		_	4	_	pF
Z _{OUT}	Output impedance		_	14–17	_	Ω

Notes

Document Number: 38-07476 Rev. *C Page 4 of 10

Driving one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, each output drives up to two 50 Ω series terminated transmission lines.

^{5.} Inputs have pull down resistors that affect the input current.



AC Parameters

 $(V_{DD} = 2.5 \text{ V} \pm 5\%, T_A = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C})$

Parameter ^[6]	Description	Condition	Min	Тур	Max	Unit
f _{VCO}	VCO frequency		200	_	400	MHz
f _{in}	Input frequency	÷2 feedback	100	-	200	MHz
		÷4 feedback	50	ı	100	
		÷6 feedback	33.33	ı	66.67	
		÷8 feedback	25	_	50	
		÷12 feedback	16.67	_	33.33	
		Bypass mode (PLL_EN# = 1)	0	_	200	
f _{refDC}	Input duty cycle		25	_	75	%
t _r , t _f	TCLK input rise and fall time	0.7 V to 1.7 V	_	_	1.0	ns
f _{MAX}	Maximum output frequency	÷2 output	100	_	200	MHz
		÷4 output	50	_	100	
		÷6 output	33.33	_	66.67	
		÷8 output	25	-	50	
		÷12 output	16.67	_	33.33	
DC	Output duty cycle	f _{MAX} < 100 MHz	47	-	53	%
		f _{MAX} > 100 MHz	44	ı	56	
t _r , t _f	Output rise and fall times	0.6 V to 1.8 V	0.1	ı	1.0	ns
t _(\$\phi\$)	Propagation delay (static phase offset)	TCLK to FB_IN, same V _{DD} , does not include jitter	-100	-	100	ps
t _{sk(O)}	Output to output skew	Skew within bank	-	-	125	ps
t _{sk(B)}	Bank to bank skew	Banks at same voltage, same frequency	-	ı	175	ps
		Banks at same voltage, different frequency	-	ı	225	
t _{PLZ, HZ}	Output disable time		-	ı	8	ns
t _{PZL, ZH}	Output enable time		-	-	10	ns
BW	PLL closed loop bandwidth (-3 dB)	÷2 feedback	-	2	_	MHz
		÷4 feedback	-	1–1.5	_	
		÷6 feedback	-	0.6	_	
		÷8 feedback	_	0.75	_	
		÷12 feedback	-	0.5	_	
t _{JIT(CC)}	Cycle to cycle jitter	Same frequency	-	-	100	ps
		Multiple frequencies	_	1	300	
t _{JIT(PER)}	Period jitter	Same frequency	_	-	100	ps
		Multiple frequencies	_	-	150	
$t_{JIT(\phi)}$	IO phase jitter	VCO < 300 MHz	_	150	_	ps
		VCO > 300 MHz	_	100	_	
t _{LOCK}	Maximum PLL lock time		-	-	1	ms

Document Number: 38-07476 Rev. *C Page 5 of 10

Note
 6. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}. Outputs are at the same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.



AC Parameters

 $(V_{DD} = 3.3 \text{ V} \pm 5\%, T_A = -40 ^{\circ}\text{C to} +85 ^{\circ}\text{C})$

Description	Condition	Min	Тур	Max	Unit
VCO frequency		200	_	500	MHz
Input frequency	÷2 feedback	100	_	200	MHz
	÷4 feedback	50	_	125	
	÷6 feedback	33.33	_	83.33	
	÷8 feedback	25	_	62.5	
	÷12 feedback	16.67	_	41.67	
	Bypass mode (PLL_EN# = 1)	0	_	200	
Input duty cycle		25	_	75	%
TCLK input rise and fall time	0.8 V to 2.0 V	_	_	1.0	ns
Maximum output frequency	÷2 output	100	_	200	MHz
	÷4 output	50	_	125	
	÷6 output	33.33	_	83.33	
	÷8 output	25	_	62.5	
	÷12 output	16.67	-	41.67	
Output duty cycle	f _{MAX} < 100 MHz	48	_	52	%
		_	_	-	
Propagation delay (static phase offset)	TCLK to FB_IN, same V _{DD} , does not include jitter	-100	-	200	ps
Output to output skew	Skew within each Bank	_	_	125	ps
Bank to bank skew	Banks at same voltage, same frequency	_	_	175	ps
	Banks at same voltage, different frequency	_	_	235	
	Banks at different voltage	_	_	425	
Output disable time		_	_	8	ns
Output enable time		_	_	10	ns
PLL closed loop bandwidth	÷2 feedback	_	2	_	MHz
(–3 dB)	÷4 feedback	_	1–1.5	_	
	÷6 feedback	_	0.6	ı	
	÷8 feedback	_	0.75	ı	
	÷12 feedback	_	0.5	-	
Cycle to cycle jitter	Same frequency	_	_	100	ps
	Multiple frequencies	_	_	275	
Period jitter	Same frequency	_	_	100	ps
	Multiple frequencies	_	_	150	1
IO phase jitter	VCO < 300 MHz	_	150	-	ps
	VCO > 300 MHz	_	100	-	1
Maximum PLL lock time		_	_	1	ms
	Input frequency Input frequency Input duty cycle TCLK input rise and fall time Maximum output frequency Output duty cycle Propagation delay (static phase offset) Output to output skew Bank to bank skew Output disable time Output enable time PLL closed loop bandwidth (-3 dB) Cycle to cycle jitter Period jitter IO phase jitter	Input frequency +2 feedback +4 feedback +6 feedback +8 feedback +8 feedback +12 fe	VCO frequency	VCO frequency	VCO frequency 200 - 500

Document Number: 38-07476 Rev. *C Page 6 of 10

Note
 7. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}. Outputs are at the same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.



Figure 2. AC Test Reference for V_{DD} = 3.3 V / 2.5 V

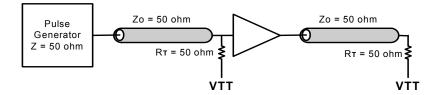


Figure 3. Propagation Delay $t(\phi)$, Static Phase Offset

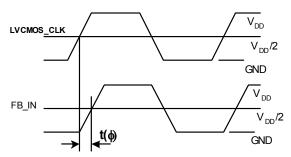


Figure 4. Output Duty Cycle (DC)

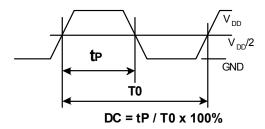
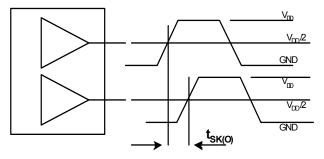


Figure 5. Output to Output Skew, $t_{\rm sk(O)}$

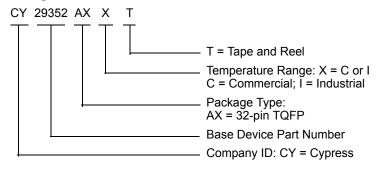




Ordering Information

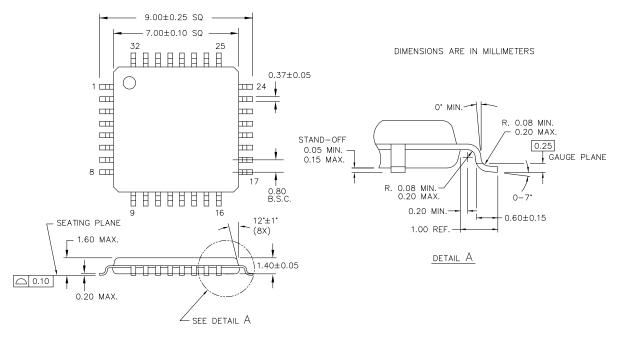
Part Number	Package Type	Product Flow
Pb-free		
CY29352AXI	32-pin TQFP	Industrial, –40 °C to +85 °C
CY29352AXIT	32-pin TQFP—tape and reel	Industrial, –40 °C to 85 °C

Ordering Code Definitions



Package Drawing and Dimension

Figure 6. 32-pin Thin Plastic Quad Flatpack 7 × 7 × 1.4 mm



51-85088 *C



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
ESD	electrostatic discharge
I/O	Input/Output
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor-Transistor Logic
PLL	phase locked loop
TQFP	thin quad flat pack
VCO	voltage-controlled oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure			
°C	degree Celsius			
Hz	Hertz			
kHz	kilo Hertz			
MHz	Mega Hertz			
μA	micro Amperes			
mA	milli Amperes			
ms	milli seconds			
ns	nano seconds			
Ω	ohms			
%	percent			
pF	pico Farads			
ppm	parts per million			
ps	pico seconds			
kV	kilo Volts			
mV	milli Volts			
V	Volts			
W	Watts			



Document History Page

	Document Title:CY29352 2.5 V or 3.3 V, 200 MHz, 11 Output Zero Delay Buffer Document Number: 38-07476					
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change		
**	124654	03/21/03	RGL	New Data Sheet		
*A	739798	See ECN	RGL	Removed the leaded parts and replaced by lead-free parts		
*B	1923227	See ECN		Corrected package thickness from 1.0 mm to 1.4 mm in Features section on page 1 and in Figure 5.		
*C	3163592	02/05/2011	CXQ	Added Ordering Code Definitions. Updated Package Drawing and Dimension. Added Acronyms and Units of Measure. Updated in new template.		

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

cypress.com/go/plc

Products

Automotive cypress.com/go/automotive Clocks & Buffers cypress.com/go/clocks Interface cypress.com/go/interface cypress.com/go/interface cypress.com/go/powerpsoc

Memory cypress.com/go/memory
Optical & Image Sensing cypress.com/go/image
PSoC cypress.com/go/psoc
Touch Sensing cypress.com/go/touch
USB Controllers cypress.com/go/USB
Wireless/RF cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2003-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document Number: 38-07476 Rev. *C Revised February 5, 2011 Page 10 of 10

Spread Aware is a trademark of Cypress Semiconductor Corporation. All products and company names mentioned in this document may be the trademarks of their respective holders.