

CY62167E MoBL[®]

16-Mbit (1 M × 16 / 2 M × 8) Static RAM

Features

- Configurable as 1 M × 16 or as 2 M × 8 SRAM
- Very high speed: 45 ns
- Wide voltage range: 4.5 V to 5.5 V
- Ultra low standby power Typical standby current: 1.5 µA Maximum standby current: 12 µA
- Ultra low active power Typical active current: 2.2 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Offered in 48-pin TSOP I package

Functional Description^[1]

The CY62167E is a high performance CMOS static RAM organized as 1 M words by 16-bits/2 M words by 8-bits. This device features advanced circuit design to provide an ultra low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power down feature that

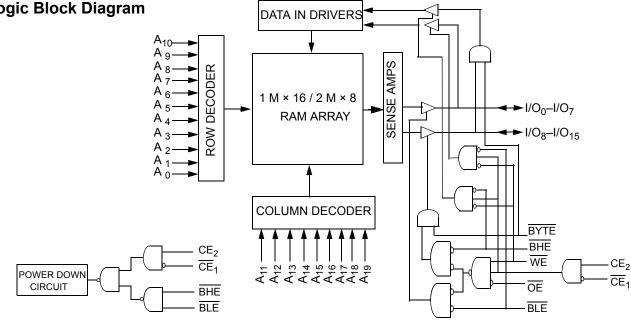
Logic Block Diagram

reduces power consumption by 99% when addresses are not toggling. Place the device into standby mode when deselected $(\overline{CE}_1 \text{ HIGH}, \text{ or } CE_2 \text{ LOW}, \text{ or both } \overline{\text{BHE}} \text{ and } \overline{\text{BLE}} \text{ are } \text{HIGH})$. The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when:

- The device is deselected (\overline{CE}_1 HIGH or CE_2 LOW)
- Outputs are disabled (OE HIGH)
- Both byte high enable and byte low enable are disabled (BHE. BLE HIGH) or
- A write operation is in progress (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW)

To write to the device, take chip enables (CE₁ LOW and CE₂ HIGH) and write enable (WE) input LOW. If byte low enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A0 through A_{19}). If byte high enable (BHE) is LOW, then data from the I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take chip enables (\overline{CE}_1 LOW and CE_2) HIGH) and output enable (OE) LOW while forcing the write enable (WE) HIGH. If byte low enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If byte high enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the "Truth Table" on page 11 for a complete description of read and write modes.



Note

1. For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

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San Jose, CA 95134-1709 408-943-2600 Revised August 16, 2010



CY62167E MoBL[®]

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Pin Configuration^[2, 3]

48-Pin TSOP I Top View

| A15 - 1 | |
|----------------------------------|-------------------|
| A15 🗖 1 | 48 🗖 <u>A16</u> |
| A14 🖬 2 A13 🖬 3 | 47 BYTE 46 Vss |
| | 46 🗖 Vss |
| A12 🗖 4 | 45 🗖 I/O15/A20 |
| A11 🗖 5 | 44 🗖 1/07 |
| A10 🖬 6 | 43 🗖 I/O14 |
| A9 🗖 7 | 42 🗖 1/06 |
| A8 🖬 8 | 41 🗖 1/013 |
| A19 🗖 9 | 40 🗖 1/05 |
| NC 🖬 10 | 39 🗖 I/O12 |
| $\overline{WE} = 11$ $CE_2 = 12$ | 38 🗖 1/04 |
| CE ₂ = 12 | 37 🗖 Vcc |
| NC 🖬 13 | 36 🗖 I/O11 |
| BHE 🗖 14 | 35 🗖 1/03 |
| BLE 🗖 15 | 34 🗖 1/010 |
| A18 🗖 16 | 33 🗖 1/02 |
| A17 🗖 17 | 32 🗖 1/09 |
| A7 🗖 18 | 31 🗖 I/O1 |
| A6 🗖 19 | 30 🗖 1/08 |
| A5 🗖 20 | 29 🗖 1/00 |
| A4 🗖 21 | 28 🗖 OE |
| A3 🗖 22 | 27 🗖 <u>Vss</u> |
| A2 🗖 23 | 26 🗖 CE1 |
| A1 🗖 24 | 25 🗖 A0 |
| | |

Product Portfolio

| | | | | | Power Dissipation | | | | | |
|------------|-----|---------------------------|-----|--|--------------------------------|-----|---------------------------------|-----|---------------------------|-----|
| Product | V | _{CC} Range (| V) | (ns) Operating I _{CC} (mA) Standby Ia | | I | | | | |
| | | | | . , | f = 1 MHz f = f _{max} | | — Standby I _{SB2} (μA) | | | |
| | Min | Typ ^[4] | Мах | | Typ ^[4] | Мах | Typ ^[4] | Max | Typ ^[4] | Мах |
| CY62167ELL | 4.5 | 5.0 | 5.5 | 45 | 2.2 | 4.0 | 25 | 30 | 1.5 | 12 |

Notes

- NC pins are not connected on the die.
 NC pins are not connected on the die.
 The BYTE pin in the 48-TSOPI package must be tied to V_{CC} to use the device as a 1 M × 16 SRAM. The 48-TSOPI package can also be used as a 2 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, pin 45 is A20, while BHE, BLE and I/O₈ to I/O₁₄ pins are not used.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ), T_A = 25 °C.



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

| Storage temperature | –65 °C to +150 °C |
|---|-------------------|
| Ambient temperature with power applied | –55 °C to +125 °C |
| Supply voltage to ground potential | –0.5 V to 6.0 V |
| DC voltage applied to outputs in high Z state ^[5, 6] | –0.5 V to 6.0 V |

Electrical Characteristics

Over the Operating Range

| DC input voltage ^[5, 6] | –0.5 V to 6.0 V |
|--|-----------------|
| Output current into outputs (LOW) | 20 mA |
| Static discharge voltage (MIL-STD-883, method 3015) | >2001 V |
| Latch-up current | >200 mA |

Operating Range

| Device | Range | Ambient Temperature | V _{CC} ^[7] |
|------------|------------|------------------------|---------------------------------------|
| CY62167ELL | Industrial | –40 °C to +85 °C | 4.5 V to 5.5 V |

| Deremeter | Description | Test Conditions | | | Unit | | |
|----------------------------------|---|----------------------------------|--|------|---------------------------|-------------------------|------|
| Parameter | Description | lest | | | Typ ^[9] | Max | Unit |
| V _{OH} | Output HIGH voltage | I _{OH} = -1.0 mA | | 2.4 | - | - | V |
| V _{OL} | Output LOW voltage | I _{OL} = 2.1 mA | | _ | - | 0.4 | V |
| V _{IH} | Input HIGH voltage | $V_{\rm CC}$ = 4.5 V to 5.5 V | V _{CC} = 4.5 V to 5.5 V | | - | V _{CC} + 0.5 V | V |
| V _{IL} | Input LOW voltage | V _{CC} = 4.5 V to 5.5 V | | -0.5 | - | 0.7 ^[8] | V |
| I _{IX} | Input leakage current | $GND \le V_I \le V_{CC}$ | | -1 | - | +1 | μA |
| I _{OZ} | Output leakage current | $GND \leq V_O \leq V_{CC}, c$ | $\text{GND} \leq \text{V}_{\text{O}} \leq \text{V}_{\text{CC}}$, output disabled | | - | +1 | μA |
| I _{CC} | V _{CC} operating supply | $f = f_{MAX} = 1/t_{RC}$ | $V_{CC} = V_{CC}(max)$ | - | 25 | 30 | mA |
| | current | f = 1 MHz | I _{OUT} = 0 mA CMOS levels | - | 2.2 | 4.0 | mA |
| I _{SB2} ^[10] | Automatic power down current—CMOS inputs | | or $CE_2 \le 0.2 \text{ V}$, or \overline{BHE} 2 V, $V_{IN} \ge V_{CC} - 0.2 \text{ V}$ or $V_{CC} = V_{CC}(max)$ | - | 1.5 | 12 | μA |

Capacitance

| Parameter ^[11] | Description | Test Conditions | Мах | Unit |
|---------------------------|--------------------|---|-----|------|
| C _{IN} | Input capacitance | $T_{A} = 25 ^{\circ}C, f = 1 \text{MHz},$ | 10 | pF |
| C _{OUT} | Output capacitance | $V_{CC} = V_{CC}(typ)$ | 10 | pF |

Thermal Resistance

| Parameter ^[11] | Description | Test Conditions | TSOP I | Unit |
|---------------------------|---|--|--------|------|
| Θ_{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 60 | °C/W |
| ΘJC | Thermal resistance (junction to case) | | 4.3 | °C/W |

Notes

5. $V_{IL}(min) = -2.0 V$ for pulse durations less than 20 ns.

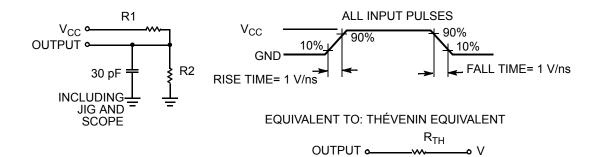
V_{IL}(mm) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
 V_{IL}(mmax) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
 Full Device AC operation is based on a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
 Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions input LOW voltage applied to the device must not be higher than 0.7 V.

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ), T_A = 25 °C

10. Chip enables (\overline{CE}_1 and \overline{CE}_2), byte enables (\overline{BHE} and \overline{BLE}) and \overline{BYTE} need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating. 11. Tested initially and after any design or process changes that may affect these parameters.



AC Test Loads and Waveforms



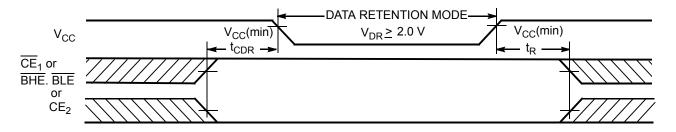
| Parameters | Values | Unit |
|-----------------|--------|------|
| R1 | 1800 | Ω |
| R2 | 990 | Ω |
| R _{TH} | 639 | Ω |
| V _{TH} | 1.77 | V |

Data Retention Characteristics

Over the operating range

| Parameter | Description | Conditions | Min | Typ ^[12] | Max | Unit |
|-----------------------------------|--------------------------------------|---|-----|----------------------------|-----|------|
| V _{DR} | V _{CC} for data retention | _ | 2.0 | - | - | V |
| I _{CCDR} ^[13] | Data retention current | $\begin{array}{l} V_{CC} = V_{\underline{DR}}, \overline{\mathbf{CE}}_1 \geq \underline{V_{CC}} - 0.2 \text{ V or } \mathbf{CE}_2 \leq \\ 0.2 \text{ V, or BHE and } \overline{BLE} \geq \underline{V_{CC}} - 0.2 \text{ V,} \\ \overline{V_{IN}} \geq \underline{V_{CC}} - 0.2 \text{ V or } \overline{V_{IN}} \leq 0.2 \text{ V} \end{array}$ | - | - | 12 | μA |
| t _{CDR} ^[14] | Chip deselect to data retention time | - | 0 | _ | _ | ns |
| t _R ^[15] | Operation recovery time | - | 45 | - | - | ns |

Data Retention Waveform^[16]



Notes

12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}(typ)$, $T_A = 25 \,^{\circ}C$. 13. Chip enables (CE_1 and CE_2), byte enables (BHE and BLE) and BYTE need to be tied to CMOS levels to meet the I_{SB2}/I_{CCDR} spec. Other inputs can be left floating. 14. Tested initially and after any design or process changes that may affect these parameters. 15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC}(min) \ge 100 \,\mu$ s.

- 16. BHE. BLE is the AND of BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling BHE and BLE.



Switching Characteristics

Over the Operating Range

| Parameter ^[17, 18] | Description | 45 | Unit | |
|-------------------------------|--|-----|------|------|
| Parameter | Description | Min | Мах | Unit |
| READ CYCLE | | | | |
| t _{RC} | Read cycle time | 45 | - | ns |
| t _{AA} | Address to data valid | - | 45 | ns |
| t _{OHA} | Data hold from address change | 10 | - | ns |
| t _{ACE} | \overline{CE}_1 LOW and CE_2 HIGH to data valid | - | 45 | ns |
| t _{DOE} | OE LOW to data valid | - | 22 | ns |
| t _{LZOE} | OE LOW to low Z ^[19] | 5 | _ | ns |
| t _{HZOE} | OE HIGH to high Z ^[19, 20] | - | 18 | ns |
| t _{LZCE} | \overline{CE}_1 LOW and CE_2 HIGH to low $Z^{[19]}$ | 10 | _ | ns |
| t _{HZCE} | CE ₁ HIGH and CE ₂ LOW to high Z ^[19, 20] | - | 18 | ns |
| t _{PU} | CE ₁ LOW and CE ₂ HIGH to power-up | 0 | _ | ns |
| t _{PD} | CE ₁ HIGH and CE ₂ LOW to power-down | _ | 45 | ns |
| t _{DBE} | BLE/BHE LOW to data valid | - | 45 | ns |
| t _{LZBE} | BLE/BHE LOW to low Z ^[19] | 10 | _ | ns |
| t _{HZBE} | BLE/BHE HIGH to high Z ^[19, 20] | _ | 18 | ns |
| | 1] | | • | • |
| t _{WC} | Write cycle time | 45 | _ | ns |
| t _{SCE} | \overline{CE}_1 LOW and CE_2 HIGH to write end | 35 | _ | ns |
| t _{AW} | Address setup to write end | 35 | _ | ns |
| t _{HA} | Address hold from write end | 0 | _ | ns |
| t _{SA} | Address setup to write start | 0 | _ | ns |
| t _{PWE} | WE pulse width | 35 | _ | ns |
| t _{BW} | BLE/BHE LOW to write end | 35 | - | ns |
| t _{SD} | Data setup to write end | 25 | _ | ns |
| t _{HD} | Data hold from write end | 0 | - | ns |
| t _{HZWE} | WE LOW to high Z ^[19, 20] | - | 18 | ns |
| t _{LZWE} | WE HIGH to low Z ^[19] | 10 | _ | ns |

Notes

Notes
17. Test conditions for all parameters other than tristate parameters assume signal transition time of 1 V/ns, timing reference levels of V_{CC}(typ)/2, input pulse levels of 0 to V_{CC}(typ), and output loading of the specified |_{QL}/I_{QH} as shown in "AC Test Loads and Waveforms" on page 5.
18. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note AN13842 for further clarification.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZE}. t_{HZBE} is less than t_{LZEE}, t_{HZCE} is less than t_{LZWE} for any device.
20. t_{HZOE}, t_{HZEE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
21. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, BHE or BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.



Switching Waveforms

Figure 1. Read Cycle No. 1 (address transition controlled [22, 23])

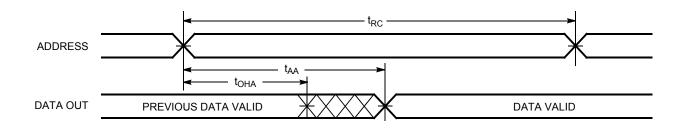
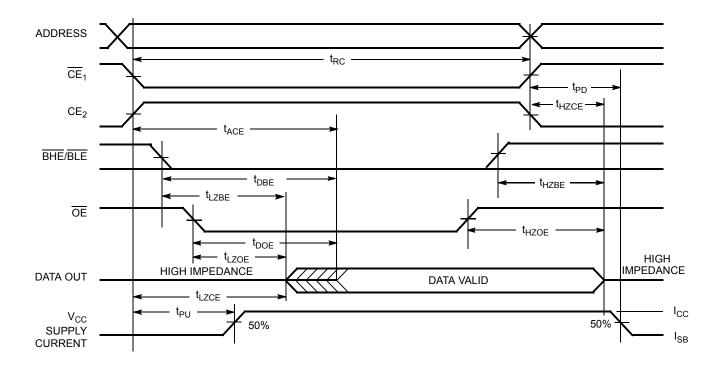


Figure 2. Read Cycle No. 2 (OE controlled ^[23, 24])



Notes

- 22. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$.

23. WE is HIGH for read cycle. 24. Address valid before or similar to \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.



Switching Waveforms (continued)

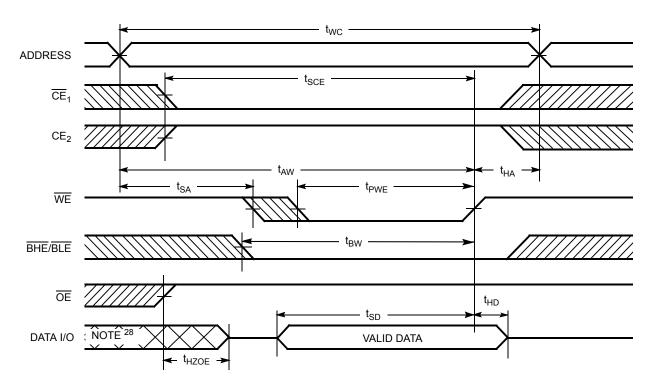


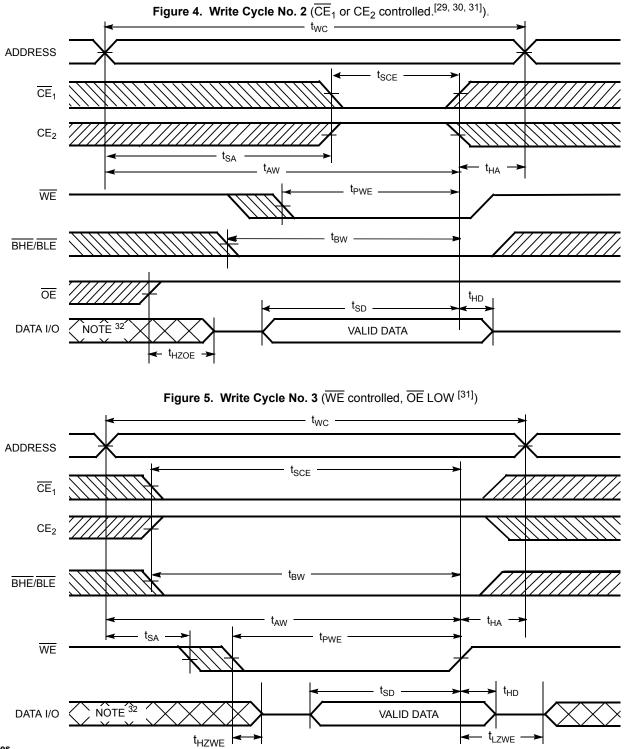
Figure 3. Write Cycle No. 1 (WE controlled ^[25, 26, 27])

Notes

- 25. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, BHE or BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 26. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 27. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{H}$, the output remains in a high impedance state.
- 28. During this period the I/Os are in output state and input signals must not be applied.



Switching Waveforms (continued)



29. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

30. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

31. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{H}$, the output remains in a high impedance state.

32. During this period the I/Os are in output state and input signals must not be applied.

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Switching Waveforms (continued)

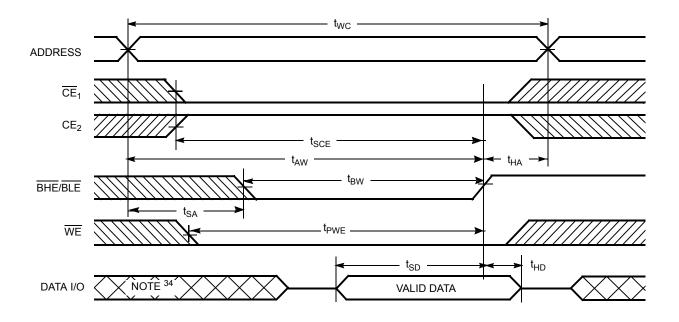


Figure 6. Write Cycle No. 4 (BHE/BLE controlled, OE LOW [33])

Notes_____33. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state. 34. During this period the I/Os are in output state and input signals must not be applied.



Truth Table

| CE ₁ | CE ₂ | WE | OE | BHE | BLE | Inputs Outputs | Mode | Power |
|-------------------|-------------------|----|----|-----|-----|--|---------------------|----------------------------|
| Н | X ^[35] | Х | Х | Х | Х | High Z | Deselect/power-down | Standby (I _{SB}) |
| X ^[35] | L | Х | Х | Х | Х | High Z | Deselect/power-down | Standby (I _{SB}) |
| X ^[35] | X ^[35] | Х | Х | Н | Н | High Z | Deselect/power-down | Standby (I _{SB}) |
| L | Н | Н | L | L | L | Data out (I/O ₀ –I/O ₁₅) | Read | Active (I _{CC}) |
| L | Н | Н | L | Н | L | Data out (I/O ₀ –I/O ₇); High Z (I/O ₈ –I/O ₁₅) | Read | Active (I _{CC}) |
| L | Н | Н | L | L | Н | High Z (I/O ₀ –I/O ₇); Data out (I/O ₈ –I/O ₁₅) | Read | Active (I _{CC}) |
| L | Н | Н | Н | L | Н | High Z | Output disabled | Active (I _{CC}) |
| L | Н | Н | Н | Н | L | High Z | Output disabled | Active (I _{CC}) |
| L | Н | Н | Н | L | L | High Z | Output disabled | Active (I _{CC}) |
| L | Н | L | Х | L | L | Data in (I/O ₀ –I/O ₁₅) | Write | Active (I _{CC}) |
| L | Н | L | Х | Н | L | Data in (I/O ₀ –I/O ₇); High Z (I/O ₈ –I/O ₁₅) | Write | Active (I _{CC}) |
| L | Н | L | Х | L | Н | High Z (I/O ₀ –I/O ₇); Data in (I/O ₈ –I/O ₁₅) | Write | Active (I _{CC}) |



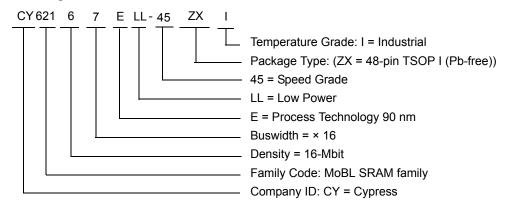
Ordering Information

Table 1 lists the CY62167ELL key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Key Features and Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---------------|------------------|--------------------|-------------------------|--------------------|
| 45 | CY62167ELL-45ZXI | 51-85183 | 48-pin TSOP I (Pb-free) | Industrial |

Ordering Code Definitions



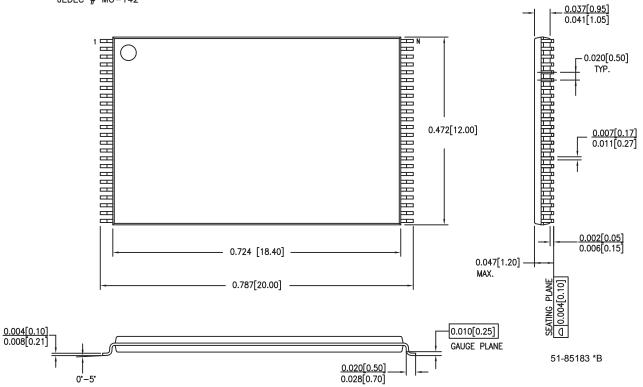


Package Diagram

Figure 7. 48-Pin TSOP I (12 mm × 18.4 mm × 1.0 mm), 51-85183

DIMENSIONS IN INCHES[MM] MIN. MAX.

JEDEC # MO-142





Acronyms

| Acronym | Description | | |
|---------|---|--|--|
| BHE | byte high enable | | |
| BLE | byte low enable | | |
| CMOS | complementary metal oxide semiconductor | | |
| CE | chip enable | | |
| I/O | input/output | | |
| ŌĒ | output enable | | |
| SRAM | static random access memory | | |
| TSOP | thin small outline package | | |
| VFBGA | very fine ball grid array | | |
| WE | write enable | | |

Document Conventions

Units of Measure

Table 2. Units of Measure

| Symbol | Unit of Measure | | | | |
|--------|-----------------|--|--|--|--|
| ns | nano seconds | | | | |
| V | volts | | | | |
| μA | micro amperes | | | | |
| mA | milli amperes | | | | |
| pF | pico Farad | | | | |
| °C | degree Celsius | | | | |
| W | watts | | | | |



PSoC Solutions

Document History Page

| | Document Title: CY62167E MoBL [®] 16-Mbit (1 M × 16 / 2 M × 8) Static RAM Document Number: 001-15607 | | | | |
|------|--|------------|--------------------|--|--|
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change | |
| ** | 1103145 | See ECN | VKN | New Data Sheet | |
| *A | 1138903 | See ECN | VKN | Converted from preliminary to final Changed I _{CC(max)} spec from 2.8 mA to 4.0 mA for f=1 MHz Changed I _{CC(typ)} spec from 22 mA to 25 mA for f=f _{max} Changed I _{CC(max)} spec from 25 mA to 30 mA for f=f _{max} Added footnote# 8 related to V _{IL} Changed I _{CCDR} spec from 10 μ A to 12 μ A Added footnote# 14 related to AC timing parameters | |
| *В | 2934385 | 06/03/10 | VKN | Included BHE, BLE in I _{SB2} , I _{CCDR} test conditions to reflect byte power down feature Added footnote #35 related to chip enable Updated package diagram Updated template | |

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