

PSRAM

2-Mbit (256K x 8)

Pseudo Static RAM

Features

- Advanced low-power architecture
- High speed: 55 ns, 70 ns
- Wide voltage range: 2.7V to 3.3V
- Typical active current: 1 mA @ f = 1 MHz
- Low standby power
- Automatic power-down when deselected

Functional Description

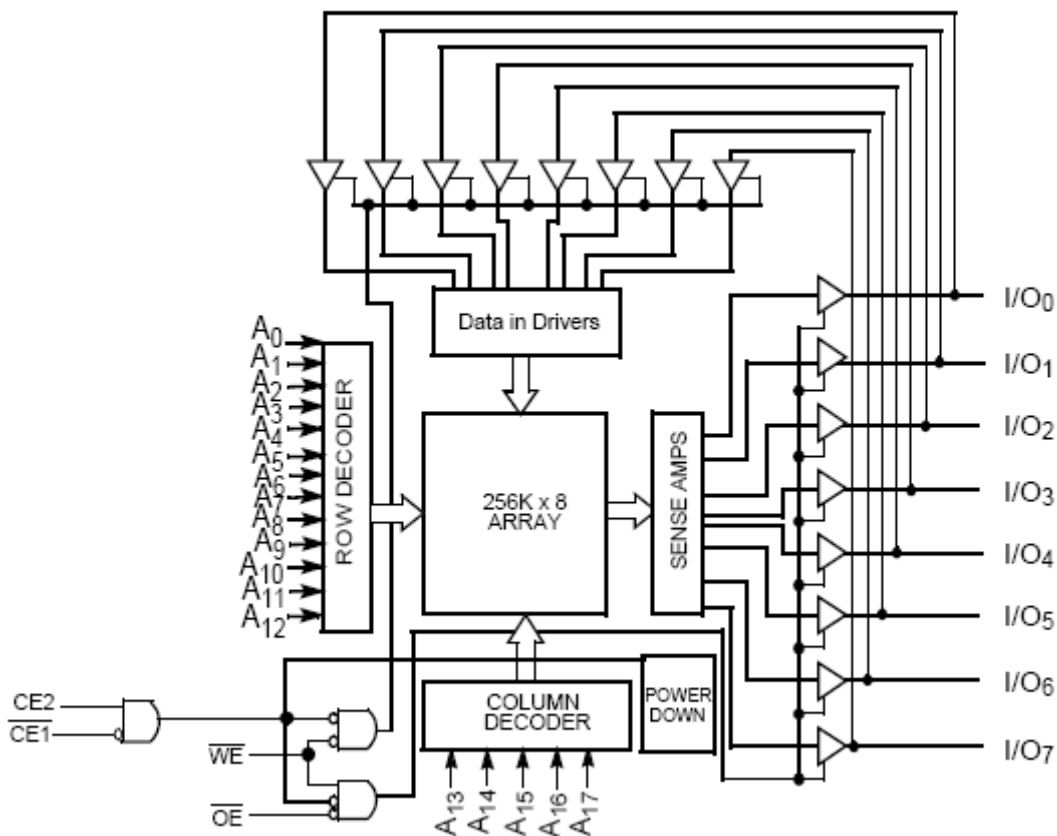
The M24L28256DA is a high-performance CMOS pseudo static RAM (PSRAM) organized as 256K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}_1) and active HIGH Chip Enable (\overline{CE}_2), and active LOW Output Enable (\overline{OE}). This device has an automatic power-down feature that reduces power consumption dramatically when deselected. Writing to the device is accomplished by asserting Chip Enable One (\overline{CE}_1) and Write

Enable (\overline{WE}) inputs LOW and Chip Enable Two (\overline{CE}_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{17}).

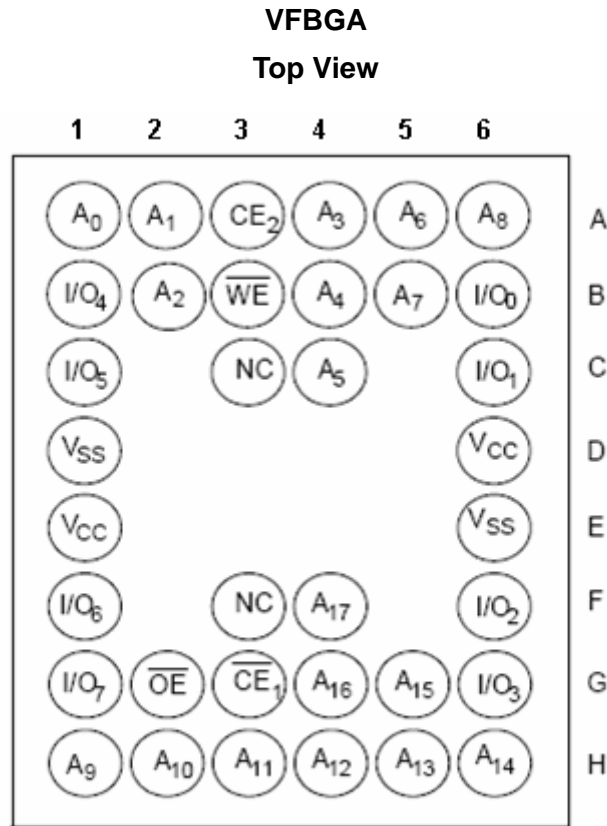
Reading from the device is accomplished by asserting the Chip Enable One (\overline{CE}_1) and Output Enable (\overline{OE}) inputs LOW while forcing Write Enable (\overline{WE}) HIGH. And Chip Enable Two (\overline{CE}_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during write operation (\overline{CE}_1 LOW, \overline{CE}_2 HIGH, and \overline{WE} LOW). See the Truth Table for a complete description of read and write modes.

Logic Block Diagram



Pin Configuration[1]



Product Portfolio

Product	V _{CC} Range (V)			Speed(ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
	f = 1MHz		f = f _{MAX}							
	Min.	Typ.	Max.		Typ.[2]	Max.	Typ.[2]	Max.	Typ. [2]	Max.
M24L28256DA	2.7	3.0	3.3	55	1	5	14	22	9	40
				70			8	15		

Notes:

1. NC “no connect”—not connected internally to the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)} and T_A = 25°C.

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)
 Storage Temperature-65°C to +150°C
 Ambient Temperature with Power Applied-40°C to +85°C
 Supply Voltage to Ground Potential-0.4V to 4.6V
 DC Voltage Applied to Outputs in High-Z State[3, 4, 5]-0.4V to 3.7V
 DC Input Voltage[3, 4, 5].....-0.4V to 3.7V
 Output Current into Outputs (LOW)20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
 Latch-up Current> 200 mA

Operating Range

Range	Ambient Temperature (T _A)	V _{CC}
Extended	-25°C to +85°C	2.7V to 3.3V

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	-55			-70			Unit
			Min.	Typ. [2]	Max.	Min.	Typ. [2]	Max.	
V _{CC}	Supply Voltage		2.7	3.0	3.3	2.7		3.3	V
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	V _{CC} -0.4			V _{CC} -0.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA			0.4			0.4	V
V _{IH}	Input HIGH Voltage		0.8* V _{CC}		V _{CC} +0.4	0.8* V _{CC}		V _{CC} +0.4	V
V _{IL}	Input LOW Voltage		-0.4		0.4	-0.4		0.4	V
I _{Ix}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disable	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}		14	22		8	15	mA
		f = 1 MHz		1	5		1	5	
I _{SB1}	Automatic \overline{CE}_1 Power-Down Current —CMOS Inputs	$\overline{CE}_1 \geq V_{CC}-0.2V, CE_2 \leq 0.2V$ V _{IN} ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V, f = f _{MAX} (Address and Data Only), f = 0		40	250		40	250	μA
I _{SB2}	Automatic \overline{CE}_1 Power-Down Current —CMOS Inputs	$\overline{CE}_1 \geq V_{CC}-0.2V, CE_2 \leq 0.2V$ V _{IN} ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V, f = 0, V _{CC} = 3.3V		9	40		9	40	μA

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	TA = 25°C, f = 1 MHz	8	pF
C _{OUT}	Output Capacitance	V _{CC} = V _{CC(typ)}	8	pF

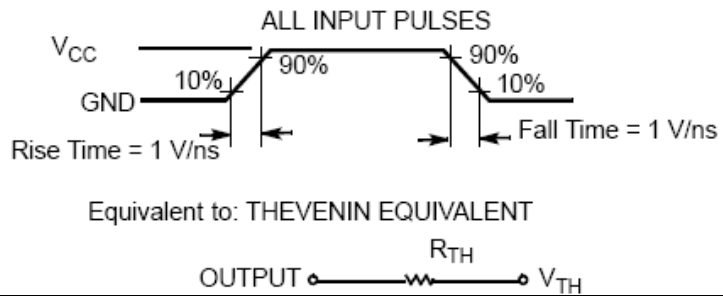
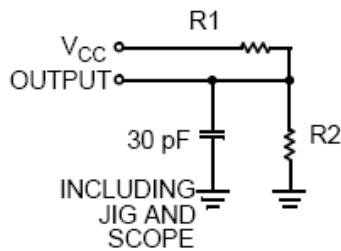
Thermal Resistance[6]

Parameter	Description	Test Conditions	BGA	Unit
θ _{JA}	Thermal Resistance(Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/ JESD51.	55	°C/W
θ _{JC}	Thermal Resistance (Junction to Case)		17	°C/W

Notes:

- 3.V_{IH(MAX)} = V_{CC} + 0.5V for pulse durations less than 20 ns.
- 4.V_{IL(MIN)} = -0.5V for pulse durations less than 20 ns.
- 5.Overshoot and undershoot specifications are characterized and are not 100% tested.
- 6.Tested initially and after design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Parameters	3.0V (V _{CC})	Unit
R1	22000	Ω
R2	22000	Ω
R _{TH}	11000	Ω
V _{TH}	1.50	V

Switching Characteristics (Over the Operating Range) [7]

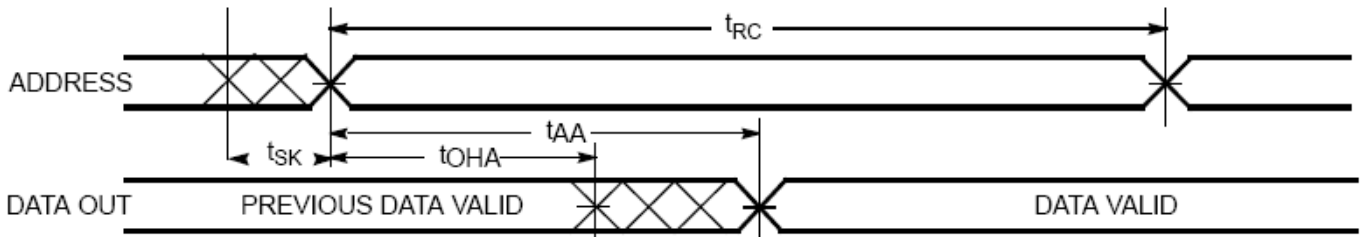
Parameter	Description	-55		-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55[11]		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		10		ns
t _{ACE}	\overline{CE}_1 LOW and CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		25		35	ns
t _{LZOE}	\overline{OE} LOW to Low Z[8, 9]	5		5		ns
t _{HZOE}	\overline{OE} HIGH to High Z[8, 9]		25		25	ns
t _{LZCE}	\overline{CE}_1 LOW and CE ₂ HIGH to LOW Z[8, 9]	5		5		ns
t _{HZCE}	\overline{CE}_1 HIGH and CE ₂ LOW to HIGH Z[8, 9]		25		25	ns
t _{SK[11]}	Address Skew		0		10	ns
Write Cycle [10]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	\overline{CE}_1 LOW and CE ₂ HIGH to Write End	45		55		ns
t _{AW}	Address Set-Up to Write End	45		55		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	\overline{WE} Pulse Width	40		55		ns
t _{SD}	Data Set-Up to Write End	25		25		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	\overline{WE} LOW to High-Z[8, 9]		25		25	ns
t _{LZWE}	\overline{WE} HIGH to Low-Z[8, 9]	5		5		ns

Notes:

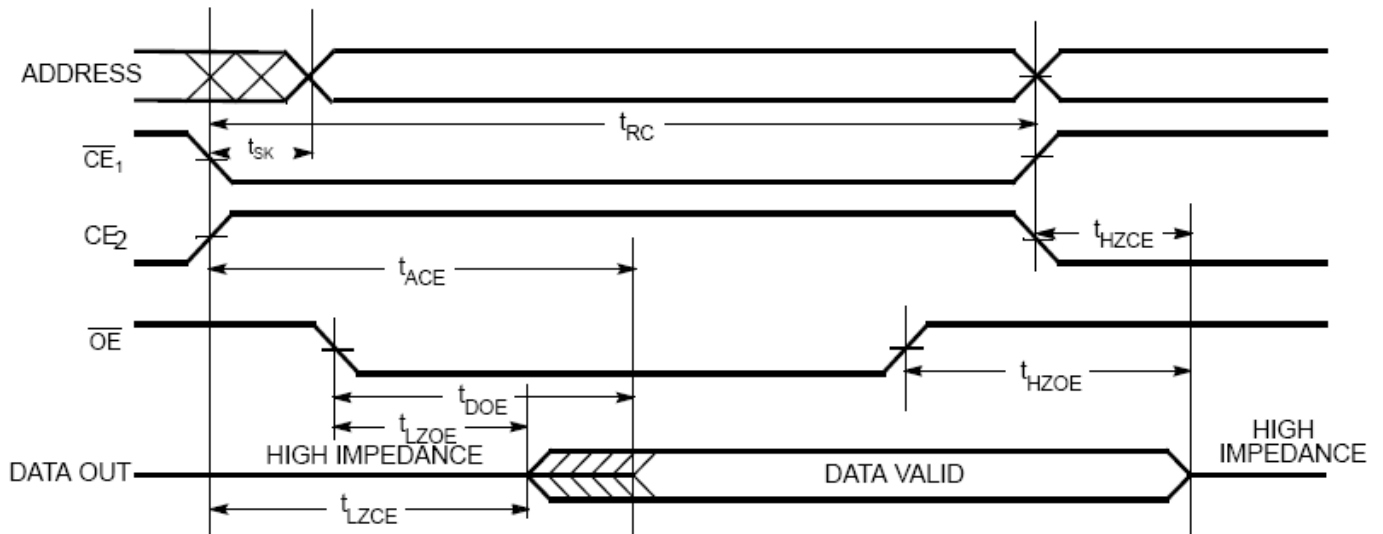
- Test conditions assume signal transition time of 1V/ns or higher, timing reference levels of V_{CC(typ)}/2, input pulse levels of 0V to V_{CC(typ)}, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance
- t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
- High-Z and Low-Z parameters are characterized and are not 100% tested.
- The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, and CE₂=V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.
- To achieve 55-ns performance, the read access should be \overline{CE} controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[11, 12, 13]



Read Cycle 2 (\overline{OE} Controlled)[11, 13]

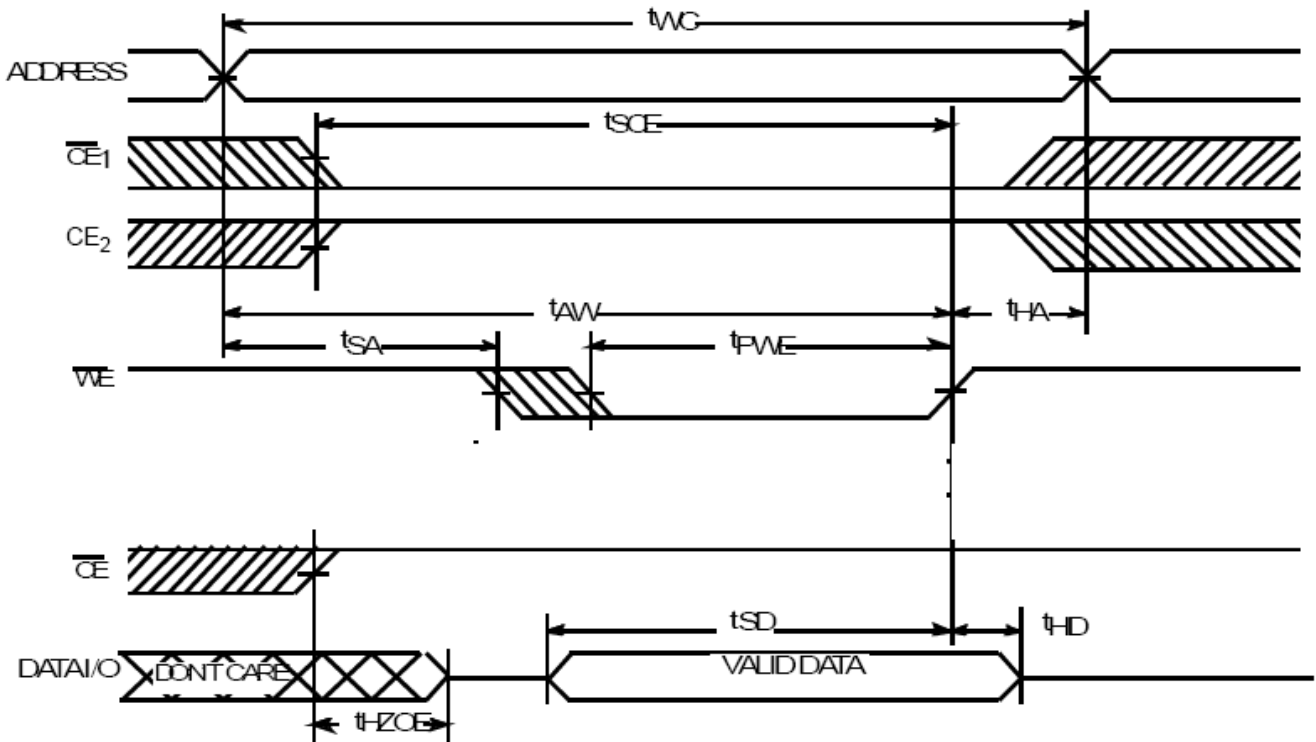


Notes:

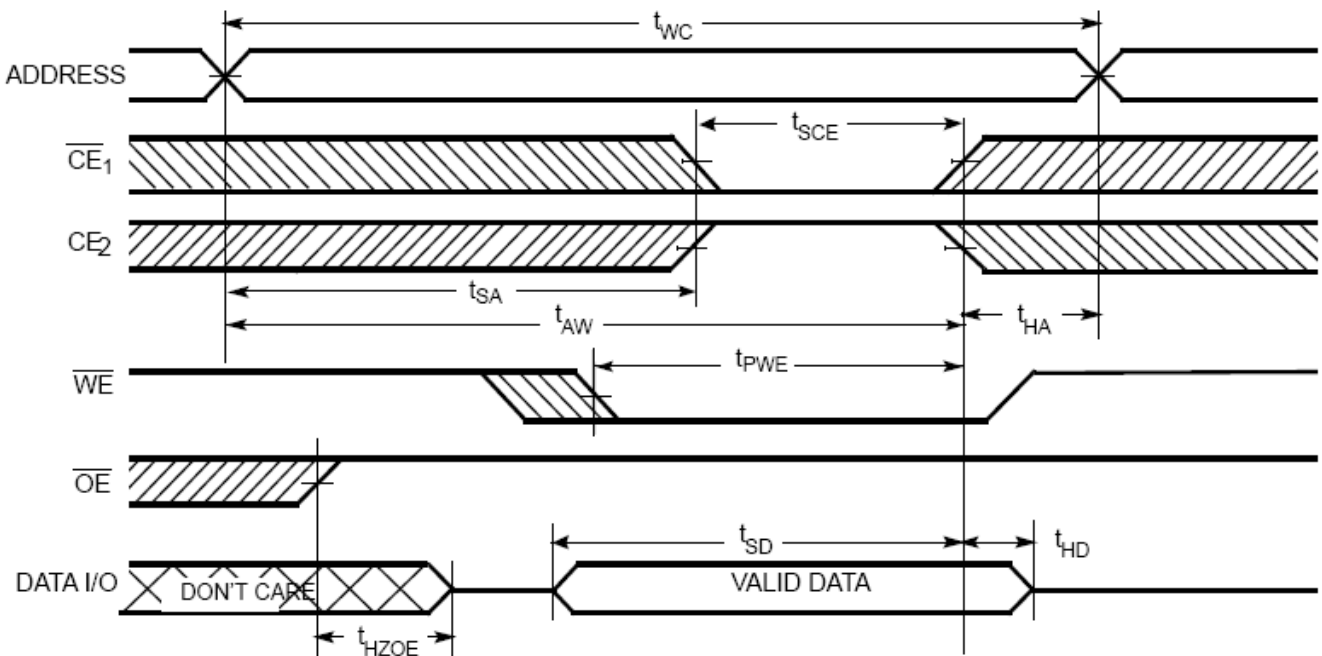
- 12. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$ and $CE_2 = V_{IH}$.
- 13. \overline{WE} is HIGH for Read Cycle.

Switching Waveforms (continued)

Write Cycle No.1 (\overline{WE} Controlled)[9,10, 14, 15, 16]



Write Cycle 2 (\overline{CE}_1 or \overline{CE}_2 Controlled) [9, 10, 14, 15, 16]



Notes:

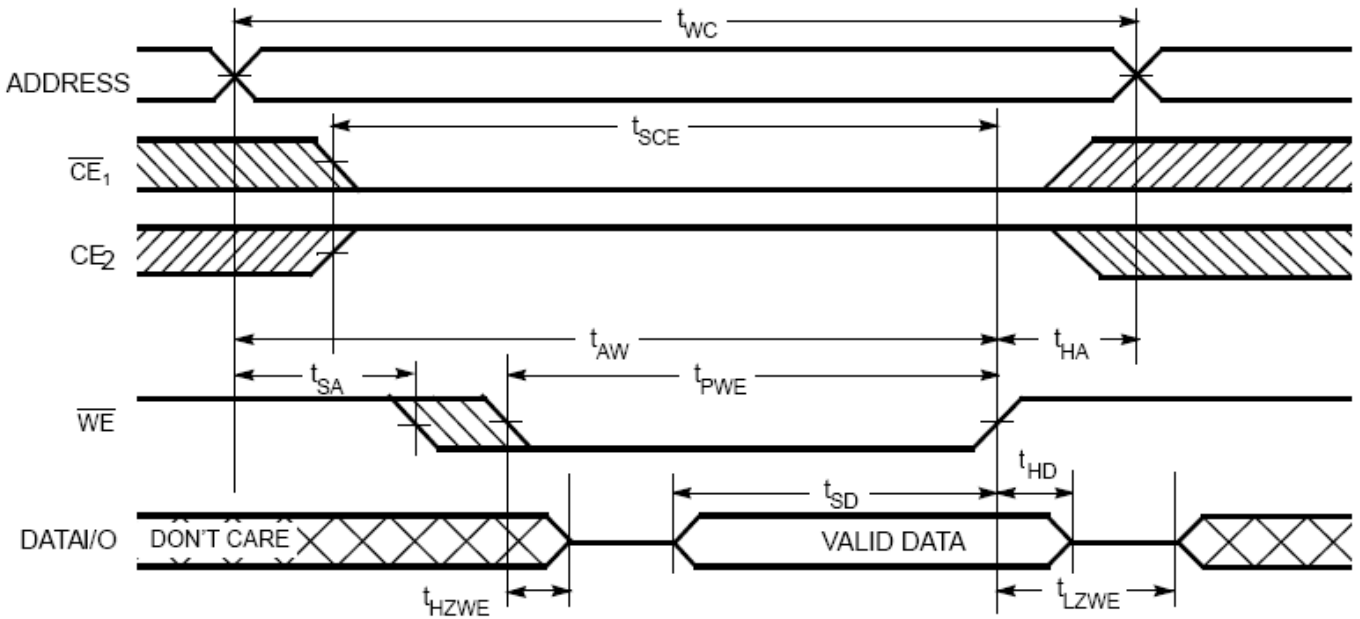
14.Data I/O is high impedance if $\overline{OE} \geq V_{IH}$.

15. If Chip Enables go INACTIVE simultaneously with $\overline{WE} = \text{HIGH}$, the output remains in a high-impedance state.

16.During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 (\overline{WE} Controlled, \overline{OE} LOW)[15, 16]



Truth Table[17]

\overline{CE}_1	\overline{CE}_2	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

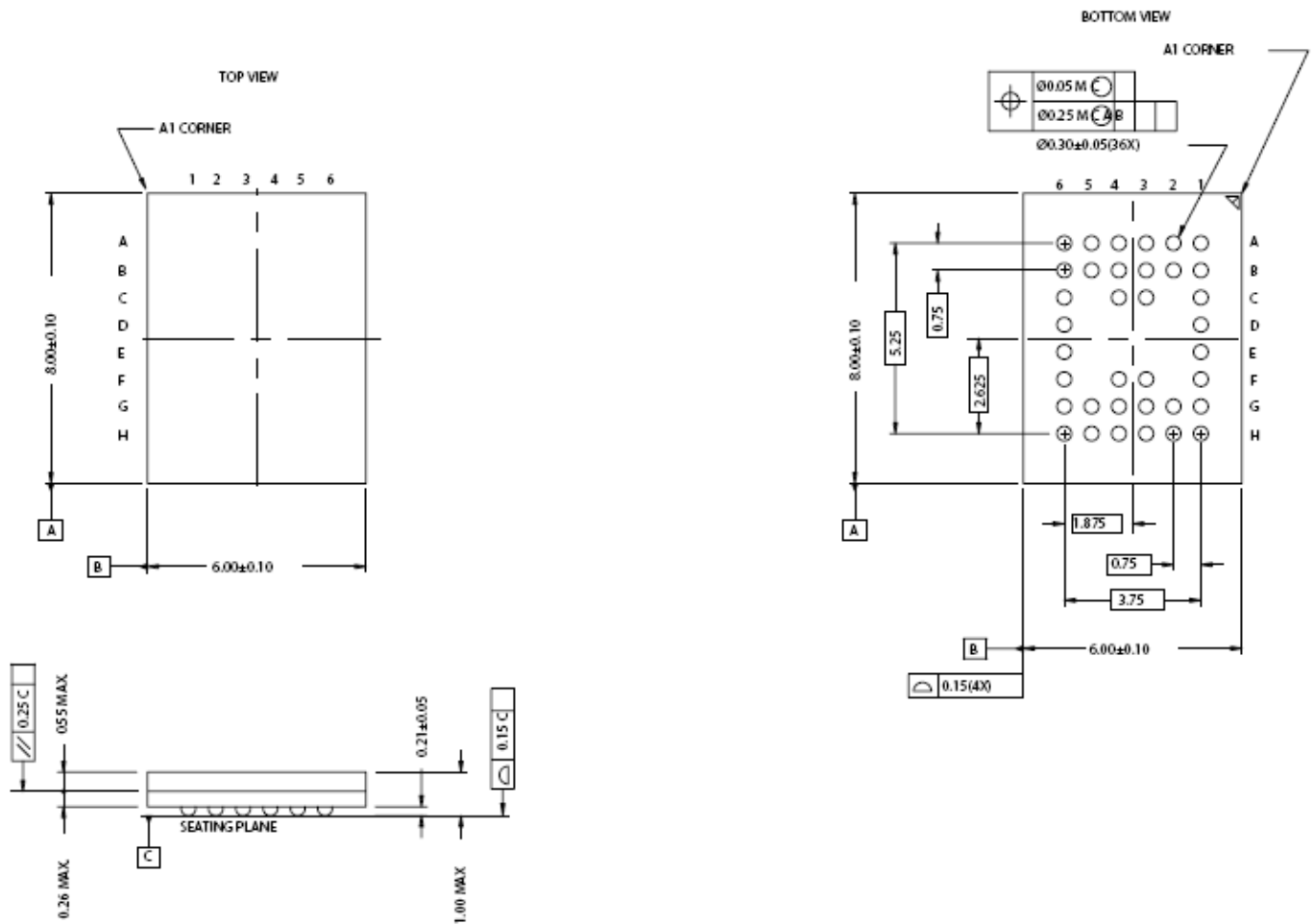
Speed (ns)	Ordering Code	Package Type	Operating Range
55	M24L28256DA-55BEG	36-Lead VFBGA (6 x 8 x 1 mm) (Pb-free)	Extended
70	M24L28256DA-70BEG	36-Lead VFBGA (6 x 8 x 1 mm) (Pb-free)	Extended

Note:

17.H = Logic HIGH, L = Logic LOW, X = Don't Care.

Package Diagrams

36-Lead VFBGA (6 x 8 x 1 mm)



Revision History

Revision	Date	Description
1.0	2007.07.19	Original

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