Ground Referenced Stereo Headphone Amplifier

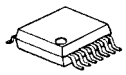
■ GENERAL DESCRIPTION

The **NJU72040** is an audio headphone amplifier .

Ground-referenced outputs eliminate output coupling capacitor. The pop noise suppression circuit removes a pop noise at the power-on and power-off.

It is suitable for audio headphone amplifer application

■ PACKAGE OUTLINE



NJU72040V

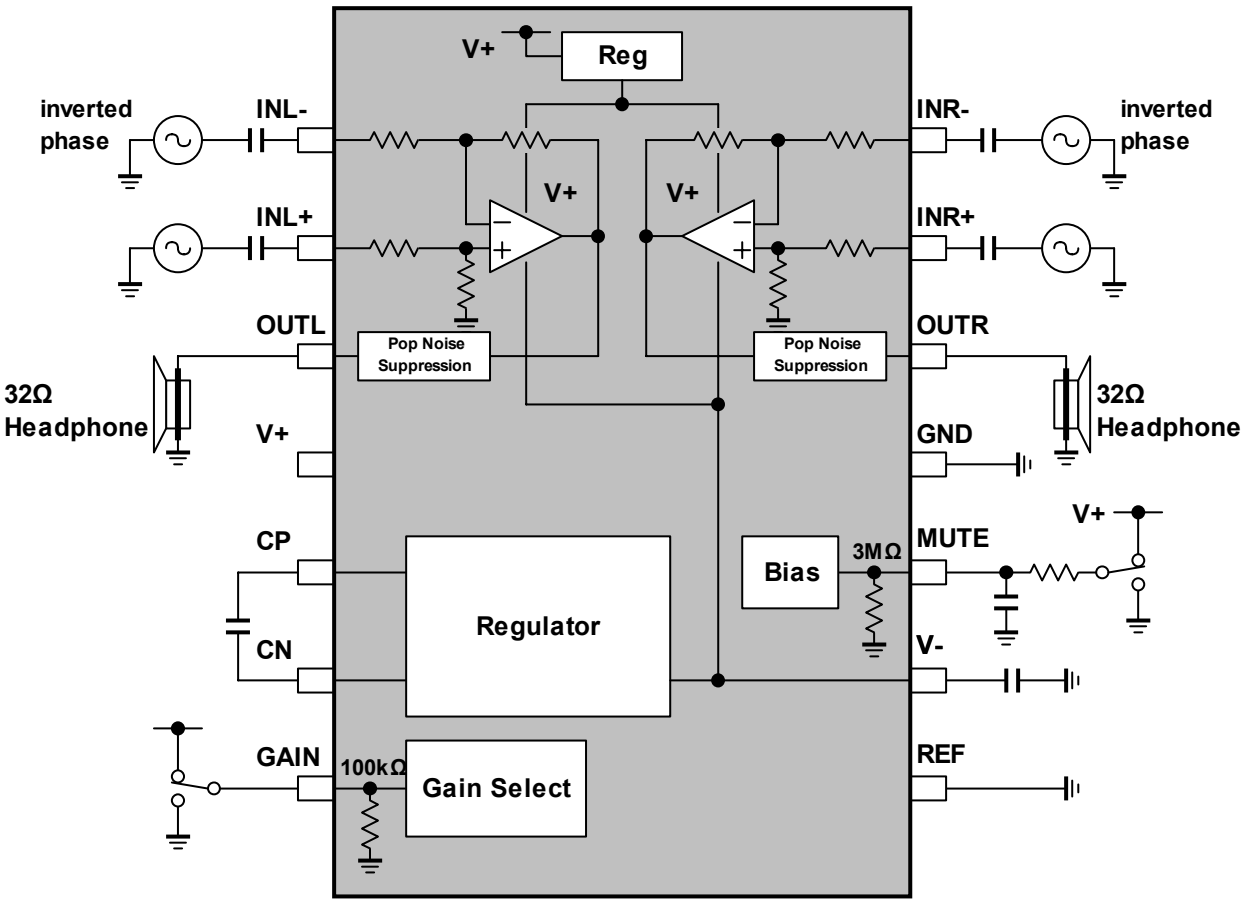
■ APPLICATIONS

● Audio applications which have audio headphone interface

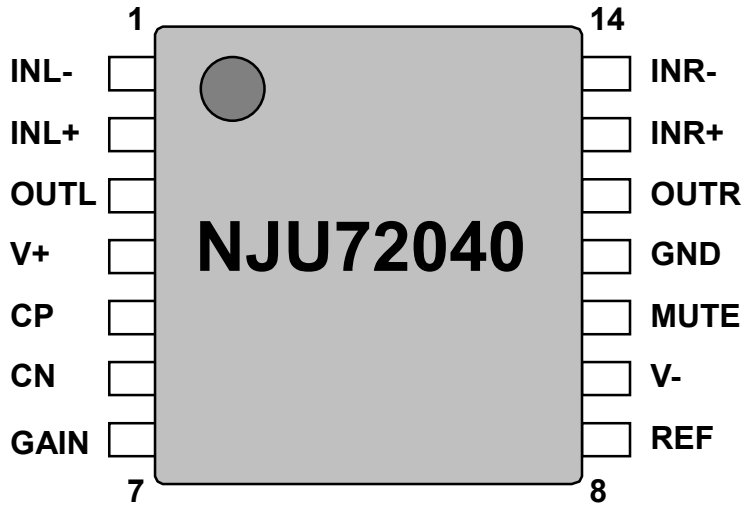
■ FEATURES

● Operating Voltage	+2.7 to +3.6V
● Operating Current	I_{DD}=10.5mA typ. at V^+=3.3V, No load, No Signal
● Output Coupling Capacitor-less	
● Pop Noise Suppression Circuit	
● Gain Select	
● C-MOS Technology	
● Package Outline	SSOP14

■ BLOCK DIAGRAM



■ **PIN CONFIGURATION**



No.	Symbol	Function	No.	Symbol	Function
1	INL-	Lch Inverted Input	8	REF	Reference Voltage Input
2	INL+	Lch Noninverted Input	9	V-	V- Power Supply
3	OUTL	Lch Output	10	MUTE	MUTE / Pop Noise Suppression
4	V+	V+ Power Supply	11	GND	Ground
5	CP	Flying Capacitor Positive Terminal	12	OUTR	Rch Output
6	CN	Flying Capacitor Negative Terminal	13	INR+	Rch Inverted Input
7	GAIN	Gain Select	14	INR-	Rch Noninverted Input

■ **ABSOLUTE MAXIMUM RATING** (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	+4	V
Power Dissipation	P_D	SSOP14 : 550(Note1)	mW
Maximum Input Voltage	V_{IM}	V^+ +0.3	V
Operating Temperature Range	Topr	-40 ~ +85	°C
Storage Temperature Range	Tstg	-40 ~ +125	°C

(Note1) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting

■ **RECOMMENDED OPERATING CONDITIONS**

(Ta=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		2.7	3.3	3.6	V

■ **ELECTRICAL CHARACTERISTICS**

(Ta=25°C, V^+=3.3V, f=1kHz, Vin=0.1Vrms[differential input], Gv=6.4dB, MUTE=OFF, R_L=32Ω unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{DD}	No signal, No load	-	10.5	15.5	mA
Input Resistance1	R_{in1}	INL-, INR-	49	61	73	kΩ
Input Resistance2	R_{in2}	INL+, INR+	103	129	155	kΩ
Voltage Gain1	G_{V1}	Gain Terminal=Low	5.4	6.4	7.4	dB
Voltage Gain2	G_{V2}	Gain Terminal=High	11.4	12.4	13.4	dB
Voltage Gain3	G_{V3}	Gain Terminal=Low, R_L=10kΩ	6.6	7.1	7.6	dB
Voltage Gain4	G_{V4}	Gain Terminal=High, R_L=10kΩ	12.6	13.1	13.6	dB
Maximum Output Power1	P_{OMAX1}	THD=3%, R_L=32Ω Input=Lch or Rch	-	80	-	mW
Maximum Output Power2	P_{OMAX2}	THD=3%, R_L=32Ω Input=Lch and Rch	-	55	-	mW
Maximum Output Voltage Level	V_{OMAX}	THD=1%, R_L=10kΩ	-	2.2	-	Vrms
Mute Level	V_{MUTE}	Rg=0Ω, Mute=ON	-	-90	-80	dB
Equivalent Input Noise Voltage	V_{NI}	Rg=0Ω, BW:400Hz-22kHz	-	-100	-95	dBV
Total Harmonic Distortion1	THD1	BW:400Hz-22kHz, R_L=32Ω	-	0.08	0.3	%
Total Harmonic Distortion2	THD2	BW:400Hz-22kHz, R_L=10kΩ	-	0.007	0.05	%
Channel Separation1	CS1	Rg=600Ω, (*1)	65	75	-	dB
Channel Separation2	CS2	Rg=600Ω, f=10kHz, (*1)	55	65	-	dB
Output Offset Voltage	V_{OS}	Rg=0Ω, Gv=12.4Db, No load	-	1	5	mV

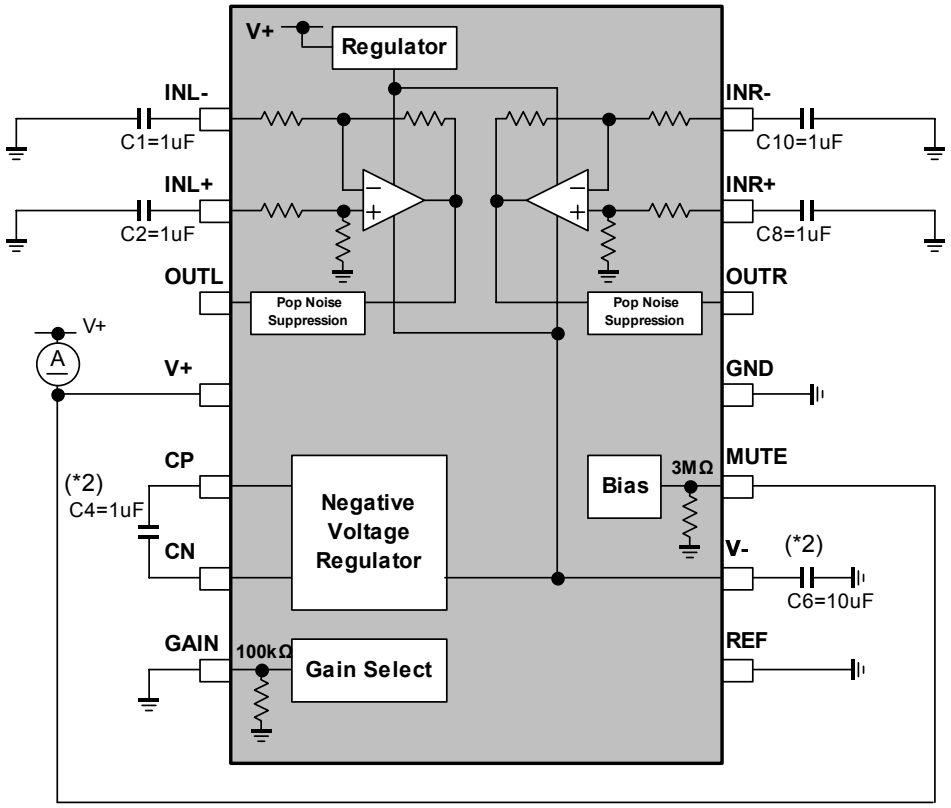
(*1)OUTL(measured terminal): 20log(OUTR/OUTL) , OUTR(measured terminal): 20log(OUTL/OUTR)

■ **CONTROL CHARACTERISTICS**

(Ta=25°C, V^+=3.3V, Gv=6.4dB, MUTE=OFF, R_L=32Ω unless otherwise specified)

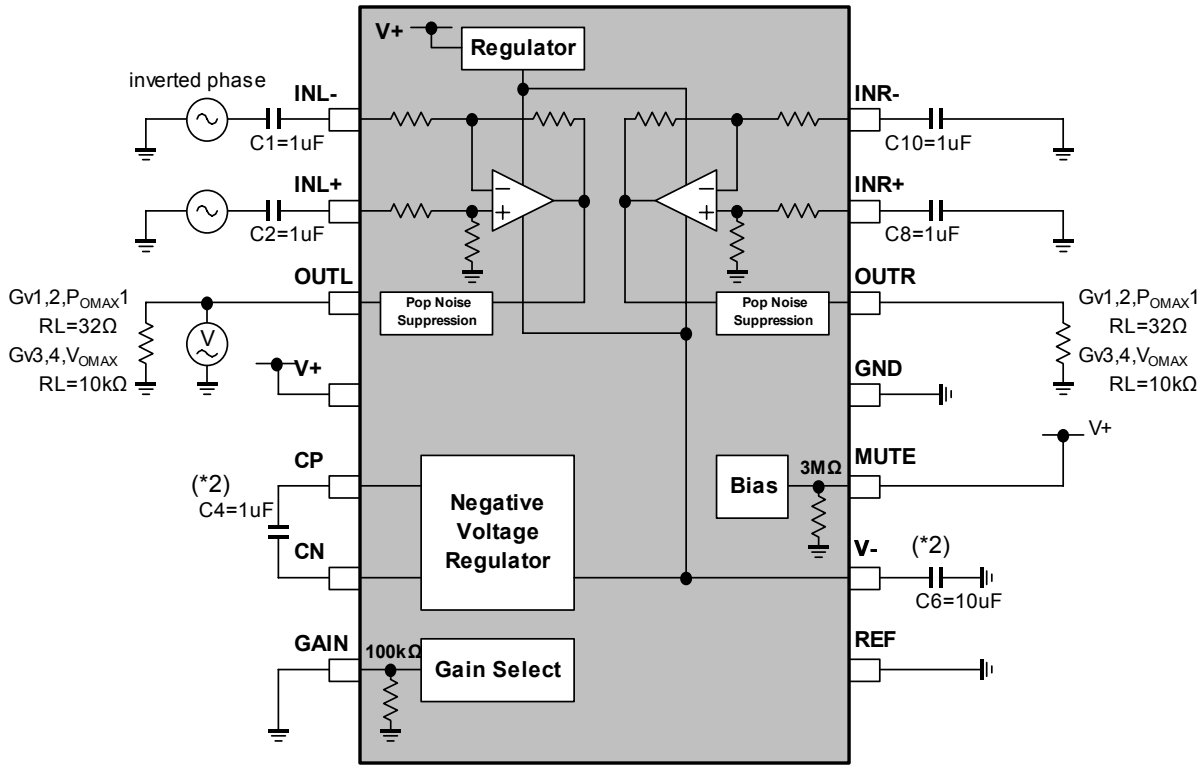
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Mute terminal High	MuteH	Mute=OFF	0.8 V^+	-	V^+	V
Mute terminal Low	MuteL	Mute=ON	0	-	0.2 V^+	V
Gain terminal High	GainH	Gv=12.4dB	0.8 V^+	-	V^+	V
Gain terminal Low	GainL	Gv=6.4dB	0	-	0.2 V^+	V

■TEST CIRCUIT (I_{DD})



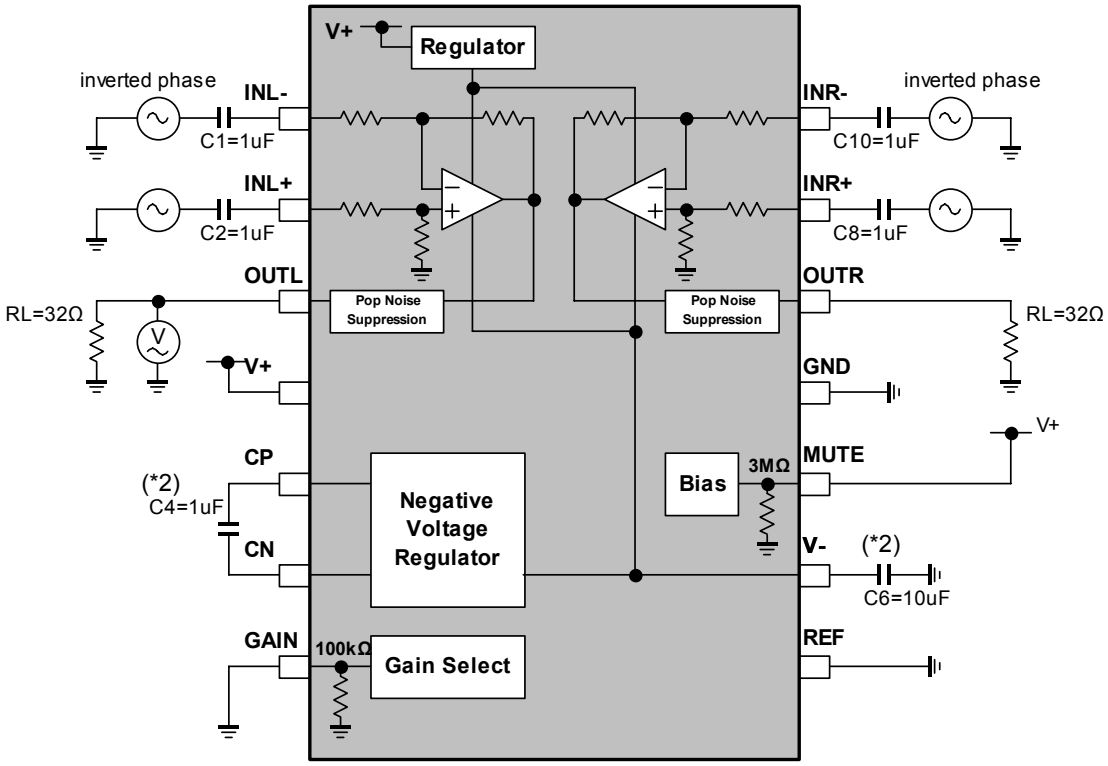
(*2): Monolithic Ceramic Capacitors

■TEST CIRCUIT (G_V1, G_V2, G_V3, G_V4, $P_{OMAX}1$, V_{OMAX})



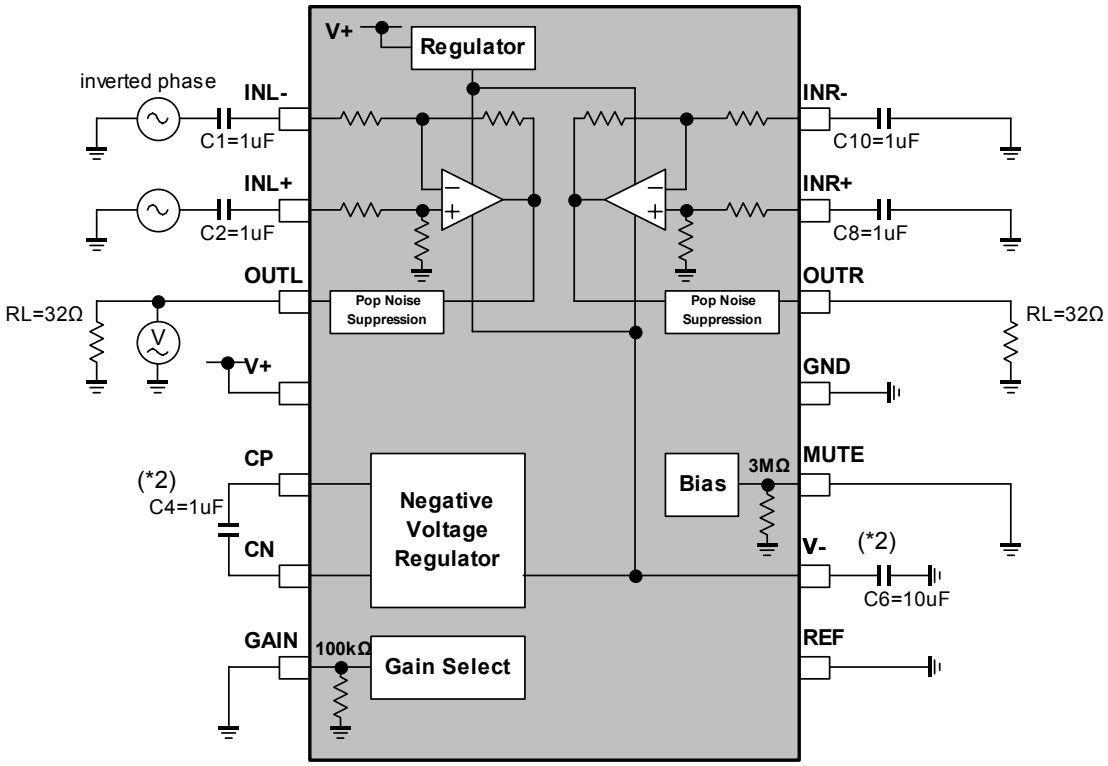
(*2): Monolithic Ceramic Capacitors

■TEST CIRCUIT (P_{OMAX}2)



(*2): Monolithic Ceramic Capacitors

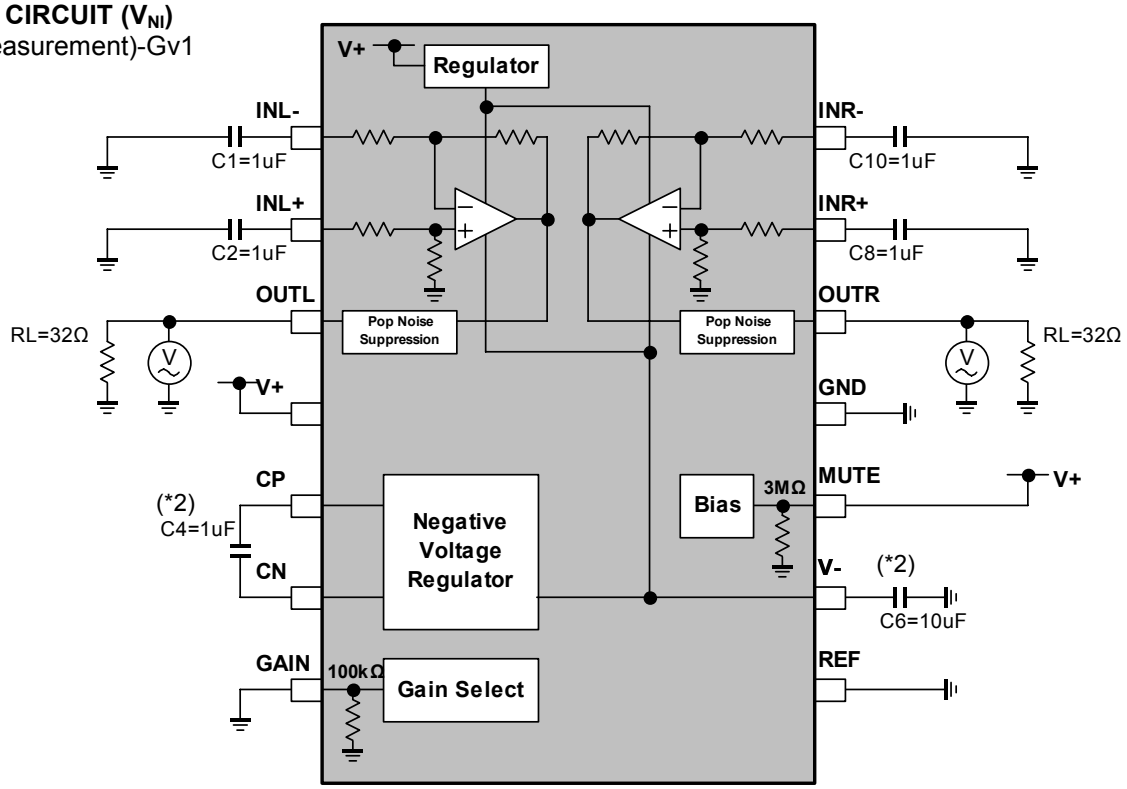
■TEST CIRCUIT (V_{MUTE})



(*2): Monolithic Ceramic Capacitors

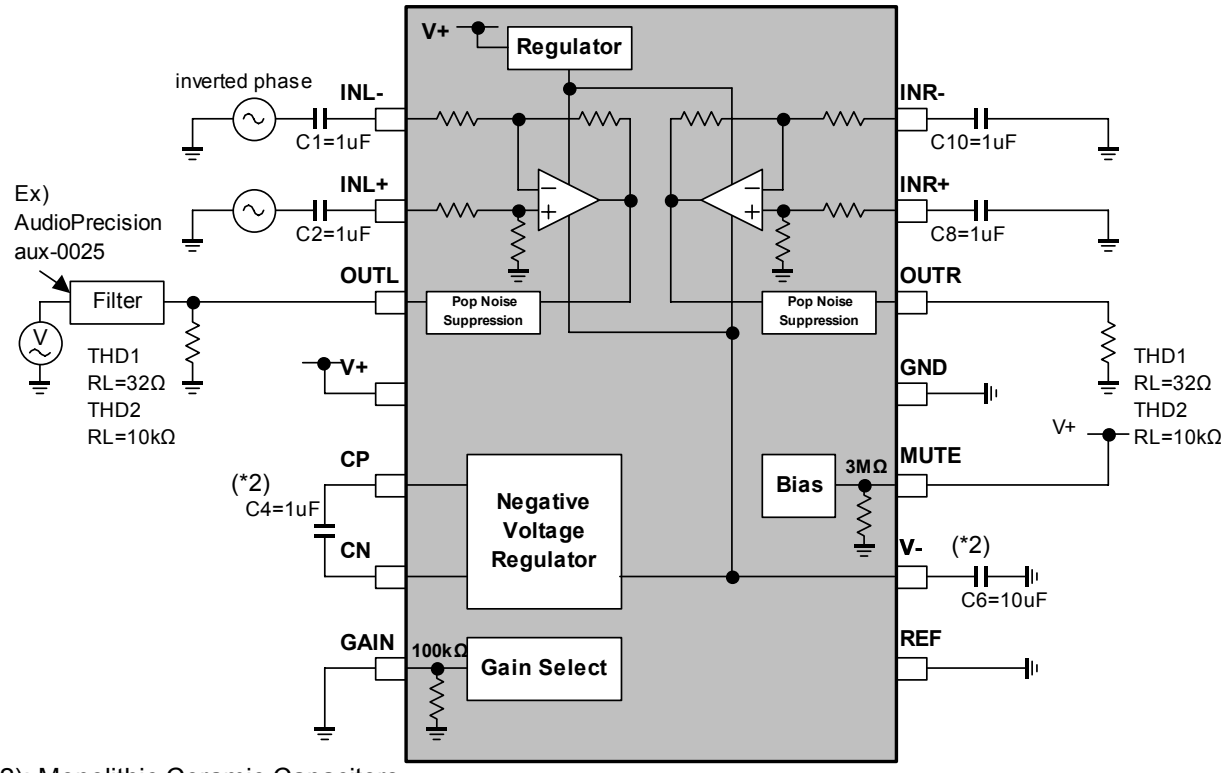
■**TEST CIRCUIT (V_{NI})**

V_{NI}=(measurement)-Gv1



(*2): Monolithic Ceramic Capacitors

■**TEST CIRCUIT (THD1, THD2)**



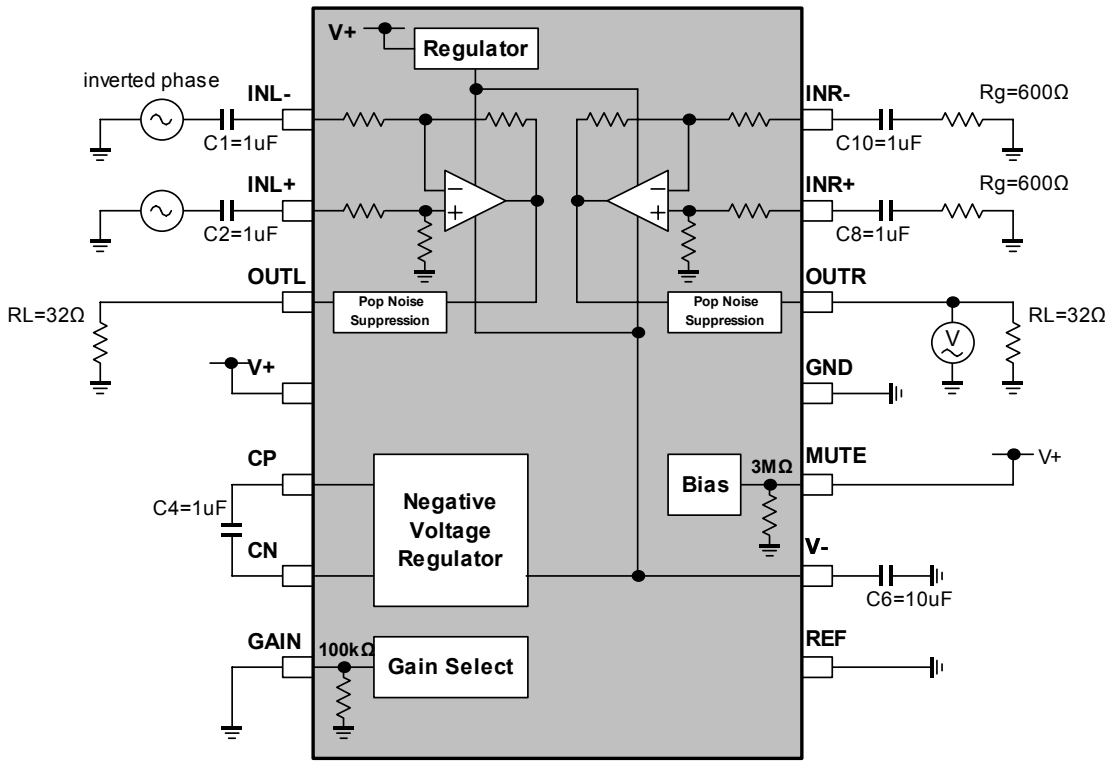
(*2): Monolithic Ceramic Capacitors

(*3): Connect a low-pass filter circuit with the corner frequency of more than 20kHz in front of an analyzer for rejecting the switching noise generated from NJU72040. Otherwise, the characteristic result may change because of the switching noise.

■**TEST CIRCUIT (CS1, CS2)**

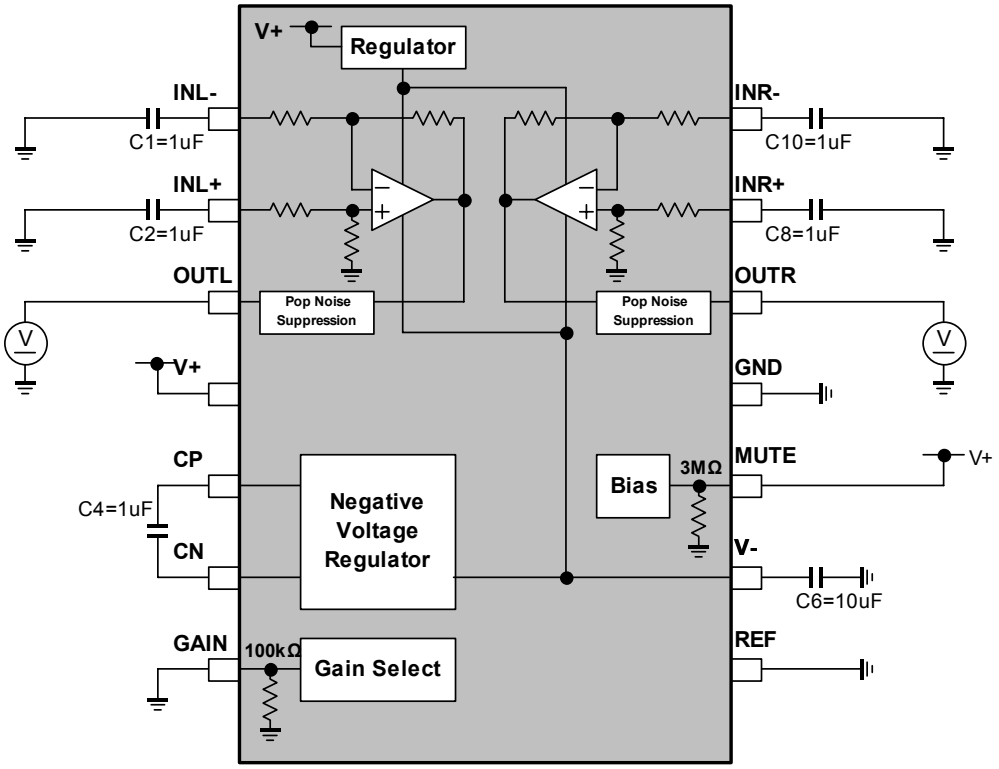
OUTL (measured terminal): CS1=CS2=20log(OUTR/OUTL)

OUTR (measured terminal): CS1=CS2=20log(OUTL/OUTR)



(*2): Monolithic Ceramic Capacitors

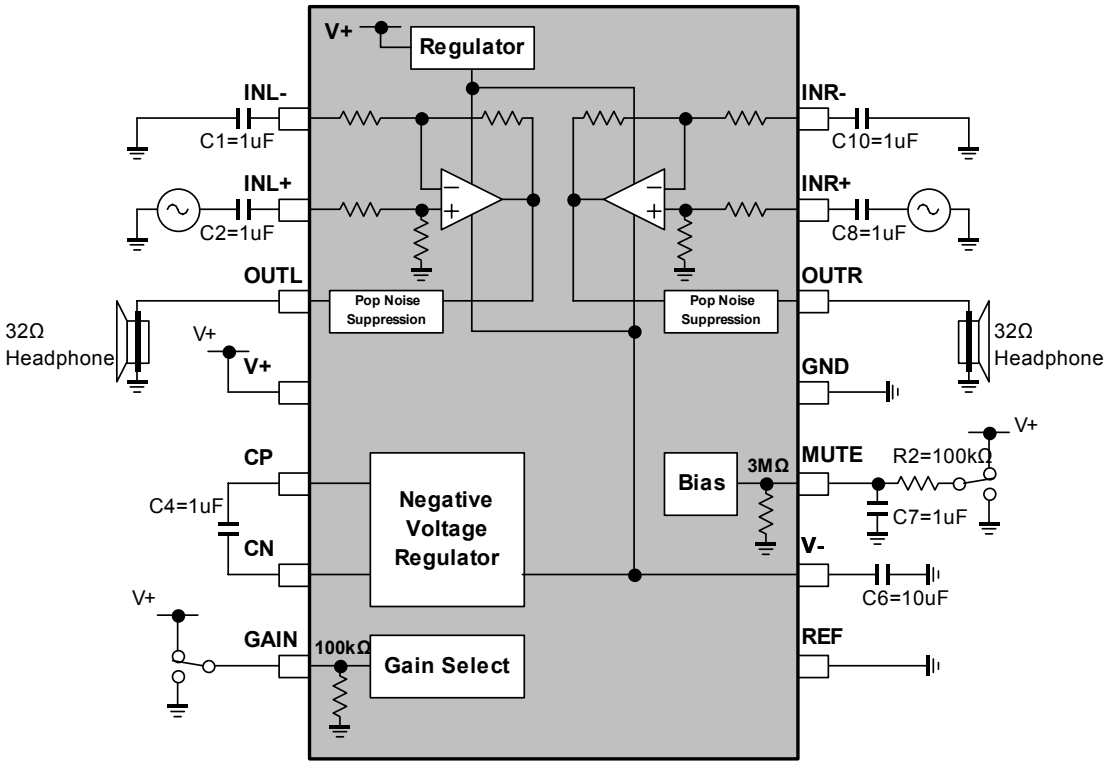
■**TEST CIRCUIT (V_{OS})**



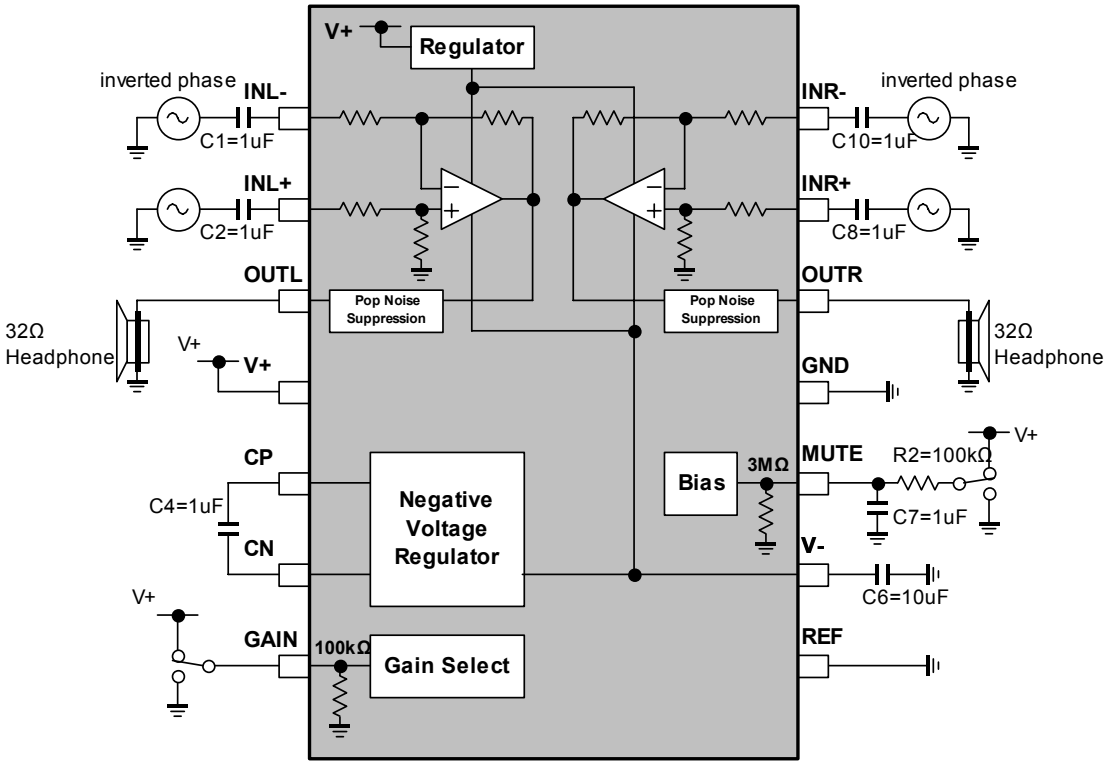
(*2): Monolithic Ceramic Capacitors

■APPLICATION CIRCUIT

(Single-end input)



(Differential input)



(*2): Monolithic Ceramic Capacitors

(*3): V- terminal (8pin) shouldn't be tied to V+ terminal (4pin)

■ APPLICATION NOTE

The NJU72040 is an audio headphone amplifier that eliminates the need for external dc-blocking output capacitors. The NJU72040 has built-in pop suppression circuitry to eliminate disturbing pop noise during power-on, power-off and mute-control.

1. Operating Principle

The NJU72040 has the built-in differential input operational amplifiers, voltage inverter, pop noise suppression circuitry, gain selectable circuitry and thermal-overload protection circuitry (Fig.1).

For single-ended input signals, connect inverted terminal (INL-, INR-) or non-inverted terminal (INL+, INR+) to ground through the capacitor. The voltage gain is selectable. In the differential circuitry, the setting gain is +6.4dB or +12.4dB for the R_L=32Ω. In the single-end input circuitry, the setting gain is +0.4dB or +6.4dB for the R_L=32Ω.

The voltage inverter for NJU72040 eliminates the need for external dc-blocking output capacitors. The pop suppression circuitry for NJU72040 eliminates the pop noise during power-on, power-off and mute-control.

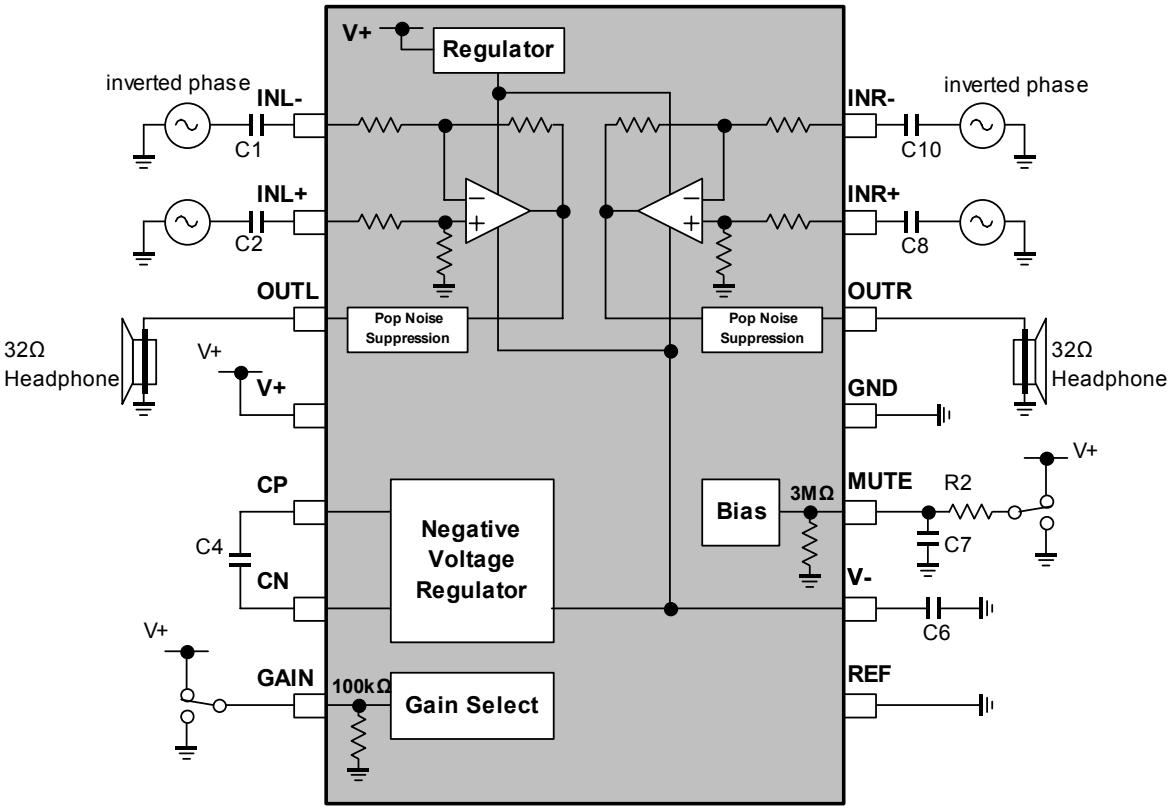


Fig.1 The NJU72040 functional block diagram

1.1 External parts

1.1.1 Input coupling capacitors C_i (C1, C2, C8, C10)

The input coupling capacitor (C_i) and the input resistance (R_{in}=61kΩ typ.) for the inverted terminal form a high-pass filter with the corner frequency determined in [$fc=1/(2\pi \times 61k\Omega \times C_i)$]. It is necessary to adjust 1uF or more.

1.1.2 Flying capacitor (C4)

Use capacitors with a low-ESR (ex. ceramic capacitors) for optimum performance. Design to provide low impedance for the wiring between CP terminal (5pin), CN terminal (6pin), and the flying capacitor (C4).

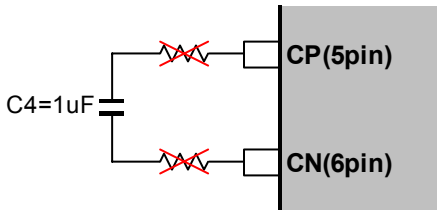


Fig.2 The NJU72040 block diagram (5pin, 6pin)

1.1.3 Hold capacitor (C6)

Use capacitors with a low-ESR (ex. ceramic capacitors) for optimum performance. Design to provide low impedance for the wiring between the hold capacitor (C6), V- terminal (9pin) and the GND on the PCB.

Separate the GND pattern connecting to the hold capacitor (C6) from that connecting to the REF terminal (8pin), thus suppressing the influence of switching noise by removing the common impedance of the GND wiring.

Design no short-circuits of V- terminal (9pin) and V+ terminal (4pin) on the PCB pattern.

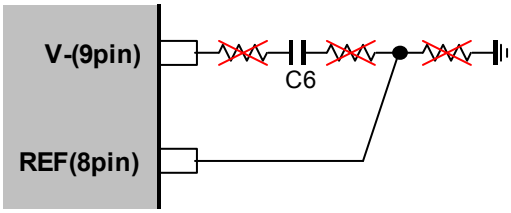


Fig.3 The NJU72040 block diagram (8pin, 9pin)

1.1.4 Mute terminal pop noise countermeasures (C7, R2)

Mute terminal needs time constant more than R2 x C7=0.1. It is necessary to adjust 100kΩ or less.

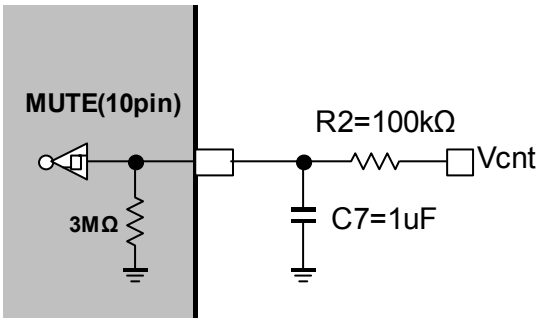


Fig.4 The NJU72040 block diagram (10pin)

1.2 Control of V+ terminal and Mute terminal

1.2.2 Power-on procedure

1. Turn on the V+.
2. After 5msec from power on, change the control voltage of MUTE terminal (Vcnt) from "Low" to "High".

* It is necessary to stabilize an IC for 5msec.

By releasing the MUTE function, the output terminal output the signal.

1.2.3 Power-off procedure

1. Change the control voltage of MUTE terminal (Vcnt) from "High" to "Low".

By the MUTE function, the output signals are stopped from output terminal.

2. Turn off the V+ after “2RC” sec from MUTE.

* It is necessary to stabilize a MUTE condition for “2RC” sec.

Ex.) R2=100kΩ, C7=1uF -> 2R2 x C7=200msec

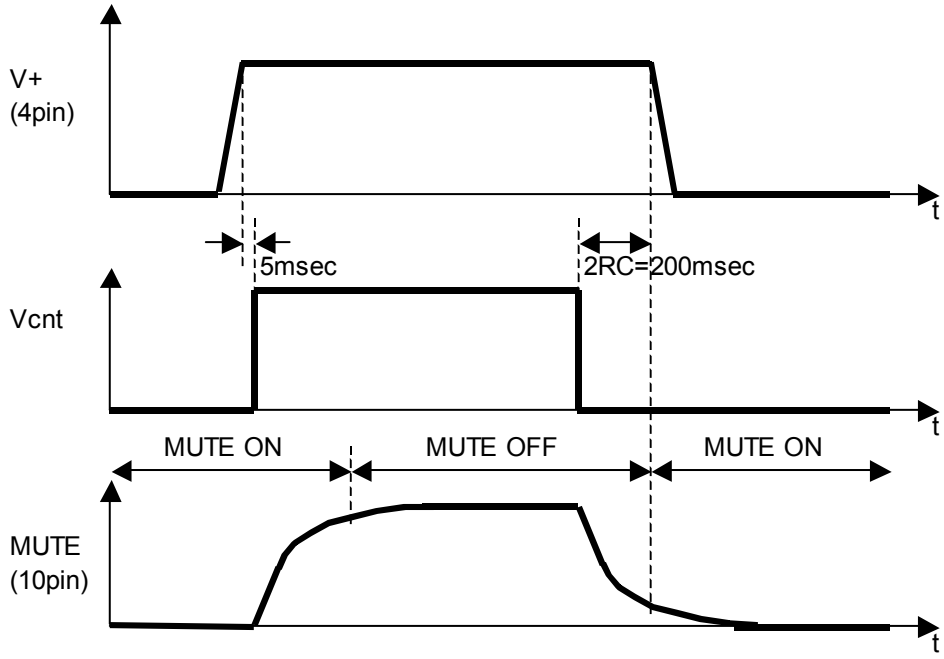
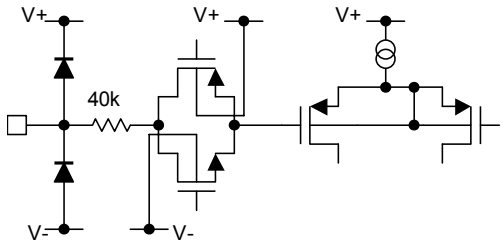
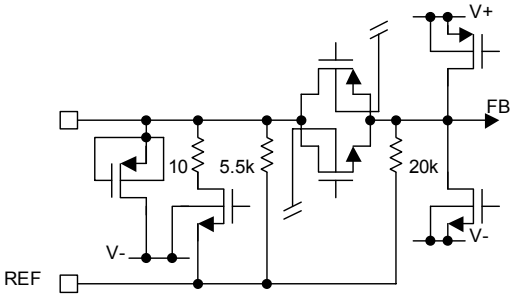
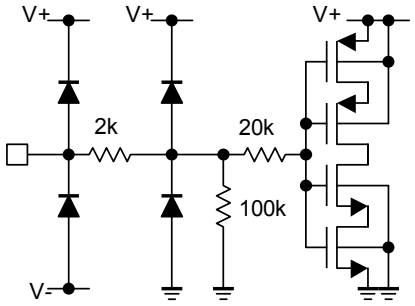
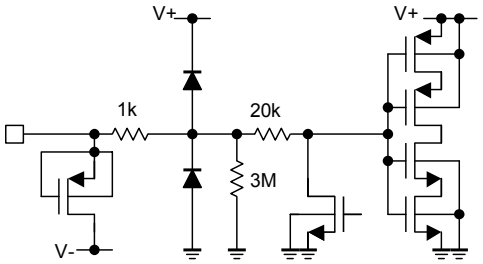
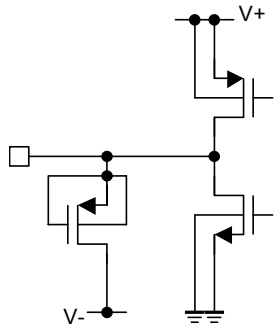
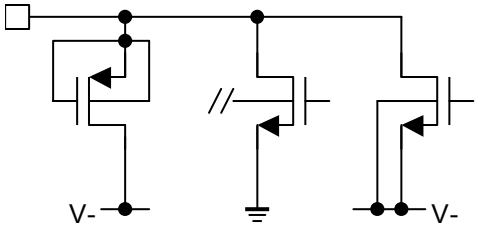
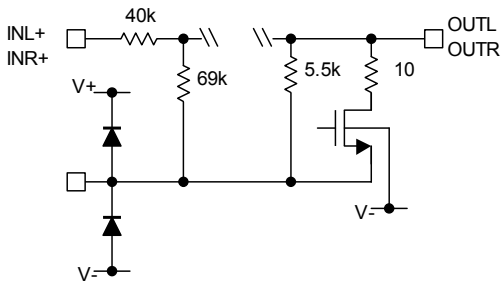


Fig.5 Turn-on / Turn-off timing chart

■TERMINAL DESCRIPTION

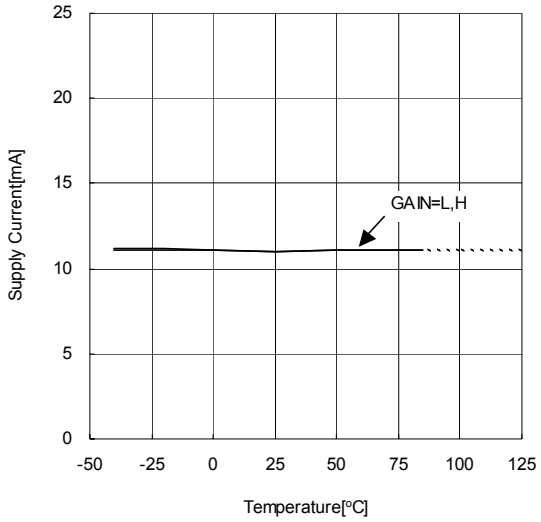
Terminal	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
1 2 13 14	INL- INL+ INR- INR+	AC Input		0V
3 12	OUTL OUTR	AC Output		0V
7	GAIN	Gain Select		0V
10	MUTE	MUTE/Pop Noise Suppression		0V

■TERMINAL DESCRIPTION

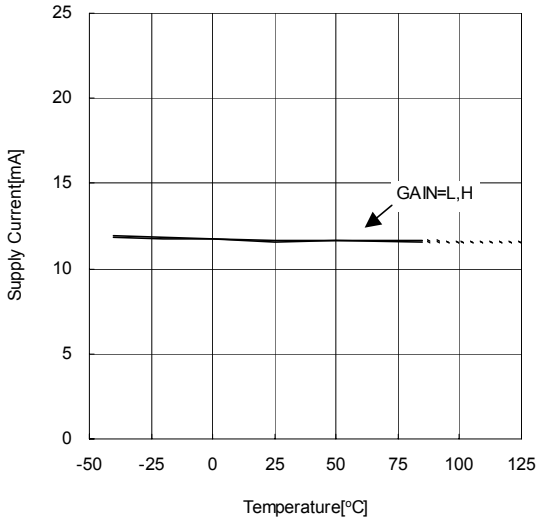
Terminal	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
5	CP	Flying Capacitor Positive Terminal		-
6	CN	Flying Capacitor Positive Terminal		-
8	REF	Reference Voltage Input		-

■ TYPICAL CHARACTERISTICS

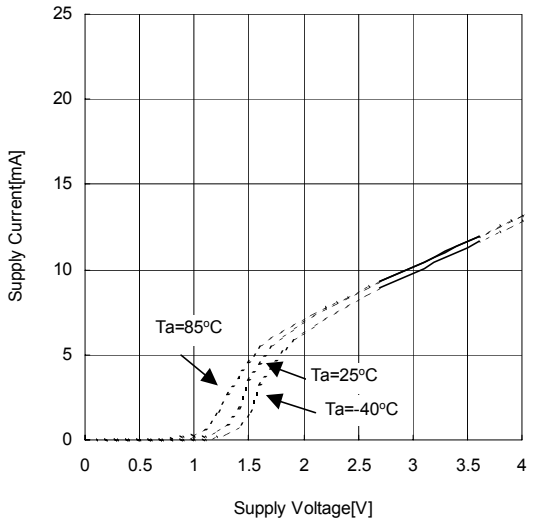
Supply Current vs Temperature
V+=3.3V, RL=NoLoad, MUTE=L



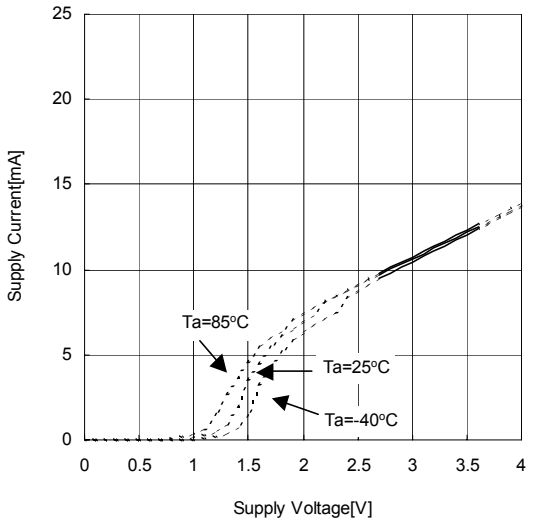
Supply Current vs Temperature
V+=3.3V, RL=NoLoad, MUTE=H



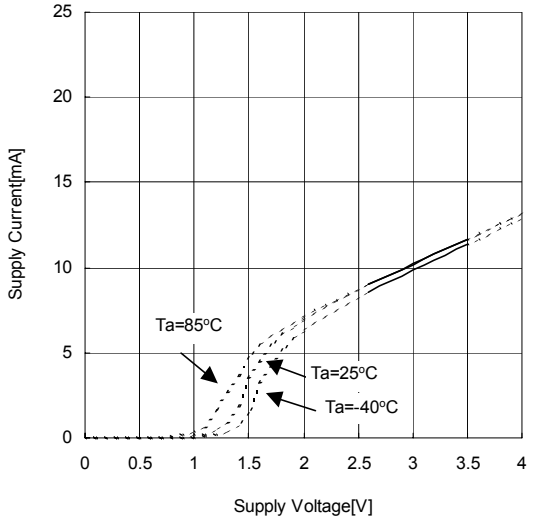
Supply Current vs Supply Voltage
RL=NoLoad, MUTE=L, GAIN=L



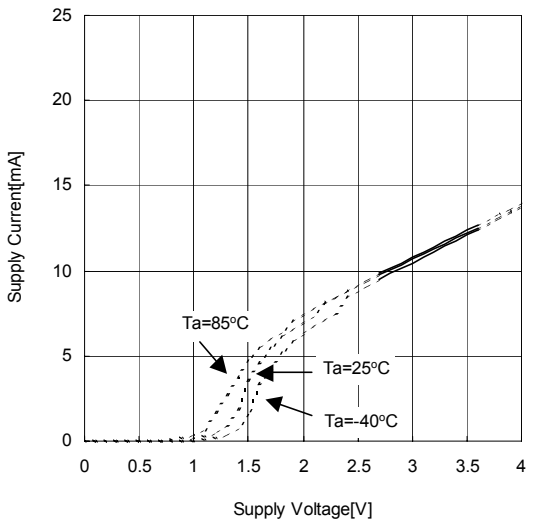
Supply Current vs Supply Voltage
RL=NoLoad, MUTE=H, GAIN=L



Supply Current vs Supply Voltage
RL=NoLoad, MUTE=L, GAIN=H

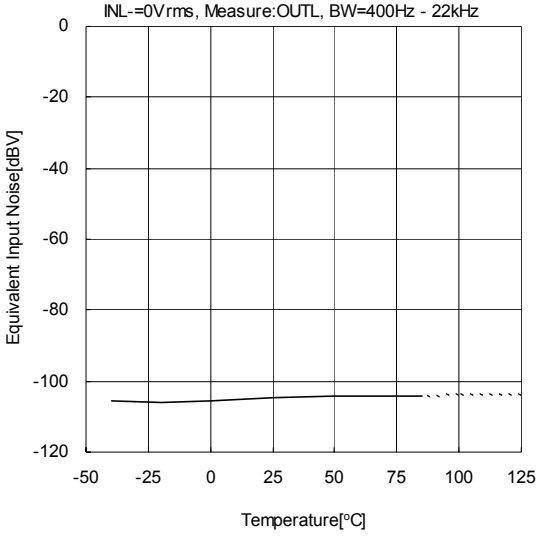


Supply Current vs Supply Voltage
RL=NoLoad, MUTE=H, GAIN=H



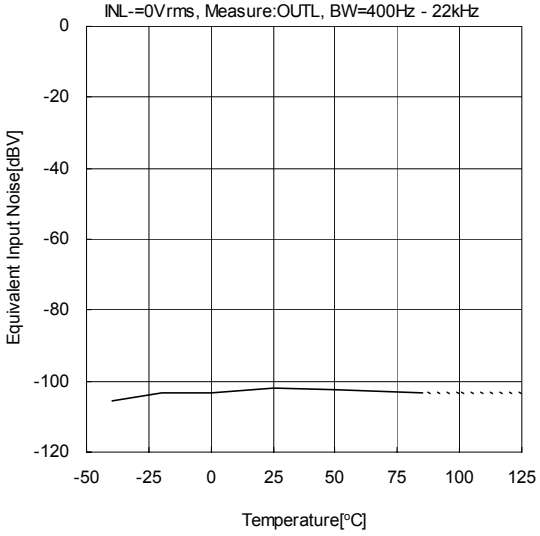
Equivalent Input Noise vs Temperature

V+=3.3V, RL=32Ω, Rg=0Ω, MUTE=H, GAIN=L, INL+=0Vrms ,
INL-=0Vrms, Measure:OUTL, BW=400Hz - 22kHz



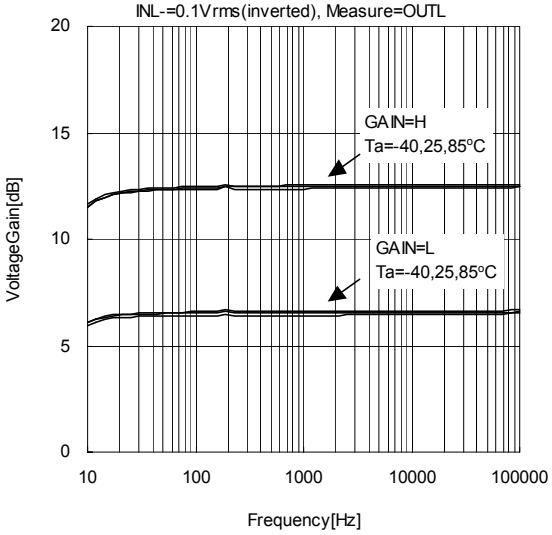
Equivalent Input Noise vs Temperature

V+=3.3V, RL=10kΩ, Rg=0Ω, MUTE=H, GAIN=L, INL+=0Vrms
INL-=0Vrms, Measure:OUTL, BW=400Hz - 22kHz



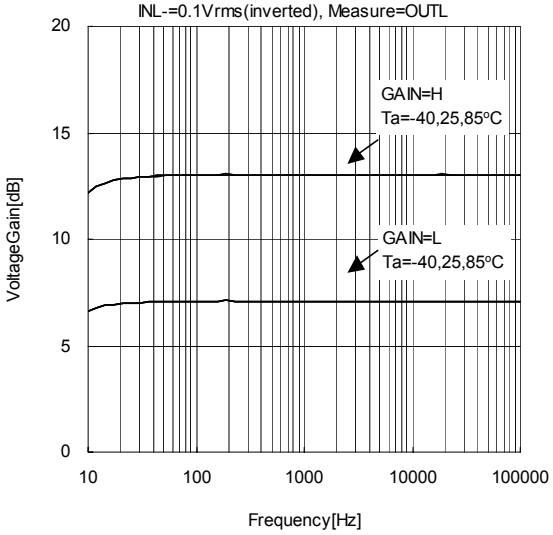
VoltageGain vs Frequency

V+=3.3V, RL=32Ω, MUTE=H, INL+=0.1Vrms
INL-=0.1Vrms(inverted), Measure=OUTL



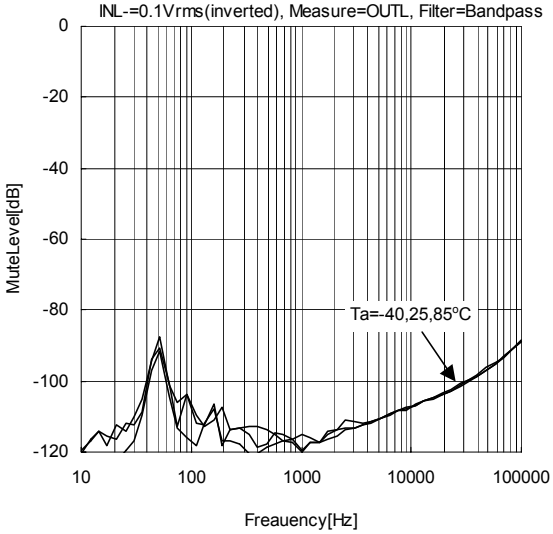
VoltageGain vs Frequency

V+=3.3V, RL=10kΩ, MUTE=H, INL+=0.1Vrms
INL-=0.1Vrms(inverted), Measure=OUTL



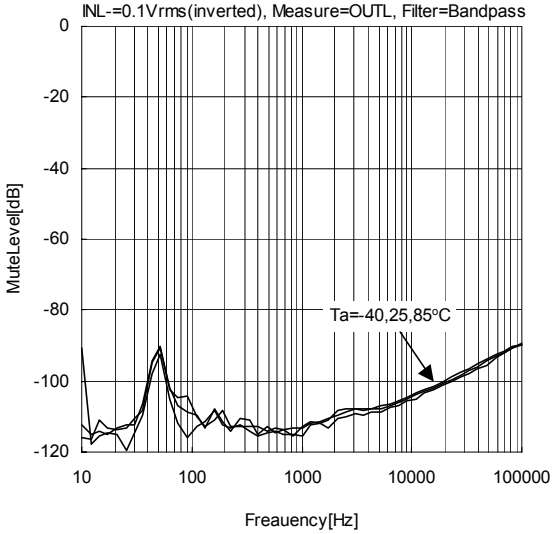
MuteLevel vs Frequency

V+=3.3V, RL=32Ω, MUTE=H, GAIN=L, INL+=0.1Vrms
INL-=0.1Vrms(inverted), Measure=OUTL, Filter=Bandpass



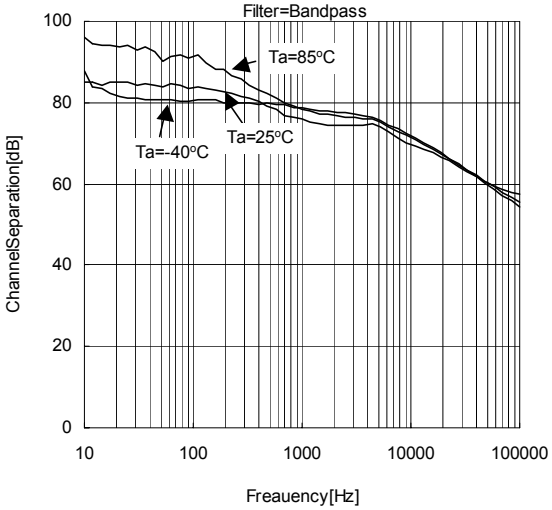
MuteLevel vs Frequency

V+=3.3V, RL=10kΩ, MUTE=H, GAIN=L, INL+=0.1Vrms
INL-=0.1Vrms(inverted), Measure=OUTL, Filter=Bandpass



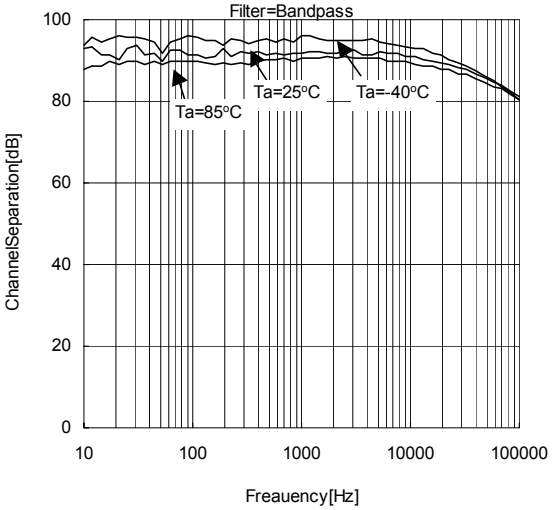
ChannelSeparation vs Frequency

V+=3.3V, RL=32Ω, Rg=600Ω , MUTE=H, GAIN=L,
INL+=0.1Vrms, INL-=0.1Vrms(inverted), Measure=OUTR
Filter=Bandpass



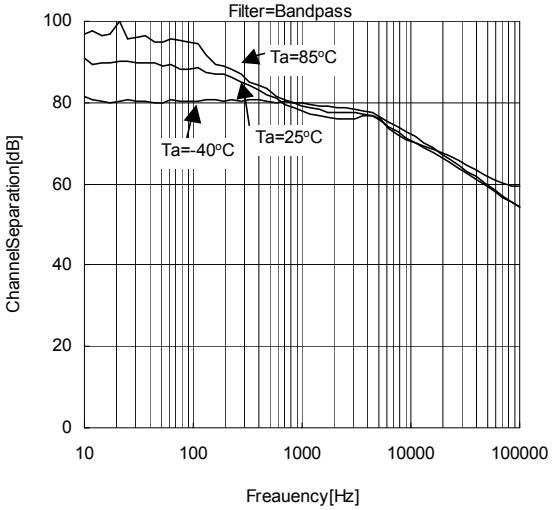
ChannelSeparation vs Frequency

V+=3.3V, RL=10kΩ, Rg=600Ω, MUTE=H, GAIN=L,
INL+=0.1Vrms, INL-=0.1Vrms(inverted), Measure=OUTR
Filter=Bandpass



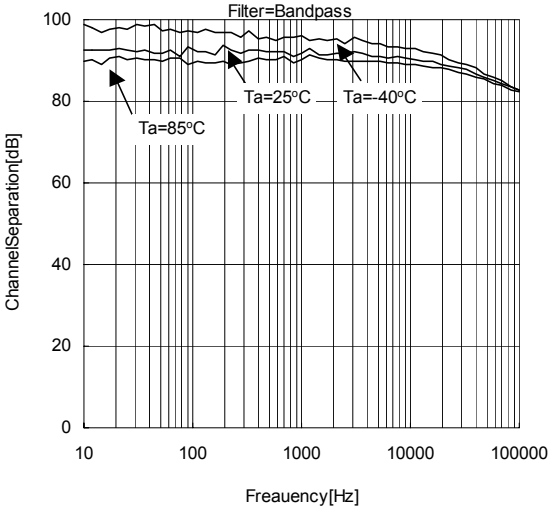
ChannelSeparation vs Frequency

V+=3.3V, RL=32Ω, Rg=600Ω, MUTE=H, GAIN=L
INR+=0.1Vrms, INR-=0.1Vrms(inverted), Measure=OUTL
Filter=Bandpass



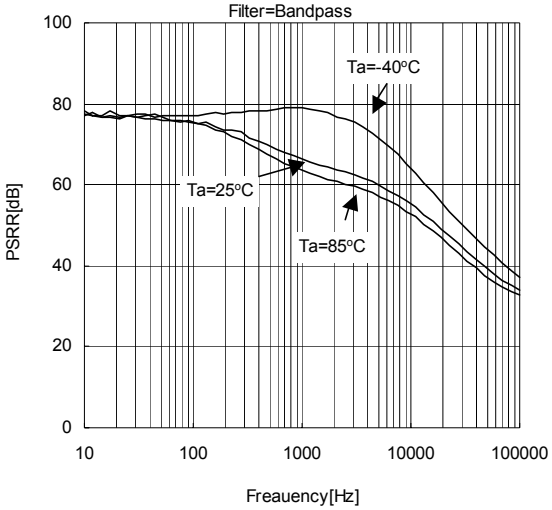
ChannelSeparation vs Frequency

V+=3.3V, RL=10kΩ, Rg=600Ω, MUTE=H, GAIN=L
INR+=0.1Vrms, INR-=0.1Vrms(inverted), Measure=OUTL
Filter=Bandpass



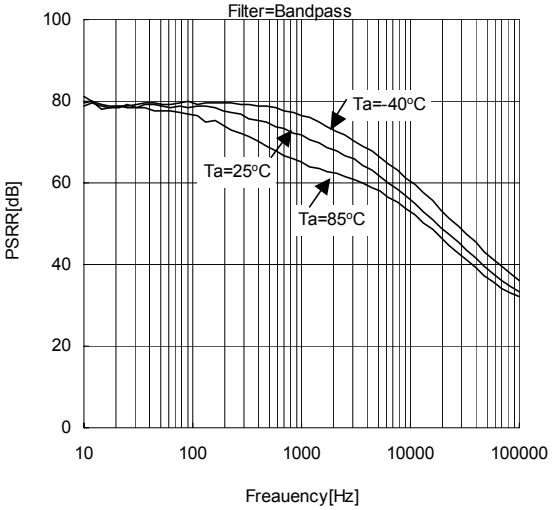
PSRR vs Frequency

V+=3.3V, RL=32Ω, MUTE=H, GAIN=L, Vripple=0.1Vrms
INL+=INR+=0Vrms, INL-=INR-=0Vrms, Measure=OUTL,OUTR
Filter=Bandpass



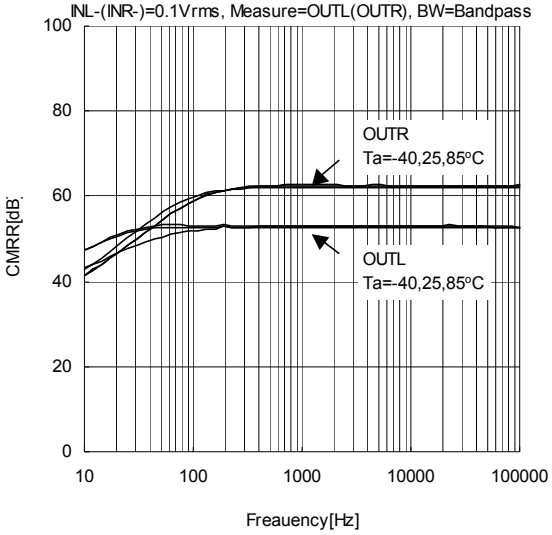
PSRR vs Frequency

V+=3.3V, RL=10kΩ, MUTE=H, GAIN=L, Vripple=0.1Vrms
INL+=INR+=0Vrms, INL-=INR-=0Vrms, Measure=OUTL,OUTR
Filter=Bandpass



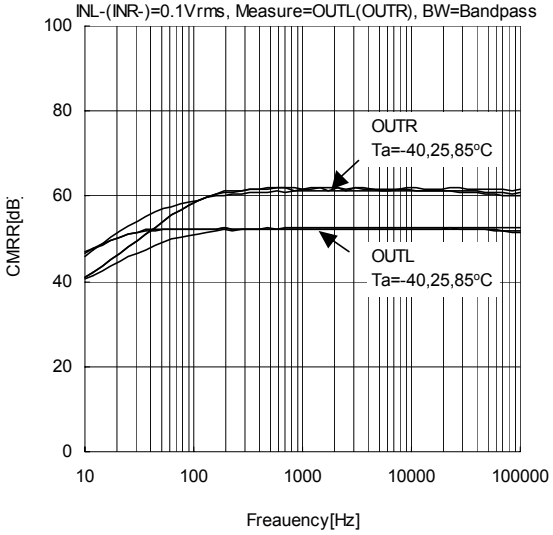
CMRR vs Frequency

V+=3.3V, RL=32Ω, MUTE=H, GAIN=L, INL+(INR+)=0.1Vrms
INL-(INR-)=0.1Vrms, Measure=OUTL(OUTR), BW=Bandpass



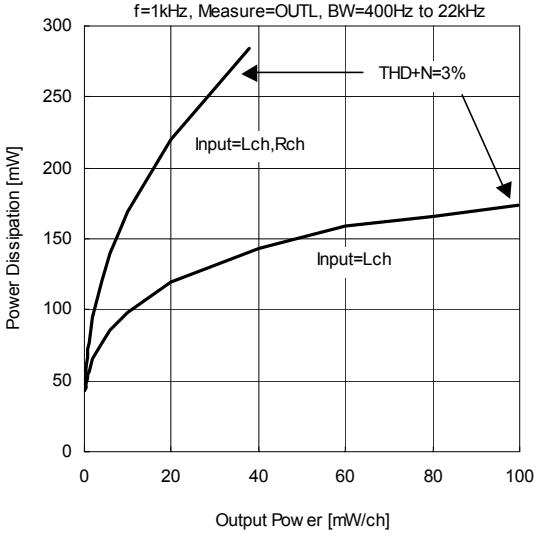
CMRR vs Frequency

V+=3.3V, RL=10kΩ , MUTE=H , GAIN=L,INL+(INR+)=0.1Vrms
INL-(INR-)=0.1Vrms, Measure=OUTL(OUTR), BW=Bandpass



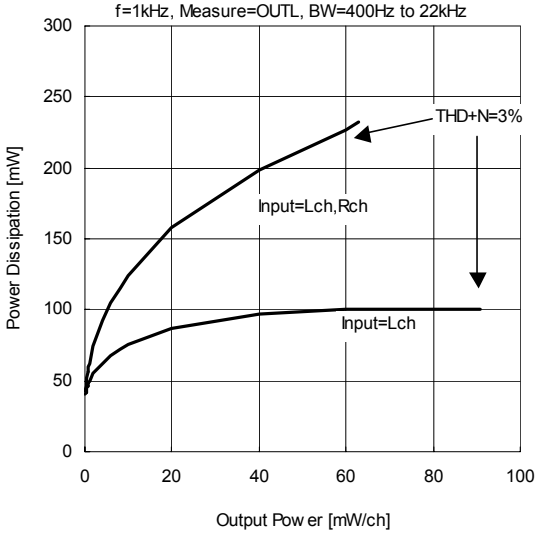
Power Dissipation vs Output Power

V+=3.3V, RL=16Ω, MUTE=H, GAIN=L, Ta=25°C
f=1kHz, Measure=OUTL, BW=400Hz to 22kHz



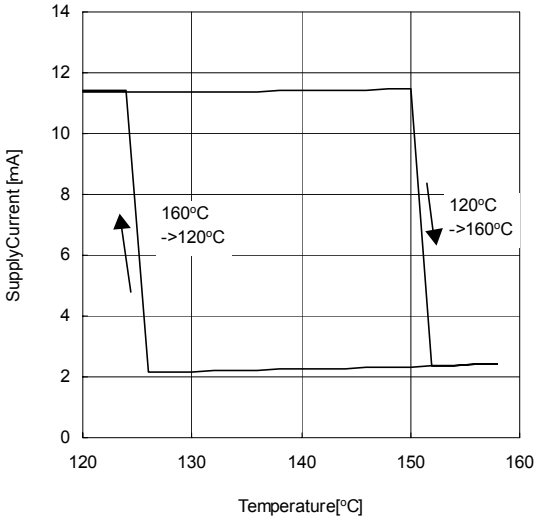
Power Dissipation vs Output Power

V+=3.3V, RL=32Ω, MUTE=H, GAIN=L, Ta=25°C
f=1kHz, Measure=OUTL, BW=400Hz to 22kHz

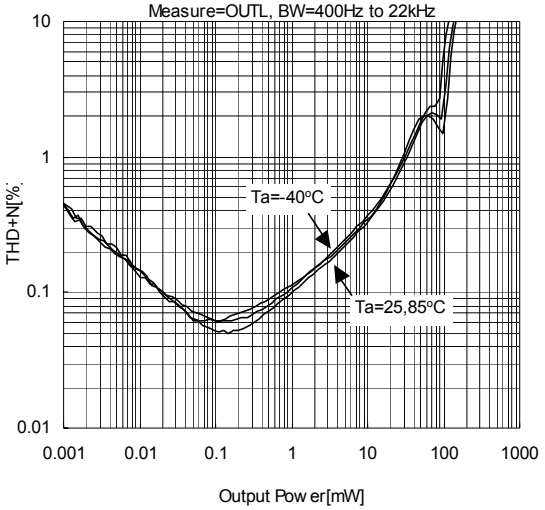


Thermal Shut Down(SupplyCurrent)

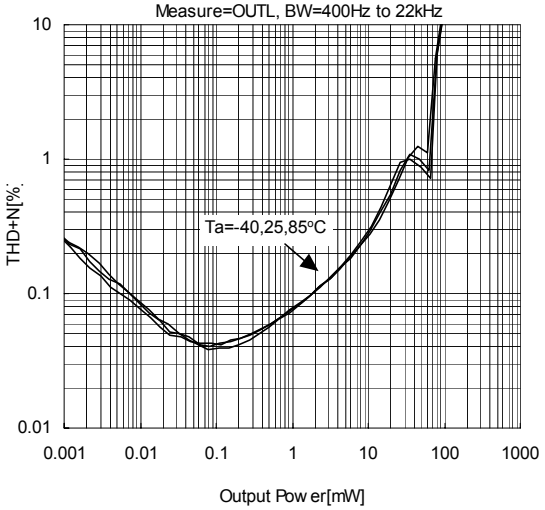
V+=3.3V , RL=32Ω , MUTE=H , GAIN=L



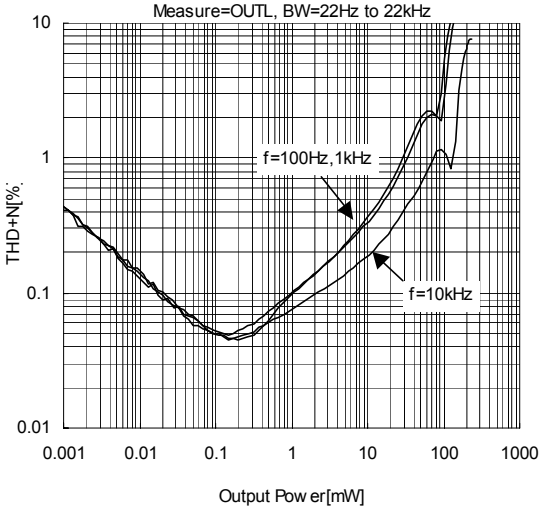
THD+N vs Output Power
V+=3.3V, RL=16Ω, MUTE=H , GAIN=L
Input=INL+,INL-(inverted), AC_GND=INR+,INR-, f=1kHz
Measure=OUTL, BW=400Hz to 22kHz



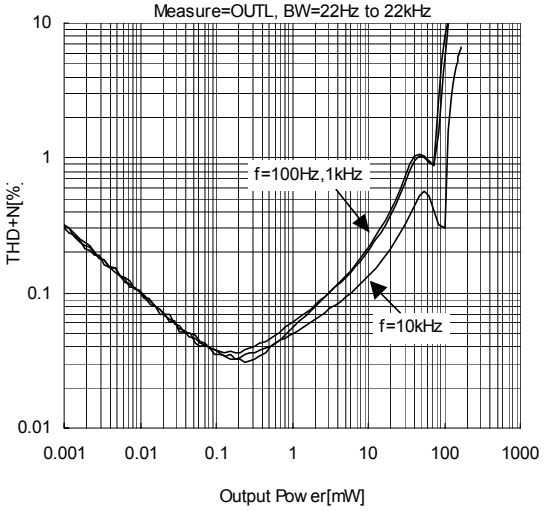
THD+N vs Output Power
V+=3.3V, RL=32Ω, MUTE=H, GAIN=L
Input=INL+,INL-(inverted), AC_GND=INR+,INR-, f=1kHz
Measure=OUTL, BW=400Hz to 22kHz



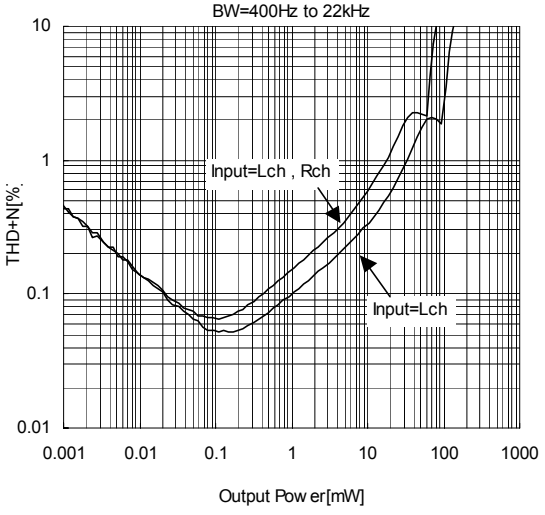
THD+N vs Output Power
V+=3.3V, RL=16Ω, MUTE=H, GAIN=L, Ta=25°C
Input=INL+,INL-(inverted), AC_GND=INR+,INR-, f=1kHz
Measure=OUTL, BW=22Hz to 22kHz



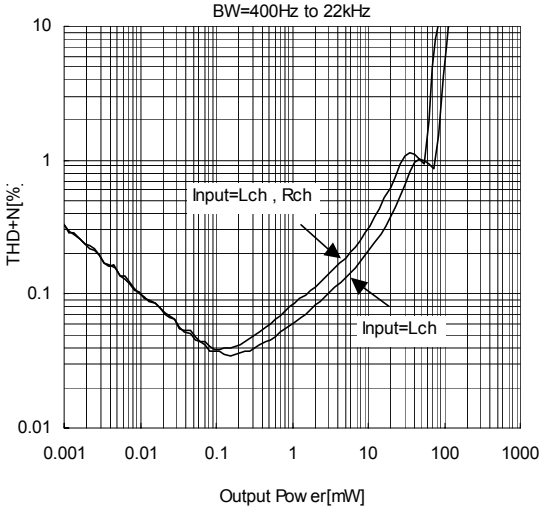
THD+N vs Output Power
V+=3.3V, RL=32Ω, MUTE=H, GAIN=L, Ta=25°C
Input=INL+,INL-(inverted), AC_GND=INR+,INR-, f=1kHz
Measure=OUTL, BW=22Hz to 22kHz



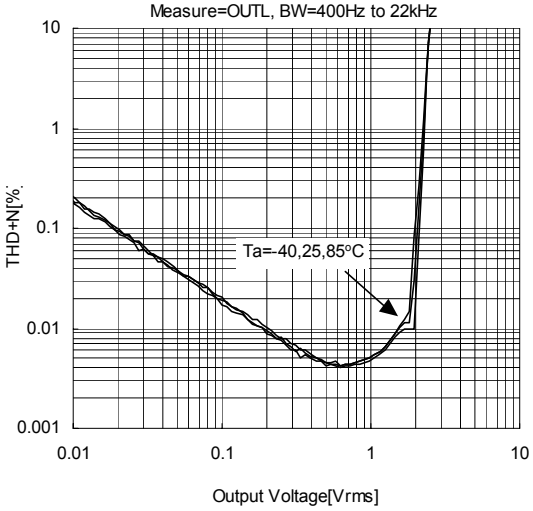
THD+N vs Output Power
V+=3.3V, RL=16Ω, MUTE=H , GAIN=L
Input=INL+/R+,INL-/R-(inverted), f=1kHz, Measure=OUTL,
BW=400Hz to 22kHz



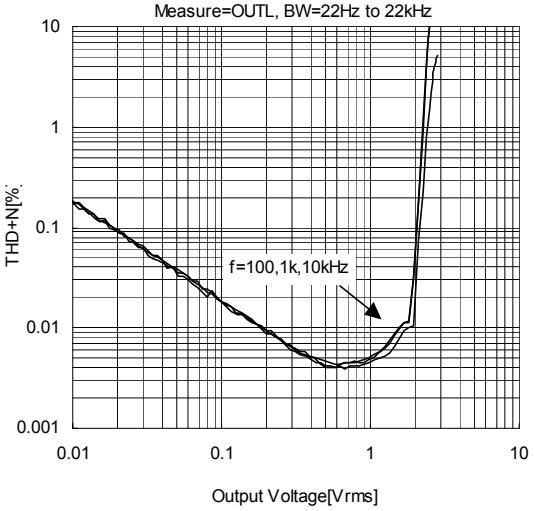
THD+N vs Output Power
V+=3.3V, RL=32Ω, MUTE=H, GAIN=L
Input=INL+/R+,INL-/R-(inverted), f=1kHz, Measure=OUTL
BW=400Hz to 22kHz



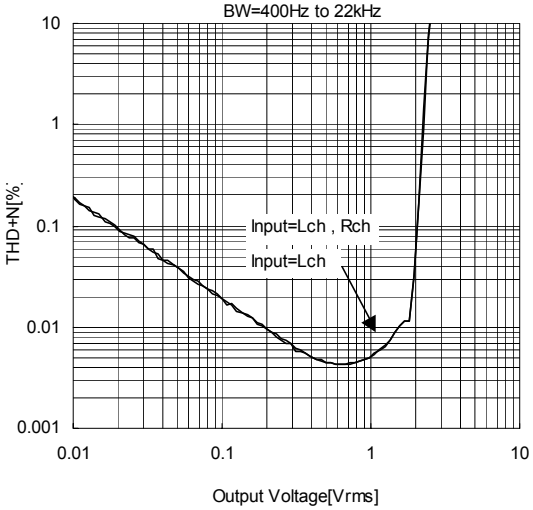
THD+N vs Output Voltage
V+=3.3V, RL=10kΩ, MUTE=H , GAIN=L
Input=INL+,INL-(inverted), AC_GND=INR+,INR-, f=1kHz
Measure=OUTL, BW=400Hz to 22kHz



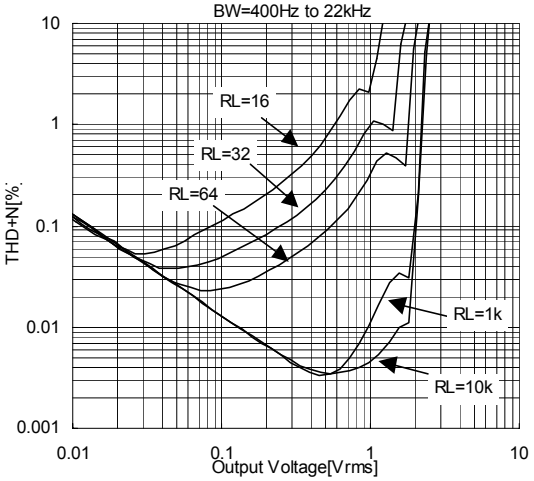
THD+N vs Output Voltage
V+=3.3V, RL=10kΩ, MUTE=H, GAIN=L, Ta=25°C
Input=INL+,INL-(inverted), AC_GND=INR+,INR-, f=1kHz
Measure=OUTL, BW=22Hz to 22kHz



THD+N vs Output Voltage
V+=3.3V, RL=10kΩ, MUTE=H, GAIN=L
Input=INL+/R+,INL-/R-(inverted), f=1kHz, Measure=OUTL
BW=400Hz to 22kHz



THD+N vs Output Voltage
V+=3.3V, MUTE=H, GAIN=L, Ta=25°C
Input=INL+,INL-(inverted), f=1kHz, Measure=OUTL ,
BW=400Hz to 22kHz



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