



# PCA9534

8-bit I<sup>2</sup>C-bus and SMBus low power I/O port with interrupt

Rev. 03 — 6 November 2006

Product data sheet

## 1. General description

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The PCA9534 is a 16-pin CMOS device that provide 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I<sup>2</sup>C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I<sup>2</sup>C-bus I/O expanders. The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, 400 kHz clock frequency, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PCA9534 consists of an 8-bit Configuration register (Input or Output selection); 8-bit Input register, 8-bit Output register and an 8-bit Polarity Inversion register (active HIGH or active LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master. Although pin-to-pin and I<sup>2</sup>C-bus address compatible with the PCF8574 series, software changes are required due to the enhancements and are discussed in *Application Note AN469*.

The PCA9534 is identical to the PCA9554 except for the removal of the internal I/O pull-up resistor which greatly reduces power consumption when the I/Os are held LOW.

The PCA9534 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I<sup>2</sup>C-bus address and allow up to eight devices to share the same I<sup>2</sup>C-bus/SMBus.

## 2. Features

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- 8-bit I<sup>2</sup>C-bus GPIO
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset

- 8 I/O pins which default to 8 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Offered in four different packages: SO16, TSSOP16, and HVQFN16 (4 × 4 × 0.85 mm and 3 × 3 × 0.85 mm versions)

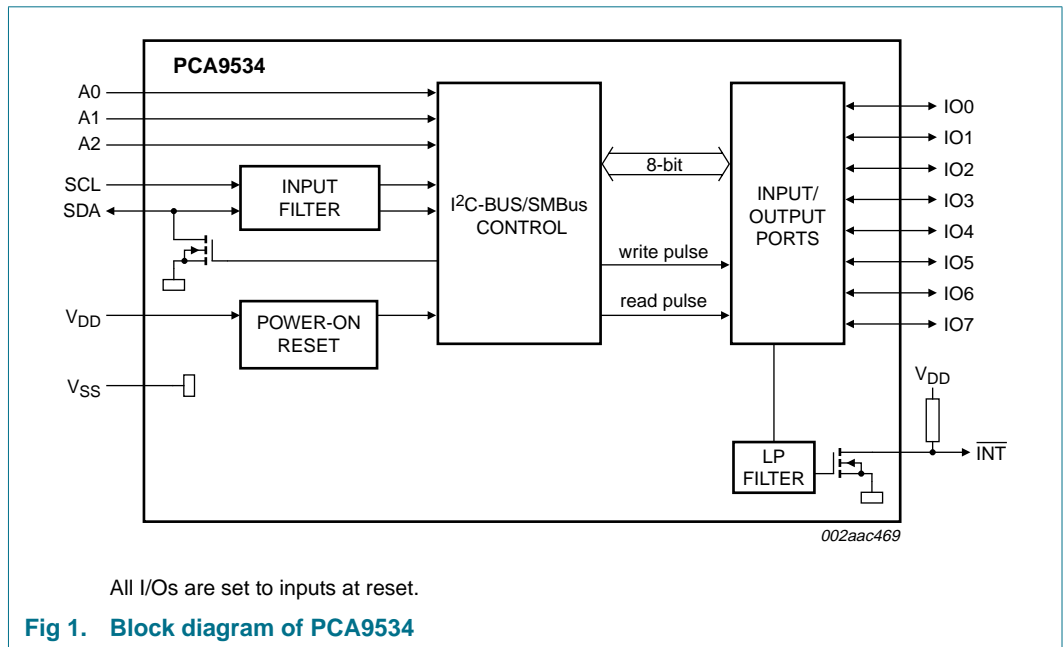
### 3. Ordering information

**Table 1. Ordering information**

*T<sub>amb</sub> = -40 °C to +85 °C.*

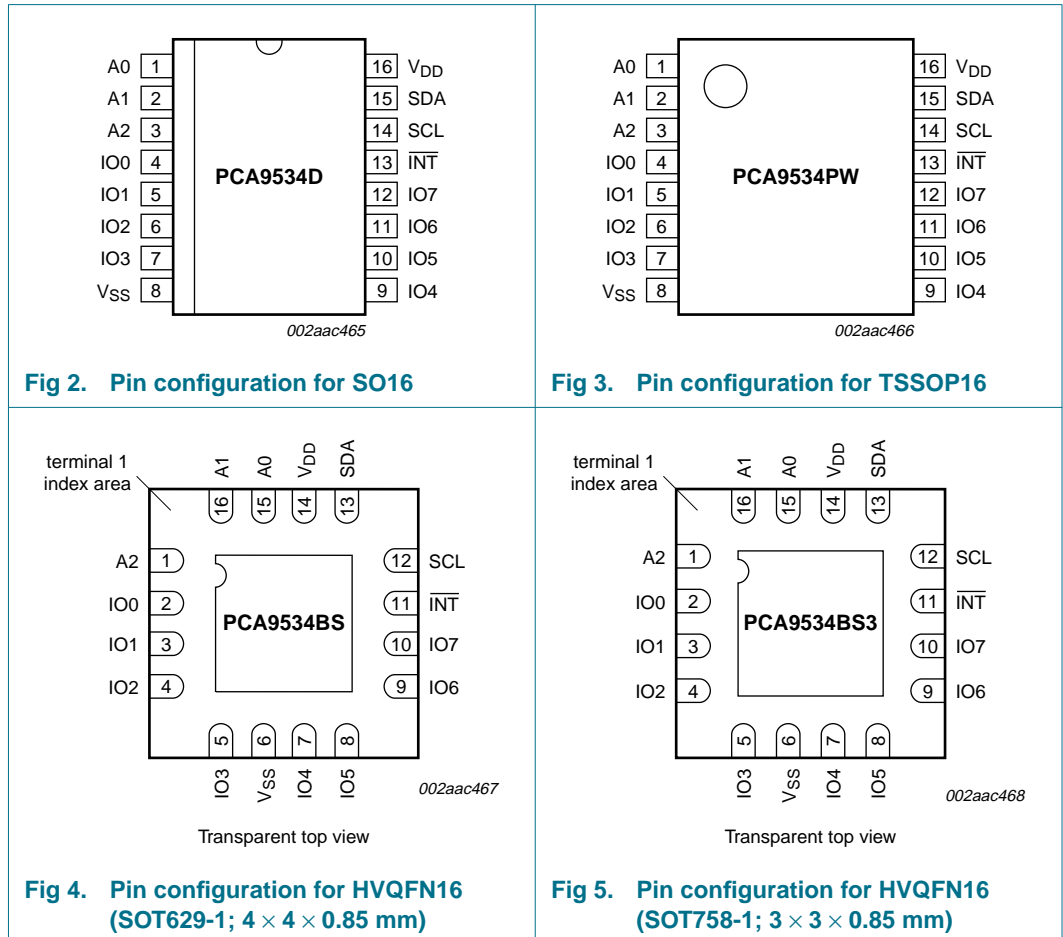
Type number	Topside mark	Package		Version
		Name	Description	
PCA9534D	PCA9534D	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA9534PW	PCA9534	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9534BS	9534	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 × 4 × 0.85 mm	SOT629-1
PCA9534BS3	P34	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1

### 4. Block diagram



## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
A0	1	15	address input 0
A1	2	16	address input 1
A2	3	1	address input 2
IO0	4	2	input/output 0
IO1	5	3	input/output 1
IO2	6	4	input/output 2
IO3	7	5	input/output 3
V <sub>SS</sub>	8	6 <sup>[1]</sup>	ground supply voltage
IO4	9	7	input/output 4
IO5	10	8	input/output 5

**Table 2. Pin description ...continued**

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
IO6	11	9	input/output 6
IO7	12	10	input/output 7
$\overline{\text{INT}}$	13	11	interrupt output (open-drain)
SCL	14	12	serial clock line
SDA	15	13	serial data line
V <sub>DD</sub>	16	14	supply voltage

[1] HVQFN package die supply ground is connected to both V<sub>SS</sub> pin and exposed center pad. V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

## 6. Functional description

Refer to [Figure 1 “Block diagram of PCA9534”](#).

### 6.1 Registers

#### 6.1.1 Command byte

**Table 3. Command byte**

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

#### 6.1.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default ‘X’ is determined by the externally applied logic level.

**Table 4. Register 0 - Input Port register bit description**

Bit	Symbol	Access	Value	Description
7	I7	read only	X	determined by externally applied logic level
6	I6	read only	X	
5	I5	read only	X	
4	I4	read only	X	
3	I3	read only	X	
2	I2	read only	X	
1	I1	read only	X	
0	I0	read only	X	

### 6.1.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

**Table 5. Register 1 - Output Port register bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	O7	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

### 6.1.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

**Table 6. Register 2 - Polarity Inversion register bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	inverts polarity of Input Port register data
6	N6	R/W	0*	
5	N5	R/W	0*	1 = Input Port register data inverted
4	N4	R/W	0*	
3	N3	R/W	0*	
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

### 6.1.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs.

**Table 7. Register 3 - Configuration register bit description**

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	configures the directions of the I/O pins
6	C6	R/W	1*	0 = corresponding port pin enabled as an output
5	C5	R/W	1*	1 = corresponding port pin configured as input (default value)
4	C4	R/W	1*	
3	C3	R/W	1*	
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

## 6.2 Power-on reset

When power is applied to  $V_{DD}$ , an internal Power-On Reset (POR) holds the PCA9534 in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the PCA9534 registers and state machine will initialize to their default states. Thereafter,  $V_{DD}$  must be lowered below 0.2 V to reset the device.

For a power reset cycle,  $V_{DD}$  must be lowered below 0.2 V and then restored to the operating voltage.

## 6.3 Interrupt output

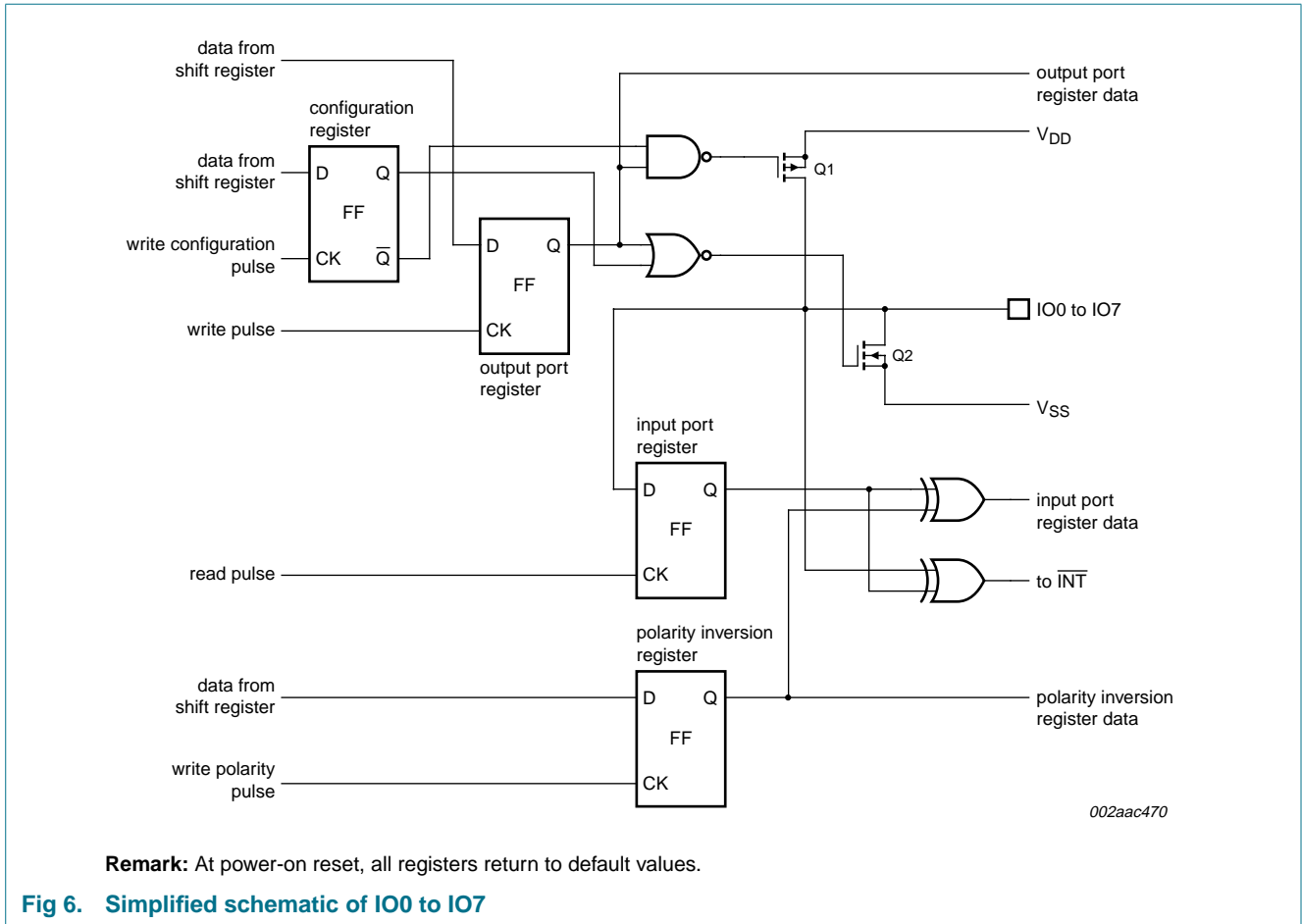
The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

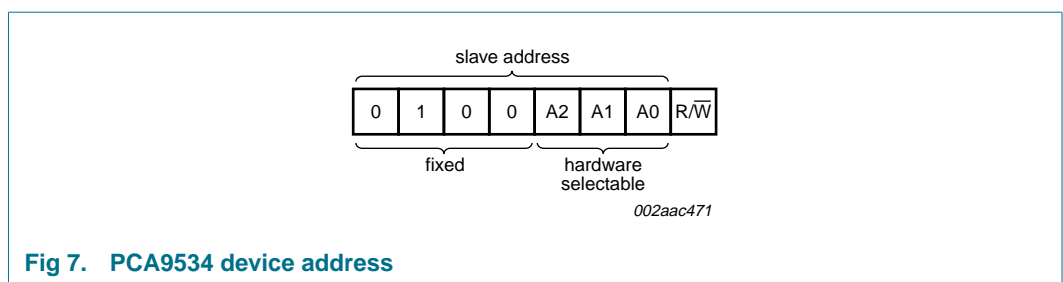
## 6.4 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above  $V_{DD}$  to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either  $V_{DD}$  or  $V_{SS}$ .



### 6.5 Device address



### 6.6 Bus transactions

Data is transmitted to the PCA9534 registers using the Write mode as shown in [Figure 8](#) and [Figure 9](#). Data is read from the PCA9534 registers using the Read mode as shown in [Figure 10](#) and [Figure 11](#). These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

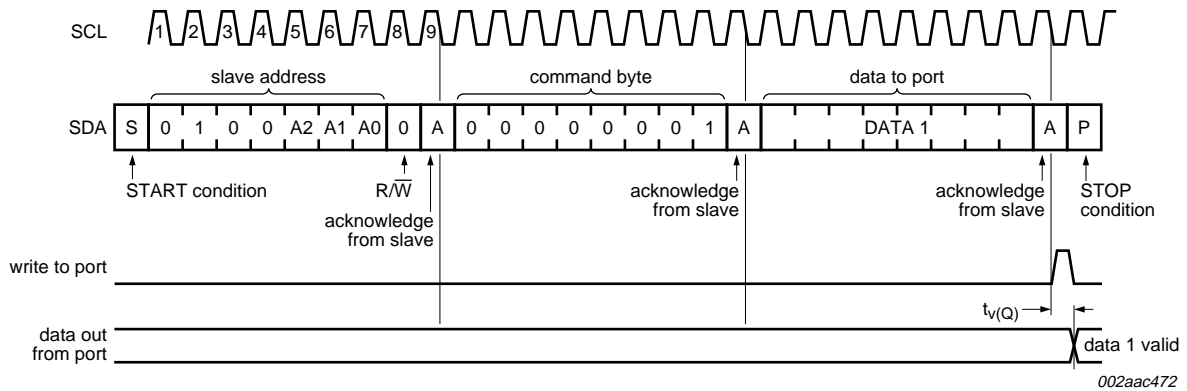


Fig 8. Write to Output Port register

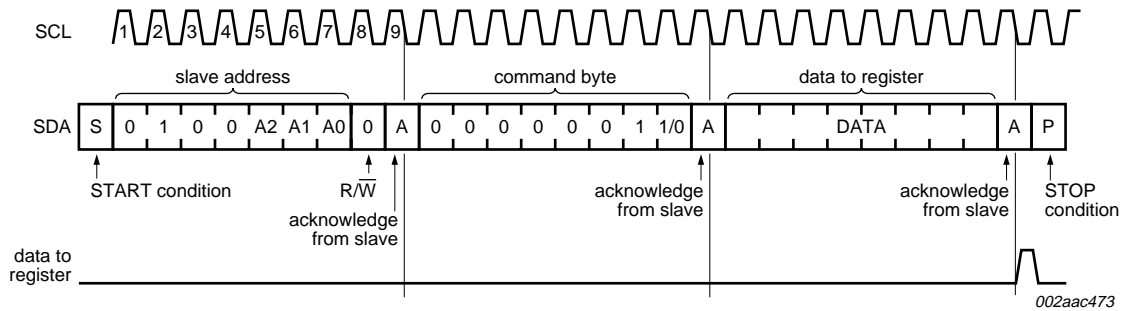


Fig 9. Write to Configuration register or Polarity Inversion register

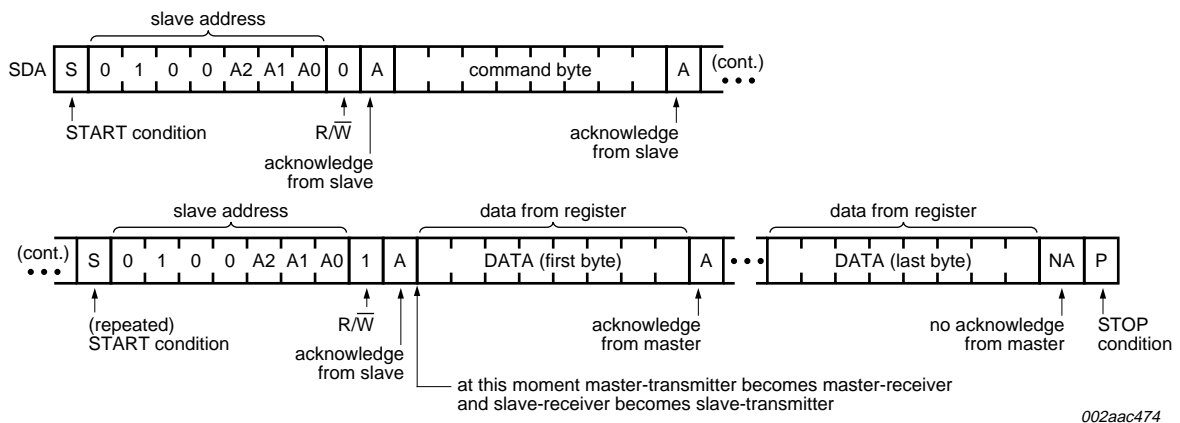
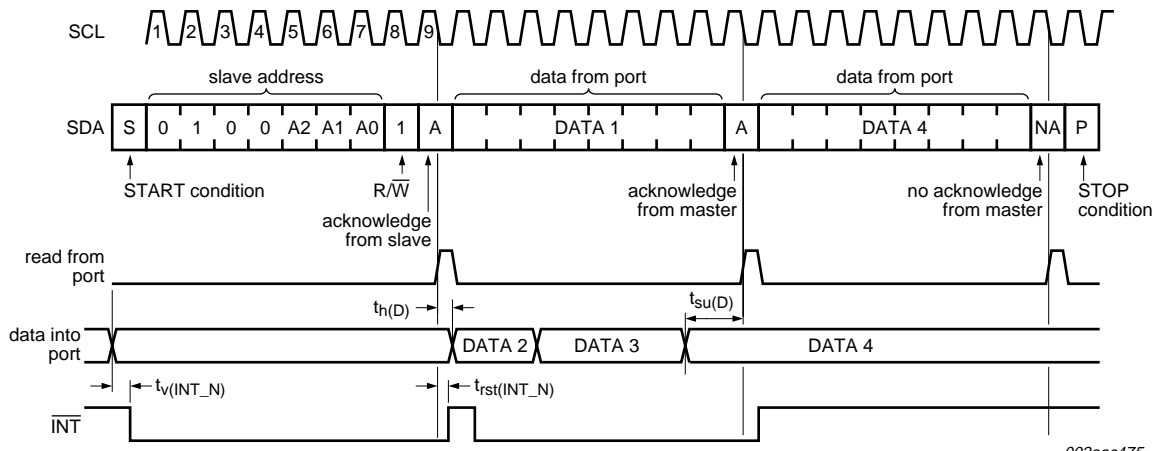


Fig 10. Read from register

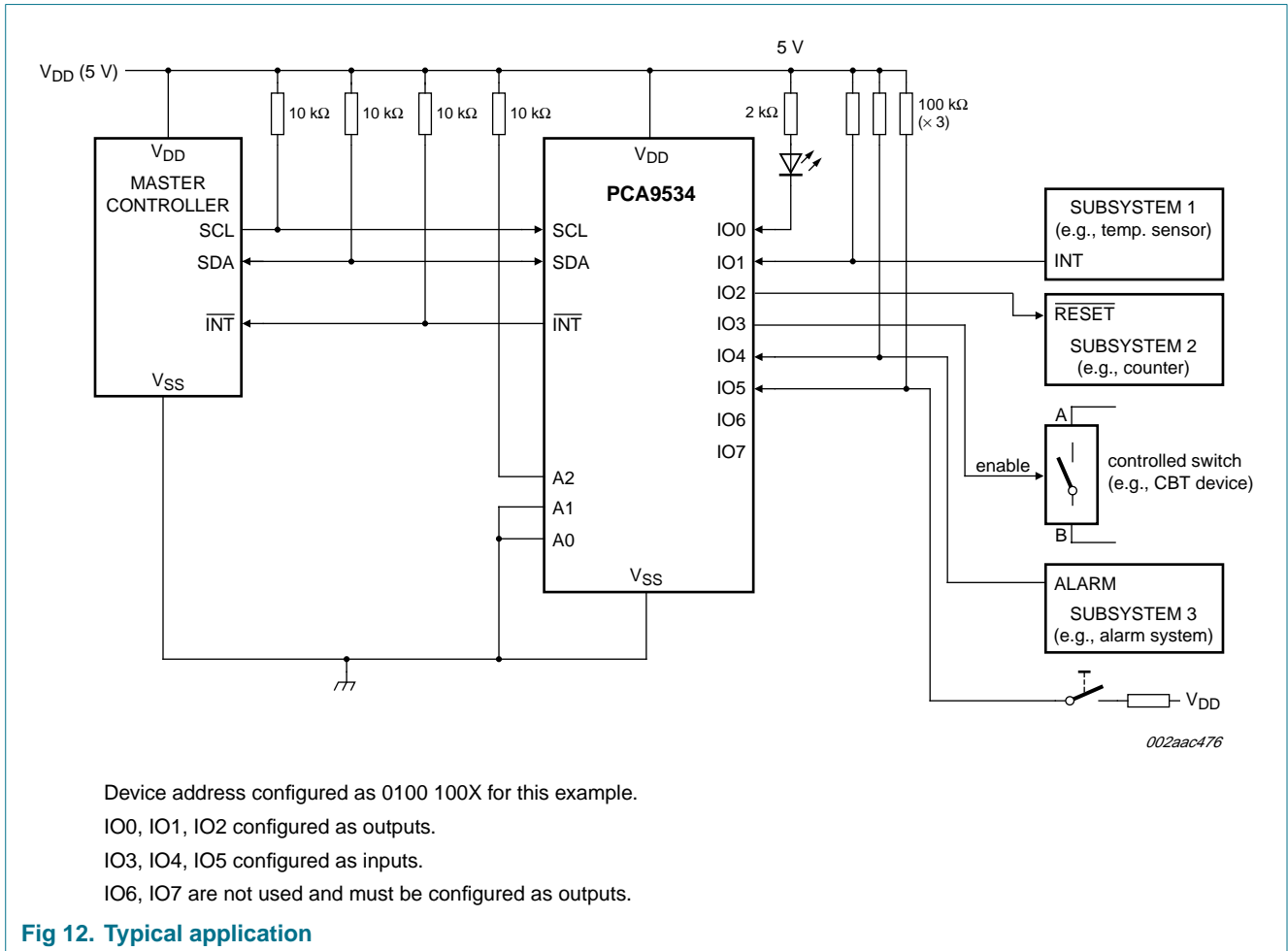




This figure assumes the command byte has previously been programmed with 00h.  
 Transfer of data can be stopped at any moment by a STOP condition.

**Fig 11. Read Input Port register**

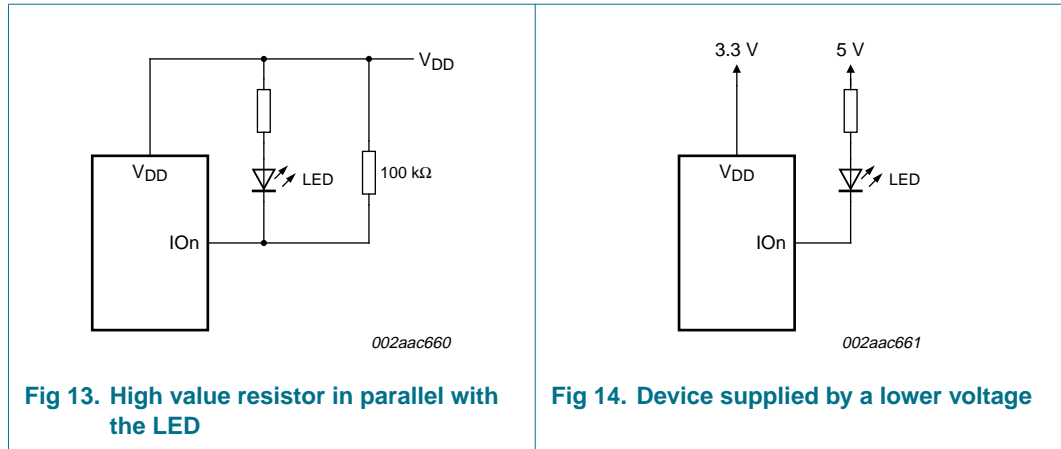
## 7. Application design-in information



### 7.1 Minimizing I<sub>DD</sub> when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V<sub>DD</sub> through a resistor as shown in Figure 12. Since the LED acts as a diode, when the LED is off the I/O V<sub>I</sub> is about 1.2 V less than V<sub>DD</sub>. The supply current, I<sub>DD</sub>, increases as V<sub>I</sub> becomes lower than V<sub>DD</sub>.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I<sub>On</sub> pins greater than or equal to V<sub>DD</sub> when the LED is off. Figure 13 shows a high value resistor in parallel with the LED. Figure 14 shows V<sub>DD</sub> less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V<sub>I</sub> at or above V<sub>DD</sub> and prevents additional supply current consumption when the LED is off.



## 8. Limiting values

**Table 8. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+6.0	V
I <sub>I</sub>	input current		-	±20	mA
V <sub>I/O</sub>	voltage on an input/output pin		V <sub>SS</sub> - 0.5	5.5	V
I <sub>O(IOn)</sub>	output current on pin IO <sub>n</sub>		-	±50	mA
I <sub>DD</sub>	supply current		-	85	mA
I <sub>SS</sub>	ground supply current		-	100	mA
P <sub>tot</sub>	total power dissipation		-	200	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C

## 9. Static characteristics

**Table 9. Static characteristics**
 $V_{DD} = 2.3\text{ V to }5.5\text{ V}; V_{SS} = 0\text{ V}; T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C};$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
$V_{DD}$	supply voltage		2.3	-	5.5	V
$I_{DD}$	supply current	operating mode; $V_{DD} = 5.5\text{ V}$ ; no load; $f_{SCL} = 100\text{ kHz}$	-	104	175	$\mu\text{A}$
$I_{stb}$	standby current	Standby mode; $V_{DD} = 5.5\text{ V}$ ; no load; $f_{SCL} = 0\text{ kHz}$ ; I/O = inputs				
		$V_I = V_{SS}$	-	0.25	1	$\mu\text{A}$
		$V_I = V_{DD}$	-	0.25	1	$\mu\text{A}$
$V_{POR}$	power-on reset voltage	no load; $V_I = V_{DD}$ or $V_{SS}$	[1] -	1.5	1.65	V
<b>Input SCL; input/output SDA</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.7 $V_{DD}$	-	5.5	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	6	-	mA
$I_L$	leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance	$V_I = V_{SS}$	-	5	10	pF
<b>I/Os</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	5.5	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.5\text{ V}; V_{DD} = 2.3\text{ V}$	[2] 8	10	-	mA
		$V_{OL} = 0.7\text{ V}; V_{DD} = 2.3\text{ V}$	[2] 10	13	-	mA
		$V_{OL} = 0.5\text{ V}; V_{DD} = 3.0\text{ V}$	[2] 8	14	-	mA
		$V_{OL} = 0.7\text{ V}; V_{DD} = 3.0\text{ V}$	[2] 10	19	-	mA
		$V_{OL} = 0.5\text{ V}; V_{DD} = 4.5\text{ V}$	[2] 8	17	-	mA
		$V_{OL} = 0.7\text{ V}; V_{DD} = 4.5\text{ V}$	[2] 10	24	-	mA
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -8\text{ mA}; V_{DD} = 2.3\text{ V}$	[3] 1.8	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 2.3\text{ V}$	[3] 1.7	-	-	V
		$I_{OH} = -8\text{ mA}; V_{DD} = 3.0\text{ V}$	[3] 2.6	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 3.0\text{ V}$	[3] 2.5	-	-	V
		$I_{OH} = -8\text{ mA}; V_{DD} = 4.75\text{ V}$	[3] 4.1	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 4.75\text{ V}$	[3] 4.0	-	-	V
$I_{LI}$	input leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance		-	5	10	pF
<b>Interrupt INT</b>						
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	-	-	mA
<b>Select inputs A0, A1, A2</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	5.5	V
$I_{LI}$	input leakage current		-1	-	1	$\mu\text{A}$

- [1]  $V_{DD}$  must be lowered to 0.2 V in order to reset part.  
 [2] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.  
 [3] The total current sourced by all I/Os must be limited to 85 mA.

## 10. Dynamic characteristics

**Table 10. Dynamic characteristics**

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
$f_{SCL}$	SCL clock frequency		0	100	0	400	kHz
$t_{BUF}$	bus free time between a STOP and START condition		4.7	-	1.3	-	$\mu$ s
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	$\mu$ s
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	$\mu$ s
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	$\mu$ s
$t_{HD;DAT}$	data hold time		0	-	0	-	$\mu$ s
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	$\mu$ s
$t_{VD;DAT}$	data valid time	[2]	300	-	50	-	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{LOW}$	LOW period of the SCL clock		4.7	-	1.3	-	$\mu$ s
$t_{HIGH}$	HIGH period of the SCL clock		4.0	-	0.6	-	$\mu$ s
$t_r$	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$ [3]	300	ns
$t_f$	fall time of both SDA and SCL signals		-	300	$20 + 0.1C_b$ [3]	300	$\mu$ s
$t_{SP}$	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
<b>Port timing</b>							
$t_{V(Q)}$	data output valid time		-	200	-	200	ns
$t_{su(D)}$	data input setup time		100	-	100	-	ns
$t_{h(D)}$	data input hold time		1	-	1	-	$\mu$ s
<b>Interrupt timing</b>							
$t_{V(INT\_N)}$	valid time on pin $\overline{INT}$		-	4	-	4	$\mu$ s
$t_{rst(INT\_N)}$	reset time on pin $\overline{INT}$		-	4	-	4	$\mu$ s

- [1]  $t_{VD;ACK}$  = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.  
 [2]  $t_{VD;DAT}$  = minimum time for SDA data output to be valid following SCL LOW.  
 [3]  $C_b$  = total capacitance of one bus line in pF.

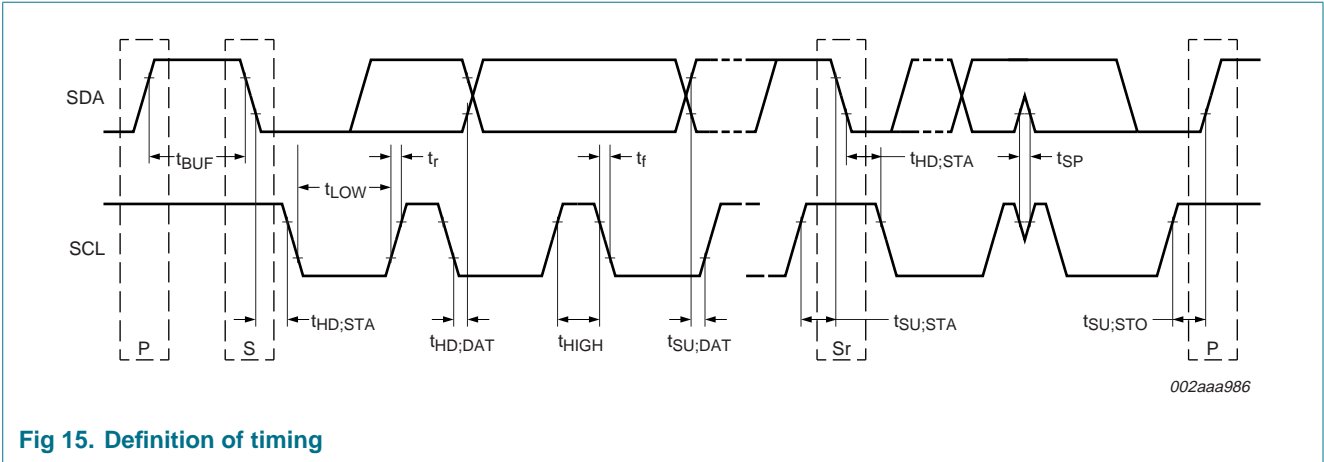


Fig 15. Definition of timing

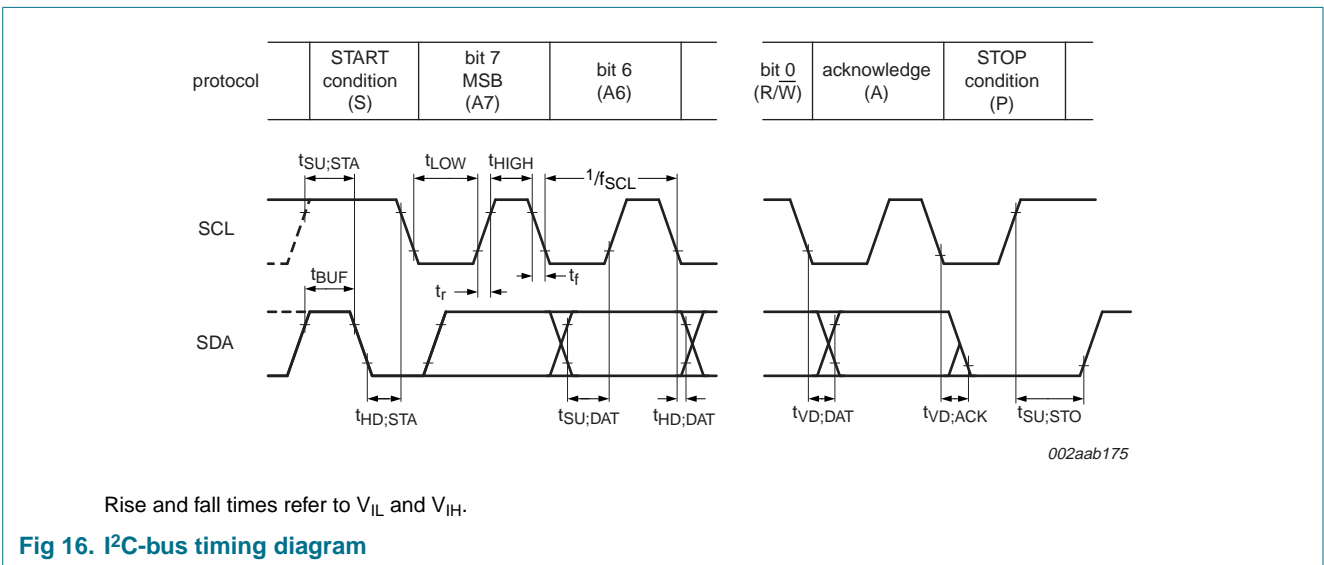


Fig 16. I<sup>2</sup>C-bus timing diagram

11. Test information

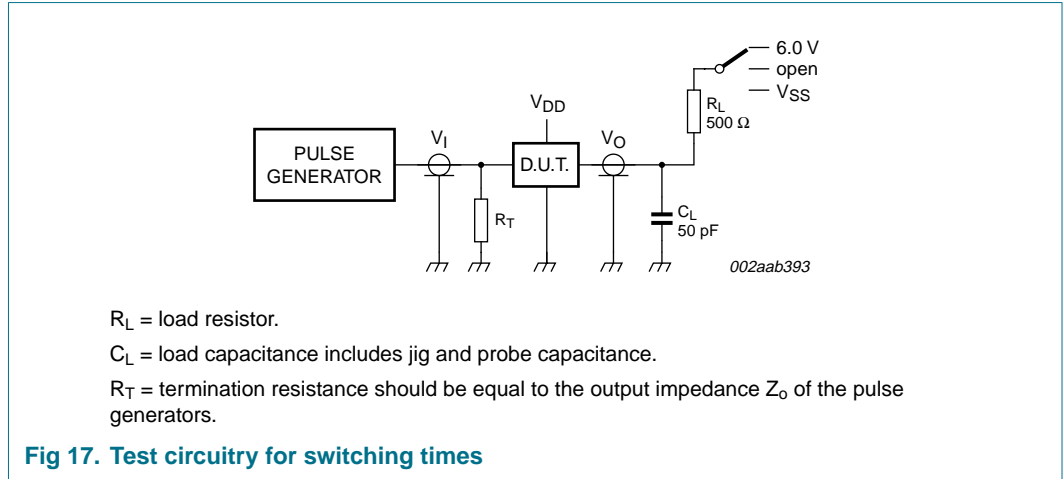


Fig 17. Test circuitry for switching times

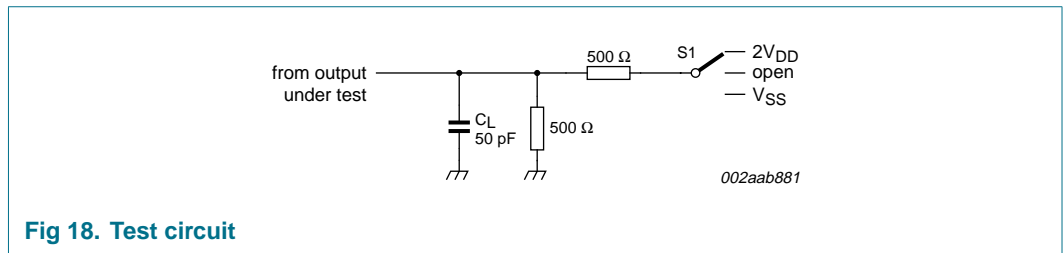


Fig 18. Test circuit

Table 11. Test data

Test	Load		Switch
	$C_L$	$R_L$	
$t_{v(Q)}$	50 pF	500 $\Omega$	$2V_{DD}$

12. Package outline

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1

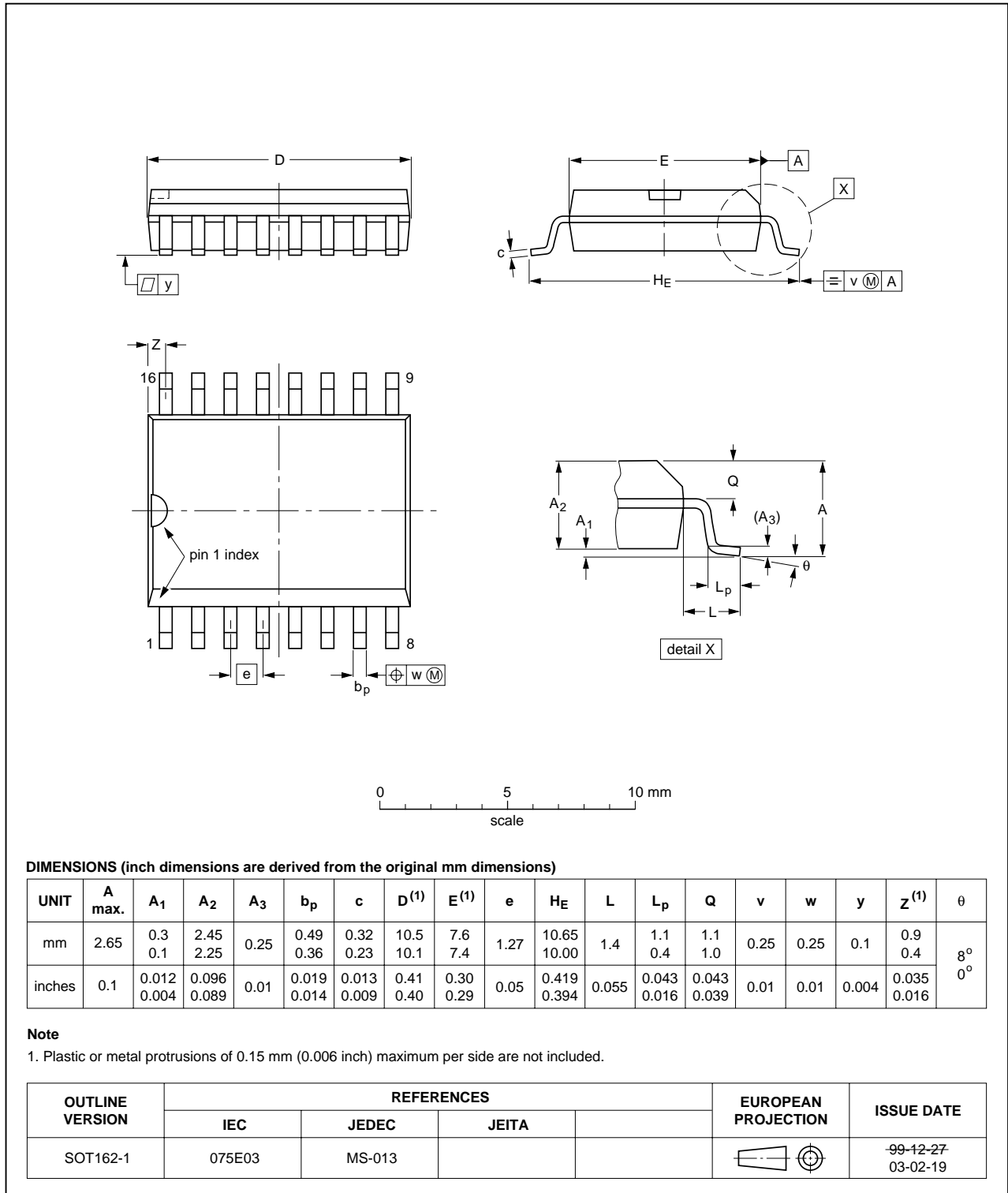


Fig 19. Package outline SOT162-1 (SO16)



TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

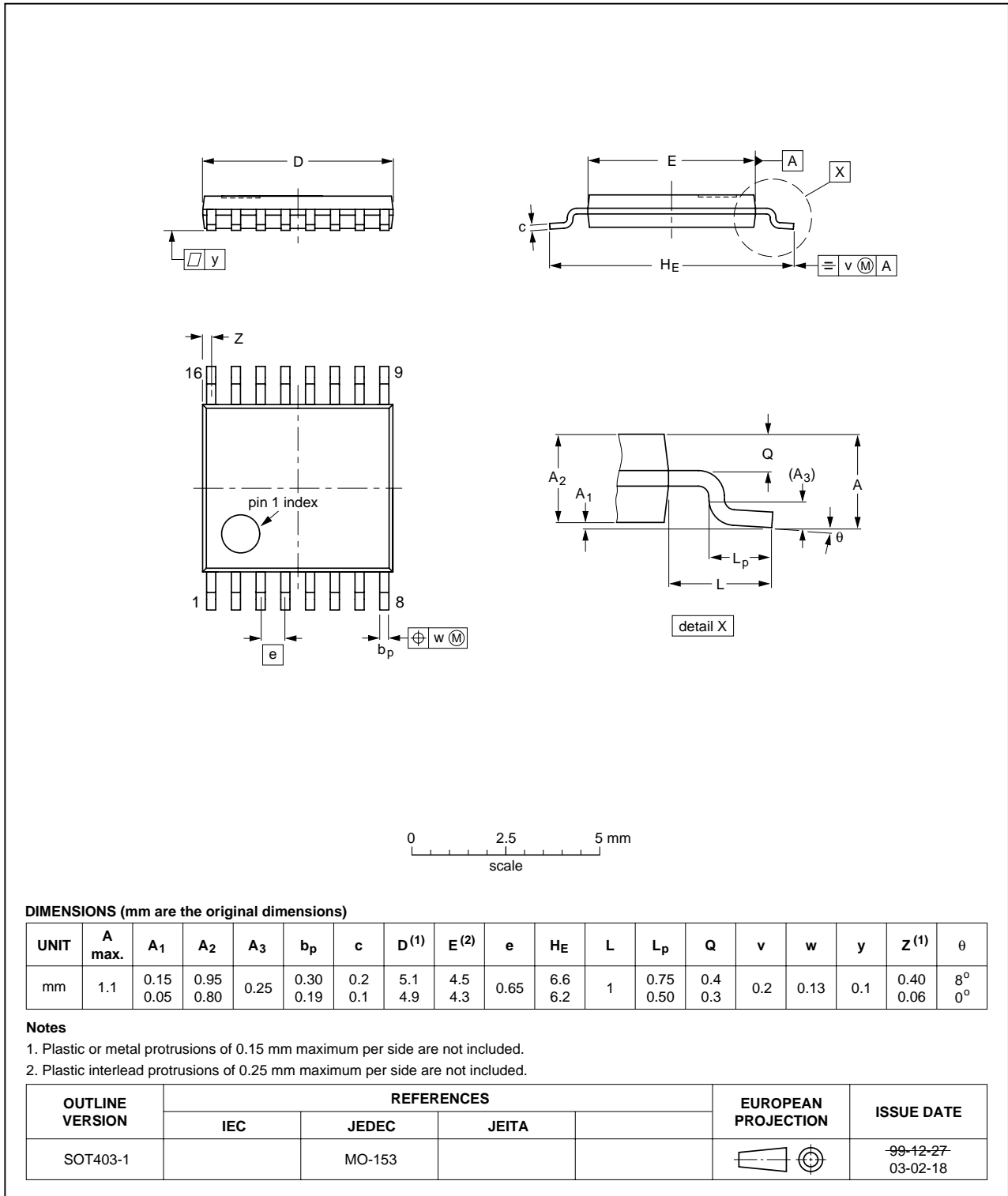


Fig 20. Package outline SOT403-1 (TSSOP16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm

SOT629-1

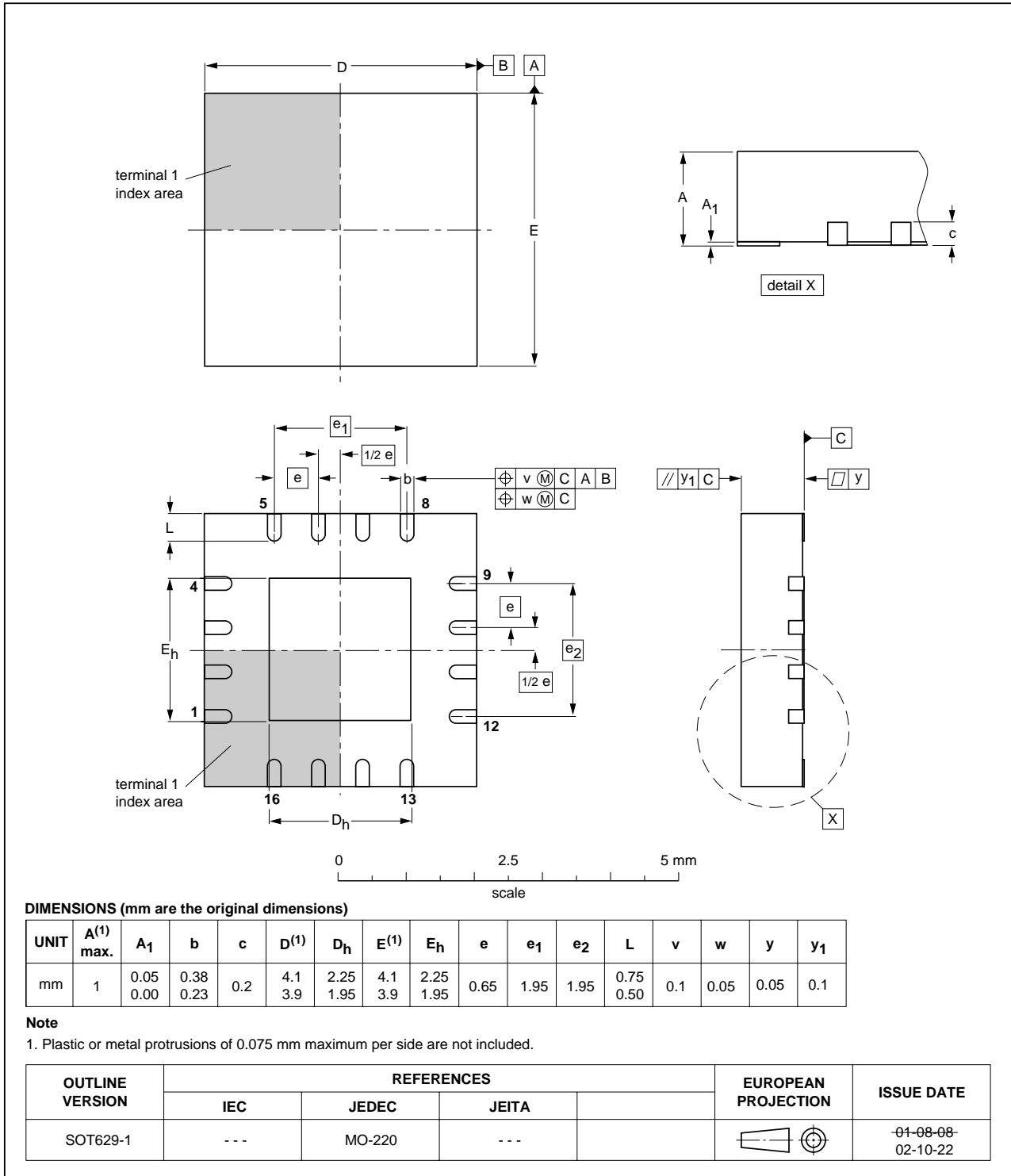


Fig 21. Package outline SOT629-1 (HVQFN16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm

SOT758-1

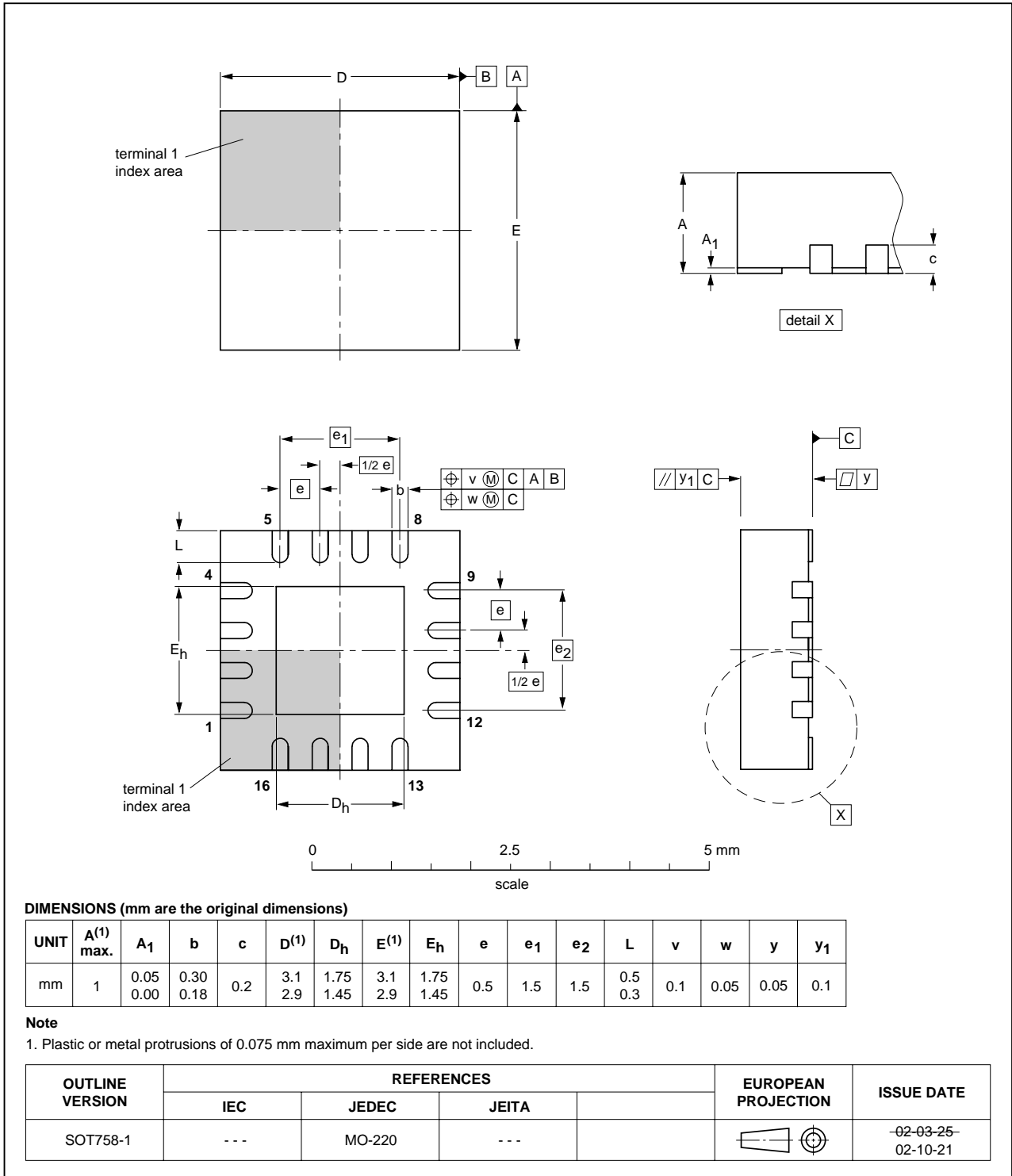


Fig 22. Package outline SOT758-1 (HVQFN16)

## 13. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

## 14. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 23](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 12](#) and [13](#)

**Table 12. SnPb eutectic process (from J-STD-020C)**

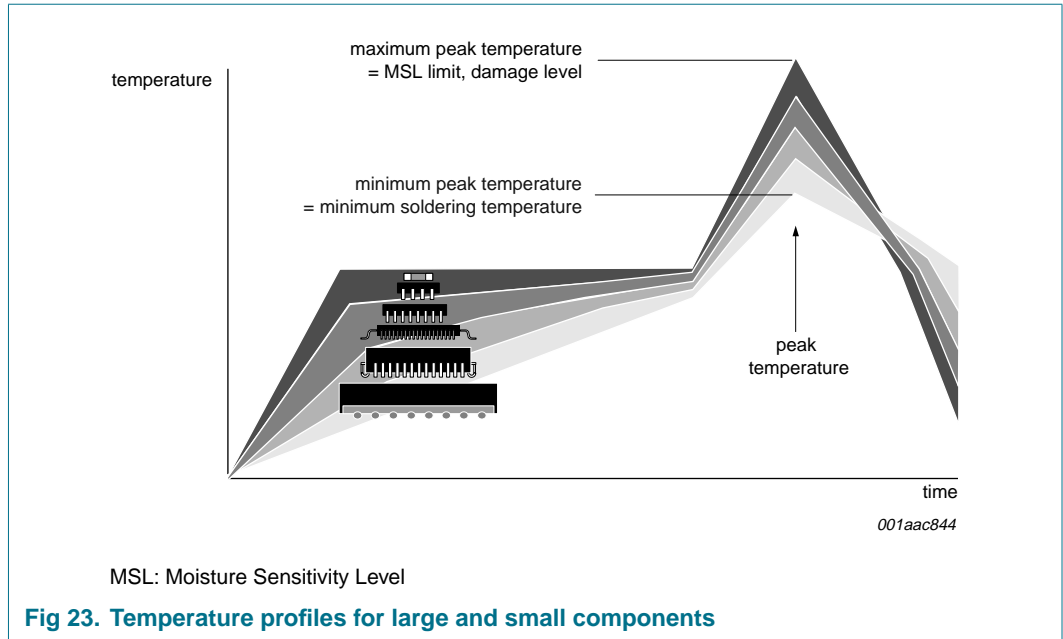
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 13. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 23](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 15. Abbreviations

**Table 14. Abbreviations**

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
MM	Machine Model
POR	Power-On Reset
SMBus	System Management Bus

## 16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9534_3	20061106	Product data sheet	-	PCA9534_2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• pin names I/O0 through I/O7 changed to IO0 through IO7</li> <li>• added HVQFN16 (SOT758-1) package</li> <li>• symbol (<math>t_{pv}</math> and <math>t_{pV}</math>) changed to <math>t_{V(Q)}</math></li> <li>• symbol (<math>t_{ph}</math> and <math>t_{pH}</math>) changed to <math>t_{h(D)}</math></li> <li>• symbol (<math>t_{ps}</math> and <math>t_{pS}</math>) changed to <math>t_{su(D)}</math></li> <li>• symbol (<math>t_{iv}</math> and <math>t_{iV}</math>) changed to <math>t_{V(INT\_N)}</math></li> <li>• symbol (<math>t_{ir}</math> and <math>t_{iR}</math>) changed to <math>t_{rst(INT\_N)}</math></li> <li>• <a href="#">Figure 6 “Simplified schematic of IO0 to IO7”</a>: removed ESD diodes</li> <li>• <a href="#">Table 8 “Limiting values”</a>: symbol “<math>I_{I/O}</math>, DC output current on an I/O” changed to “<math>I_{O(IO_n)}</math>, output current on pin IO<sub>n</sub>”</li> <li>• <a href="#">Table 9 “Static characteristics”</a>, sub-section “I/Os”: symbol <math>I_{IL}</math> changed to <math>I_{LI}</math></li> <li>• added <a href="#">Section 15 “Abbreviations”</a></li> </ul>			
PCA9534_2 (9397 750 13506)	20040930	Product data sheet	-	PCA9534_1
PCA9534_1 (9397 750 12454)	20031202	Product data	ECN 853-2319 01-A14517 of 14 Nov 2003	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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