

Features

- Very High-speed: 45 ns
- Temperature ranges
 - Industrial: -40 °C to 85 °C
 - Automotive-A: -40 °C to 85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62138CV25/30/33
- Ultra low standby power
 - Typical standby current: 1 μA
 - Maximum standby current: 5 μA
- Ultra low active power
 - Typical active current: 1.6 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} Features
- Automatic power down when deselected
- complementary metal oxide semiconductor (CMOS) for Optimum speed and power
- Offered in Pb-free 36-Ball VFBGA, 32-Pin TSOP II, 32-Pin SOIC, 32-Pin TSOP I and 32-Pin STSOP Packages

Functional Description

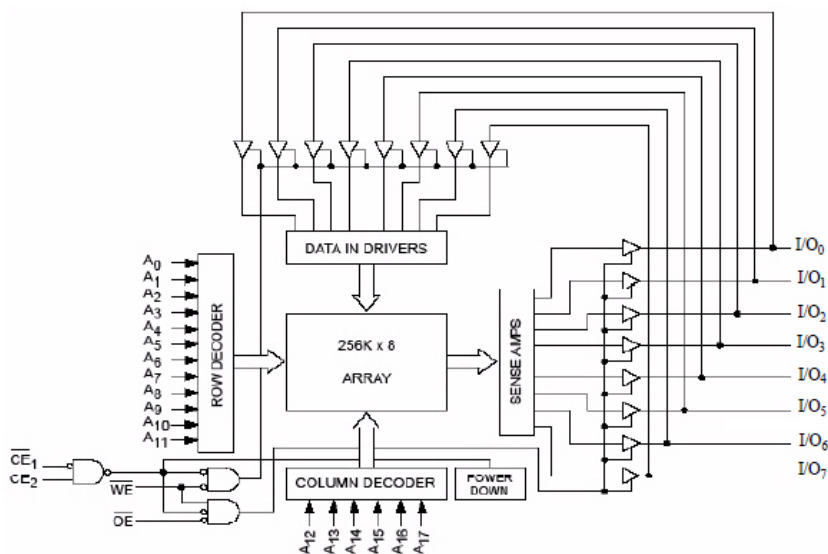
The CY62138FV30^[1] is a high performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Place the device into standby mode reducing power consumption when deselected (\overline{CE}_1 HIGH or CE_2 LOW).

To write to the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (WE) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₇).

To read from the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O₀ through I/O₇) are placed in a high impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW and CE_2 HIGH and WE LOW).

Logic Block Diagram



Note

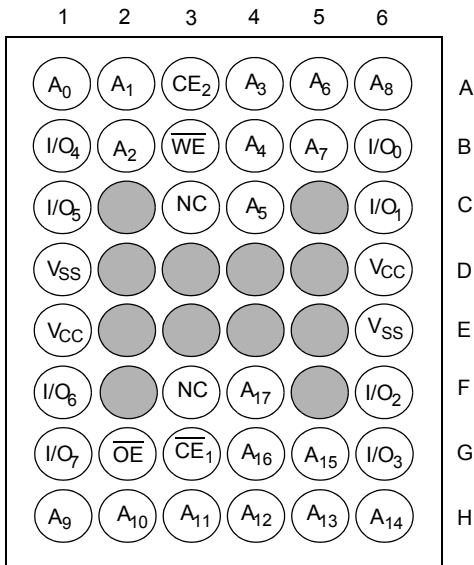
1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at <http://www.cypress.com>.

Contents

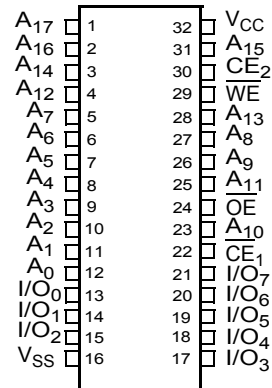
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Pin Configuration

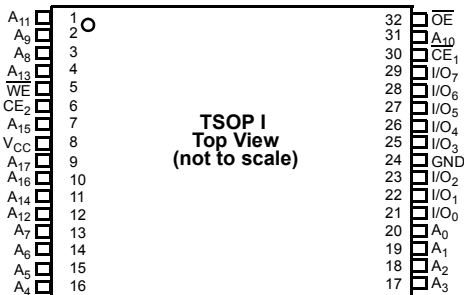
36-Ball VFBGA (Top View) ^[2]



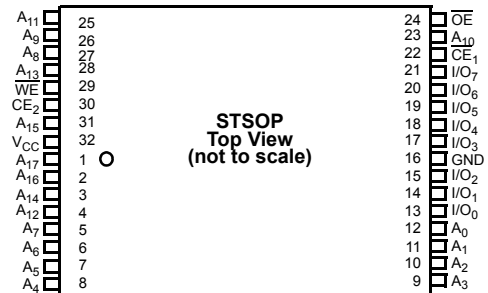
32-Pin SOIC/TSOP II (Top View)



32-Pin TSOP I (Top View)



32-Pin STSOP (Top View)



Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
						f = 1 MHz		f = f _{max}			
Min	Typ ^[3]	Max	Typ ^[3]	Max	Typ ^[3]	Max	Typ ^[3]	Max			
CY62138FV30LL	Ind'I/Auto-A	2.2	3.0	3.6	45	1.6	2.5	13	18	1	5

Notes

- NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential	-0.3 V to 3.9 V
DC voltage applied to outputs in High-Z State ^[4, 5]	-0.3 V to 3.9 V

DC input voltage ^[4, 5]	-0.3 V to 3.9 V
Output current into outputs (LOW)	20 mA
Static Discharge Voltage	> 2001 V (MIL-STD-883, Method 3015)
Latch-up current	> 200 mA

Product	Range	Ambient Temperature	V _{CC} ^[6]
CY62138FV30LL	Ind'I/Auto-A	-40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	45 ns (Ind'I/Auto-A)			Unit
			Min	Typ ^[7]	Max	
V _{OH}	Output HIGH voltage	I _{OH} = -0.1 mA	2.0	-	-	V
		I _{OH} = -1.0 mA, V _{CC} ≥ 2.70 V	2.4	-	-	V
V _{OL}	Output LOW voltage	I _{OL} = 0.1 mA	-	-	0.4	V
		I _{OL} = 2.1 mA, V _{CC} ≥ 2.70 V	-	-	0.4	V
V _{IH}	Input HIGH voltage	V _{CC} = 2.2 V to 2.7 V	1.8	-	V _{CC} + 0.3V	V
		V _{CC} = 2.7 V to 3.6 V	2.2	-	V _{CC} + 0.3V	V
V _{IL}	Input LOW voltage	V _{CC} = 2.2 V to 2.7 V	-0.3	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V				
		V _{CC} = 2.2 V to 3.6 V	-0.3	-	0.8	V
V _{CC} = 2.2 V to 3.6 V	-0.3	-	0.6	V		
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , output disabled	-1	-	+1	μA
I _{CC}	V _{CC} Operating supply current	f = f _{max} = 1/t _{RC}	-	13	18	mA
		f = 1 MHz				
		V _{CC} = V _{CCmax} I _{OUT} = 0 mA CMOS levels				
I _{SB1} ^[8]	Automatic CE Power-down Current CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, f = f _{max} (address and data only), f = 0 (OE, and WE), V _{CC} = 3.60 V	-	1	5	μA
I _{SB2} ^[8]	Automatic CE Power-down Current CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, f = 0, V _{CC} = 3.60 V	-	1	5	μA

Capacitance

Parameter ^[9]	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	10	pF
C _{OUT}	Output Capacitance	V _{CC} = V _{CC(typ.)}	10	pF

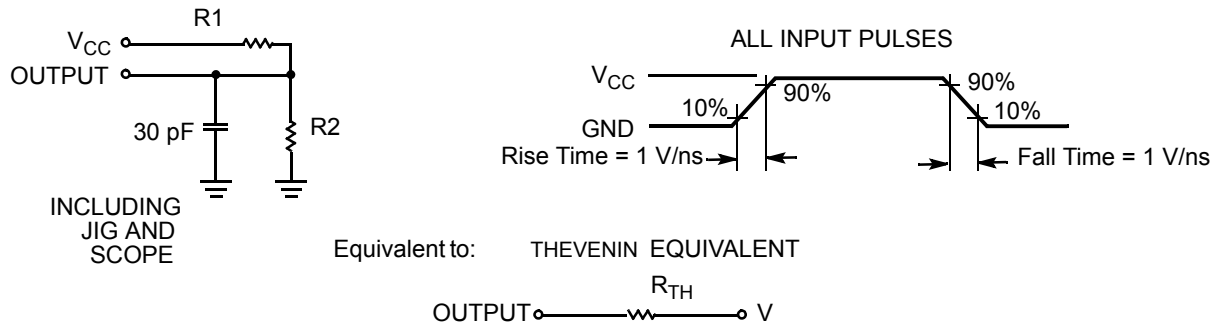
Notes

- V_{IL(min)} = -2.0V for pulse durations less than 20 ns.
- V_{IH(max)} = V_{CC}+0.75V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C
- Chip enables (\overline{CE}_1 and CE₂) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Parameter ^[10]	Description	Test Conditions	SOIC	VFBGA	TSOP II	STSOP	TSOP I	Unit
Θ_{JA}	Thermal resistance (Junction to Ambient)	Still air, soldered on a 3 x 4.5 inch, two layer printed circuit board	44.53	38.49	44.16	59.72	50.19	°C/W
Θ_{JC}	Thermal resistance (Junction to Case)		24.05	17.66	11.97	15.38	14.59	°C/W

Figure 1. AC Test Loads and Waveforms

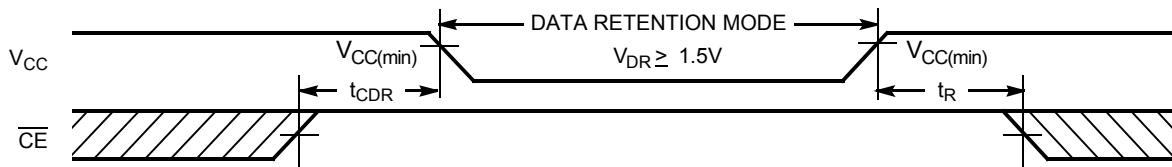


Parameter	2.5 V (2.2 V to 2.7 V)	3.0 V (2.7 V to 3.6 V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ ^[11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR} ^[12]	Data retention current	$V_{CC} = 1.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	1	4	μA
t_{CDR} ^[10]	Chip deselect to data retention time		0	–	–	ns
t_R ^[13]	Operation recovery time		45	–	–	ns

Figure 2. Data Retention Waveform^[14]



Notes

- 10. Tested initially and after any design or process changes that may affect these parameters.
- 11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$
- 12. Chip enables (\overline{CE}_1 and CE_2) must be at CMOS level to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating
- 13. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ $\geq 100\ \mu\text{s}$ or stable at $V_{CC(min)}$ $\geq 100\ \mu\text{s}$.
- 14. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.

Switching Characteristics (Over the Operating Range)

Parameter ^[15]	Description	45 ns (Ind'l/Auto-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to data valid	–	45	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	ns
t_{LZOE}	\overline{OE} LOW to Low-Z ^[16]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to High-Z ^[16,17]	–	18	ns
t_{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[16]	10	–	ns
t_{HZCE}	\overline{CE}_1 HIGH or CE_2 LOW to High-Z ^[16,17]	–	18	ns
t_{PU}	\overline{CE}_1 LOW and CE_2 HIGH to Power-up	0	–	ns
t_{PD}	\overline{CE}_1 HIGH or CE_2 LOW to Power-down	–	45	ns
Write Cycle^[18]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to Write Start	0	–	ns
t_{PWE}	\overline{WE} pulse Width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[16,17]	–	18	ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[16]	10	–	ns

Notes

15. Test conditions for all parameters other than tristate parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the [AC Test Loads and Waveforms](#) on page 5.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the output enters a high impedance state.
18. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.

Switching Waveforms

Figure 3. Read Cycle 1 (Address transition controlled) [20, 21]

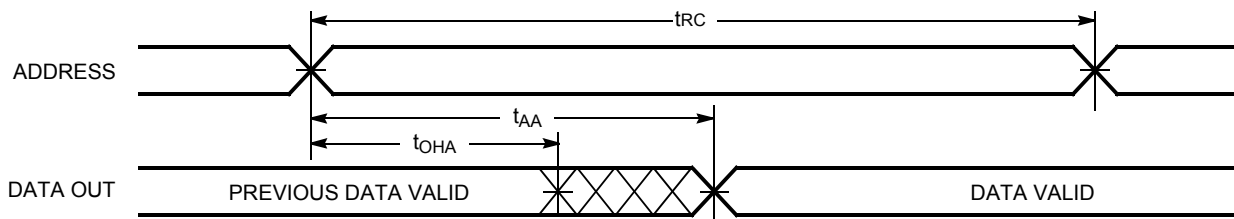


Figure 4. Read Cycle No. 2 (\overline{OE} controlled) [21, 22, 25]

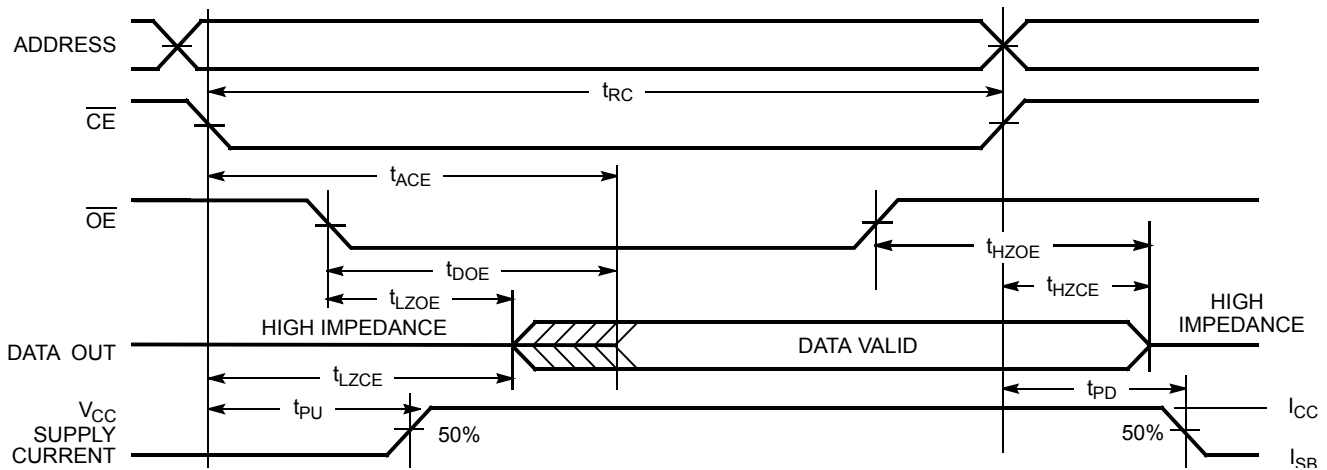
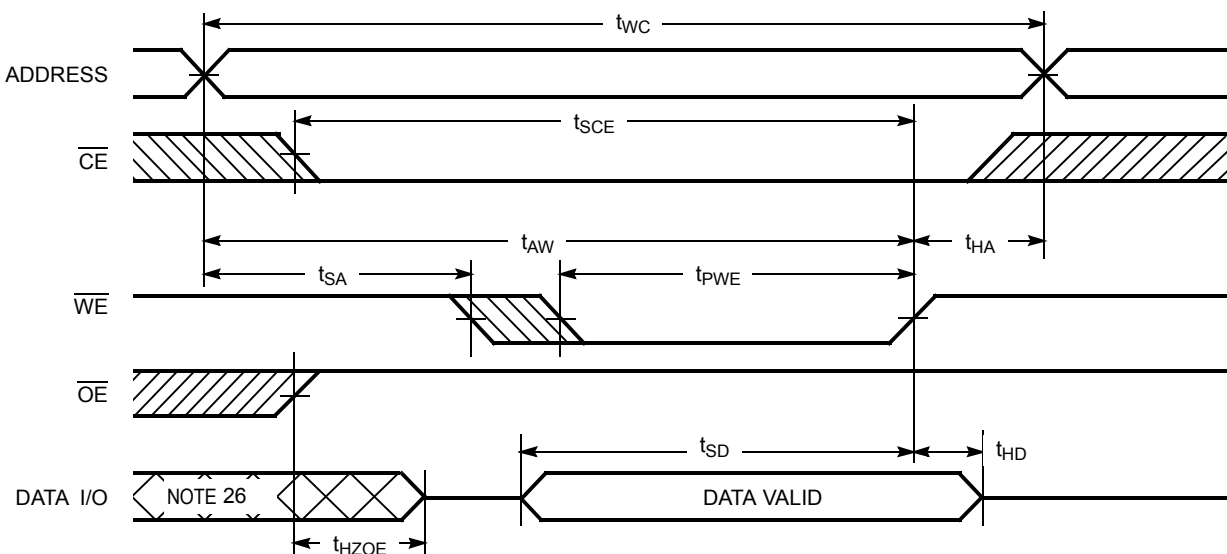


Figure 5. Write Cycle No. 1 (\overline{WE} controlled) [19, 23, 24, 25]



Notes

19. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write
20. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
21. \overline{WE} is HIGH for read cycle.
22. Address valid before or similar to \overline{CE}_1 transition LOW and CE_2 transition HIGH.
23. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
24. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in high impedance state.
25. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
26. During this period, the I/Os are in output state. Do not apply input signals

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 (\overline{CE}_1 or CE_2 controlled) [27, 28, 29, 30]

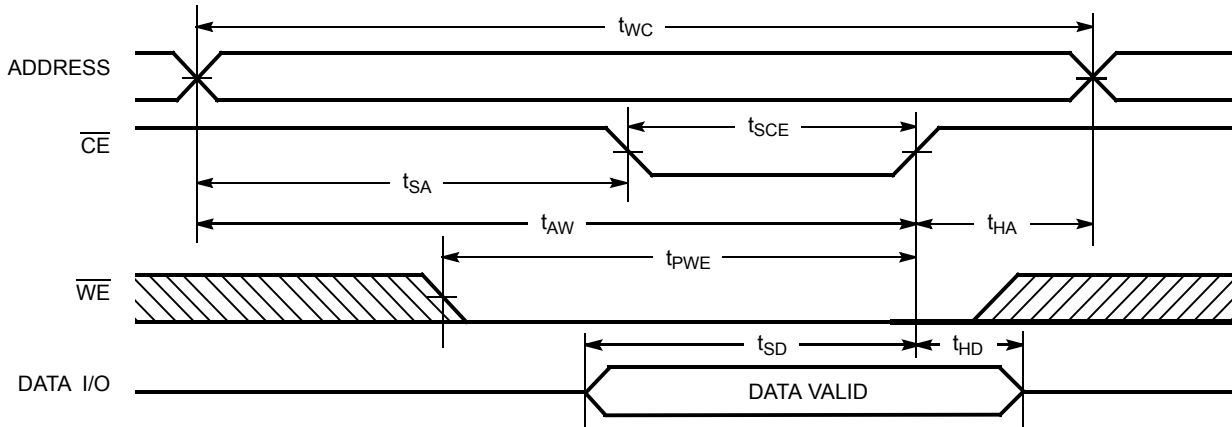
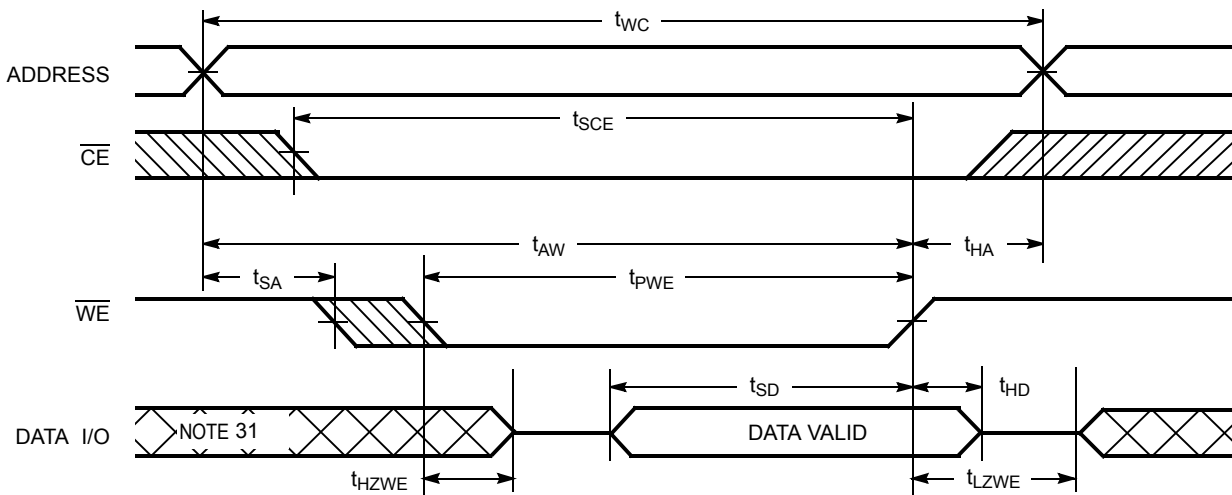


Figure 7. Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) [27, 30]



Truth Table

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode	Power
H	X ^[32]	X	X	High-Z	Deselect / Power-down	Standby (I_{SB})
X ^[32]	L	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data out	Read	Active (I_{CC})
L	H	H	H	High-Z	Output disabled	Active (I_{CC})
L	H	L	X	Data in	Write	Active (I_{CC})

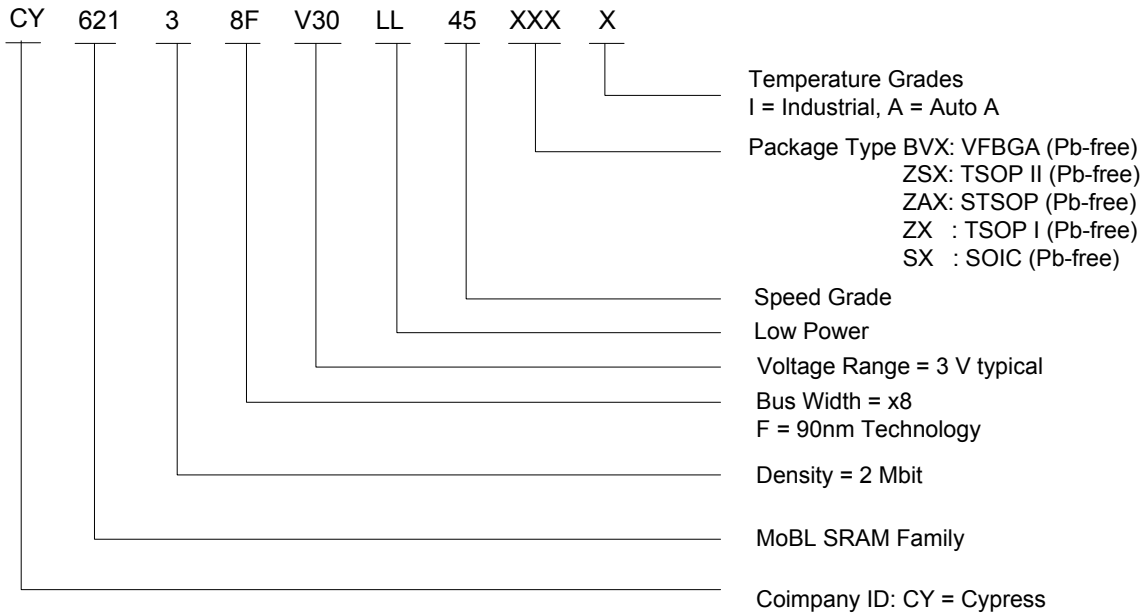
Notes

- 27. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 28. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.
- 29. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 30. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in high impedance state.
- 31. During this period, the I/Os are in output state. Do not apply input signals.
- 32. The 'X' (Don't care) state for the Chip enables (\overline{CE}_1 and CE_2) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

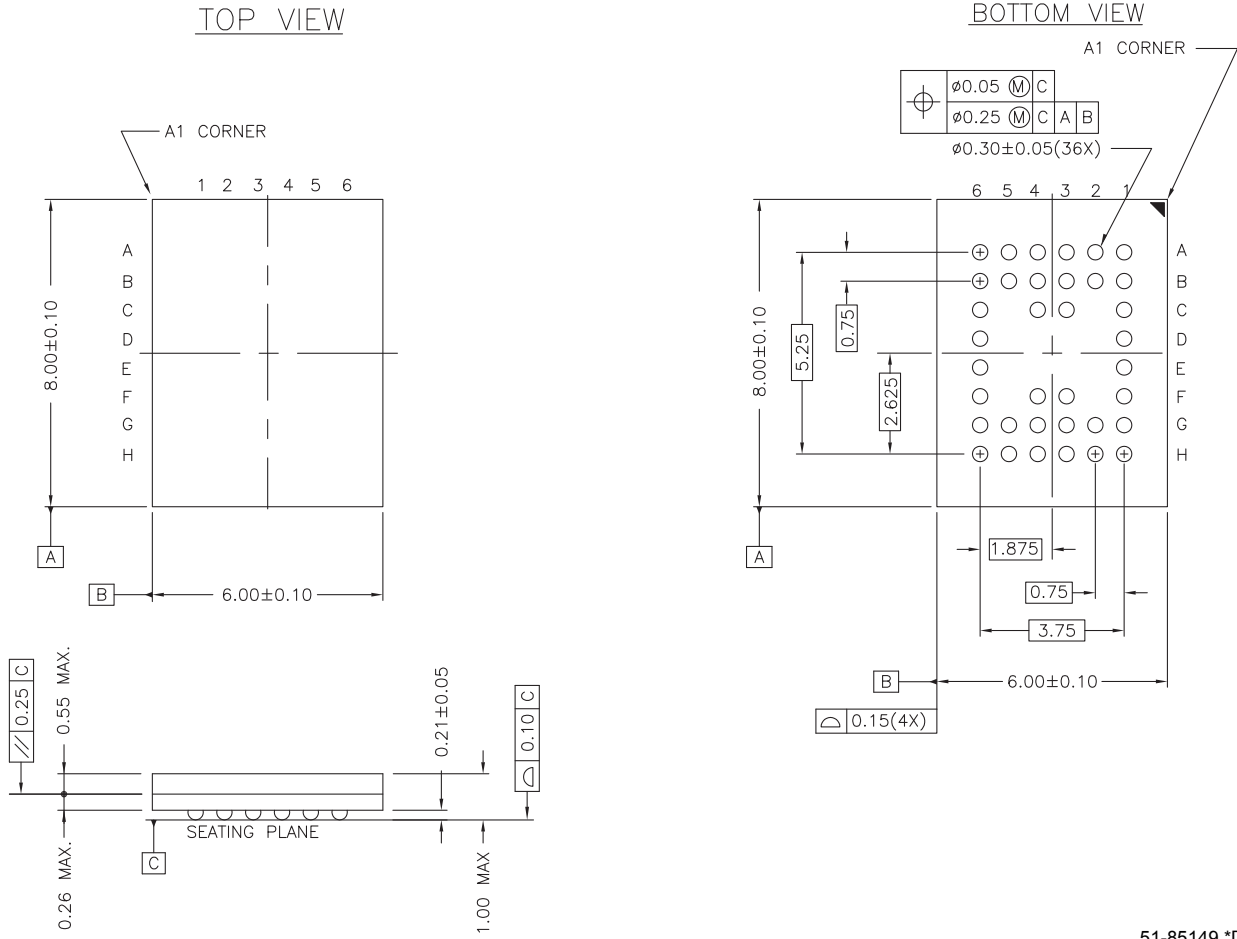
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138FV30LL-45BVXI	51-85149	36-ball VFBGA (Pb-free)	Industrial
	CY62138FV30LL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
	CY62138FV30LL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	
	CY62138FV30LL-45ZXI	51-85056	32-pin TSOP I (Pb-free)	
	CY62138FV30LL-45SXI	51-85081	32-pin SOIC (Pb-free)	
	CY62138FV30LL-45ZAXA	51-85094	32-pin STSOP (Pb-free)	Automotive-A

Ordering Code Definition



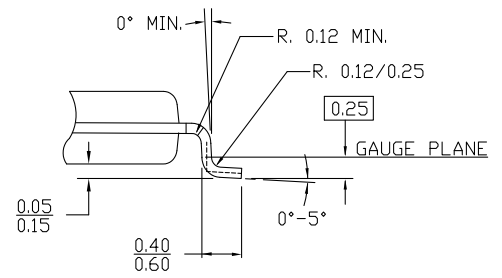
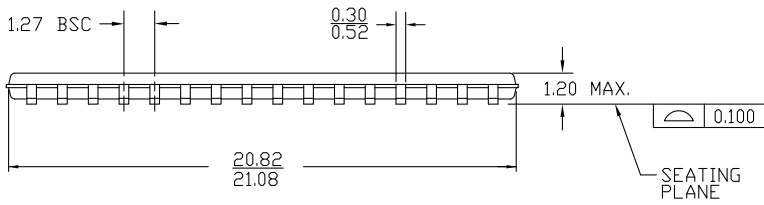
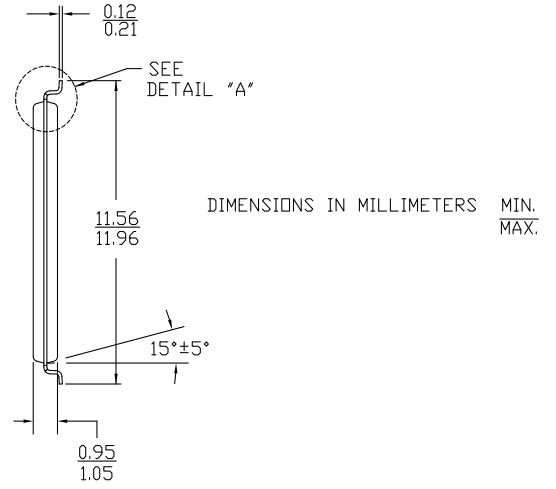
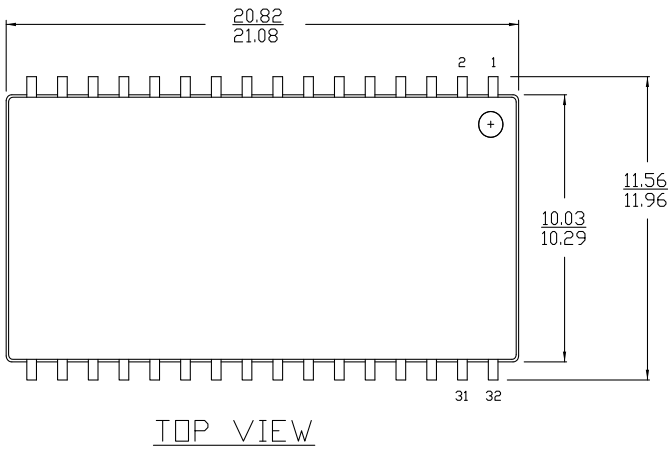
Package Diagrams

Figure 8. 36-Ball VFBGA (6 x 8 x 1 mm), 51-85149



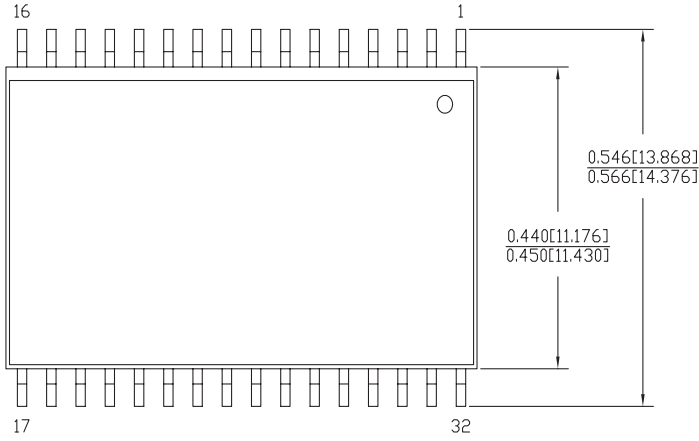
51-85149 *D

Figure 9. 32-Pin TSOP II, 51-85095



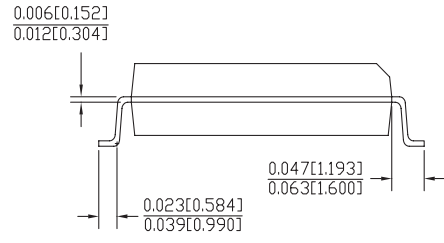
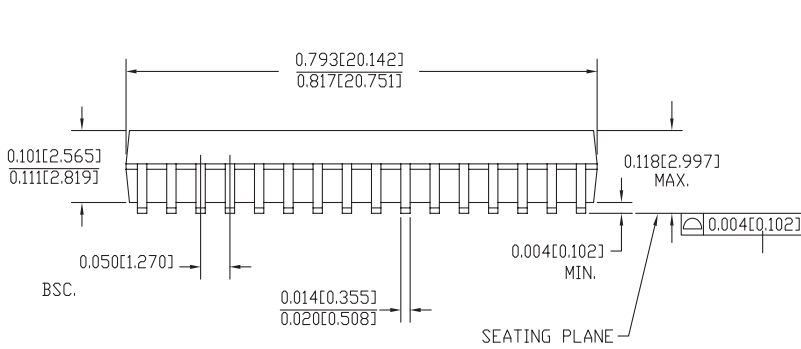
51-85095 *A

Figure 10. 32-Pin (450 Mil) Molded SOIC, 51-85081



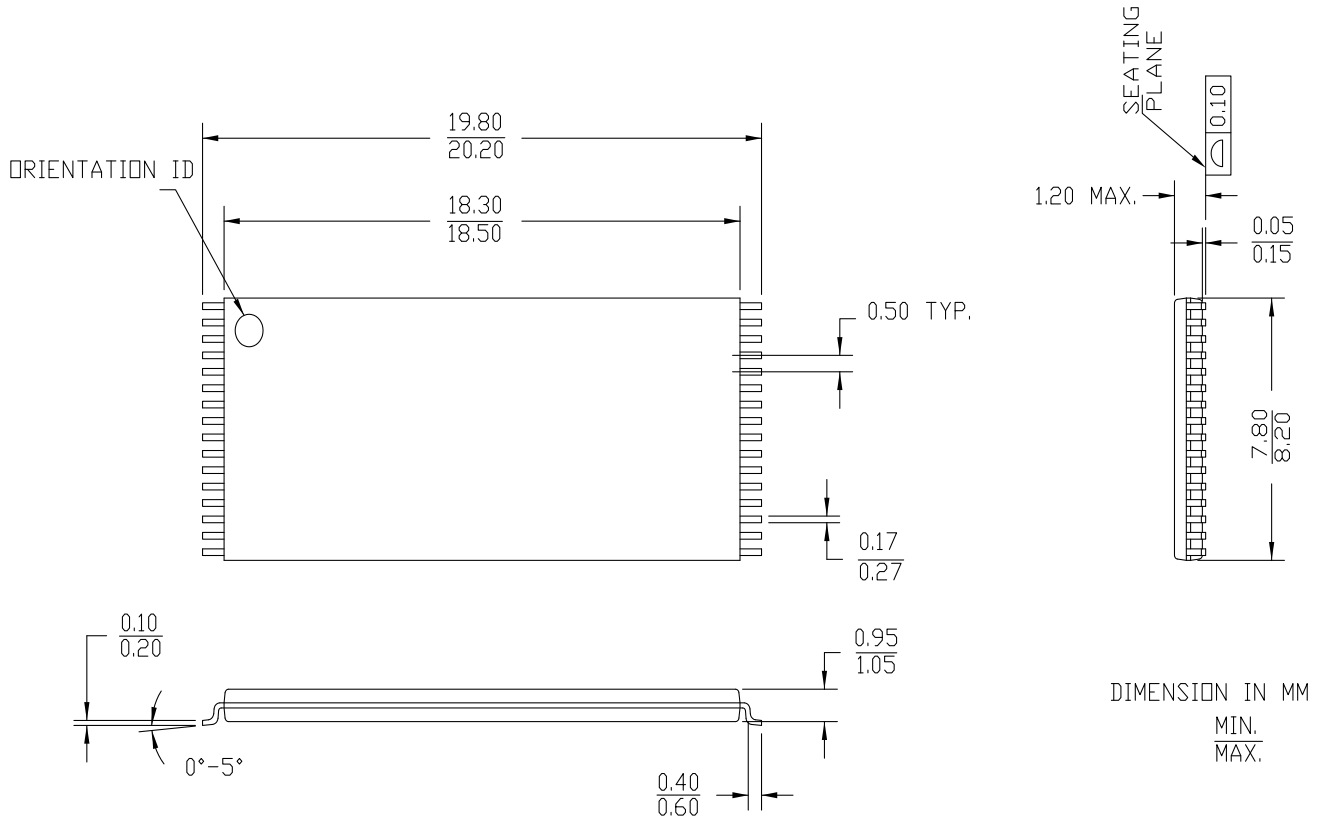
DIMENSIONS IN INCHES[MM] MIN. MAX.
 PACKAGE WEIGHT 1.42gms

PART #	
S32.45	STANDARD PKG.
SZ32.45	LEAD FREE PKG.



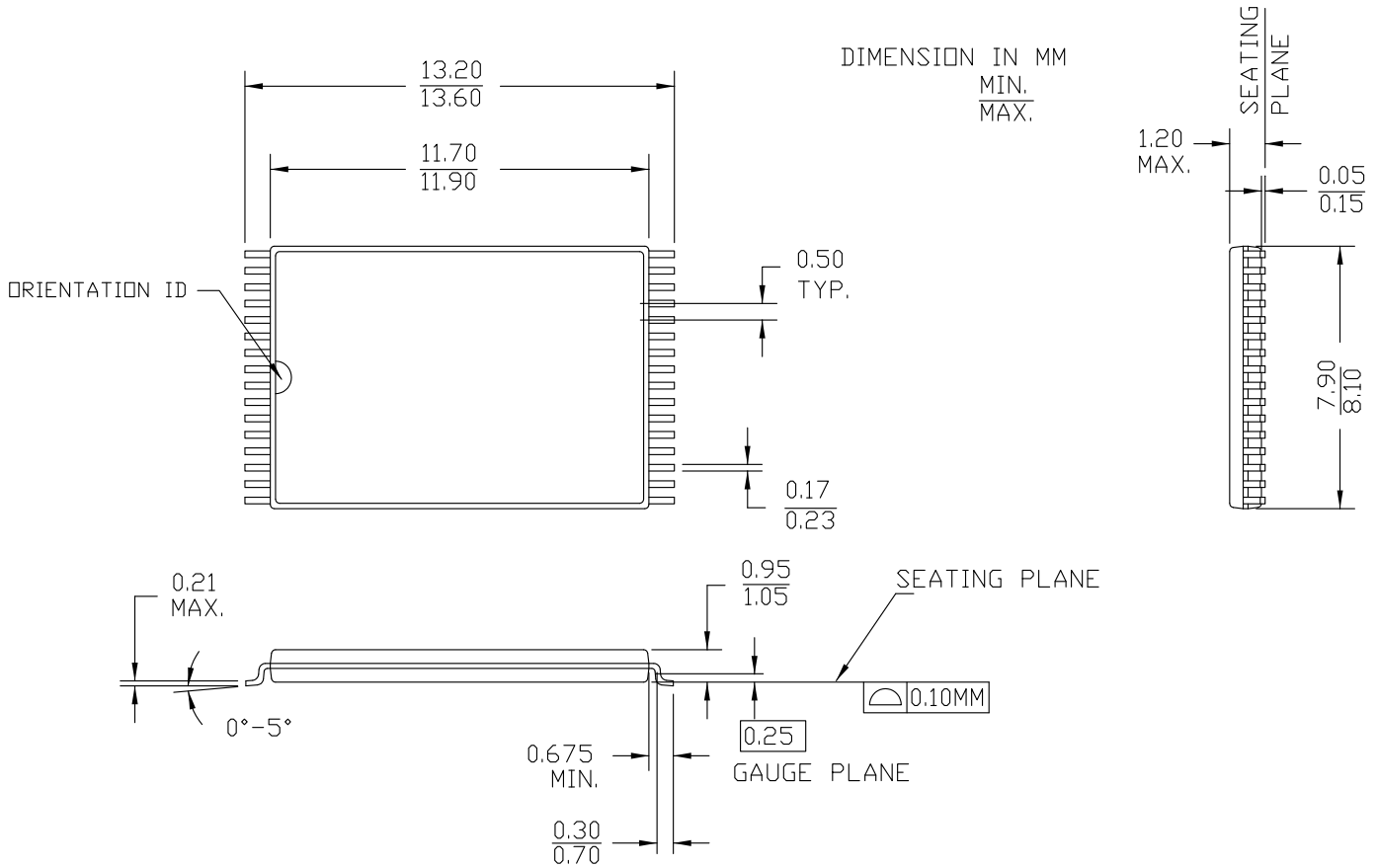
51-85081 *C

Figure 11. 32-Pin TSOP I (8 x 20 mm), 51-85056



51-85056 * E

Figure 12. 32-Pin STSOP (8 x 13.4 mm), 51-85094



51-85094 * E

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
VFBGA	very fine ball grid array
TSOP	thin small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY62138FV30 MoBL®, 2-Mbit (256K x 8) Static RAM				
Document Number: 001-08029				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	463660	See ECN	NXR	New data sheet
*A	467351	See ECN	NXR	Added 32-pin TSOP II package, 32 pin TSOP I and 32 pin STSOP packages Changed ball A3 from NC to CE ₂ in 36-ball FBGA pin out
*B	566724	See ECN	NXR	Converted from Preliminary to Final Corrected typo in 32 pin TSOP II pin configuration diagram on page #2 (changed pin 24 from CE ₁ to OE and pin 22 from CE to CE ₁) Changed the I _{CC(max)} value from 2.25 mA to 2.5 mA for test condition f=1 MHz Changed the I _{SB2(typ)} value from 0.5 μA to 1 μA Changed the I _{SB2(max)} value from 2.5 μA to 5 μA Changed the I _{CCDR(typ)} value from 0.5 μA to 1 μA and I _{CCDR(max)} value from 2.5 μA to 4 μA
*C	797956	See ECN	VKN	Added 32-pin SOIC package Updated VIL spec for SOIC, TSOP-II, TSOP-I, and STSOP packages on Electrical characteristics table
*D	809101	See ECN	VKN	Corrected typo in the Ordering Information table
*E	940341	See ECN	VKN	Added footnote #7 related to I _{SB2} and I _{CCDR}
*F	2769239	09/25/09	VKN/AESA	Included Automotive-A information
*G	3055119	10/12/2010	RAME	Updated and converted all tablenotes into Footnote Added Acronyms and Units of Measure table Added Ordering Code Definition Updated All Package Diagrams . Updated datasheet as per new template.
*H	3061313	10/15/2010	RAME	Minor changes: Corrected "IO" to "I/O"
*I	3078557	11/04/2010	RAME	Corrected 55 C to -55C in Ambient Temperature with Power applied in Maximum Ratings Section

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

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