8-Output Regulator with Sequencing and I²C

FEATURES

- **Triple I²C Adjustable High Efficiency Step-Down DC/DC Converters: 1.6A, 1A, 1A**
- **High Efficiency 1.2A Buck-Boost DC/DC Converter**
- **Triple 250mA LDO Regulators**
- **Pushbutton ON/OFF Control with System Reset**
- **Flexible Pin-Strap Sequencing Operation**
- **I²C and Independent Enable Control Pins**
- Power Good and Reset Outputs
- Dynamic Voltage Scaling and Slew Rate Control
- Selectable 2.25MHz or 1.12MHz Switching Frequency
- Always-Alive 25mA LDO Regulator
- 8µA Standby Current
- 40-Pin 6mm × 6mm × 0.75mm QFN

APPLICATIONS

- Handheld Instruments and Scanners
- Portable Industrial Devices
- Automotive Infotainment
- Medical Devices
- High End Consumer Devices
- Multirail Systems
- Supports Freescale i.MX, Marvell PXA and Other Application Processors

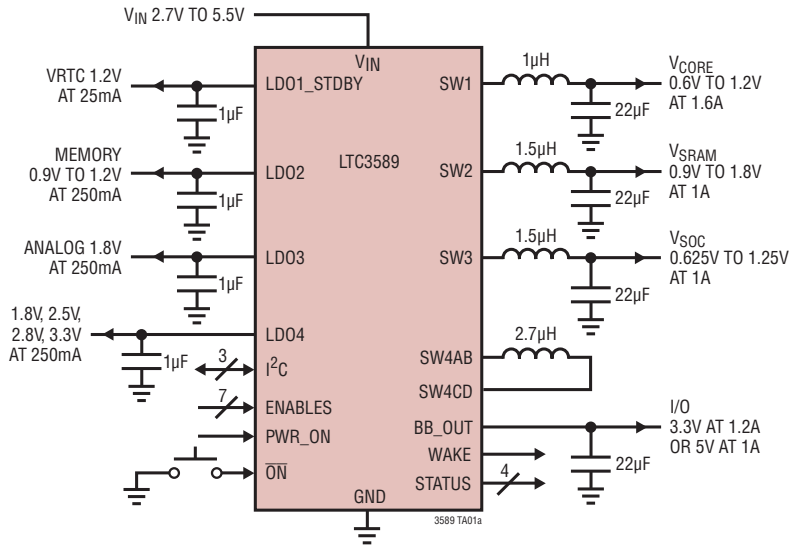
DESCRIPTION

The LTC®3589 is a complete power management solution for ARM and ARM-based processors and advanced portable microprocessor systems. The device contains three synchronous step-down DC/DC converters for core, memory and SoC rails, a synchronous buck-boost regulator for I/O at 3.3V to 5V, and three 250mA LDO regulators for low noise analog supplies. An I²C serial port is used to control regulator enables, output voltage levels, dynamic voltage scaling and slew rate, operating modes and status reporting.

Regulator start-up is sequenced by connecting outputs to enable pins in the desired order or via the I²C port. System power-on, power-off and reset functions are controlled by pushbutton interface, pin inputs, or I²C interface.

The LTC3589 supports i.MX, PXA and OMAP processors with eight independent rails at appropriate power levels. Other features include interface signals such as the VSTB pin that toggles between programmed run and standby output voltages on up to four rails simultaneously. The device is available in a low profile 40-pin 6mm × 6mm exposed pad QFN package.

TYPICAL APPLICATION



Start-Up Sequence

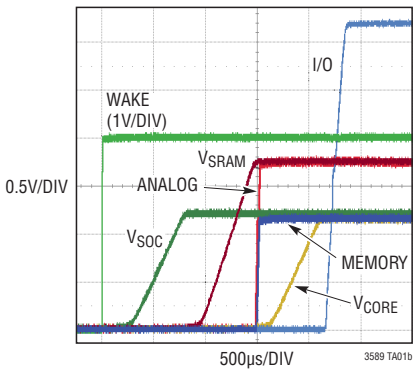


TABLE OF CONTENTS

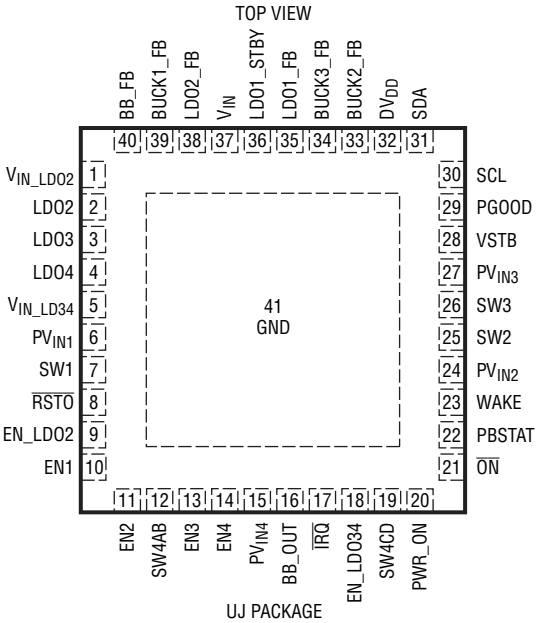
Features **1**
Applications **1**
Typical Application **1**
Description **1**
Absolute Maximum Ratings **3**
Pin Configuration **3**
Order Information **3**
Electrical Characteristics **4**
Typical Performance Characteristics **9**
Pin Functions **13**
Block Diagram **15**
Operation **16**
Introduction 16
Always-On LDO 17
Step-Down Switching Regulators 19
Buck-Boost Switching Regulator 23
Slewing DAC Reference Operation 27
Pushbutton Operation 28
Enable and Power-On Sequencing 30
Fault Detection, Shutdown, and Reporting 31
I^2C Operation 33
Thermal Considerations and Board Layout 39
Applications Information **41**
Typical Application **43**
Package Description **44**
Revision History **45**
Typical Application **46**
Related Parts **46**

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 3)

SW1, SW2, SW3, SW4AB, SW4CD (Transients < 1ms, Duty Cycle < 1%) ..... –0.3V to 7V
PV_{IN1}, PV_{IN2}, PV_{IN3}, PV_{IN4} ..... –0.3V to V_{IN} + 0.3V
V_{IN_LDO2}, V_{IN_LDO34} ..... –0.3V to V_{IN} + 0.3V
V_{IN}, DV_{DD} ..... –0.3V to 6V
LDO1_STBY, LDO1_FB, BUCK1_FB, BUCK2_FB, BUCK3_FB, BB_FB, BB_OUT, LDO2, LDO2_FB, LDO3, LDO4, PGOOD, VSTB, EN1, EN2, EN3, EN4, EN_LDO2, EN_LDO34, $\overline{ON}$, PBSTAT, WAKE, $\overline{RSTO}$, PWR_ON, IRQ, ... –0.3V to 6V
SDA, SCL ..... –0.3V to DV_{DD} + 0.3V
Operating Junction Temperature Range (Note 2) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3589EUJ#PBF	LTC3589EUJ#TRPBF	LTC3589UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3589IUJ#PBF	LTC3589IUJ#TRPBF	LTC3589UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3589HUJ#PBF	LTC3589HUJ#TRPBF	LTC3589UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_LDO2} = V_{IN_LDO34} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Input Supply Voltage, V_{IN}		●	2.7		5.5	V
$I_{VINLDO1}$	V_{IN} Quiescent Current	All Enables = 0V	●		8	18	µA
f_{OSC}	Oscillator Frequency		●	1.8	2.25	2.6	MHz
Step-Down Switching Regulators 1, 2, and 3							
I_{VIN}	Pulse-Skipping Mode V_{IN} Quiescent Current per Buck Burst Mode® V_{IN} Quiescent Current per Buck	V_{FB} = 0.85V (Note 5)	● ●		120 23	200 40	µA µA
I_{FB}	Feedback Pin Input Current	V_{FB} = 0.8V		–50		50	nA
D_X	Maximum Duty Cycle	V_{FB} = 0V		100			%
R_{SW}	SW Pull-Down Resistance	Regulators Disabled			2.5		kΩ
t_{SS}	Soft-Start Rate	(Note 6)			0.8		V/ms
$V_{FB(MAX)}$	Maximum Feedback Voltage	BxDTV1 = BxDTV2 = 11111, V_{IN} = 2.7V to 5.5V	●	0.735	0.75	0.765	V
$V_{FB(LSB)}$	Feedback LSB Step Size				12.5		mV
$V_{FB(MIN)}$	Minimum Feedback Voltage	BxDTV1 = BxDTV2 = 00000, V_{IN} = 2.7V to 5.5V	●	0.351	0.3625	0.374	V
1.6A Step-Down Switching Regulator 1 (Buck 1)							
I_{LIM1}	Peak PMOS Current Limit SW1		●	2.0	2.7		A
RP1	$R_{DS(ON)}$ of PMOS1	I_{SW1} = 100mA			180		mΩ
RN1	$R_{DS(ON)}$ of NMOS1	I_{SW1} = 100mA			110		mΩ
1.0A Step-Down Switching Regulators 2 and 3							
$I_{LIM2, 3}$	Peak PMOS Current Limit SW2 and SW3		●	1.5	1.9		A
RP2, 3	$R_{DS(ON)}$ of PMOS2 and PMOS3				250		mΩ
RN2, 3	$R_{DS(ON)}$ of NMOS2 and NMOS3				130		mΩ
1.2A Buck-Boost Switching Regulator 4 (Buck-Boost)							
I_{VIN}	PWM Mode V_{IN} Quiescent Current Burst Mode V_{IN} Quiescent Current	V_{BB_FB} = 0.85V (Note 5)	● ●		115 19	170 35	µA µA
V_{BB_FB}	Feedback Voltage	V_{IN} = 2.7V to 5.5V, V_{OUT} = 5.5V	●	0.776	0.8	0.824	V
V_{OUTBB}	Output Voltage Range			1.8		5.0	V
I_{LIM4}	Peak PMOS Current Limit SW4AB		●	2.3	2.9		A
I_{PEAK4}	Forward Burst Current Limit (Switch A)	Burst Mode Operation			600		mA
I_{LIMR4}	Reverse Current Limit (Switch D)				1		A
I_{ZERO4}	Reverse Burst Current Limit (Switch D)	Burst Mode Operation			0		mA
RP4	$R_{DS(ON)}$ of Switch A and Switch D	I_{SW4AB} = I_{SW4CD} = 100mA			160		mΩ
RN4	$R_{DS(ON)}$ of Switch B and Switch C	I_{SW4AB} = I_{SW4CD} = –100mA			110		mΩ
R_{OUT4}	BB_OUT Pull-Down Resistance	Regulator Disabled			2.5		kΩ
t_{SS}	Soft-Start Rate	(Note 6)			2		V/ms
I_{FB}	Feedback Pin Input Current	V_{FB} = 0.85V		–50		50	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_LDO2} = V_{IN_LDO34} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO Regulators							
t_{LDO_SS}	Soft-Start Time LDO2, LDO3, LDO4				100		µs
R_{LDO_PD}	Output Pull-Down Resistance LDO2, LDO3, LDO4	LDO Disabled			2.5		kΩ
Always-On Regulator (LDO1_STDBY)							
V_{LDO1_FB}	LDO1 Feedback Voltage		●	0.76	0.8	0.84	V
V_{LDO1}	LDO1 Line Regulation	I_{LDO1_STBY} = 1mA, LDO1_STBY = 1.2V, V_{IN} = 2.7V to 5.5V			0.15		%/V
	LDO1 Load Regulation	I_{LDO1} = 0.1mA to 25mA, LDO1_STBY = 1.2V			0.1		%
I_{LDO1}	Available Output Current		●	25			mA
I_{LDO1_SC}	Short-Circuit Output Current Limit				65	100	mA
V_{DROP1}	Dropout Voltage (Note 4)	I_{LDO1} = 25mA, LDO1_STBY = 3.3V			200		mV
I_{LDO1_FB}	LDO1_FB Input Current	V_{LDO1_FB} = 0.85V		–50		50	nA
LDO Regulator 2 (LDO2)							
V_{IN_LDO2}	V_{IN_LDO2} Input Voltage Range		●	1.7		V_{IN}	V
I_{VIN_LDO2}	V_{IN_LDO2} Quiescent Current V_{IN_LDO2} Shutdown Current	Regulator Enabled Regulator Disabled	● ●		12 0	20 1	µA µA
I_{VIN}	V_{IN} Quiescent Current	EN_LDO2 = High	●		50	85	µA
$V_{FB2(MAX)}$	LDO2 Maximum Feedback Voltage	L2DTV1 = L2DTV2 = 11111	●	0.735	0.75	0.765	V
$V_{FB2(LSB)}$	LDO2 Feedback LSB Step Size				12.5		mV
$V_{FB2(MIN)}$	LDO2 Minimum Feedback Voltage	L2DTV1 = L2DTV2 = 00000 V_{IN_LDO2} = V_{IN} = 2.7V to 5.5V, I_{LDO2} = 1mA	●	0.351	0.3625	0.374	V
	LDO2 Line Regulation	I_{LDO2} =1mA, V_{INLDO2} = 2.7V to 5.5V			0.01		%/V
	LDO2 Load Regulation	I_{LDO2} = 1mA to 250mA			0.01		%
I_{OUT2}	LDO2 Available Output Current		●	250			mA
I_{SC2}	LDO2 Short-Circuit Current Limit			300	450	600	mA
V_{DROP2}	Dropout Voltage (Note 4)	I_{LDO2} = 200mA, V_{LDO2} = 2.5V I_{LDO2} = 200mA, V_{LDO2} = 1.2V			140 350	180 500	mV mV
I_{LDO2_FB}	LDO2_FB Input Current	V_{LDO2_FB} = 0.8V		–50		50	nA
LDO Regulator 3 (LDO3)							
V_{IN_LDO34}	V_{IN_LDO34} Input Range		●	2.35		V_{IN}	V
I_{VIN_LDO34}	V_{IN_LDO34} Quiescent Current V_{IN_LDO34} Shutdown Current	Regulator Enabled Regulator Disabled	● ●		15 0	25 1	µA µA
I_{VIN}	V_{IN} Quiescent Current		●		50	85	µA
V_{LDO3}	LDO3 Output Voltage	V_{IN_LDO34} = V_{IN} = 2.7V to 5V, I_{LDO3} = 1mA	●	1.746	1.8	1.854	V
	LDO3 Line Regulation	I_{LDO3} =1mA, $V_{INLDO34}$ = 2.7V to 5.5V			0.01		%/V
	LDO3 Load Regulation	I_{LDO3} = 1mA to 250mA			0.05		%
I_{LDO3}	LDO3 Available Output Current		●	250			mA
I_{LDO3_SC}	LDO3 Short-Circuit Current Limit			300	450	600	mA
V_{DROP3}	LDO3 Dropout Voltage (Note 4)	I_{LDO3} = 200mA, V_{LDO3} = 1.8V			190	250	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_LDO2} = V_{IN_LDO34} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO Regulator 4 (LDO4)							
V_{IN_LDO34}	V_{IN_LDO34} Input Range		●	2.35		V_{IN}	V
I_{VIN_LDO34}	V_{IN_LDO34} Quiescent Current V_{IN_LDO34} Shutdown Current	Regulator Enabled Regulator Disabled	● ●		14 0	24 1	µA µA
I_{VIN}	Enabled V_{IN} Quiescent Current		●		50	85	µA
V_{LDO4}	LDO 4 Output Voltage	I_{LDO4} = 1mA, L2DTV2[6:5] = 00 L2DTV2[6:5] = 01 L2DTV2[6:5] = 10 L2DTV2[6:5] = 11	● ● ● ●	2.716 2.425 1.746 3.201	2.8 2.5 1.8 3.3	2.884 2.575 1.854 3.399	V V V V
	LDO4 Line Regulation	I_{LDO4} =1mA, V_{INLDO4} = 2.7V to 5.5V, V_{OUT} = 1.8V			0.01		%/V
	LDO4 Load Regulation	I_{LDO4} = 1mA to 250mA			0.05		%
I_{LDO4}	LDO4 Available Output Current		●	250			mA
I_{LDO4_SC}	LDO4 Short-Circuit Current Limit			300	450	600	mA
V_{DROP4}	LDO4 Dropout Voltage (Note 4)	I_{LDO4} = 200mA, V_{LDO4} = 3.3V I_{LDO4} = 200mA, V_{LDO4} = 1.8V			120 190	160 250	mV mV
Enable Inputs							
V_{ENx_THR}	Threshold Rising, All Enables Low		●		0.8	1.2	V
V_{ENx_THR2} V_{ENx_THF2}	Threshold Rising, Any Enable High Threshold Falling, Any Enable High		● ●	 0.420	0.5 0.45	0.530	V V
R_{ENX}	Input Pull-Down Resistance				4.5		MΩ
VSTB, PWR_ON Inputs							
V_{VSTB_THR} V_{VSTB_THF}	VSTB Pin Threshold Rising VSTB Pin Threshold Falling		● ●	 0.4	0.8 0.7	1.2	V V
R_{VSTB}	Pull-Down Resistence				4.5		MΩ
V_{PWR_ONTHR} V_{PWR_ONTHF}	PWR_ON Pin Threshold Rising PWR_ON Pin Threshold Falling		● ●	 0.4	0.8 0.7	1.2	V V
R_{PWR_ON}	Pull-Down Resistence				4.5		MΩ
I^2C Port							
DV_{DD}	DV_{DD} Input Supply Voltage		●	1.6		5.5	V
I_{DVDD}	DV_{DD} Quiescent Current	SCL/SDA = 0kHz			0.5		µA
V_{DVDD_UVLO}	DV_{DD} UVLO Level				0.8		V
ADDRESS	LTC3589 Device Address – Write LTC3589 Device Address – Read				01101000 01101001		
V_{IH} SDA, SCL V_{IL} SDA, SCL	SDA and SCL Input Threshold Rising SDA and SCL Input Threshold Falling			70		 30	$\%DV_{DD}$ $\%DV_{DD}$
I_{IHSCx} I_{ILSCx}	SDA and SCL Input Current	SDA = SCL = 0V to 5.5V		–250		250	nA
V_{OL} SDA	SDA Output Low Voltage	I_{SDA} = 3mA	●			0.4	V
f_{SCL}	SCL Clock Operating Frequency					400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
t_{HD_STA}	Hold Time After (Repeated) Start Condition			0.6			µs
t_{SU_STA}	Repeated Start Condition Set-Up Time			0.6			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_LDO2} = V_{IN_LDO34} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SU_STO}	Stop Condition Set-Up Time			0.6			µs
$t_{HD\_DAT(O)}$	Data Hold Time Output			0		900	ns
$t_{HD\_DAT(I)}$	Data Hold Time Input			0			ns
t_{SU_DAT}	Data Set-Up Time			100			ns
t_{LOW}	SCL Clock Low Period			1.3			µs
t_{HIGH}	SCL Clock High Period			0.6			µs
t_f	Data Fall Time	C_B = Capacitance of One BUS Line (pF)		$20 + 0.1C_B$		300	ns
t_r	Data Rise Time	C_B = Capacitance of One BUS Line (pF)		$20 + 0.1C_B$		300	ns
t_{SP}	Input Spike Supression Pulse Width					50	ns
Pushbutton Interface							
$V_{\overline{ON}\_TH}$	$\overline{ON}$ Threshold Rising $\overline{ON}$ Threshold Falling		● ●	 0.4	0.8 0.7	1.2	V V
$I_{\overline{ON}}$	$\overline{ON}$ Input Current	$\overline{ON}$ = V_{IN} $\overline{ON}$ = 0V		–100	 40	100	nA µA
$t_{\overline{ON}\_PBSTAT1}$	$\overline{ON}$ Low Time to PBSTAT Low				50		ms
$t_{\overline{ON}\_PBSTAT2}$	$\overline{ON}$ High Time to PBSTAT High				0.2		µs
$t_{\overline{ON}\_WAKE}$	$\overline{ON}$ Low Time to WAKE High				400		ms
$t_{\overline{ON}\_HR}$	$\overline{ON}$ Low Time to Hard Reset				5		s
t_{PBSTAT_PW}	PBSTAT Minimum Pulse Width				50		ms
t_{PBSTAT_BK}	PBSTAT Blanking from WAKE Low				1		s
t_{WAKE_OFF}	Minimum WAKE Low Time				1		s
t_{WAKE_ON}	WAKE High Time with PWR_ON = 0V				5		s
t_{PWR_ON}	PWR_ON High to WAKE High				50		ms
t_{PWR_OFF}	PWR_ON Low WAKE Low				50		ms
Status Output Pins (PBSTAT, WAKE, PGOOD, $\overline{RSTO}$, $\overline{IRQ}$)							
V_{PBSTAT}	PBSTAT Output Low Voltage	I_{PBSTAT} = 3mA			0.1	0.4	V
I_{PBSTAT}	PBSTAT Output High Leakage Current	V_{PBSTAT} = 3.8V		–0.1		0.1	µA
V_{WAKE}	WAKE Output Low Voltage	I_{WAKE} = 3mA			0.1	0.4	V
I_{WAKE}	WAKE Output High Leakage Current	V_{WAKE} = 3.8V		–0.1		0.1	µA
V_{PGOOD}	PGOOD Output Low Voltage	I_{PGOOD} = 3mA			0.1	0.4	V
I_{PGOOD}	PGOOD Output High Leakage Current	V_{PGOOD} = 3.8V		–0.1		0.1	µA
V_{PGOOD}	PGOOD Threshold Rising PGOOD Threshold Falling				–6 –8		% %
V_{NRSTO}	LDO1 Power Good Threshold Rising LDO1 Power Good Threshold Falling				–6 –8		% %
V_{UVLO}	Undervoltage Lockout Rising Undervoltage Lockout Falling				2.65 2.55	2.7	V V
V_{UVWARN}	Undervoltage Warning Rising Undervoltage Warning Falling				3 2.9		

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_LDO2} = V_{IN_LDO34} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\overline{RSTO}}$	$\overline{RSTO}$ Output Low Voltage	$I_{\overline{RSTO}}$ = 3mA			0.1	0.4	V
$I_{\overline{RSTO}}$	$\overline{RSTO}$ Output High Leakage Current	$V_{\overline{RSTO}}$ = 3.8V		–0.1		0.1	µA
$V_{\overline{IRQ}}$	$\overline{IRQ}$ Output Low Voltage	$I_{\overline{IRQ}}$ = 3mA			0.1	0.4	V
$I_{\overline{IRQ}}$	$\overline{IRQ}$ Output High Leakage Current	$V_{\overline{IRQ}}$ = 3.8V		–0.1		0.1	µA

Note 1: Stresses beyond those listed Under Absolute Maximum ratings may cause permanent damage to the device. Exposure to any Absolute Maximum rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3589 is tested under pulsed load conditions such that $T_J \approx T_A$.

The LTC3589E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3589I is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC3589H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (PD, in Watts) according to the formula:

$T_J = T_A + (PD \bullet \theta_{JA})$, where the package junction to ambient thermal impedance θ_{JA} = 34°C/W.

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The LTC3589 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating temperature may impair device reliability.

Note 4: Dropout voltage is defined as ($V_{IN} – V_{LDO}$) for LDO1 or ($V_{IN\_LDO} – V_{LDO}$) for other LDOs when V_{LDO} is 3% lower than V_{LDO} measured with $V_{IN} = V_{IN\_LDO}$ = 4.3V.

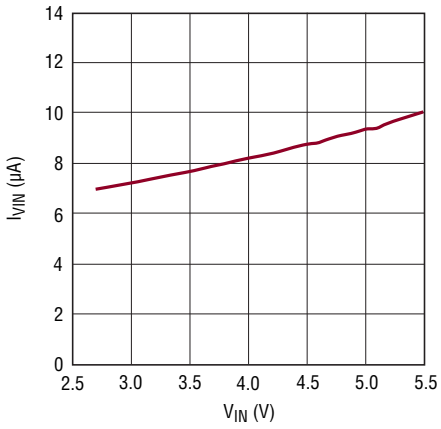
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 6: Soft-start measured in test mode with regulator error amplifier in unity gain mode.

TYPICAL PERFORMANCE CHARACTERISTICS

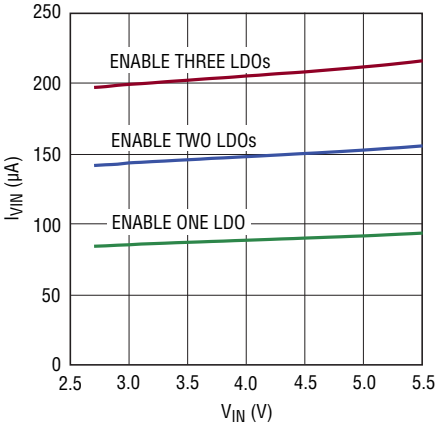
V_{IN} = 3.8V, T_A = 25°C, unless otherwise noted.

Standby I_{VIN} vs V_{IN}



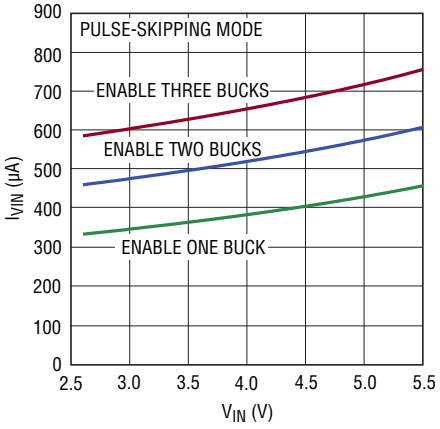
22554 G01

LDO2 to LDO4 I_{VIN} vs V_{IN}



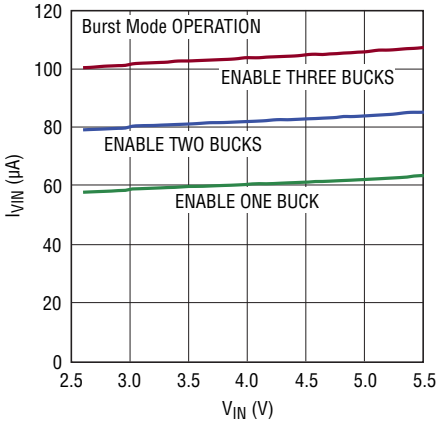
3589 G02

Step-Down Switching Regulator I_{VIN} vs V_{IN}



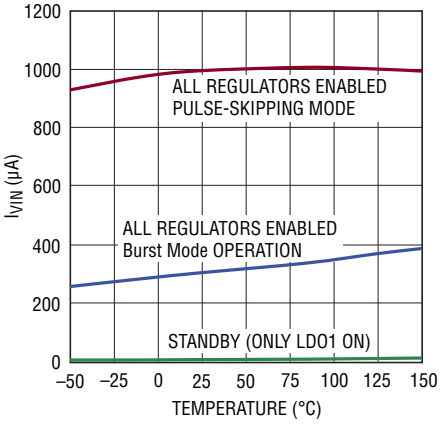
3589 G03

Step-Down Switching Regulator I_{VIN} vs V_{IN}



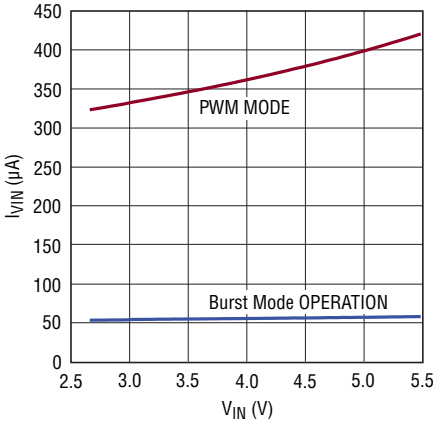
3589 G04

Input Supply Current vs Temperature



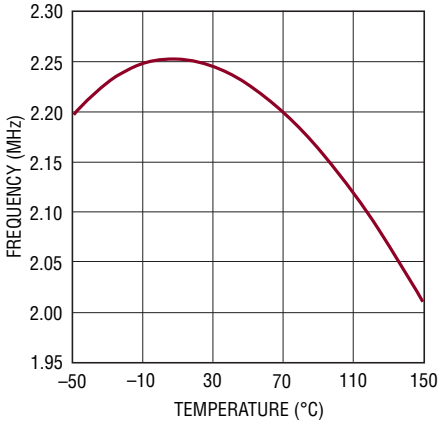
3589 G05

Buck-Boost I_{VIN} vs V_{IN}



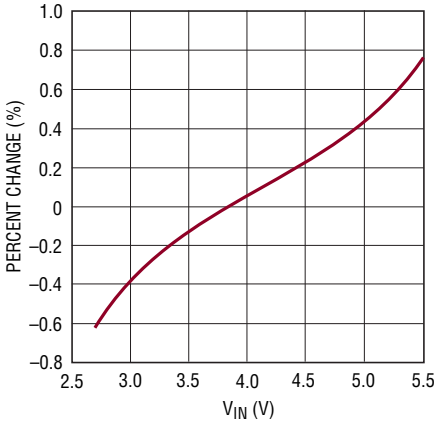
3589 G06

Oscillator Frequency vs Temperature



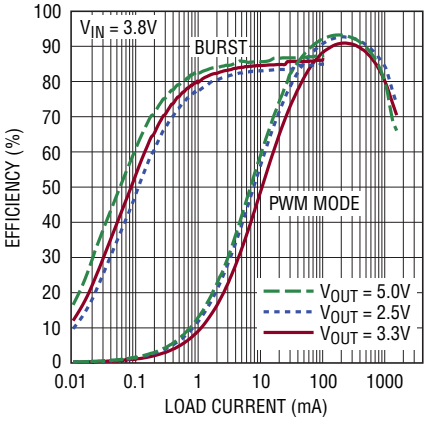
3589 G07

Switching Frequency Change vs V_{IN}



3589 G08

Buck-Boost Efficiency vs I_{OUT}

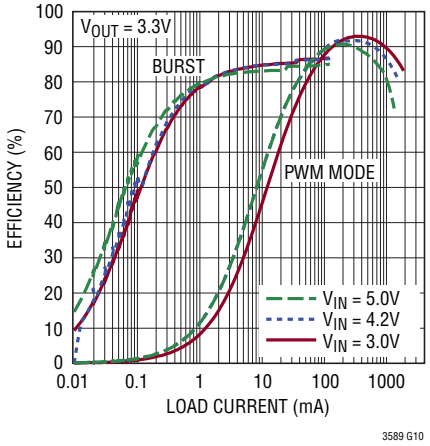


3589 G9

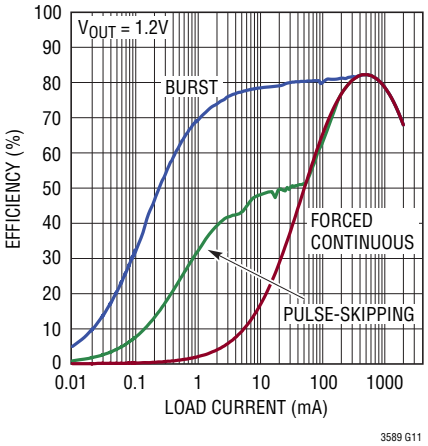
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, T_A = 25°C, unless otherwise noted.

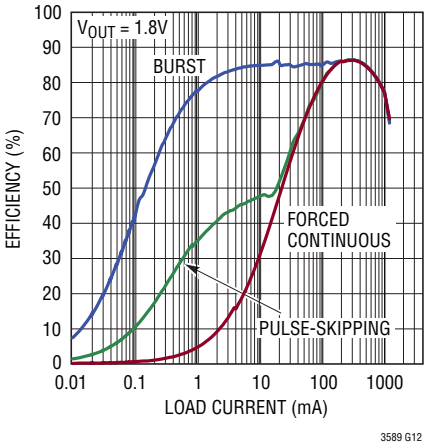
Buck-Boost Efficiency vs I_{OUT}



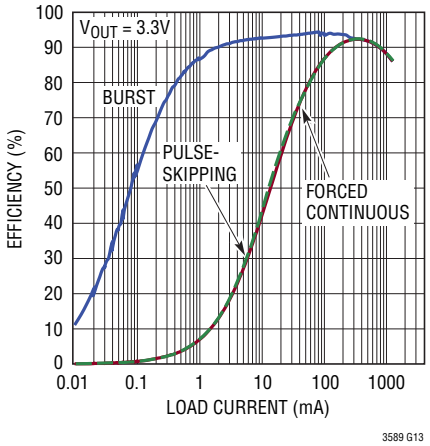
Step-Down Switching Regulator 1 Efficiency vs I_{OUT}



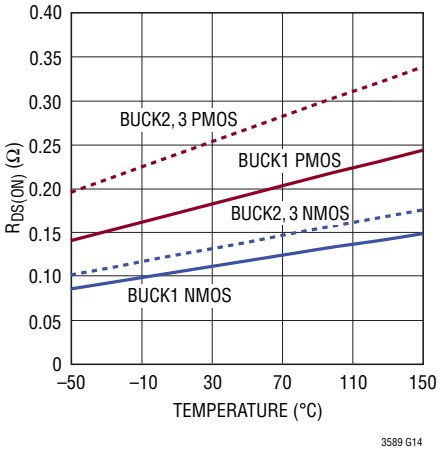
Step-Down Switching Regulator 2 Efficiency vs I_{OUT}



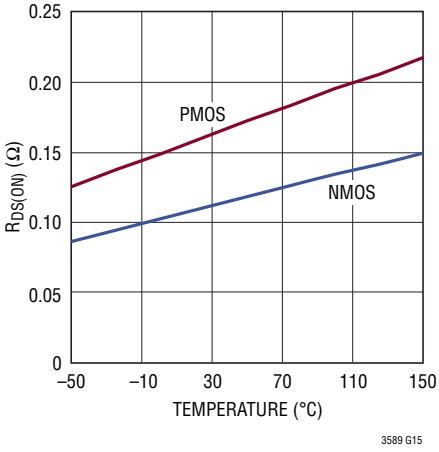
Step-Down Switching Regulator 3 Efficiency vs I_{OUT}



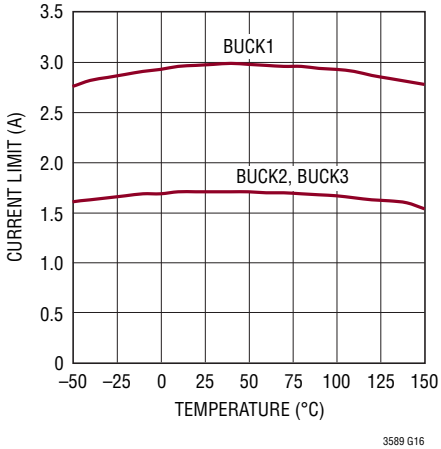
Step-Down Switching Regulator $R_{DS(ON)}$ vs Temperature



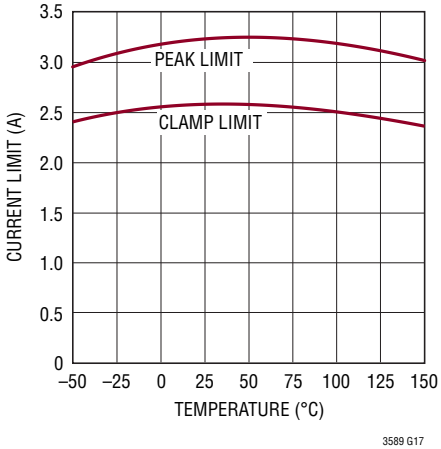
Buck-Boost $R_{DS(ON)}$ vs Temperature



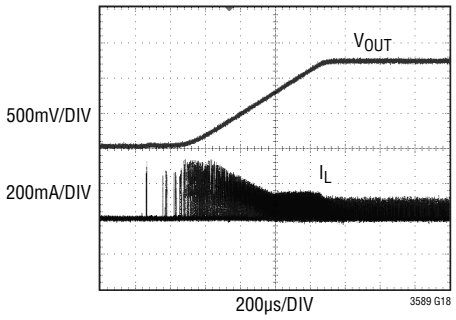
Step-Down Switching Regulator Current Limit vs Temperature



Buck-Boost Current Limit vs Temperature



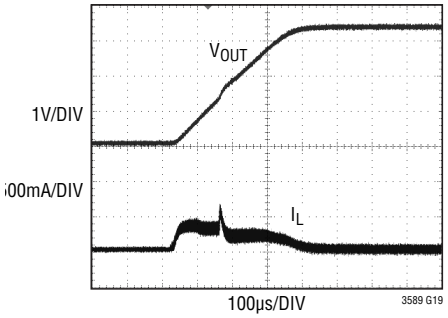
Step-Down Switching Regulator Soft-Start



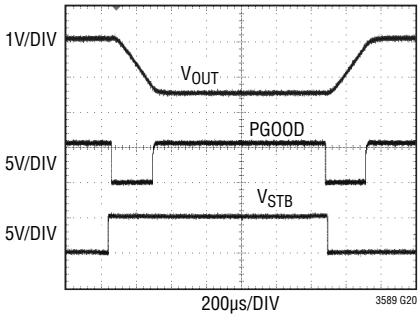
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, T_A = 25°C, unless otherwise noted.

Buck-Boost Switching Regulator Soft-Start

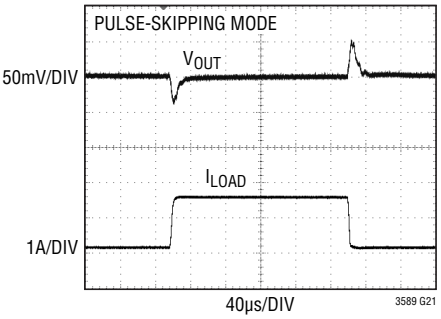


Dynamic Voltage Slew



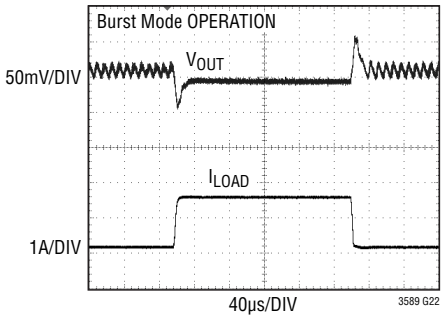
V_{RRCR} = 1.75mV/µs

Step-Down Switching Regulator 1 Load Step



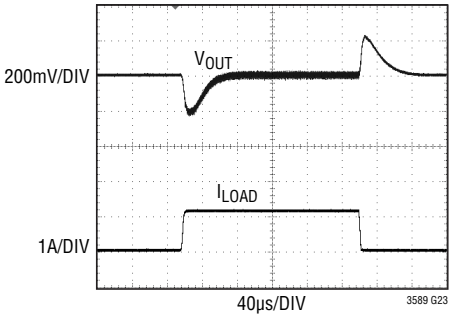
LOAD CAPACITANCE = 44µF

Step-Down Switching Regulator 1 Load Step



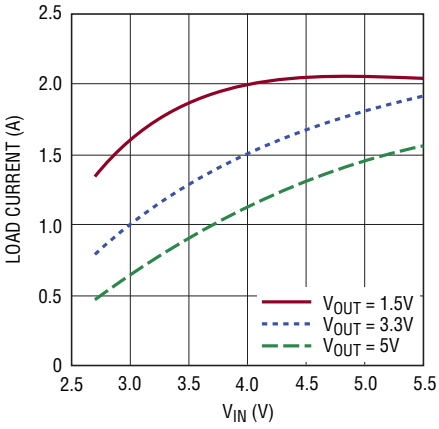
LOAD CAPACITANCE = 44µF

Buck-Boost Switching Regulator 1 Load Step

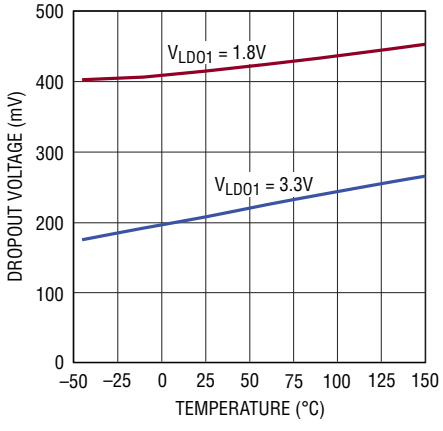


LOAD CAPACITANCE = 22µF

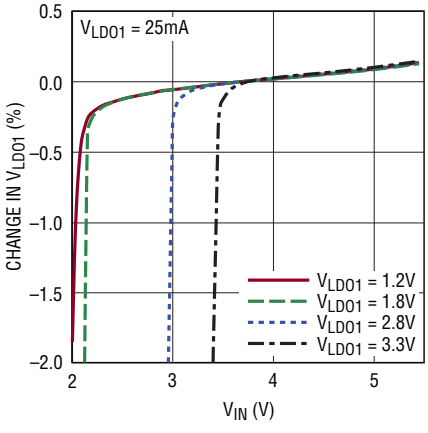
Maximum Buck-Boost Load Current vs V_{IN}



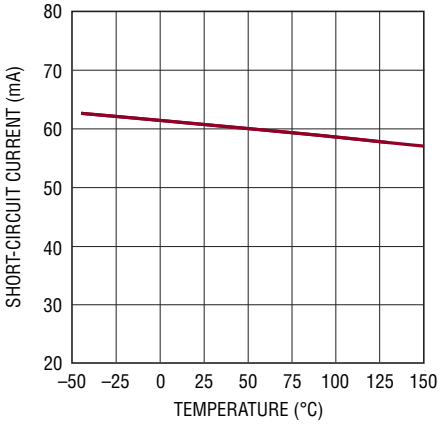
LDO1 Dropout Voltage vs Temperature



LDO1 Output Change vs V_{IN}



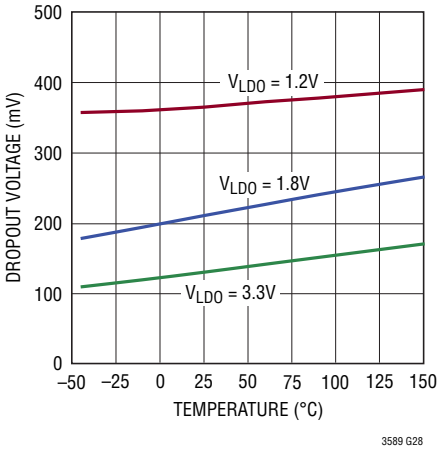
LDO1 Short-Circuit Current vs Temperature



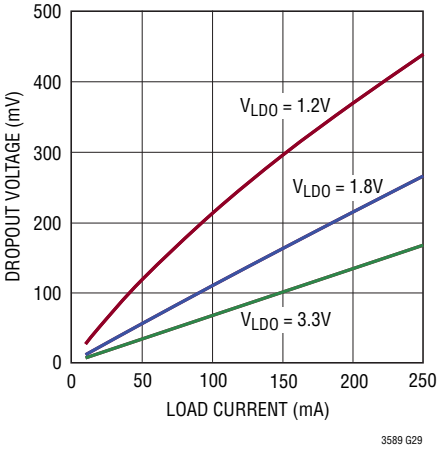
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, T_A = 25°C, unless otherwise noted.

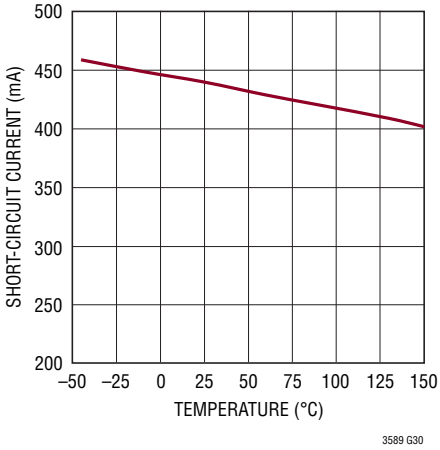
LDO2, LDO3, LDO4 Dropout Voltage vs Temperature



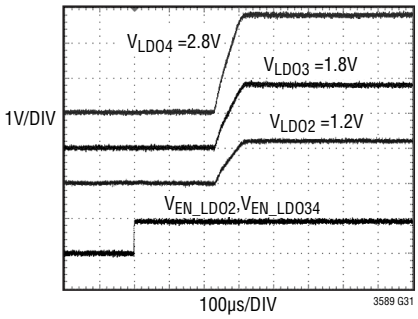
LDO2, LDO3, LDO4 Dropout Voltage vs Load Current



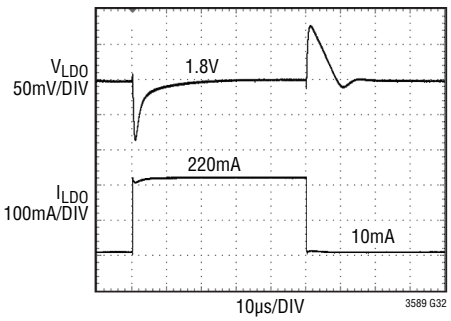
LDO2, LDO3, LDO4 Short-Circuit Current vs Temperature



LDO2, LDO3, LDO4 Enable Response

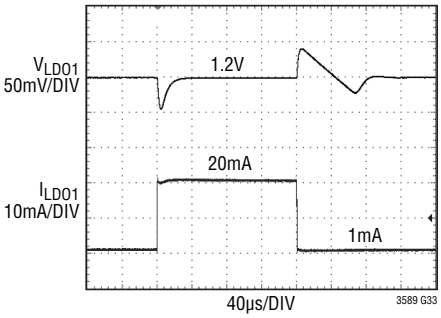


LDO2, LDO3, LDO4 Load Step Response



LOAD CAPACITANCE = 1µF

LDO1 Load Step Response



LOAD CAPACITANCE = 1µF

PIN FUNCTIONS

V_{IN_LDO2} (Pin 1): Power Input for LDO2. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO2 (Pin 2): Output Voltage of LDO2. Nominal output voltage is set with a resistor feedback divider that servos to an I^2C register controlled DAC reference. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO3 (Pin 3): Output Voltage of LDO3. Nominal output voltage is fixed at 1.8V. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO4 (Pin 4): Output Voltage of LDO4. Output voltages of 1.8V, 2.5V, 2.8V, and 3.3V are selected via the I^2C port. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

V_{IN_LDO34} (Pin 5): Power Input for LDO3 and LDO4. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor.

PV_{IN1} (Pin 6): Power Input for Step-Down Switching Regulator 1. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 4.7µF or greater ceramic capacitor.

SW1 (Pin 7): Switch Pin for Step-Down Switching Regulator 1. Connect one side of step-down switching regulator 1 inductor to this pin.

$\overline{RSTO}$ (Pin 8): Reset Output. Open-drain output pulls low when the always-on regulator LDO1 is below regulation and during a hard reset initiated by a pushbutton input.

EN_LDO2 (Pin 9): Enable LDO2 Logic Input. Active high input to enable LDO2. A weak pull-down forces EN_LDO2 low when left floating.

EN1 (Pin 10): Enable Step-Down Switching Regulator 1. Active high input to enable step-down switching regulator 1. A weak pull-down forces EN1 low when left floating.

EN2 (Pin 11): Enable Step-Down Switching Regulator 2. Active high input to enable step-down switching regulator 2. A weak pull-down forces EN2 low when left floating.

SW4AB (Pin 12): Switch Pin for Buck-Boost Switching Regulator 4. Connected to the buck-boost internal power switches A and B. Connect an inductor between this pin and SW4CD (Pin 19).

EN3 (Pin 13): Enable Step-Down Switching Regulator 3. Active high input to enable step-down switching regulator 3. A weak pull-down forces EN3 low when left floating.

EN4 (Pin 14): Enable Buck-Boost Switching Regulator 4. Active high input to enable buck-boost switching regulator 4. A weak pull-down forces EN4 low when left floating.

PV_{IN4} (Pin 15): Power Input for Switching Regulator 4. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 4.7µF or greater ceramic capacitor.

BB_OUT (Pin 16): Output Voltage of Buck-Boost Switching Regulator 4. This pin must be bypassed to ground with a 22µF or greater ceramic capacitor.

$\overline{IRQ}$ (Pin 17): Interrupt Request Output. Open-drain driver is pulled low for power good, undervoltage, and overtemperature warning and fault conditions. Clear $\overline{IRQ}$ by writing to the I^2C CLIRQ command register.

EN_LDO34 (Pin 18): Enable LDO3 and LDO4 Logic Input. Active high to enable LDO3 and LDO4. Disable LDO4 via I^2C software commands using I^2C command registers OVEN or L2DTV2. A weak pull-down forces EN_LDO34 low when left floating.

SW4CD (Pin 19): Switch Pin for Buck-Boost Switching Regulator 4. Connected to the buck-boost internal power switches C and D. Connect an inductor between this node and SW4AB (Pin 12).

PWR_ON (Pin 20): External Power-On. Handshaking pin to acknowledge successful power-on sequence. PWR_ON must be driven high within five seconds of WAKE going high to keep power on. It can be used to activate the WAKE output by driving high. Drive low to shut down WAKE.

$\overline{ON}$ (Pin 21): Pushbutton Input. A weak internal pull-up forces $\overline{ON}$ high when left floating. A normally open push-button is connected from $\overline{ON}$ to ground to force a low state on this pin.

PIN FUNCTIONS

PBSTAT (Pin 22): Pushbutton Status. Open-drain output to be used for processor interrupts. PBSTAT mirrors the status of $\overline{ON}$ pushbutton pin. PBSTAT is delayed 50ms from $\overline{ON}$ pin for debounce.

WAKE (Pin 23): System Wake Up. Open-drain driver output releases high when signaled by pushbutton activation or PWR_ON input. It may be used to initiate a pin-strapped power-up sequence by connecting to a regulator enable pin to initiate a pin-strapped power-on sequence.

PVIN2 (Pin 24): Power Input for Step-Down Switching Regulator 2. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 4.7µF or greater ceramic capacitor.

SW2 (Pin 25): Switch Pin for Step-Down Switching Regulator 2. Connect one side of step-down switching regulator 2 inductor to this pin.

SW3 (Pin 26): Switch Pin for Step-Down Switching Regulator 3. Connect one side of step-down switching regulator 3 inductor to this pin.

PVIN3 (Pin 27): Power Input for Step-Down Switching Regulator 3. Tie this pin to the V_{IN} supply. This pin should be bypassed to ground with a 4.7µF or greater ceramic capacitor.

VSTB (Pin 28): Voltage Standby. When VSTB is low, DAC reference registers are selected by bit values in command register VCCR. When VSTB is high, the DAC registers are forced xxDVT2 registers. Tie VSTB to ground if unused.

PGOOD (Pin 29): Power Good Output. Open-drain output pulls down when any regulator falls below power good threshold and during regulator dynamic voltage slew unless disabled in I²C register. Pulls down when all regulators are disabled.

SCL (Pin 30): Clock Input Pin for the I²C Serial Port. The I²C logic levels are scaled with respect to DV_{DD}.

SDA (Pin 31): Data Input Pin for the I²C Serial Port. The I²C logic levels are scaled with respect to DV_{DD}.

DV_{DD} (Pin 32): Supply Voltage for I²C Serial Port. This pin sets the logic reference level of SCL and SDA I²C pins. DV_{DD} resets I²C registers to power on state when driven to <1V. SCL and SDA logic levels are scaled to DV_{DD}. Connect a 0.1µF decoupling capacitor from this pin to ground.

BUCK2_FB (Pin 33): Feedback Input for Step-Down Switching Regulator 2. Set full-scale output voltage using resistor divider connected from the output of step-down switching regulator 2 to this pin to ground.

BUCK3_FB (Pin 34): Feedback Input for Step-Down Switching Regulator 3. Set full-scale output voltage using resistor divider connected from the output of step-down switching regulator 3 to this pin to ground.

LDO1_FB (Pin 35): Feedback Input for LDO1. Set output voltage using a resistor divider connected from LDO1_STDBY to this pin to ground.

LDO1_STDBY (Pin 36): Always-On LDO1 Output. This pin provides an always-on supply voltage useful for light loads such as a watchdog microprocessor or a real-time clock. Connect a 1µF capacitor from LDO1_STBY to ground.

V_{IN} (Pin 37): Supply Voltage Input. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor.

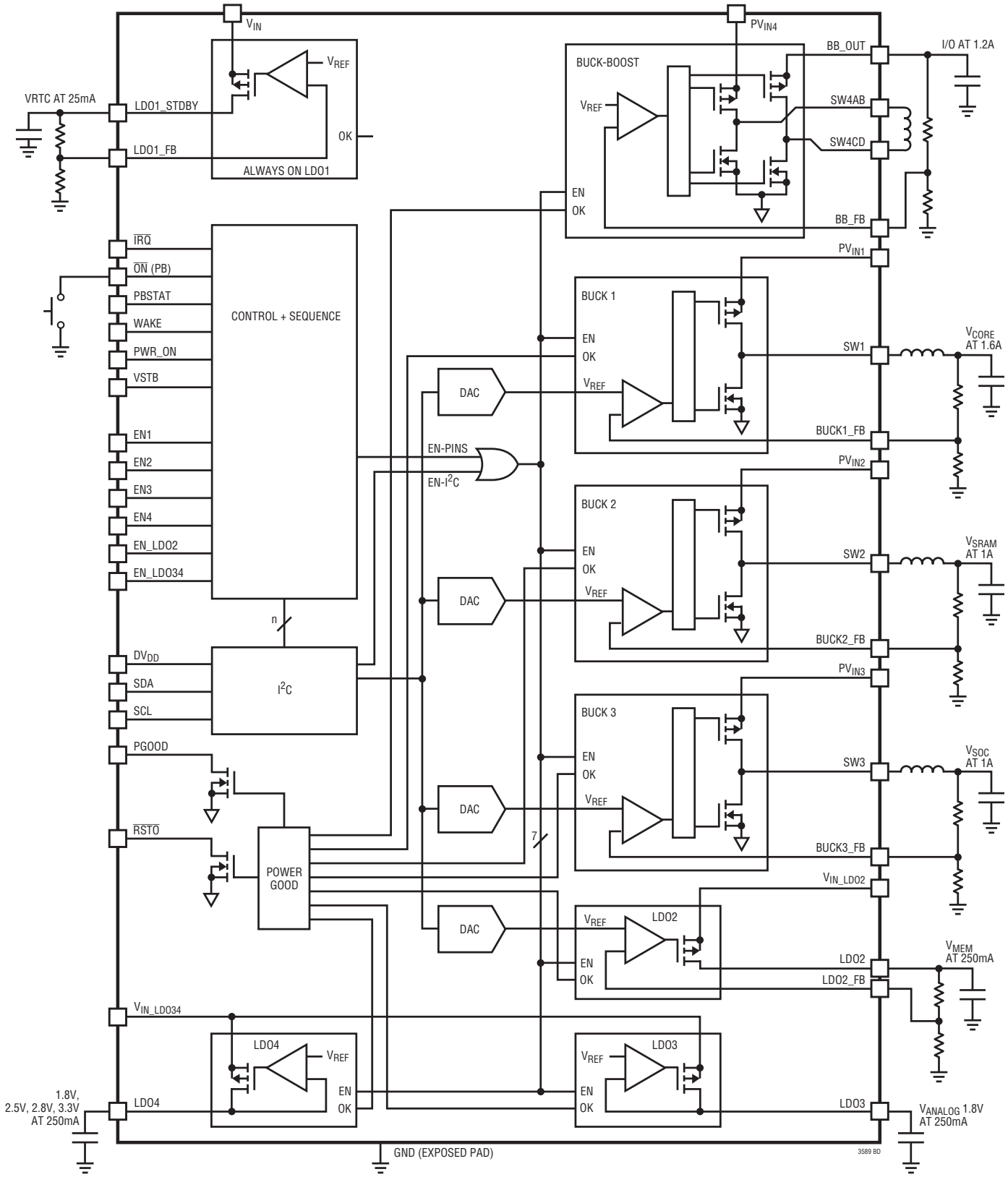
LDO2_FB (Pin 38): Feedback Input for LDO2. Set full-scale output voltage using a resistor divider connected from LDO2_OUT to this pin to ground.

BUCK1_FB (Pin 39): Feedback Input for Step-Down Switching Regulator 1. Set full-scale output voltage using resistor divider connected from the output of step-down switching regulator 1 to this pin to ground.

BB_FB (Pin 40): Feedback Input for Buck-Boost Switching Regulator 4. Set the output voltage using resistor divider connected from BB_OUT to this pin to ground.

GND (Exposed Pad Pin 41): Ground. The Exposed Pad must be connected to a continuous ground plane on the second layer of the printed circuit board by several interconnect vias directly under the LTC3589 for maximum heat transfer.

BLOCK DIAGRAM



OPERATION

INTRODUCTION

The LTC3589 is a complete power management solution for portable microprocessors and peripheral devices. It generates a total of eight voltage rails for supplying power to the processor core, SDRAM, system memory, PC cards, always-on real-time clock and HDD functions. Supplying the voltage rails are an always-on low quiescent current 25mA LDO, one 1.6A and two 1A step-down regulators, a 1.2A buck-boost regulator, and three 250mA low dropout regulators. Supporting the multiple regulators is a highly configurable power-on sequencing capability, dynamic voltage slewing DAC output voltage control, a pushbutton interface controller, regulator control via an I^2C interface, and extensive status and interrupt outputs.

The LTC3589 operates over an input supply range of 2.7V to 5.5V. The input supplies for the 250mA LDO regulators may operate as low as 1.7V to limit power loss at low output voltages.

The always-on LDO1 provides a resistor programmable output voltage as low as 0.8V and is capable of supplying 25mA. With only the always-on LDO active the LTC3589 draws just 8µA (typical). Always-on LDO1 will continue to operate with V_{IN} levels as low as 2.0V (typical) to maintain memory and RTC function as long as possible.

Each of the 250mA LDO regulators has unique output voltage configurations. LDO3 has a fixed 1.8V output. LDO4 has four output levels selectable via the I^2C interface. Its possible outputs are 1.8V, 2.5V, 2.8V, and 3.3V. LDO2 has a dynamically slewing DAC set point reference and an external feedback pin to set the output voltage range with a resistive divider. Each LDO draws 60µA (typical) quiescent current.

The LTC3589 includes three internally compensated constant-frequency current mode step-down switching regulators providing 1A, 1A, and 1.6A. Step-down regulator switching frequencies of 2.25MHz or 1.125MHz are independently selected for each step-down regulator using the I^2C command registers. The power-on default frequency is 2.25MHz. Each of the step-down regulators have dynamically slewing DAC input references and external feedback pins to set output voltage range. The step-down regulators three operating modes, pulse-skipping, burst, or forced continuous, are set using the I^2C interface. In pulse-skipping mode the regulator will support 100% duty cycle. For best efficiency at low output loads select Burst Mode operation. Forced continuous mode minimizes output voltage ripple at light loads.

The 4-switch buck-boost DC/DC voltage mode converter generates a user-programmable output voltage rail from 1.8V to 5V. Utilizing a proprietary switching algorithm, the buck-boost converter maintains high efficiency and low noise operation with input voltages that are above, below or equal to the required output rail. The buck-boost error amplifier uses a fixed 0.8V reference and the output voltage is set by an external resistor divider. Burst Mode operation is enabled through the I^2C control registers. No external compensation components are required for the buck-boost converter.

The reference inputs for the three step-down regulators and LDO2 are 5-bit D to A converters with up-down ramping at selectable slew rates. The slew endpoint voltages and select bits are stored in I^2C registers for each DAC. A select bit in the I^2C command registers chooses which register to use for each target voltage. Variable reference slew rates from 0.88mV/µs to 7mV/µs are selectable in the I^2C register. Each of the four DACs has independent voltage, voltage select, and slew rate control registers.

The LTC3589 is equipped with a pushbutton control circuit that will activate the WAKE output, indicate pushbutton status via the PBSTAT pin, and initiate a hard reset shutdown of the regulators. Grounding the $\overline{ON}$ pin with the pushbutton for 400ms will force the WAKE pin to release HIGH. The WAKE pin output can be tied to the enable pin of the first regulator in a power-on sequence. Once in the power-on state, subsequent pushes of the button longer than 50ms are mirrored by the PBSTAT output. Holding $\overline{ON}$ LOW for five seconds disables all the regulators, pulls down the WAKE pin, and pulls down $\overline{RSTO}$ for one second to indicate to the processor that a hard reset occurred. All regulator enables and pushbutton inputs are inhibited for one second following the hard reset.

The LTC3589 has flexible options for enabling and sequencing the regulator enables. The regulators are enabled using input pins or the I^2C serial port. To define a power-on

OPERATION

sequence tie the enable of the first regulator to be powered up to the WAKE pin. Connect the first regulators output to the enable pin of the second regulator, and so on. One or more regulators may be started in any sequence. Each enable pin has a 200µs (typical) delay between the pin and the internal enable of the regulator. When the system controllers are satisfied that power rails are up, the controller must drive PWR_ON HIGH to keep WAKE active. To ensure correct start-up sequencing, the regulators outputs are monitored by voltage comparators which require each output to discharge below 300mV before re-enabling. A software control command register function is available which sets the regulators to effectively ignore their enable pins but respond to I²C register enables. This function enables software-only control of any combination of pin-strapped regulators and is useful for implementing system power saving modes. Keep-alive mode exempts selected regulators from turning off during normal shutdown. In keep-alive mode, the LTC3589 powers down normally and is ready for the next start-up sequence, but selected regulators are kept on to power memory or other functions during system standby modes.

The LTC3589 will shut down all regulators and pull down the WAKE pin under high temperature, V_{IN} undervoltage, and extended low regulator output voltage conditions. Status of a hard shutdown is reported by the $\overline{IRQ}$ status pin and the IRQSTAT status register.

The I²C serial port on the LTC3589 contains 13 command registers for controlling each of the regulators, one read-only register for monitoring each regulators power good status, one read-only register for reading the cause of an $\overline{IRQ}$ event, and one clear IRQ command register. The LTC3589 I²C supports random addressing of any register.

ALWAYS-ON LDO

The LTC3589 includes a low quiescent current low dropout regulator that remains powered whenever a valid supply is present on V_{IN}. The always-on LDO will remain active until V_{IN} drops below 2.0V (typical). This is below the 2.5V undervoltage threshold in effect for the rest of the LTC3589 circuits. The always-on LDO is used to provide power to a standby microcontroller, real-time clock, or other keep-alive circuits. The LDO is guaranteed to support a 25mA load. A 1µF low impedance ceramic bypass capacitor from LDO1_STBY to GND is required for compensation. A power good monitor pulls $\overline{RSTO}$ LOW for a minimum of 14ms (typical) whenever LDO1_STBY is 8% below its regulation target. An LDO1_STBY undervoltage condition is reported in the PGOOD status register. The output voltage of LDO1 is set with a resistor divider connected from LDO1_STBY to the feedback pin LDO1_FB, as shown in Figure 1.

$$V_{LDO\_STBY} = 0.8 \bullet \left(1 + \frac{R1}{R2}\right)(V)$$

Typical values for R1 are in the range of 40k to 1M.

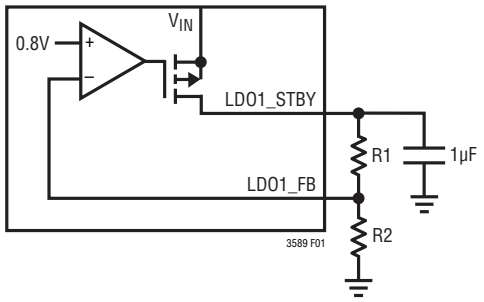


Figure 1. Always-On LDO Application Circuit

LDO1_STBY is protected from short-circuits and overloading.

250mA LDO REGULATORS

Three LDO regulators on the LTC3589 will each deliver up to 250mA output. The LDO regulators are enabled by pin input or I²C command register. Pin EN_LDO2 enables LDO2 and pin EN_LDO34 enables LDO3 and LDO4 together. An I²C command register bit is available to decouple LDO4 from pin EN_LDO34 so that LDO4 is under command register control only. All the regulators have current limit protection circuits. When disabled, a 2.5k internal pull-down resistor is connected to the regulators output.

OPERATION

To help reduce LDO power loss in the system, the regulators have dedicated supply inputs that may be lower than the main V_{IN} supply. Connect a low ESR 1µF capacitor to each of the output pins LDO2, LDO3, and LDO4.

LDO Regulator 2

One of the LTC3589 dynamic slewing DACs serves as the reference input of LDO2. The output range of LDO2 is set using an external resistor divider connected from LDO2 to the feedback pin LDO2_FB, as shown in Figure 2. Set the output voltage of LDO2 using the following formula:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \bullet (0.3625 + L2DTVx \bullet 0.0125)$$

L2DTVx is the five bit word contained in the LDO2 dynamic target voltage 1 (L2DTV1) or the LDO2 dynamic target voltage 2 (L2DTV2) command registers. The default value of L2DTVx[4-0] is 11001 to output a reference voltage of 0.675V. LDO2 is enabled by writing bit 4 in the output voltage enable (OVEN) command register to 1 or driving the LDO2_EN pin high. Whenever the command is given to slew LDO2 DAC reference to a lower voltage an integrated 2.5k pull-down resistor is connected to LDO2 output.

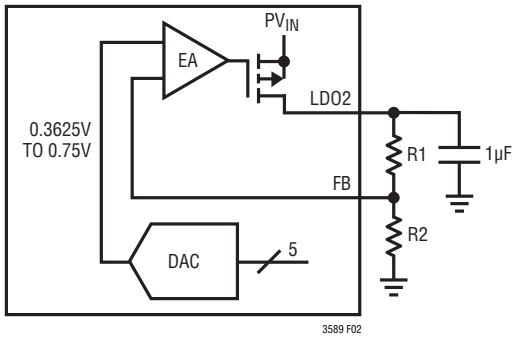


Figure 2. LDO2 Application Circuit

Table 1. Shows the I²C command register settings used to control LDO2.

Table 1. LDO 2 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
OVEN[4]	0* 1	Disable Enable
SCR2[4]	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately
VCCR[5]	0* 1	Select Register L2DTV1 (V1) Reference Select Register L2DTV2 (V2) Reference
VCCR[6]	1	Initiate Dynamic Voltage Slew
VRRCR[7-6]	00 01 10 11*	Reference Slew Rate = 0.88mV/µs Reference Slew Rate = 1.75mV/µs Reference Slew Rate = 3.5mV/µs Reference Slew Rate = 7mV/µs
L2DTV1[4-0]	11001*	DAC Dynamic Target Voltage V1
L2DTV1[5]	0* 1	Force PGOOD Low When Slewing Normal PGOOD Operation When Slewing
L2DTV1[7]	0* 1	Shutdown LDO2 Normally Keep LDO2 Alive
L2DTV2[4-0]	11001*	DAC Dynamic Target Voltage V2

* Denotes Default Power-On Value

LDO Regulator 3

LDO3 is a fixed 1.8V output regulator. LDO3 is enabled by driving pin EN_LDO34 high or by writing command register OVEN[5] to 1.

Table 2 shows the I²C command register settings used to control LDO3.

Table 2. LDO 3 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
OVEN[5]	0* 1	Disable Enable
SCR2[5]	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately

* Denotes Default Power-On Value

OPERATION

LDO Regulator 4

LDO4 has four output voltage options that are controlled by the contents of command register L2DTV2 bits 6 and 5. By default, pin EN_LDO34 enables and disables LDO3 and LDO4 simultaneously when command register bits OVEN[5] and OVEN[6] are LOW. When EN_LDO34 is LOW, LDO3 and LDO4 are controlled by writing to command register bits OVEN[5] and OVEN[6] respectively. When command register bit L2DTV2[7] is HIGH, control of LDO4 is disconnected from pin EN_LDO34 and controlled by command register bit OVEN[6] regardless of the status of EN_LDO34. Table 3 shows the I²C command register settings used to control LDO4.

Table 3. LDO 4 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
OVEN[6]	0* 1	Disable Enable
SCR2[6]	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately
L2DTV2[6-5]	00* 01 10 11	V_{LDO4} = 2.8V V_{LDO4} = 2.5V V_{LDO4} = 1.8V V_{LDO4} = 3.3V
L2DTV2[7]	0* 1	LDO4 Enable Controlled by EN_LDO34 LDO4 Enable Controlled by OVEN[6]

* Denotes Default Power-On Value

STEP-DOWN SWITCHING REGULATORS

Output Voltage Programming

Each of the step-down converters uses a dynamically slewing DAC output for its reference. The full-scale output voltage is set by using a resistor divider connected from the step-down switching regulator output to the feedback pins (B1_FB, B2_FB, and B3_FB), as shown in Figure 3. Set the output voltage of step-down switching regulators using the following formula:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \bullet (0.3625 + BxDTVx \bullet 0.0125)(V)$$

BxDTVx is the decimal value of the five bit binary number in the I²C BxDTV1 or BxDTV2 command registers. BxDTV1 and BxDTV2 default to 11001 to output a reference voltage

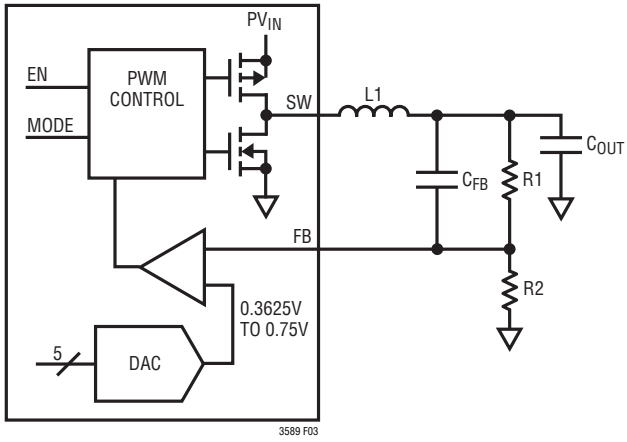


Figure 3. Step-Down Switching Regulator Application Circuit

of 0.675V. Typical values for R1 are in the range of 40k to 1M. The capacitor C_{FB} cancels the pole created by the feedback resistors and the input capacitance on the FB pin and also helps to improve load step transient response. A value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 10pF and 33pF may yield improved transient response.

Operating Modes

The step-down switching regulators include three possible operating modes to meet the noise and power needs of a variety of applications.

In pulse-skipping mode, at the start of every cycle, a latch is set that turns on the main P-channel MOSFET switch. During the cycle, a current comparator compares the peak inductor current to the output of an error amplifier. The output of the current comparator resets the latch. At this time the P-channel MOSFET switch turns off and the N-channel MOSFET synchronous rectifier turns on. The N-channel MOSFET synchronous rectifier will turn off when the end of the clock cycle is reached or if the inductor current drops through zero. Using this method of operation, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary loop compensation is internal to the step-down switching regulator requiring only a single ceramic output capacitor for stability. At light loads in pulse-skipping mode, the inductor current may reach zero on each pulse that will

OPERATION

turn off the N-channel MOSFET synchronous rectifier. In this case the switch node (SW1, SW2, or SW3) goes HIGH impedance and the switch node will ring. This is discontinuous operation and is normal behavior for a switching regulator. At very light loads in pulse-skipping mode, the step-down switching regulators will automatically skip pulses as needed to maintain output regulation. At high duty cycle ($V_{OUTX} > V_{IN}/2$) it is possible for the inductor current to reverse at light loads causing the step-down switching regulator to operate continuously. When operating continuously, regulation and low noise output voltage are maintained, but input operating current will increase to a few milliamps.

In the forced continuous mode of operation, the inductor current is allowed to be less than zero over the full range of duty cycles. Operating in forced continuous mode is a lower noise option at light loads than pulse-skipping operation but with the drawback of higher V_{IN} current due to the continuous operation of the MOSFET switch and rectifier. Since the inductor current is allowed to be negative in forced continuous operation the step-down switching regulator has the ability to sink output current. The LTC3589 automatically forces the step-down switching regulator into forced continuous mode when dynamically slewing the DAC voltage reference down.

When the LTC3589 step-down switching regulators are in Burst Mode operation, they automatically switch between fixed frequency pulse-skipping operation and hysteretic Burst Mode control as a function of the load current. At light loads the step-down switching regulators control the inductor current directly and use a hysteretic control loop to minimize both noise and switching losses. While in Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The step-down switching regulator then goes into a low power sleep mode during which the output capacitor provides the load current. In sleep mode, most of the switching regulator's circuitry is powered off to conserve battery power. When the output voltage drops below the regulation point the regulator's circuitry is powered on and another burst cycle begins. As the load current increases, the time between burst cycles decreases. Above a load current about ¼ rated output load, the step-down switching regulators will switch to low noise constant-frequency PWM operation.

Set the mode of operation for the step-down switching regulators by using the I^2C command register SCR1. Each of the three regulators has independent mode control.

A step-down switching regulator may enter a dropout condition when its input voltage drops to near its programmed output voltage. For example, a discharging battery voltage of 3.4V dropping to the regulators programmed output voltage of 3.3V. When this happens the duty cycle of the P-channel MOSFET switch is increased until it turns on continuously with 100% duty cycle. In dropout, the regulators output voltage equals the regulators input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor DC resistance.

Table 4, Table 5, and Table 6 show the I^2C command register settings used to control the step-down switching regulators.

Table 4. Step-Down Switching Regulator 1 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
SCR1[1-0]	00* 01 10	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode
OVEN[0]	0* 1	Disable Enable
SCR2[0]	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately
VCCR[1]	0* 1	Select Register B1DTV1 (V1) Reference Select Register B1DTV2 (V2) Reference
VCCR[0]	1	Initiate Dynamic Voltage Slew
VRRCR[1-0]	00 01 10 11*	Reference Slew Rate = 0.88mV/µs Reference Slew Rate = 1.75mV/µs Reference Slew Rate = 3.5mV/µs Reference Slew Rate = 7mV/µs
B1DTV1[5]	0* 1	Force PGOOD Low When Slewing Normal PGOOD Operation When Slewing
B1DTV1[4-0]	11001*	DAC Dynamic Target Voltage V1
B1DTV2[4-0]	11001*	DAC Dynamic Target Voltage V2
B1DTV2[5]	0* 1	2.25MHz Switching Frequency 1.125MHz Switching Frequency
B1DTV2[6]	0* 1	Switch on Clock Phase 1 Switch on Clock Phase 2
B1DTV2[7]	0* 1	Shutdown Regulator 1 Normally Keep Regulator 1 Alive

* Denotes Default Power-On Value

OPERATION

Soft-Start

Soft-start is accomplished by gradually increasing the input reference voltage on each step-down switching regulator from 0V to the dynamic reference DAC output level at a rate of 0.8V/ms. This allows each output to rise slowly, helping minimize inrush current required to charge up the regulator output capacitor. A soft-start cycle occurs whenever a regulator is enabled either initially or while powering up following a fault condition. A soft-start cycle is not triggered by a change of operating modes or a dynamic voltage slew. During soft-start the converter is forced to pulse-skipping mode regardless of the settings in the SCR1 command register.

Table 5. Step-Down Switching Regulator 2 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
SCR1[3-2]	00* 01 10	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode
OVEN[1]	0* 1	Disable Enable
SCR2[1]	0* 1	Wait for Output Below 300mV Before Enable Enable immediately
VCCR[3]	0* 1	Select Register B2DTV1 (V1) Reference Select Register B2DTV2 (V2) Reference
VCCR[2]	1	Initiate Dynamic Voltage Slew
VRRCR[3-2]	00 01 10 11*	Reference Slew Rate = 0.88mV/µs Reference Slew Rate = 1.75mV/µs Reference Slew Rate = 3.5mV/µs Reference Slew Rate = 7mV/µs
B2DTV1[5]	0* 1	Force PGOOD Low When Slewing Normal PGOOD Operation When Slewing
B2DTV1[4-0]	11001*	DAC Dynamic Target Voltage V1
B2DTV2[4-0]	11001*	DAC Dynamic Target Voltage V2
B2DTV2[5]	0* 1	2.25MHz Switching Frequency 1.125MHz Switching Frequency
B2DTV2[6]	0* 1	Switch on Clock Phase 1 Switch on Clock Phase 2
B2DTV2[7]	0* 1	Shutdown Regulator 2 Normally Keep Regulator 2 Alive

* Denotes Default Power-On Value

Switching EMI Control

The step-down switching regulators contain new patent pending circuitry to limit the edge rate of the switch nodes SW1, SW2, and SW3. This new circuitry controls the transition of the switch node over a period of a few nanoseconds, significantly reducing radiated EMI and conducted supply noise while maintaining high efficiency. Since slowing the slew rate of the switch nodes causes efficiency loss, the slew rate of the step-down switching regulators is adjustable using the I^2C command register B1DTV1 bits 6 and 7. Optimize efficiency or EMI as necessary with four different slew rate settings. The power-on default is the fastest slew rate, highest efficiency setting.

Table 6. Step-Down Switching Regulator 3 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
SCR1[5-4]	00* 01 10	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode
OVEN[2]	0* 1	Disable Enable
SCR2[2]	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately
VCCR[5]	0* 1	Select Register B3DTV1 (V1) Reference Select Register B3DTV2 (V2) Reference
VCCR[4]	1	Initiate Dynamic Voltage Slew
VRRCR[5-4]	00 01 10 11*	Reference Slew Rate = 0.88mV/µs Reference Slew Rate = 1.75mV/µs Reference Slew Rate = 3.5mV/µs Reference Slew Rate = 7mV/µs
B3DTV1[5]	0* 1	Force PGOOD Low When Slewing Normal PGOOD Operation When Slewing
B3DTV1[4-0]	11001*	DAC Dynamic Target Voltage V1
B3DTV2[4-0]	11001*	DAC Dynamic Target Voltage V2
B3DTV2[5]	0* 1	2.25MHz Switching Frequency 1.125MHz Switching Frequency
B3DTV2[6]	0* 1	Switch on Clock Phase 1 Switch on Clock Phase 2
B3DTV2[7]	0* 1	Shutdown Regulator 3 Normally Keep Regulator 3 Alive

* Denotes Default Power-On Value

OPERATION

Operating Frequency

The switching frequency of each of the LTC3589 step-down switching regulators may be independently set using I²C command register bits B1DTV2[5], B2DTV2[5] and B3DTV2[5]. The power-on default frequency is 2.25MHz. Writing bit BxDTV2[5] HIGH will reduce the switching frequency to 1.125MHz. Selection of the operating frequency is determined by desired efficiency, component size and converter duty cycle.

Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses but requires larger inductance and capacitance values for comparable output ripple voltage. The lowest duty cycle of the step-down switching regulator is determined by the converters minimum on-time. Minimum on-time is the shortest time duration that the converter is capable of turning its top PMOS on and off again. The time consists of the gate charge time plus internal delays associated with peak current sensing. The minimum on-time of the LTC3589 is approximately 90ns. If the duty cycle falls below what can be accommodated by the minimum on-time, the converter will begin to skip cycles. The output voltage will continue to be regulated but the ripple voltage and current will increase. With the switching frequency set to 2.25MHz, the minimum supported duty cycle is 20%. Switching at 1.125MHz the converter can support a 10% duty cycle.

Phase Selection

To reduce the cycle by cycle peak current drawn by the switching regulators, the clock phase of each of the LTC3589 step-down switching regulators can be set using I²C command register bits B1DTV2[6], B2DTV2[6] and B3DTV2[6]. The internal full-rate clock has a nominal duty cycle of 20% while the half-rate clocks have a 50% duty cycle. Setting the command register bits high will delay the start of each converter switching cycle by 20% or 50% depending on the selected operating frequency.

Inductor Selection

The choice of step-down switching regulator inductor influences the efficiency of the converter and the magnitude of the output voltage ripple. Larger inductance values reduce inductor current ripple and therefore lower output voltage ripple. A larger value inductor improves efficiency by lowering the peak current to be closer to the average output current. Larger inductors, however, generally have higher series resistance that counters the efficiency advantage of reduced peak current.

Inductor ripple current is a function of switching frequency, inductance, V_{IN}, and V_{OUT}, as shown in this equation:

$$\Delta I_L = \frac{1}{f \bullet L} \bullet V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In an example application the LTC3589 step-down switching regulator 3 has a maximum load of 1A, V_{IN} equals 3.8V, and V_{OUT} is set for 1.2V. A good starting design point for inductor ripple is 30% of output current or 300mA. Using the equation for ripple current, a 1.2µH inductor should be selected.

An inductor with low DC resistance will improve converter efficiency. Select an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure the inductor does not saturate during normal operations. If short-circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the step-down converter. Table 7 shows inductors that work well with the step-down switching regulators.

Input/Output Capacitor Selection

Low ESR (equivalent series resistance) ceramic capacitors should be used at both the output and input supply of the switching regulators. Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 22µF capacitor is sufficient for the step-down

OPERATION

switching regulator outputs. For good transient response and stability the output capacitor should retain at least 10µF of capacitance over operating temperature and bias voltage. Place at least 4.7µF decoupling capacitance as close as possible to each PV_{IN} pin. Refer to Table 11 for recommended ceramic capacitor manufacturers.

BUCK-BOOST SWITCHING REGULATOR

Output Voltage Programming

Set the output voltage of the LTC3589 buck-boost switching regulator using an external resistor divider connected from BB_OUT to the feedback pin BB_FB and to GND, as shown in Figure 4.

$$V_{BB\_OUT} = 0.8 \bullet \left(1 + \frac{R1}{R2}\right)(V)$$

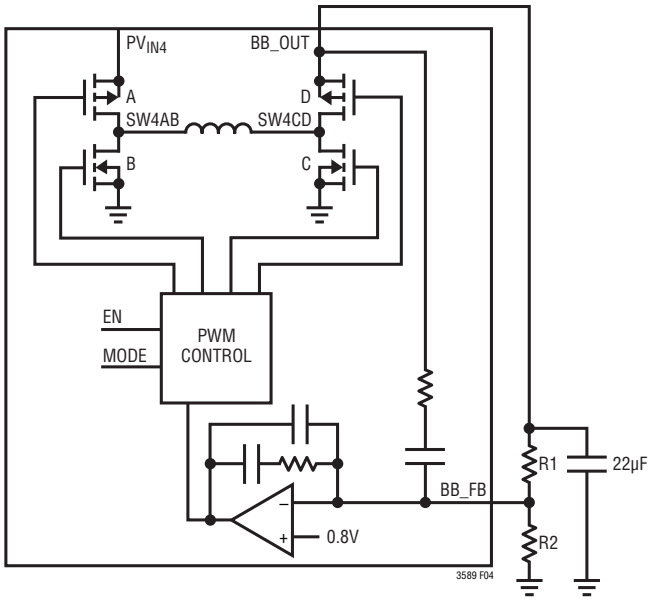


Figure 4. Buck-Boost Switching Regulator Application Circuit

Table 7. Inductors for Step-Down Switching Regulator 1

MANUFACTURERS	PART NUMBER	VALUE (µH)	DCR (Ω)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft	XPL4020-102ML	1.0	0.029	4.00	4.2 × 4.2 × 2.0
	XPL4020-152ML	1.5	0.036	3.60	4.2 × 4.2 × 2.0
	XPL4020-222ML	2.2	0.060	2.60	4.2 × 4.2 × 2.0
	LPS6225-222ML	2.2	0.045	3.90	6.0 × 6.0 × 2.0
	LPS6225-332ML	3.3	0.055	3.50	6.0 × 6.0 × 2.0
	LPS6225-472ML	4.7	0.065	3.00	6.0 × 6.0 × 2.0
Cooper	SD14-1R2-R	1.2	0.034	3.35	5.2 × 5.2 × 1.45
	SD14-1R5-R	1.5	0.039	2.91	5.2 × 5.2 × 1.45
	SD14-2R0-R	2.0	0.045	2.56	5.2 × 5.2 × 1.45
	SD25-2R2-R	2.2	0.031	2.80	5.2 × 5.2 × 2.5
Sumida	CDRH5D16NP-3R3N	3.3	0.045	2.60	5.6 × 5.6 × 1.8
TDK	VLF5014ST-1R0N2R7	1.0	0.050	2.7	4.8 × 4.6 × 1.4
	VLF5014st-2R2N2R3	2.2	0.073	2.3	4.8 × 4.6 × 1.4
	VLCF5020T-2R2N2R6-1	2.2	0.071	2.6	5.0 × 5.0 × 2.0
TOKO	1124BS-1R2N	1.2	0.047	2.9	4.5 × 4.7 × 1.8
	1124BS-1R8N	1.8	0.056	2.7	4.5 × 4.7 × 1.8
Tokin	H-DI-0520-2R2	2.2	0.048	2.6	5.3 × 5.3 × 2.0
	H-DI-0630-2R4	2.4	0.028	2.5	6.3 × 6.3 × 3.0
	H-DI-0630-3R8	3.8	0.040	2	6.3 × 6.3 × 3.0
Wurth	744042001	1.0	0.028	2.60	4.8 × 4.8 × 1.8
	744052002	2.5	0.030	2.4	5.8 × 5.8 × 1.8
	744053003	3.0	0.024	2.8	5.8 × 5.8 × 2.8
	7440530047	4.7	0.030	2.4	5.8 × 5.8 × 2.8
	7440430022	2.2	0.023	2.5	4.8 × 4.8 × 2.8

OPERATION

Table 8. Inductors for Step-Down Switching Regulators 2 and 3

MANUFACTURERS	PART NUMBER	VALUE (µH)	DCR (Ω)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft	XPL4020-102ML	1.0	0.029	4.00	4.2 × 4.2 × 2.0
	XPL4020-152ML	1.5	0.036	3.60	4.2 × 4.2 × 2.0
	XPL4020-472ML	4.7	0.130	1.90	4.2 × 4.2 × 2.0
Cooper	SD14-1R2-R	1.2	0.034	3.35	5.2 × 5.2 × 1.45
	SD14-3R2-R	3.2	0.066	2.00	5.2 × 5.2 × 1.45
	SD25-3R3-R	3.3	0.038	2.21	4.8 × 4.8 × 2.5
Sumida	CDRH5D16NP-4R7N	4.7	0.064	2.05	5.6 × 5.6 × 1.8
	CDRH38D16RHPNP-3R3M	3.3	0.059	1.46	4.2 × 4.2 × 1.8
TDK	VLF5014ST-2R2N2R3	2.2	0.073	2.3	4.8 × 4.6 × 1.4
	VLCF5020T-2R7N2R2-1	2.7	0.083	2.2	5.0 × 5.0 × 2.0
	VLCF5020T-3R3N2R0-1	3.3	0.096	2	5.0 × 5.0 × 2.0
TOKO	1124BS-2R4N	2.4	0.065	2.30	4.5 × 4.7 × 1.8
	1124BS-3R3N	3.3	0.074	2.10	4.5 × 4.7 × 1.8
Tokin	H-DI-0520-3R3	3.3	0.062	2.00	5.3 × 5.3 × 2.0
	H-DI-0520-4R7	4.7	0.090	1.80	5.3 × 5.3 × 2.0
	H-DI-0630-3R8	3.8	0.040	2.00	6.3 × 6.3 × 3.0
	H-DI-0630-4R7	4.7	0.043	1.90	6.3 × 6.3 × 3.0
Wurth	744043004	4.7	0.052	1.55	5.0 × 5.0 × 3.0
	744052002	2.5	0.030	2.4	5.8 × 5.8 × 1.8
	7440530047	4.7	0.030	2.4	5.8 × 5.8 × 2.8
	744042003	3.3	0.055	1.95	4.8 × 4.8 × 1.8
	7440430022	2.2	0.023	2.5	4.8 × 4.8 × 2.8

The value of R1 plays a role in setting the dynamics of the buck-boost voltage mode control loop. In general, a larger value for R1 will increase stability but reduce the speed of the transient response. A good starting point is to choose R1 equal to 1MΩ and calculate the value of R2 needed to set the target output voltage. If a large output capacitor is used, the bandwidth of the converter is reduced and R1 may be reduced to improve transient response. If a large inductor or small output capacitor is used then a larger R1 should be used to bring the loop toward more stable operation.

Operating Modes

Table 9 shows the I^2C command registers used to control the operating modes of the LTC3589 buck-boost converter. When command register SCR1 bit 6 is LOW, the LTC3589 buck-boost switching regulator operates in a fixed frequency pulse width modulation mode using voltage mode feedback control. A proprietary switching algorithm allows the converter to transition between buck, buck-boost, and boost modes without discontinuity in inductor current or loop characteristics. The switch topology is shown in the application circuit in Figure 4.

Table 9. Buck-Boost Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
SCR1[6]	0*	Continuous Mode
	1	Burst Mode Operation
OVEN[3]	0*	Disable
	1	Enable
SCR2[3]	0*	Wait for Output Below 300mV Before Enable
	1	Enable Immediately

* Denotes Default Power-On Value

When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Switch D turns on continuously and switch C remains off. Switches A and B are pulse width modulated to produce the required duty cycle to support the output

OPERATION

regulation voltage. As the input voltage decreases, switch A remains on for a larger portion of the switching cycle. When the duty cycle reaches approximately 85%, the switch pair AC begins turning on for a small fraction of the switching period. As the input voltage decreases further, the AC switch pair remains on for longer durations and the duration of the BD phase decreases proportionately. As the input voltage drops below the output voltage, the AC phase will eventually increase to the point that there is no longer any BD phase. At this point, switch A remains on continuously while switches CD operate as a boost converter to regulate the desired output voltage.

The buck-boost is set to Burst Mode operation by writing a 1 to command register SCR1 bit 6. Using Burst Mode operation at light loads improves efficiency and reduces standby current at zero loads. In Burst Mode operation, the inductor is charged with bursts of fixed peak amplitude current pulses. The current pulses are repeated as often as necessary to maintain the target output voltage. The maximum output current that can be supplied in Burst Mode operation is dependent upon the input and output voltage. Typically $I_{OUT(MAX)}$ in Burst Mode operation is equal to:

$$I_{OUT(MAX)} = \frac{0.28 \bullet V_{IN}}{V_{OUT} + V_{IN}} (A)$$

If the buck-boost load exceeds the maximum Burst Mode current capability then the output rail will lose regulation and the power good comparator will indicate a fault condition.

When the LTC3589 buck-boost is not enabled, a 2.5k pull-down resistor is connected between BB_OUT and ground.

Soft-Start

The buck-boost converter has an internal voltage mode soft-start circuit that ramps the buck-boosts error amp reference from 0V to 800mV at a rate of 2V/ms. During soft-start, the converter is regulating to the ramping reference and will respond to output load transients. During soft-start the buck-boost converter is forced into continuous mode operation regardless of the state of the SCR1 command register.

Current Limit Operation

The LTC3589 buck-boost regulator has current limit circuits to limit forward current through the A switch and reverse current through the D switch. The primary forward current limit circuit injects a small fraction of the inductor current into the feedback node whenever the inductor current exceeds 2.7A (typical). Forcing the current into the feedback node in the high gain feedback circuit has the effect of lowering the output voltage until the average current in switch A is equal to the current limit. The average limit uses the error amplifier in its active linear state so once the fault condition is removed the recovery is smooth with little overshoot.

A hard short on the output of the buck-boost will cause the inductor current to exceed the 2.7A average current limit. A second current limit turns off switch A in the event peak inductor current reaches 3A (typical). The instantaneous forward current limit provides extra protection in the event of a sudden hard short.

The reverse current comparator on the D switch monitors the current entering the BB_OUT pin. When this current exceeds 1A (typical) switch D will turn off for the remainder of the switching cycle. This feature protects the buck-boost converter from excessive reverse current if the buck-boost output is held above the regulation point by an external source.

Inductor Selection

Inductor selection criteria for the buck-boost are similar to those given for the step-down switching regulators. The buck-boost converter is designed to work with inductors in the range of 1µH to 3.3µH. For most applications use a 1.5µH inductor. Choose an inductor with a DC current rating at least two times larger than the maximum load current to

OPERATION

Table 10. Inductors for Buck-Boost Switching Regulator

MANUFACTURERS	PART NUMBER	VALUE (µH)	DCR (Ω)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft	XPL4020-152ML	1.5	0.036	3.60	4.2 × 4.2 × 2.0
	XPL4020-222ML	2.2	0.060	2.60	4.2 × 4.2 × 2.0
	XPL4020-332ML	3.3	0.085	2.40	4.2 × 4.2 × 2.0
	LPS6225-332ML	3.3	0.055	3.50	6.0 × 6.0 × 2.0
	LPS6225-472ML	4.7	0.065	3.00	6.0 × 6.0 × 2.0
Cooper	SD14-1R5-R	1.5	0.039	2.91	5.2 × 5.2 × 1.45
	SD14-2R0-R	2.0	0.045	2.56	5.2 × 5.2 × 1.45
	SD14-2R5-R	2.5	0.060	2.29	5.2 × 5.2 × 1.45
	SD14-3R2-R	3.2	0.066	2.00	5.2 × 5.2 × 1.45
	SD25-3R3-R	3.3	0.038	2.21	4.8 × 4.8 × 2.5
Sumida	CDRH5D16NP-3R3N	3.3	0.045	2.60	5.6 × 5.6 × 1.8
	CDRH5D16NP-4R7N	4.7	0.064	2.05	5.6 × 5.6 × 1.8
TDK	VLF5014ST-2R2N2R3	2.2	0.073	2.3	4.8 × 4.6 × 1.4
	VLCF5020T-2R7N2R2-1	2.7	0.083	2.2	5.0 × 5.0 × 2.0
	VLCF5020T-3R3N2R0-1	3.3	0.096	2	5.0 × 5.0 × 2.0
TOKO	1124BS-1R8N	1.8	0.056	2.70	4.5 × 4.7 × 1.8
	1124BS-3R3N	3.3	0.074	2.10	4.5 × 4.7 × 1.8
Tokin	H-DI-0520-3R3	3.3	0.062	2.00	5.3 × 5.3 × 2.0
	H-DI-0630-3R8	3.8	0.040	2.00	6.3 × 6.3 × 3.0
Wurth	744052002	2.5	0.030	2.4	5.8 × 5.8 × 1.8
	7440420027	2.7	0.047	2.2	4.8 × 4.8 × 1.8
	744053003	3.0	0.024	2.8	5.8 × 5.8 × 2.8
	7440530047	4.7	0.030	2.4	5.8 × 5.8 × 2.8

ensure that the inductor does not saturate during normal operation. If output short-circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the buck-boost converter. Table 9 shows several inductors that work well with the LTC3589 buck-boost regulator.

Capacitor Selection

Low ESR ceramic capacitors should be used at both the output and input supply of the buck-boost switching regulator. Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 22µF capacitor is sufficient for the buck-boost switching regulator output. For good transient response and stability the output capacitor should retain at least 10µF of capacitance over operating temperature and bias voltage. Place at least 4.7µF decoupling capacitance as close as possible to PV_{IN4} pin. Refer to Table 11 for recommended ceramic capacitor manufacturers.

Table 11. Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

OPERATION

SLEWING DAC REFERENCE OPERATION

Controlling the DAC References

The three LTC3589 step-down switching regulators and linear regulator LDO2 have programmable DAC reference inputs. Each DAC is programmable from 0.3625V to 0.75V in 12.5mV steps:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \bullet (0.3625 + BxDTVx \bullet 0.0125)(V)$$

The DAC references may be commanded to independently slew between two voltages at one of four selectable slew rates. Table 12 summarizes the command registers used to control slewing DAC operation.

Table 12. Slewing DAC Command Register Control Summary

COMMAND REGISTER[BIT]	FUNCTION
VCCR[0], VCCR[2], VCCR[4], VCCR[6]	Voltage Change Control Register GO / Slew Write a 1 to Initiate a Slew to the Voltage Selected in VCCR[1], VCCR[3], VCCR[5], VCCR[7] Respectively. Bits are Reset to 0 at the End of the Slew Operation.
VCCR[1], VCCR[3], VCCR[5], VCCR[7]	Voltage Change Control Register Dynamic Target Select Write a 0 to Select Voltage V1 Stored in Registers B1DTV1[4-0], B2DTV1[4-0], B3DTV1[4-0], L2DTV1[4-0]. Write a 1 to Select Voltage V2 in Registers B1DTV2[4-0], B2DTV2[4-0], B3DTV2[4-0], L2DTV2[4-0].
B1DTV1[4-0], B2DTV1[4-0], B3DTV1[4-0], L2DTV1[4-0]	Dynamic Target Voltage 1 Five Bits Corresponding to V1 Output from Each DAC.
B1DTV1[5], B2DTV1[5], B3DTV1[5], L2DTV1[5]	PGOOD Mask Write a 1 to Continue Normal PGOOD Operation When Slewing. Write a 0 to Force PGOOD to Pull Low During Slew.
B1DTV2[4-0], B2DTV2[4-0], B3DTV2[4-0], L2DTV2[4-0]	Dynamic Target Voltage 2 Five Bits Corresponding to V2 Output from Each DAC.
VRRCR[1-0], VRRCR[3-2], VRRCR[5-4], VRRCR[7-6]	Voltage Ramp Rate Control Two Bits That Set the DAC Output Slew Rate for Step-Down Switching Regulator and LDO2.

Setting and Slewing the DAC Outputs

The 5-bit word in dynamic target voltage command registers B1DTV1, B2DTV1, B3DTV1, and L2DTV1 programs reference voltage V1. The 5-bit word in command registers B1DTV2, B2DTV2, B3DTV2, and L2DTV2 programs reference voltage V2. A resistor divider network on the output and feedback pins of the regulators set their output voltage.

A 0 or 1 to the odd bits of voltage change control register VCCR selects DAC output voltages V1 or V2, respectively. A slew of the DAC is initiated by writing a 1 to an even bit of register VCCR. The DAC output will slew to either voltage, V1 or V2, as selected by the odd bits of register VCCR. Slew begins when the I^2C STOP condition is detected. At the end of the slewing operation the GO bits in command register VCCR are cleared.

The slew rate for each regulator is set in the ramp rate control register VRRCR. Each DAC has independent output voltage registers, voltage register select, and slew rate and start controls. The regulators do not have to be enabled to change the DAC outputs.

The VSTB pin is used to set the DAC controlled output rails to a low power standby condition. When VSTB is driven HIGH, all four of the DAC references will immediately slew to V2. To use VSTB to set the rails to standby voltage, select V1 for normal rail voltages and V2 for standby rail voltages. Drive VSTB high to immediately slew all the DAC outputs to V2. When VSTB is driven LOW, the DAC outputs will slew to V1.

The default power-up value of all the dynamic target voltage registers is 11001 corresponding to a DAC output voltage of 0.675V. The DTV registers may be reprogrammed prior to initiating a power-up sequence or at any time for dynamic slewing.

When a step-down switching regulator output is slewing down its mode is automatically switched to forced continuous to enable the regulator to sink current. When LDO2 is slewing down, a 2.5k pull-down is connected to its output.

OPERATION

Table 13 shows command register and feedback divider settings to enable slewing step-down switching regulator 1 between 1.2V and 1V in 70µs. The voltage ramp rate control register bits VRRCR[1:0] are set to 01 which selects a ramp rate of 1.75mV/µs at the DAC output. The slew rate at the regulator output is a function of the feedback resistor divider gain. In this example, the slew is equal to 1.75 • (1 + 301/499) = 2.8mV/µs. Therefore, a slew of 200mV will take 70µs. To initiate a change from 1.2V to 1V write 11 to voltage change control register bits VCCR[1:0]. VCCR[1] selects target register B1DTV2 to set the regulator reference input to 0.625V. VCCR[0] set to 1 initiates the dynamic slew to go to the new voltage. To slew back to 1.2V write 01 to command register bits VCCR[1:0].

Table 13. Dynamic Slewing Example for Step-Down Switching Regulator 1

COMMAND REGISTER	V_{OUT} =1.2V	V_{OUT} =1V	
VRRCR[1:0]	01	01	Dynamic Slew Rate
VCCR[1]	0	1	Select DTV
B1DTV1[4:0]	11111	11111	Resistor Divider Shown in Figure 3 R1 = 301kΩ R2 = 499kΩ
B1DTV2[4:0]	10101	10101	

PUSHBUTTON OPERATION

State Event Diagram

Figure 5 shows the LTC3589 pushbutton state diagram. Upon first power application to V_{IN} an internal power-on reset circuit puts the pushbutton into power-down (PDN) state and initiates a one second timer. Status pin $\overline{RSTO}$ is pulled LOW until one second is timed out and the always-alive LDO1 has indicated power good status. After the one second interval the pushbutton circuit will transition to the power-off (POFF) state. The pushbutton will not leave the POFF state and enter the power-up state (PUP) until $\overline{ON}$ is held LOW for at least 400ms (PB400ms) or until PWR_ON is activated by the PWR_ON pin. When the controller enters the PUP state the open-drain WAKE pin releases HIGH. The WAKE pin is typically used to enable the first regulator in a start-up sequence. The pushbutton state will stay in PUP for five seconds before transitioning to the power-on (PON) state. Before leaving PUP, the PWR_ON pin must be brought HIGH by the application to indicate that the system rails are correct. If PWR_ON is not active at the end of five seconds the pushbutton controller will continue directly through PON to the power-down (PDN) state and pull the WAKE pin down. Three events will cause the pushbutton to leave the PON state: 1) lowering the PWR_ON pin, 2) forcing a hard reset by holding the $\overline{ON}$ pin LOW for five seconds, and 3) a fault condition is detected. Fault conditions are low V_{IN}, device over temperature, or extended undervoltage of one of the regulator outputs. All regulator enables, the $\overline{ON}$ input, and PWR_ON signals are inhibited for one second while in the PDN state. After one second in PDN the pushbutton controller returns to POFF.

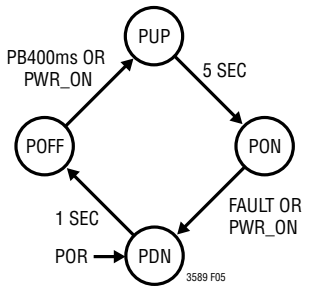


Figure 5. Pushbutton Controller State Diagram

PBSTAT Operation

PBSTAT goes LOW 50ms after the initial pushbutton application ($\overline{ON}$ LOW) and will stay LOW for a minimum of 50ms. PBSTAT will go HIGH coincident with $\overline{ON}$ going HIGH unless $\overline{ON}$ goes HIGH before the 50ms minimum on-time.

OPERATION

Power-Up Using the Pushbutton

When in the POFF state, the LTC3589 is in complete shutdown except the always active LDO1 and regulators enabled with the keep-alive control bits. Pull the $\overline{ON}$ pin to ground with a pushbutton for 400ms to begin a power-up sequence with the WAKE pin tied to an enable pin. Drive PWR_ON high within five seconds to signal the LTC3589 to remain in the power-on state.

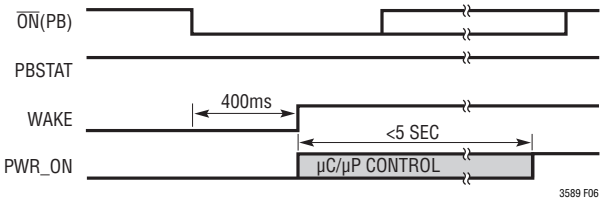


Figure 6. Power-Up Using the Pushbutton

Power-Down Using the Pushbutton

The pushbutton power-down operation is performed by the system microprocessor by monitoring the PBSTAT pin. Once in the PON state, the system controller is responsible for deciding what action to take with a pushbutton event. When the $\overline{ON}$ pin is held LOW for a 50ms debounce period, the PBSTAT pin is pulled LOW. The system controller should monitor the PBSTAT pin to determine the pushbutton has been pushed. If the controller decides that a power-down is desired, then it should drive the PWR_ON pin LOW.

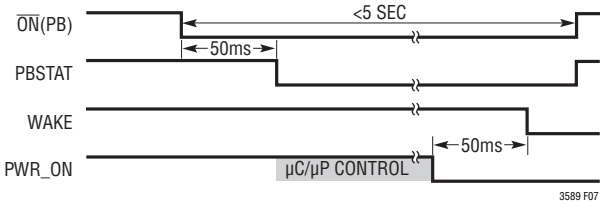


Figure 7. Power Down Using Pushbutton

Power-Up and Down Using PWR_ON Pin

An alternate power-up method is to drive the PWR_ON pin to a HIGH state. After a delay of 50ms from the PWR_ON signal, the WAKE pin will pull HIGH to drive regulator enable pins. When PWR_ON is HIGH for five seconds, the sequence controller will enter the PON state. To power down, drive the PWR_ON pin LOW. 50ms later WAKE will pull low, all enabled regulators are disabled and the OVEN command register is reset to 0x00.

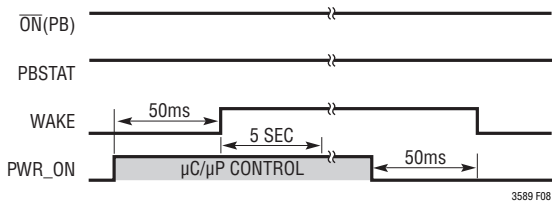


Figure 8. Power-Up and Down Using PWR_ON Pin

Hard Reset Using the Pushbutton

When the $\overline{ON}$ pin is pulled LOW for five seconds, a hard reset is initiated. At the end of five seconds, WAKE is pulled LOW, the I^2C command registers are reset to POR states, enable pin states are ignored, and the one second power-down timer is started. During the power-down time, the enables continue to be ignored to allow the regulator outputs to discharge. The $\overline{RSTO}$ pin is pulled LOW for the power-down time to indicate a pushbutton hard reset occurred. If the PWR_ON pin is LOW at the end of the one second power-down time, the LTC3589 will remain in sleep mode. If PWR_ON is HIGH at the end of one second and there are no fault conditions, the LTC3589 will power-up in the same way shown in Figure 8.

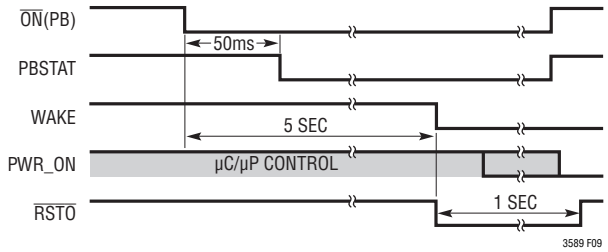


Figure 9. Hard Reset Using the Pushbutton

Hard Reset Due to a Fault Condition

A hard reset due to V_{IN} undervoltage, extended undervoltage of an output rail, or an overtemperature condition initiates a hard shutdown of the LTC3589. When the fault occurs, wake is pulled LOW, the I^2C command registers are reset to POR states, enable pin inputs are ignored, and the one second power-down timer is started. During the power-down time, the enables continue to be ignored to

OPERATION

allow the regulator outputs to discharge. If the PWR_ON pin is LOW at the end of the power-down time, the LTC3589 will remain in sleep mode with just the always-active LDO operating. If PWR_ON is HIGH at the end of one second and the fault condition has cleared, the LTC3589 will power-up in the same way shown in Figure 8. Neither $\overline{IRQ}$ nor the status registers are cleared by the fault induced shutdown.

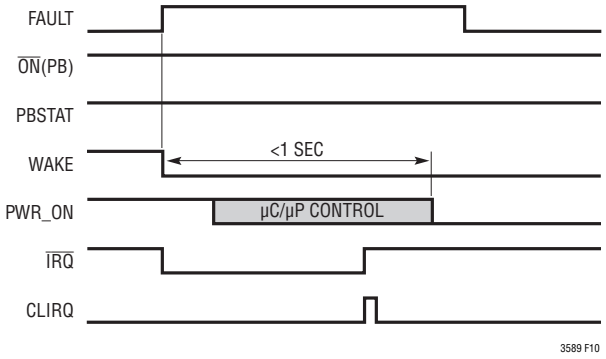


Figure 10. Hard Reset Due to a Fault Condition

ENABLE AND POWER-ON SEQUENCING

Enable Input Pin Operation

The regulator enable input pins facilitate pin-strapping an output rail to the enable pin of the next regulator in the desired sequence. The regulator enable inputs normally have a 0.8V (typical) input threshold. If any enable is driven HIGH, the remaining enable input thresholds switch to a more accurate 500mV (typical) threshold.

Figure 11 shows an application circuit for a typical pin-strapped start-up sequence. Holding $\overline{ON}$ LOW for 400ms

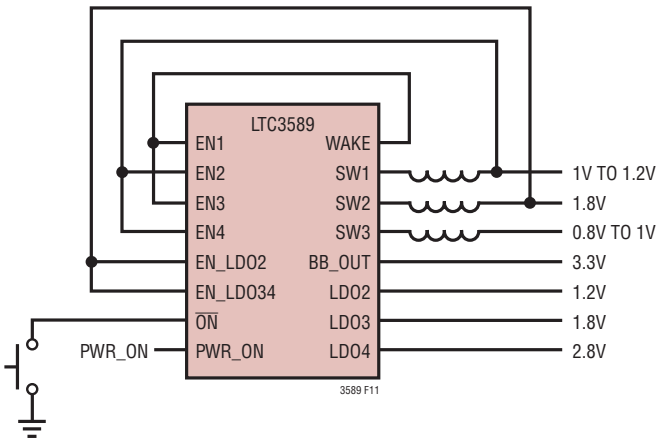


Figure 11. Pin-Strap Start-Up Sequence Application Circuit

brings up the WAKE pin that is tied to EN1 and EN3 to enable step-down switching regulators 1 and 3. The output of regulator 1 is tied to EN2 and EN4 that enables step-down switching regulator 2 and the buck-boost switching regulator 4. The output of step-down switching regulator 2 is tied to EN_LDO2 and EN_LDO3 to enable LDO2, LDO3 and LDO4. Within five seconds of WAKE going HIGH, the microprocessor or microcontroller must drive PWR_ON HIGH to tell LTC3589 that rails are good and to stay in the power-on state.

Figure 12 shows the start-up timing for the application shown in Figure 11. There is a 200µs (typical) delay between the enable pin and the internal enable signal to each regulator.

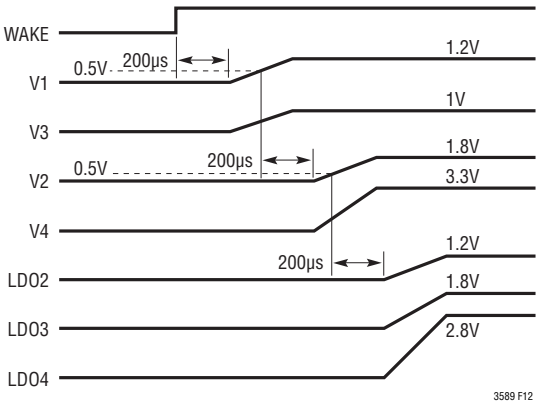


Figure 12. Pin-Strap Sequencing Timing

Depending on settings in I^2C system control register 2 (SCR2), a regulator's output must discharge to less than 300mV before it will respond to its enable. The output discharge feature is to guarantee proper start-up sequencing. This feature and the 2.5k pull-down resistors may be overridden by bit settings in command register SCR2.

Keep-Alive Operation

For systems which require an active supply rail when in system standby, any of the three LTC3589 step-down switching regulators or LDO2 may be kept alive regardless of the status of PWR_ON and WAKE. Writing a 1 to a regulator's keep-alive bit in its dynamic target voltage register will keep a regulator alive when the LTC3589 is in standby mode. A regulator with its keep-alive bit set will stay enabled until the bit is reset writing the bit LOW,

OPERATION

resetting the LTC3589 with a pushbutton hard reset, or a fault condition (UVLO, PGOOD, timeout or thermal shutdown) occurs. PGOOD and fault status are reported in the IRQSTAT and PGSTAT registers and on the IRQ and PGOOD pins for keep-alive regulators when PWR_ON and WAKE are LOW.

Software Control Mode

Once a power-up sequence is completed each regulator may be enabled and disabled individually by the system as needed for power mode requirements. Setting the output voltage enable command register bit OVEN[7] HIGH disconnects each regulator from its enable pin so control is solely through the OVEN command register. To enter software control mode, set command bit OVEN[7] HIGH and the desired enable bits in OVEN[6:0] HIGH. Any of the regulators enabled in OVEN[6:0] will stay on regardless of the state of their enable pins when OVEN[7] is HIGH. Setting the regulator enable bits and the software control bit in OVEN[7] may occur on the same I^2C start-stop sequence. A normal shutdown using PWR_ON resets all eight bits of the OVEN register to 0x00 to ensure all regulators are shut off.

FAULT DETECTION, SHUTDOWN, AND REPORTING

The LTC3589 monitors V_{IN}, output rail voltages and internal die temperature. A warning condition is indicated when V_{IN} is less than 2.9V and when internal die temperature approaches the thermal shutdown temperature. A fault condition occurs when V_{IN} is less than 2.6V, any regulator output is 8% low for 14ms, or the internal die temperature is HIGH. Warning and fault states are reported via the $\overline{IRQ}$, PGOOD, and $\overline{RTSO}$ pins. Specific fault states are read via the I^2C serial port status registers IRQSTAT and PGSTAT.

$\overline{RSTO}$ Pin Function

The $\overline{RSTO}$ (reset output) pin is an open-drain output for use as a power-on reset signal. It is pulled LOW at initial power until LDO1 is within 8% of its target and the initial one second start-up timer is finished. $\overline{RSTO}$ remains HIGH during normal operation and will be pulled low if LDO1 loses regulation for more than 25µs or a pushbutton hard reset is initiated. $\overline{RSTO}$ is released high 14ms after LDO1 returns to regulation.

Figure 13 shows a initial power-up for the $\overline{RSTO}$ pin. If V_{IN} is not above its undervoltage thresholds at the end of the 1 second start-up time, the IRQ pin will be pulled LOW and an undervoltage bit will be set in the IRQSTAT status register.

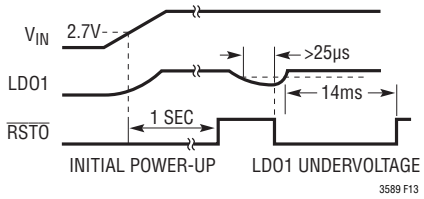


Figure 13. Initial Power-Up and LDO1 Undervoltage $\overline{RSTO}$ Timing

PGOOD Pin and PGSTAT Status Register Function

Each LTC3589 regulator has an internal power good output that is active whenever the regulators feedback pin is closer than 7% (typical) from its input reference voltage. If any of the internal power good signals indicate a low voltage for longer than 25µs (typical), the PGOOD pin is pulled LOW and the appropriate bit in the PGSTAT status register (Table 14) is set.

Table 14. PGSTAT Read-Only Register Bit Definitions

PGSTAT[BIT]	VALUE	SETTING
0	0 1	LDO1_STBY Output Low LDO1_STBY Output Good
1	0 1	Step-Down Switching Regulator 1 Output Low Step-Down Switching Regulator 1 Output Good
2	0 1	Step-Down Switching Regulator 2 Output Low Step-Down Switching Regulator 2 Output Good
3	0 1	Step-Down Switching Regulator 3 Output Low Step-Down Switching Regulator 3 Output Good
4	0 1	Buck-Boost Regulator 4 Output Low Buck-Boost Regulator 4 Output Good
5	0 1	LDO2 Output Low LDO2 Output Good
6	0 1	LDO3 Output Low LDO3 Output Good
7	0 1	LDO4 Output Low LDO4 Output Good

OPERATION

Figure 14 shows the PGOOD pin and PGSTAT status register timing. When no regulator is enabled, the PGOOD pin is pulled LOW and PGSTAT bits are LOW. PGOOD and the PGSTAT bits are HIGH 250µs after the last enabled regulator is within 7% of its target.

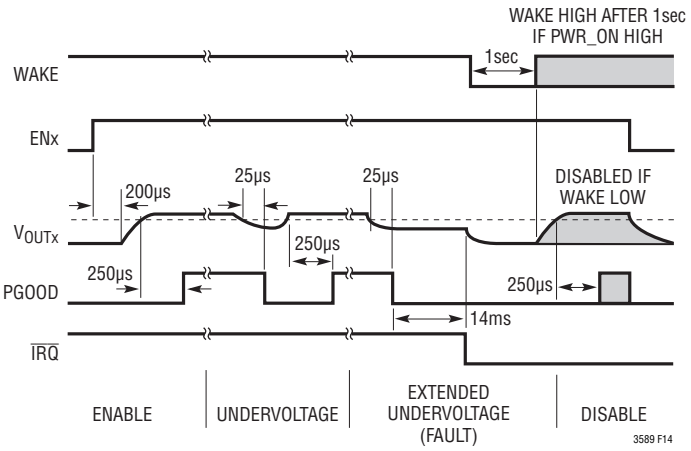


Figure 14. PGOOD Pin and PGSTAT Status Register Timing

If any enabled regulator output falls more than 7% low for longer than 25µs PGOOD is pulled LOW and a corresponding status bit in the PGSTAT register is set to 0. The PGOOD pin and PGSTAT status bit remain LOW for as long as the low voltage condition persists plus 250µs.

An extended low output rail causing the PGOOD pin to be LOW for longer than 14ms defines a PGOOD timeout fault condition that triggers a hard reset if not masked in I^2C register bit SCR2[7]. When SCR2[7] is HIGH, PGOOD remains in normal operation.

During a dynamic voltage slew, PGOOD is pulled LOW unless bit 5 in the dynamic target voltage register for each regulator is set HIGH. The status register PGSTAT is unaffected by a dynamic voltage slew.

Undervoltage Detection

The LTC3589 undervoltage (UV) detection circuit will output a fault condition, locking out regulator operation, until V_{IN} reaches 2.7V. Once V_{IN} is above 2.7V the LTC3589 will operate normally until V_{IN} drops to 2.55V (typical). When V_{IN} drops below 2.55V, the fault condition initiates a hard shutdown reset. Figure 15 shows undervoltage warning and fault detection levels.

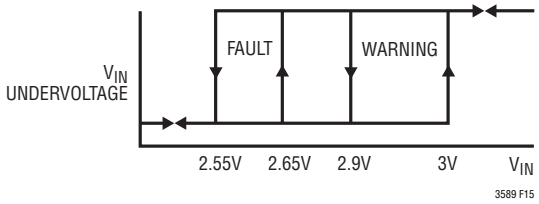


Figure 15. UV Detection Hard Reset and Warning Levels

An undervoltage warning sets register bit IRQSTAT[4] and pulls the $\overline{IRQ}$ pin LOW.

To minimize standby quiescent current the UVLO and thermal sensor circuits are disabled when all the regulators are off.

Thermal Shutdown Fault and Warning

Similar to the V_{IN} undervoltage detection circuits the overtemperature detection circuits check for warning and fault levels. An overtemperature fault will initiate a fault induced shutdown. An overtemperature warning sets register bit IRQSTAT[6] and pulls the $\overline{IRQ}$ pin LOW.

IRQ Pin and IRQSTAT Status Register Function

The $\overline{IRQ}$ pin and IRQSTAT status register report PGOOD timeout fault, V_{IN} undervoltage warning and fault, and high temperature warning and fault. Table 15 shows the meaning of the IRQSTAT read-only status register bits.

Table 15. IRQSTAT Read-Only Register Bit Definitions

IRQSTAT[BIT]	VALUE	SETTING
3	1	PGOOD Timeout Fault (PGOOD Low > 14ms)
4	1	V_{IN} Undervoltage Warning (V_{IN} < 2.9V)
5	1	V_{IN} Undervoltage Fault (V_{IN} < 2.6V)
6	1	Thermal Limit Warning (T_J > 130°C)
7	1	Thermal Limit Fault (T_J > 150°C)

OPERATION

Figure 16 shows the timing of the $\overline{IRQ}$ and IRQSTAT status register following a warning (V_{IN} <2.9V or high temperature warning) event. When a warning occurs, $\overline{IRQ}$ is latched LOW and bit IRQSTAT[4] or IRQSTAT[5] is set. $\overline{IRQ}$ remains low and the IRQSTAT status bits remain active until the I²C CLIRQ command is given and the warning condition has passed.

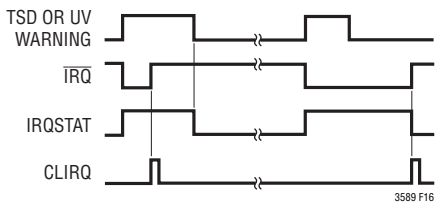


Figure 16. $\overline{IRQ}$ and IRQSTAT Status Register Warning Timing

Figure 17 shows the timing of the $\overline{IRQ}$ pin and IRQSTAT status register following a fault induced hard shutdown event. When a fault occurs, IRQ is latched LOW and bit IRQSTAT[3], IRQSTAT[5], or IRQSTAT[7] is set. $\overline{IRQ}$ remains LOW until the CLIRQ command is issued. When the CLIRQ command has been issued, the IRQSTAT status bit remains set for the one second enable inhibit time or as long as the fault condition persists, whichever is longer.

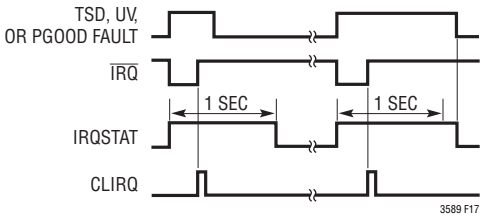


Figure 17. $\overline{IRQ}$ and IRQSTAT Status Register Fault Timing

Fault Induced Shutdown

Any of the three fault conditions will initiate a hard reset shutdown triggering the following events: 1) A bit corresponding to the fault is set in status register IRQSTAT, 2) $\overline{IRQ}$ and WAKE pins are pulled LOW, 3) enable pin inputs are ignored and the regulators are disabled, 4) all enable bits and software control mode bit in the output voltage enable OVEN command register are cleared, and 5) the pushbutton controller is sent to the PDN state for one second and then to POFF. Re-enabling of regulators is inhibited until both the fault condition and the one second time out have passed to allow regulator outputs sufficient time to discharge. When one second timeout and the fault condition are both passed, if PWR_ON is HIGH, WAKE will come up and the LTC3589 will respond to any enable pins that are also HIGH.

I²C OPERATION

I²C Interface

The LTC3589 communicates with a bus master using the standard I²C 2-wire interface. The two bus lines, SDA and SCL, must be HIGH when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines. The LTC3589 is both a slave receiver and slave transmitter. The I²C control signals, SDA and SCL are scaled internally to the DV_{DD} supply. DV_{DD} should be connected to the same power supply as the bus pull-up resistors.

The I²C port has an undervoltage lockout on the DV_{DD} pin. When DV_{DD} is below approximately 1V, the I²C serial port is reset to power-on states and registers are set to default values.

OPERATION

I²C Bus Speed

The I²C port operates at speeds up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

I²C START and STOP Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LTC3589, the master may transmit a STOP condition that commands the LTC3589 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus it then free for communication with another I²C device.

I²C Byte Format

Each byte sent to or received from the LTC3589 must be 8 bits long followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LTC3589 most significant bit (MSB) first.

I²C Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. When the LTC3589 is written to, it acknowledges its write address and subsequent register address and data bytes. When reading from the LTC3589, it acknowledges its read address and 8-bit status byte.

An acknowledge pulse (active LOW) generated by the LTC3589 lets the master know that the latest byte of information was transferred. The master generates the clock cycle and releases the SDA line (HIGH) during the acknowledge clock cycle. The LTC3589 pulls down the SDA line during the write acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

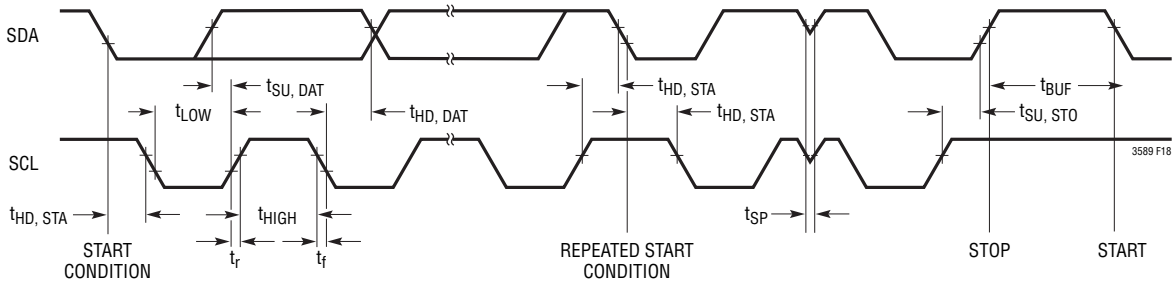


Figure 18. LTC3589 I²C Timing

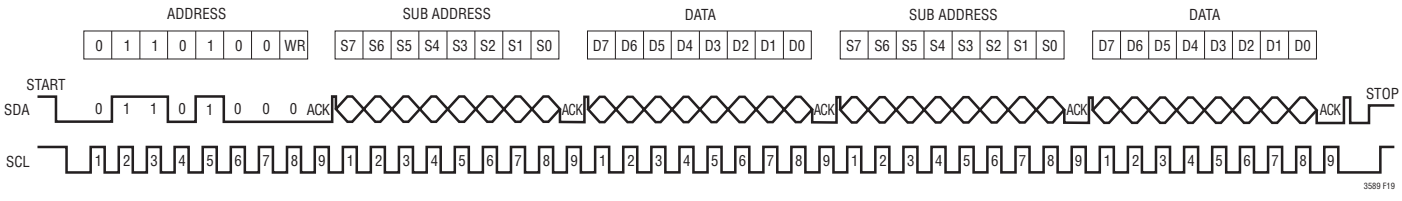


Figure 19. LTC3589 I²C Serial Port Multiple Write Pattern

OPERATION

I²C Slave Address

The LTC3589 responds to factory programmed read and write addresses. The write address is 0x68. The read address is 0x69. The least significant bit of the address byte, known as the read/write bit, is 0 when writing data to the LTC3589 and 1 when reading from it.

I²C Sub-Addressed Writing

The LTC3589 has 14 command registers for control inputs. They are accessed by the I²C port via a sub-addressed writing system.

Each write cycle of the LTC3589 consists of a series of three or more bytes beginning with the LTC3589 write address. The second byte is the sub address of the command register being written to. The sub address is a pointer to the register where the data in the third byte will be stored. The third byte is the data to be written to the just-received sub address. Continue alternating sub address and data bytes to write multiple registers in a single START sequence.

I²C Bus Write Operation

The master initiates communication with the LTC3589 with a START condition and the LTC3589's write address. If the address matches that of the LTC3589, the LTC3589 returns an acknowledge pulse. The master should then deliver the sub address. Again the LTC3589 acknowledges and the cycle is repeated for the data byte. The data byte is transferred to an internal holding latch upon the return of its acknowledge by the LTC3589. Continue writing sub address and data pairs into the holding latches. Addressing the LTC3589 is not required for each sub address and data pair. If desired a REPEAT-START condition may be initiated by the master where another device on the I²C bus is addressed. The LTC3589 remembers the valid data it has received. Once all the devices on the I²C have been addressed and sent valid data and a global STOP has been sent, the LTC3589 will update its command latches with the data it has received.

I²C Sub-Addressed Reading

The LTC3589 I²C interface supports random address reading of the I²C command and status registers. Before reading a register, the registers sub address must be written. Send a START condition followed by the LTC3589 write address followed by the sub address of the register to be read. The sub address is now stored as a pointer to the register. Send a REPEAT-START condition followed by the LTC3589 read address. Following the acknowledgment of its read address the LTC3589 returns one bit of information for each of the next 8 clock cycles. A STOP condition is not required for the read operation. The read sub address is stored until a new sub address is written.

Verify the data written to the internal data hold latches prior to committing date to the command registers by reading back the data before sending a STOP condition.

Continuously poll a register by repeatedly sending a START condition followed by the LTC3589 read address, and then clocking the data out after the read address acknowledge.

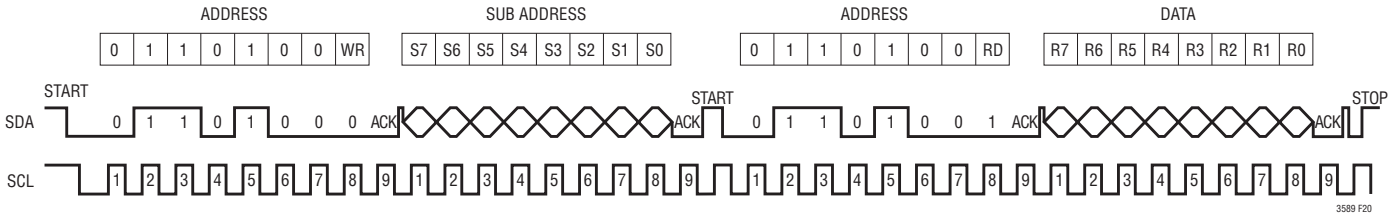


Figure 20. LTC3589 I²C Serial Port Read Pattern

OPERATION

I²C Command and Status Registers

Table 16 and Table 17 show the LTC3589 I²C command and status registers. System control register (SCR1) sets the operating modes of the switching regulators. Each step-down switching regulator has pulse-skipping, Burst Mode operation, or forced continuous operation. The buck-boost switching regulator can be put in continuous or Burst Mode operation.

The output voltage enable (OVEN) command register controls the individual enables of each regulator. When OVEN[7] is set to a logic LOW value, bits OVEN[6-0] are ORed with their respective enable pins. When OVEN[7] is HIGH, the input pins EN1, EN2, EN3, EN4, EN_LDO2, and EN_LDO34, are ignored and the LTC3589 regulators respond only to the OVEN register. When the regulators are configured in a hard wired power-up sequence, setting OVEN[7] allows software control of individual regulators. When the PWR_ON pin is pulled LOW all bits in the OVEN register are reset to POR state of 0x00.

System control register 2 (SCR2) controls the operation of the regulator start-up and regulator power good (PGOOD) hard shutdown operation. Set command register SCR2[7] to inhibit a hard shutdown of the regulators in the event of an extended low output rail voltage. The low output voltage event is still reported via the IRQ pin and IRQSTAT status register. Set the bits in SCR2[6-0] LOW to force a regulator to ignore its enable until its output has fallen to less than 300mV (typical). If set HIGH, the regulator will enable without waiting for its output to discharge and will not engage the 2.5k discharge resistor.

LDO2 and step-down switching regulators 1 to 3 each have a pair of control bits in the voltage change control register VCCR. The reference select bit selects which of two 5-bit words are used as inputs to the regulators feedback reference DAC inputs. The slew go bit initiates a DAC slew to the voltage selected by the reference select bit. When the slew is complete, the slew go bits are reset LOW.

Accessing the CLIRQ command register will clear the $\overline{IRQ}$ pin and will let the $\overline{IRQ}$ pin to release HIGH. The pin is cleared when the LTC3589 acknowledges the sub address. Data written to the CLIRQ command register is ignored.

There are eight command registers that are used to store the 5-bit dynamic target voltage input to the feedback reference slewing DACs – B1DTV1, B1DTV2, B2DTV1, B2DTV2, B3DTV1, B3DTV2, L2DTV1 and L2DTV2. The registers ending with V2 use bits 4 through 0 to store the V2 feedback reference voltage for the regulators. The regulators input reference voltage is set to V2 by setting the reference select bits HIGH in VCCR and writing to the go bits in VCCR. The V2 voltage is also selected whenever the VSTB pin is driven HIGH. The registers ending with V1 use bits 4 through 0 to store the V1 feedback voltage reference for the regulators. The regulators input reference voltage is set to V1 voltage by setting the reference select bits LOW in command register VCCR. Whenever a new dynamic target voltage is set, either by changing the 5-bit value or by changing the reference select bits in VCCR, the go bits in VCCR must be written to initiate the dynamic voltage slew. When bit 5 in B1DTV1, B2DTV1, B3DTV1, and L2DTV1 is LOW the PGOOD pin pulls LOW during a dynamic voltage slew. Bits 7 and 6 in B1DTV1 set the switch DV/DT rate for all the step-down switching regulators. Bit 5 in registers B1DTV2, B2DTV2 and B3DTV2 selects the switching frequency of step-down switching regulators 1, 2 and 3. Writing the bit LOW sets the switching frequency to 2.25MHz. Writing the bit HIGH sets the switching frequency to 1.125MHz.

The dynamic slew rates of the four feedback reference DACs are independently set using bits in voltage ramp rate command register (VRRCR). The rate shown is the slew of the DAC output as it slews up or down to its target value. The slew rate of the output voltage is scaled by the gain of the resistor divider network that sets the regulator output voltage. For example, a regulator set to an output voltage of 1.2V when the dynamic target voltage reference is 0.75V has a gain of 1.6. Slewing the regulator output from 1.2V to 1V requires slewing the DAC output down 125mV from 750mV to 625mV. With a VRRCR slew rate setting of 01 the slew time of the regulator output is 71µs.

OPERATION

Table 16. LTC3589 Command Register Table

REG	NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
0x07	SCR1		Buck-Boost Mode: 0 = Continuous 1 = Burst Mode	Step-Down Switching Regulator 3 Mode : 0 0 = Pulse-Skipping 0 1 = Burst 1 0 = Forced Continuous		Step-Down Switching Regulator 2 Mode : 0 0 = Pulse-Skipping 0 1 = Burst 1 0 = Forced Continuous		Step-Down Switching Regulator 1 Mode : 0 0 = Pulse-Skipping 0 1 = Burst 1 0 = Forced Continuous		0000 0000
0x10	OVEN	Software Control Mode: 0 = Enable with Pin or OVEN Register 1 = Enable/ Disable with OVEN Register Only	EN_LDO4	EN_LDO3	EN_LDO2	EN4	EN3	EN2	EN1	0000 0000
0x12	SCR2	Mask PGOOD Hard Shutdown: 0 = Allow PGOOD Timeout Hard Shutdown. 1 = Inhibit PGOOD Hard Shutdown.	LDO4 Start-Up: 0 = Wait for Output < 300mV Before Enable 1 = Don't Wait and Disable Discharge Resistor.	LDO3 Start-Up: 0 = Wait for Output < 300mV Before Enable 1 = Don't Wait and Disable Discharge Resistor.	LDO2 Start-Up: 0 = Wait for Output < 300mV Before Enable 1 = Don't Wait and Disable Discharge Resistor.	Buck-Boost Start-Up: 0 = Wait for Output < 300mV Before Enable 1 = Don't Wait and Disable Discharge Resistor.	Step-Down Switching Regulator 3 Start-Up: 0 = Wait for Output < 300mV Before Enable 1 = Don't Wait and Disable Discharge Resistor.	Step-Down Switching Regulator 2 Start-Up: 0 = Wait for Output < 300mV Before Enable 1 = Don't Wait and Disable Discharge Resistor.	Step-Down Switching Regulator 1 Start-Up: 0 = Wait for output < 300mV Before Enable 1 = Don't Wait and Disable Discharge Resistor.	0000 0000
0x20	VCCR	LDO2 Reference Select: 0 = L2DTV1[4-0] 1 = L2DTV2[4-0]	Start LDO2 Slew: 0 = Went 1 = GO	Step-Down Switching Regulator 3 Reference Select: 0 = B3DTV1[4-0] 1 = B3DTV2[4-0]2	Start Step-Down Switching Regulator 3 Slew: 0 = Went 1= GO	Step-Down Switching Regulator 2 Reference Select: 0 = B2DTV1[4-0] 1 = B2DTV2[4-0]	Start Step-Down Switching Regulator 2 Slew: 0 = Went 1= GO	Step-Down Switching Regulator 1 Reference Select: 0 = B1DTV1[4-0] 1 = B1DTV2[4-0]2	Start Step-Down Switching Regulator 1 Slew: 0 = Went 1= GO	0000 0000
0x21	CLIRQ									
0x23	B1DTV1	Step-Down Switching Regulator Switch DV/DT Control: 00 = 1ns 01 = 2ns 10 = 4ns 11 = 8ns		PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing.	Step-Down Switching Regulator 1 Feedback Reference Input (V1) 00000 = 362.5mV 11001 = 675mV 11111 = 750mV 12.5mV Step Size					0001 1001

OPERATION

Table 16. LTC3589 Command Register Table

REG	NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
0x24	B1DTV2	Keep-Alive Mode: 0 = Normal Shutdown 1 = Keep-Alive	Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2	Step-Down Switching Regulator 1 Clock Rate 0 = 2.25MHz 1 = 1.12MHz	Step-Down Switching Regulator 1 Feedback Reference Input (V2) 00000 = 362.5mV 11001 = 675mV 11111 = 750mV 12.5mV Step Size					0001 1001
0x25	VRRCR	LDO2 Dynamic Reference Slew Rate: 00 = 0.88mV/µs 01 = 1.75mV/µs 10 = 3.5mV/µs 11 = 7mV/µs		Step-Down Switching Regulator 3 Dynamic Reference Slew Rate: 00 = 0.88mV/µs 01 = 1.75mV/µs 10 = 3.5mV/µs 11 = 7mV/µs		Step-Down Switching Regulator 2 Dynamic Reference Slew Rate: 00 = 0.88mV/µs 01 = 1.75mV/µs 10 = 3.5mV/µs 11 = 7mV/µs		Step-Down Switching Regulator 1 Dynamic Reference Slew Rate: 00 = 0.88mV/µs 01 = 1.75mV/µs 10 = 3.5mV/µs 11 = 7mV/µs		1111 1111
0x26	B2DTV1	Unused		PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing.	Step-Down Switching Regulator 2 Feedback Reference Input (V1) 00000 = 362.5mV 11001 = 675mV 11111 = 750mV 12.5mV Step Size					0001 1001
0x27	B2DTV2	Keep-Alive Mode: 0 = Normal Shutdown 1 = Keep-Alive	Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2	Step-Down Switching Regulator 2 Clock Rate 0 = 2.25MHz 1 = 1.125MHz	Step-Down Switching Regulator 2 Feedback Reference Input (V2) 00000 = 362.5mV 11001 = 675mV 11111 = 750mV 12.5mV Step Size					0001 1001
0x29	B3DTV1	Unused		PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing.	Step-Down Switching Regulator 3 Feedback Reference Input (V1) 00000 = 362.5mV 11001 = 675mV 11111 = 750mV 12.5mV Step Size					0001 1001
0x2A	B3DTV2	Keep-Alive Mode: 0 = Normal Shutdown 1 = Keep-Alive	Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2	Step-Down Switching Regulator 3 Clock Rate 0 = 2.25MHz 1 = 1.125MHz	Step-Down Switching Regulator 3 Feedback Reference Input (V2) 00000 = 362.5mV 11001 = 675mV 11111 = 750mV 12.5mV Step Size					0001 1001

OPERATION

Table 16. LTC3589 Command Register Table

REG	NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
0x32	L2DTV1	Keep-Alive Mode: 0 = Normal Shutdown 1 = Keep-Alive	Unused	PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Changed When Slewing.	LDO 2 Feedback Reference Input (V1) 00000 = 362.5mV 11001 = 675mV 11111 = 750mV 12.5mV Step Size					0001 1001
0x33	L2DTV2	LDO4 Control MODE: 0 = LDO4 Enable with EN_LDO34 1 = LDO4 Enable with OVEN[6]	LDO4 Output Voltage: 00 = 2.8V 01 = 2.5V 10 = 1.8V 11 = 3.3V		LDO 2 Feedback Reference Input (V2) 00000 = 362.5mV 11001 = 675mV 11111 = 750mV 12.5mV Step Size					0001 1001

Table 17. LTC3589 Read-Only Status Register Table

REG	NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0x02	IRQSTAT	Thermal Limit Hard Shutdown Occurred	Near Thermal Limit	Undervoltage Hard Shutdown Occurred	Near Undervoltage Limit	PGOOD Timeout Hard Shutdown Occurred	Unused	Unused	Unused
0x13	PGSTAT	LDO4 Status: 0 = V_{OUT} Low 1 = V_{OUT} Good	LDO3 Status: 0 = V_{OUT} Low 1 = V_{OUT} Good	LDO2 Status: 0 = V_{OUT} Low 1 = V_{OUT} Good	Buck_Boost Status: 0 = V_{OUT} Low 1 = V_{OUT} Good	Step-Down Switching Regulator 3 Status: 0 = V_{OUT} Low 1 = V_{OUT} Good	Step-Down Switching Regulator 2 Status: 0 = V_{OUT} Low 1 = V_{OUT} Good	Step-Down Switching Regulator 1 Status: 0 = V_{OUT} Low 1 = V_{OUT} Good	LDO1 Status: 0 = V_{OUT} Low 1 = V_{OUT} Good

THERMAL CONSIDERATIONS AND BOARD LAYOUT

Printed Circuit Board Power Dissipation

In order to ensure optimal performance and the ability to deliver maximum output power to any regulator, it is critical that the exposed ground pad on the backside of the LTC3589 package be soldered to a ground plane on the board. The exposed pad is the only GND connection for the LTC3589. Correctly soldered to a 2500mm^2 ground plane on a double sided 1oz copper board the LTC3589 has a thermal resistance (θ_{JA}) of approximately 34°C/W. Failure to make good thermal contact between the exposed pad on the backside of the package and an adequately sized ground plane will result in thermal resistances far greater than 34°C/W.

To ensure the junction temperature of the LTC3589 die does not exceed the maximum rated limit and to prevent overtemperature faults, the power output of the LTC3589 must be managed by the application. The total power dissipation in the LTC3589 is approximated by summing the power dissipation in each of the switching regulators and the LDO regulators.

The power dissipation in a switching regulator is estimated by:

$$P_{D(SWX)} = (V_{OUTX} \bullet I_{OUTX}) \bullet \frac{100 - Eff}{100}$$

Where V_{OUTX} is the programmed output voltage, I_{OUTX} is the load current and Eff is the % efficiency that can

OPERATION

be measured or looked up in an efficiency table for the programmed output voltage.

The power dissipated by an LDO regulator is estimated by:

$$P_{D(LDOX)} = (V_{IN(LDOX)} - V_{LDOX}) \bullet I_{LDOX}$$

Where V_{LDOX} is the programmed output voltage, $V_{IN(LDOX)}$ is the LDO supply voltage, and I_{LDOX} is the output load current. If one of the switching regulator outputs is used as an LDO supply voltage, remember to include the LDO supply current in the switching regulator load current for calculating power loss.

An example using the equations above with the parameters in Table 18 shows an application that is at the maximum junction temperature of 125°C at an ambient temperature of 85°C. LDO2, LDO3, and LDO4 are powered by step-down switching regulator 2 and the buck-boost switching regulator. The total load on those two switching regulators is the sum of the application load and the LDO load. This example is with the LDO regulators at one half rated current and the switching regulators at three quarters rated current.

Table 18. T_J Calculation Example

OUTPUT	V_{IN}	V_{OUT}	APP LOAD	TOTAL LOAD	EFF	POWER DISS
LDO1_VSTB	3.8V	1.2V	10mA	10mA		30mW
LDO2	1.8V	1.2V	100mA	100mA		60mW
LDO3	3.3V	1.8V	100mA	100mA		150mW
LDO4	3.3V	2.5V	100mA	100mA		80mW
V_{OUT1}	3.8V	1.2V	1.2A	1.2A	80%	290mW
V_{OUT2}	3.8V	1.8V	0.65A	0.75A	90%	140mW
V_{OUT3}	3.8V	1.25V	0.75A	0.75A	85%	140mW
V_{OUT4}	3.8V	3.3V	0.70A	0.90A	90%	300mW
					TOTAL POWER	1180mW
INTERNAL JUNCTION TEMPERATURE AT 85°C AMBIENT						125°C

Printed Circuit Board Layout

When laying out the printed circuit board, the following checklist should be followed to ensure proper operation of the LTC3589:

1. Connect the exposed pad of the package (Pin 41) directly to a large ground plane to minimize thermal and electrical impedance.
2. The switching regulator input supply traces and their decoupling capacitors should be as short as possible. Connect the GND side of the capacitors directly to the ground plane of the board. The decoupling capacitors provide the AC current to the internal power MOSFETs and their drivers. It is important to minimize inductance from the capacitors to the LTC3589 pins.
3. Minimize the switching power traces connecting SW1, SW2, SW3, and buck-boost switch pins SW4AB and SW4CD to the inductors to reduce radiated EMI and parasitic coupling. Keep sensitive nodes such as the feedback pins away from or shielded from the large voltage swings on the switching nodes.
4. Minimize the length of the connection between the step-down switching regulator inductors and the output capacitors. Connect the GND side of the output capacitors directly to the thermal ground plane of the board.
5. Minimize the length of the connection between the buck-boost regulator output (BB_OUT) and the output capacitor. Connect the GND side of the output capacitor directly to the thermal ground plane of the board.

APPLICATIONS INFORMATION

The LTC3589 is optimized to support several families of advanced portable applications processors including the Marvell PXA3xx and PXA168 Xscale processors, the Freescale i.MX family including the new i.MX51, the TI OMAP processors utilizing their Smart reflex, and many additional ARM processors.

PXA3XX Monahans Processor Support

The PXA3XX processors are hard-coded to communicate with a PMIC at specific command register addresses in order to power up the processor supply rails from the low power state. The LTC3589 I^2C device address and command register addresses map to PXA3xx command register sub-address requirements. The LTC3589 write address is 0x68. The key command register addresses for PXA3xx support are the Output Voltage Enable (OVEN) register at address 0x10. VCC_APPS/A_EN is mapped to OVEN bit 0 (enable step-down switching regulator 1). VCC_SRAM/S_EN is mapped to OVEN bit 2 (enable step-down switching regulator 3). The voltage change control register (VCCR) at command register address 0x20 controls the dynamic voltage select and go bits required to command a voltage change and slew when coming out of low voltage standby or sleep modes into run mode. The dynamic target voltage (xxDTV[1,2]) registers map to the mandatory command register addresses. The full register map for the LTC3589 shown in Table 15 and Table 16 supports Monahans, hard-coded I^2C commands for start-of-day operation, voltage-change sequence, supply enable, and return-to-D0 state sequence.

The LTC3589 does not specifically reference the Monahans SYS_EN and PWR_EN enable pins but supports these signals with individual enable input pins EN[1-4] and EN_LDO[2,34] that should be hard-wired to SYS_EN or PWR_EN as required for proper system-level power sequencing.

The LTC3589 $\overline{RSTO}$ signal is used to drive the Monahans hard reset signal nRESET and is based on the state of the always-active regulator output LDO1_STBY and by a pushbutton hard reset request. The release of the $\overline{RSTO}$ output is delayed a minimum of 10ms as required or as long as 1s when the LTC3589 is reset using its pushbutton controller.

PXA16X Armada Processor Support

LTC3589 includes spare register bits that can be accessed by the processor for setting and recalling hibernate and resume operation.

The keep-alive function allow a step-down switching regulator to maintain system memory during a hibernate shutdown state of the Armada processor.

i.MX Processor Support

The LTC3589 has hardware features specifically designed for the latest i.MX family of processors from Freescale Semiconductor. The i.MX51 controls the VSTB input pin of the LTC3589 to command transitions between the run mode core voltage and the lower level standby voltage. The run and standby voltage levels are initially programmed in I^2C command registers xxBTV1 and xxBTV2. When the VSTB pin is asserted high all four dynamically controlled output supply rails will slew to the xxBTV2 set point. When xxBTV1 and xxBTV2 are set at the same value, as they are by default, then no slewing occurs. This allows the single VSTB pin to control any combination of the four DAC controlled regulators to slew between two programmed output voltages. When VSTB is de-asserted back to a zero value the regulators slew back up to the xxBTV1 set point.

Earlier i.MX family processors such as the i.MX31 included two VSTB pins used for controlling the regulator outputs for a low voltage standby mode, nominal voltage run mode, and a higher voltage overdrive mode. The LTC3589 can be used with these processors using the VSTB input pin

APPLICATIONS INFORMATION

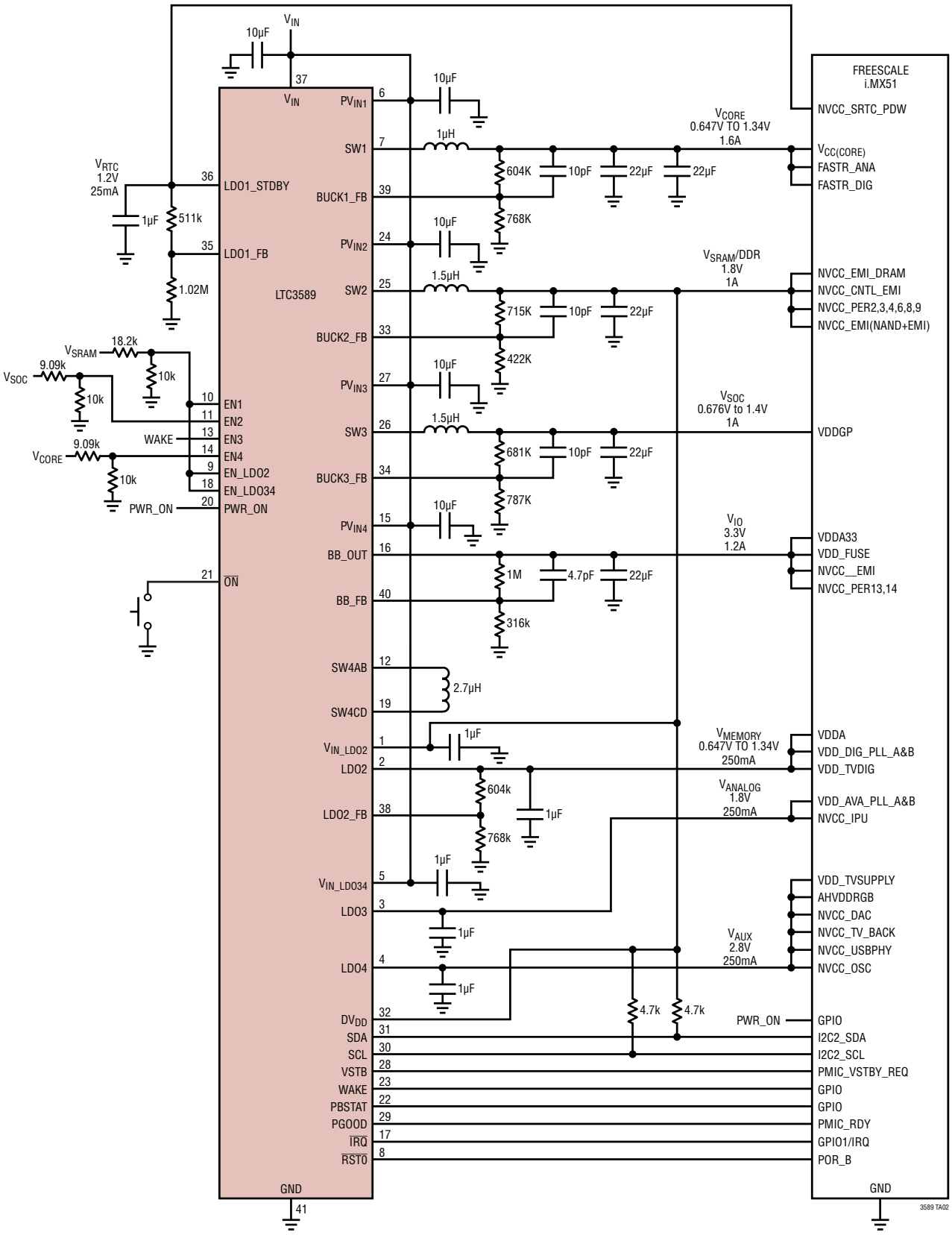
to select between run and standby voltages and using minimal software overhead to set the overdrive voltage in I²C command registers.

The default DAC reference value in all xxBTVx registers is 0x19. This accommodates i.MX processors and others requiring an overdrive voltage. The value can be increased up to 0x1F for overdrive or supply margining above the nominal run voltage. Once programmed into the I²C command registers xxBTVx two voltage outputs are selected by the VSTB pin. All voltage levels and changes are fully controllable using the I²C serial port.

OMAP3 and DaVinci Processor Support

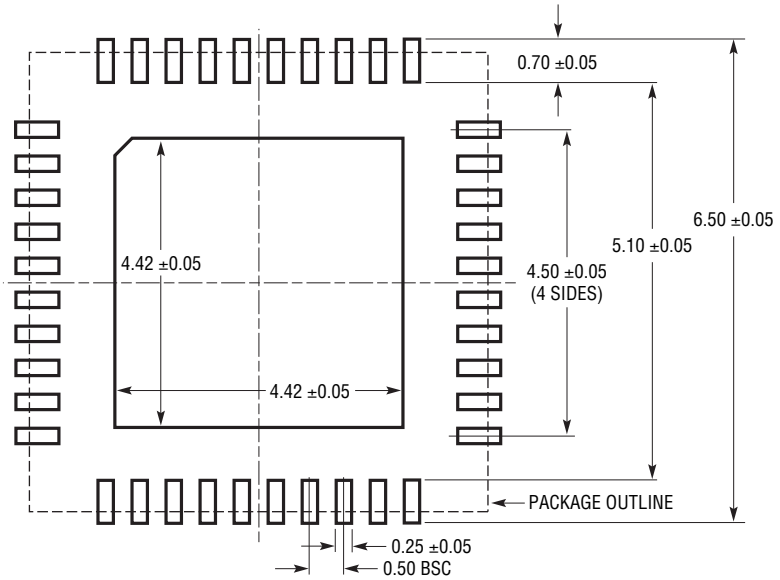
The OMAP3 family of ARM processors has similar requirements to the processors described above. The LTC3589 I²C control can fully accommodate the smart reflex dynamic voltage control with proper embedded software drivers tailored to the LTC3589 register mapping. The LTC3589 demo board demonstrates configuring and dynamically slewing and sequencing the outputs using I²C control. The same provisions can be incorporated into embedded software drivers for the OMAP3 or any other target processor.

TYPICAL APPLICATION

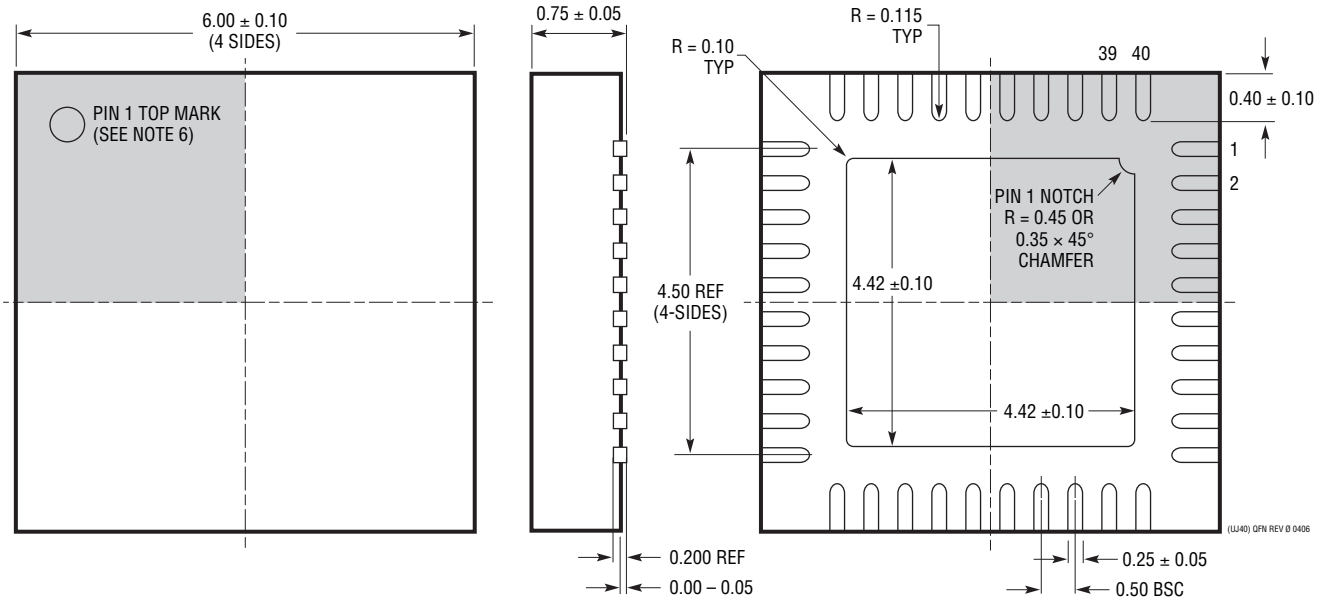


PACKAGE DESCRIPTION

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

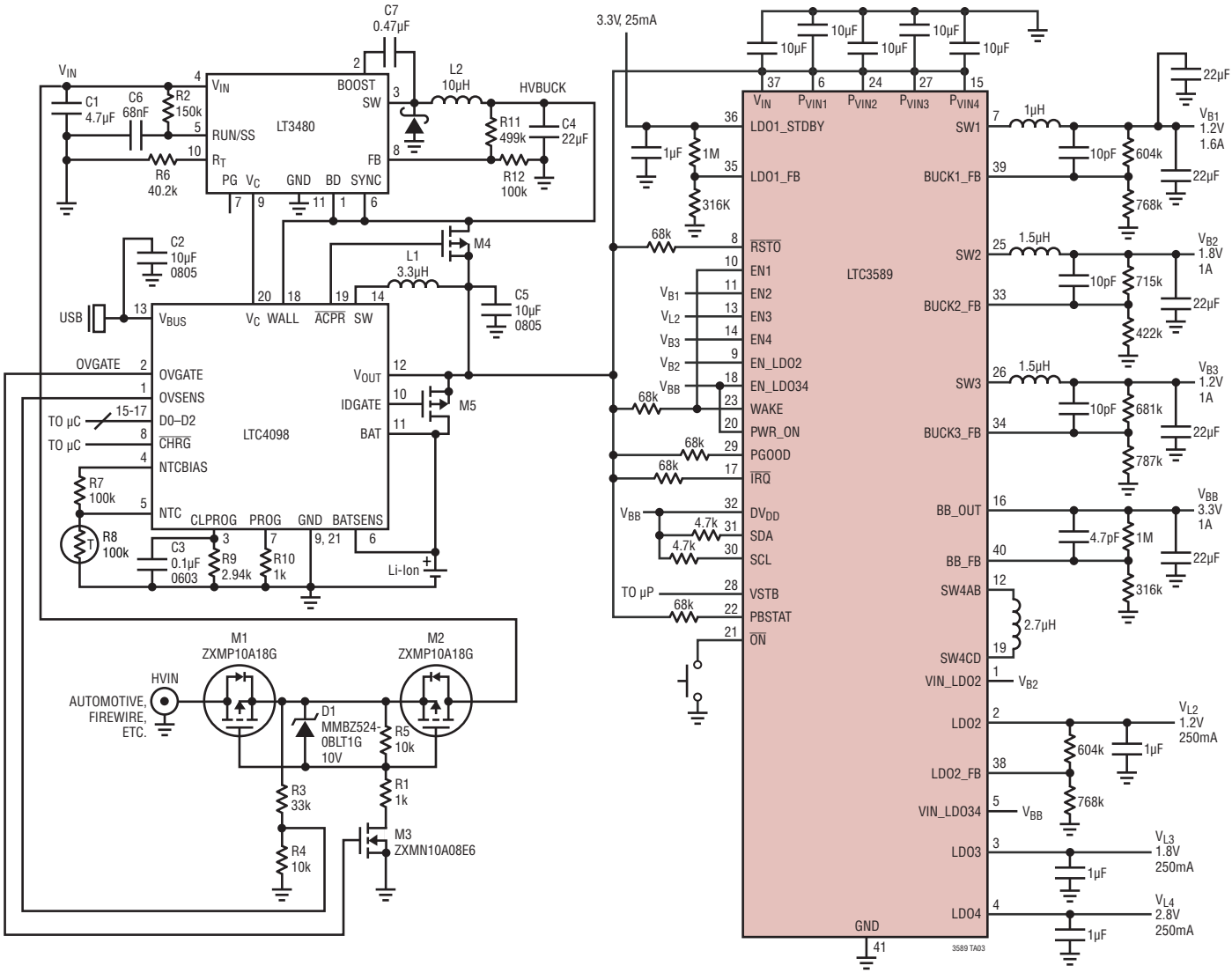
NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	9/10	Removed 0V from LDO4 on Block Diagram	15
B	12/10	Updated Part Marking in Order Information section	3

TYPICAL APPLICATION

Integrated Power IC for Mobile µProcessor System with USB/Automotive Battery Charger



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3101	1.8V to USB, Multioutput DC/DC Converter with Low Loss USB Power Controller	Seamless Transition Between Multiple Input Power Sources, V_{IN} Range: 1.8V to 5.5V, Buck-Boost Converter V_{OUT} Range: 1.5V to 5.25V, 3.3V_{OUT} at 800mA for $V_{IN} \geq 3V$, Dual 350mA Buck Regulators, V_{OUT}: 0.6V to V_{IN}, 38µA Quiescent Current in Burst Mode Operation, 24-Lead 4mm × 4mm × 0.75mm QFN Package
LTC3556	Switching USB Power Manager PMIC with Li-Ion/Polymer Charger	Complete Multifunction PMIC: Switching Power Manager, 1A Buck-Boost + 2 Buck Regulators + LDO, 4mm × 5mm QFN-28 Package
LTC3577/ LTC3577-1/ LTC3577-3/ LTC3577-4	Highly Integrated Portable/ Navigation PMIC	Complete Multifunction PMIC: Linear Power Manager and Three Buck Regulators, 10-LED Boost Reg, 4mm × 7mm QFN-44 Package, -1 and -4 Versions Have 4.1V V_{FLOAT}, -3 Version for SiRF Atlas IV Processors
LTC3586/ LTC3586-1	Switching USB Power Manager PMIC with Li-Ion/Polymer Charger	Complete Multifunction PMIC: Switching Power Manager, 1A Buck-Boost + 2 Bucks + Boost + LDO, 4mm × 6mm QFN-38 Package, -1 Version Has 4.1V V_{FLOAT}.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 1210 REV B • PRINTED IN USA