

Very Low Capacitance Diode Array

This diode array is configured to protect up to two high speed data transmission lines, used in Low Voltage Differential Signal (LVDS) ports. Acting as a line terminator, minimizes overshoot and undershoot conditions

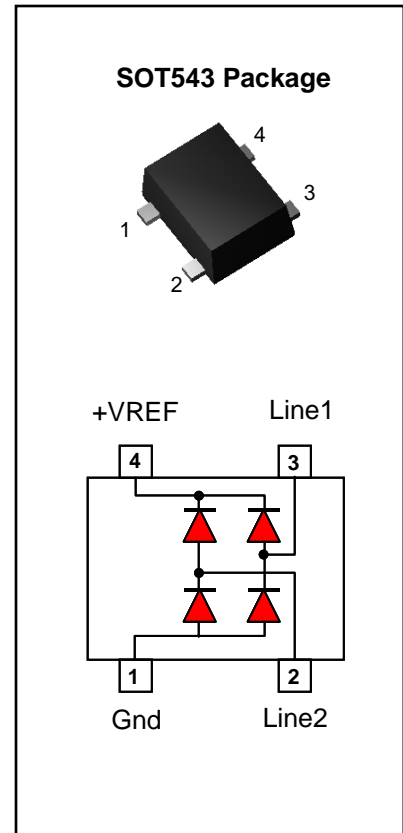
due to bus impedance as well as protect against over-voltage events as electrostatic discharges. This configuration comes in the new SOT543 package, offering a significant printed circuit board space savings compared to the SOT143.

SPECIFICATION FEATURES

- Maximum Capacitance of 1.0pF at 0Vdc 1MHz Line-to-Ground
- Maximum Leakage Current of 1.0 μ A @ VRWM
- New SMT Package SOT543
- IEC61000-4-2 Full Compliance; 15kV Air, 8kV Contact*
- 100% Tin Matte finish (LEAD-FREE PRODUCT)

APPLICATIONS

- USB 2.0 and Firewire Port Protection
- HDMI Version 1.3
- DVI



MAXIMUM RATINGS $T_j = 25^\circ\text{C}$ Unless otherwise noted

| Rating | Symbol | Value | Units |
|--|-----------|-------------|------------------|
| Peak Pulse Current (8/20 μ s Waveform) | I_{PPM} | 12 | A |
| Rectifier Repetitive Peak Reverse Voltage | V_{RRM} | 70 | V |
| Operating Junction Temperature Range | T_J | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Soldering Temperature, t max = 10s | T_L | 260 | $^\circ\text{C}$ |

Note: ESD Testing requires to connect a TVS between +VREF and GND, if there is no +VREF Bias connected.

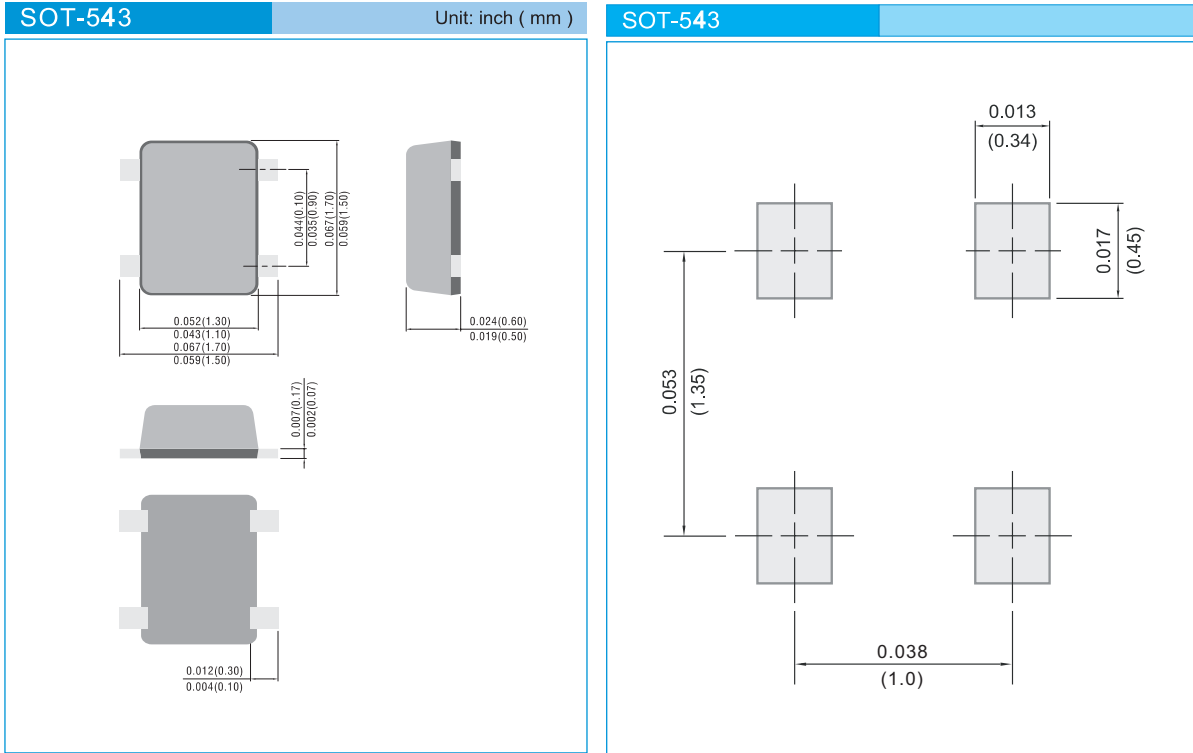


ELECTRICAL CHARACTERISTICS Tj = 25°C unless otherwise noted

| Parameter | Symbol | Conditions | Min | Typical | Max | Units |
|---|-----------|---|-----|---------|-----|---------|
| Reverse Stand-Off Voltage | V_{RWM} | | | | 70 | V |
| Reverse Breakdown Voltage | V_{BR} | $I_{BR} = 50\mu A$ | 85 | | | V |
| Reverse Leakage Current | I_R | $V_R = 70V$ | | | 1.0 | μA |
| Diode Surge Forward Voltage (8/20 μs) | V_{FC} | $I_{pp} = 1A$ | | | 2.0 | V |
| Diode Surge Forward Voltage (8/20 μs) | V_{FC} | $I_{pp} = 5A$ | | | 7.0 | V |
| Diode Surge Forward Voltage (8/20 μs) | V_{FC} | $I_{pp} = 12A$ | | | 12 | V |
| Off State Capacitance | C_T | 0 Vdc Bias f = 1MHz Between I/O Line and GND | | 0.8 | 1.0 | pF |
| | | 0 Vdc Bias f = 1MHz Between I/O lines | | 0.5 | 0.6 | pF |



PACKAGE DIMENSIONS - SOT543



APPLICATION EXAMPLE

