



# FDC365P

## P-Channel PowerTrench® MOSFET -35V, -4.3A, 55mΩ

### Features

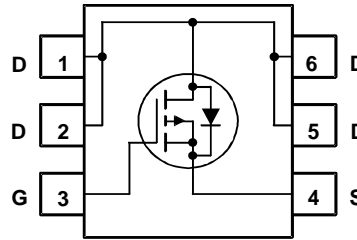
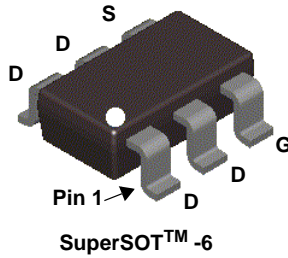
- Max  $r_{DS(on)}$  = 55mΩ at  $V_{GS} = -10V$ ,  $I_D = -4.2A$
- Max  $r_{DS(on)}$  = 80mΩ at  $V_{GS} = -4.5V$ ,  $I_D = -3.2A$
- RoHS Compliant

### General Description

This P-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench® technology to deliver low  $r_{DS(on)}$  and optimized  $Bvdss$  capability to offer superior performance benefit in the applications.

### Applications

- Inverter
- Power Supplies



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	-35	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	-Continuous (Note 1a)	-4.3	A
	-Pulsed	-20	
$P_D$	Power Dissipation (Note 1a)	1.6	W
	Power Dissipation (Note 1b)	0.8	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	156	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.365P	FDC365P	SSOT6	7"	8mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-35			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-26		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -28\text{V}, V_{GS} = 0\text{V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		5.0		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{V}, I_D = -4.2\text{A}$		45	55	m $\Omega$
		$V_{GS} = -4.5\text{V}, I_D = -3.2\text{A}$		70	80	
		$V_{GS} = -10\text{V}, I_D = -4.2\text{A}, T_J = 125^\circ\text{C}$		69	90	
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{V}, I_D = -4.2\text{A}$		8.7		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		530	705	pF
$C_{oss}$	Output Capacitance			105	135	pF
$C_{riss}$	Reverse Transfer Capacitance			55	80	pF
$R_g$	Gate Resistance		$f = 1\text{MHz}$		6.1	

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -20\text{V}, I_D = -4.2\text{A},$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$		7	13	ns	
$t_r$	Rise Time			3	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			15	28	ns	
$t_f$	Fall Time			3	10	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{V to } -10\text{V}$		11	15	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{V to } -5\text{V}$		6	9	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = -20\text{V},$ $I_D = -4.2\text{A}$		1.7		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			2.2		nC	

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -1.3\text{A}$ (Note 2)		-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -4.2\text{A}, di/dt = 100\text{A}/\mu\text{s}$		16	29	ns
$Q_{rr}$	Reverse Recovery Charge			7	14	nC

#### Notes:

- 1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



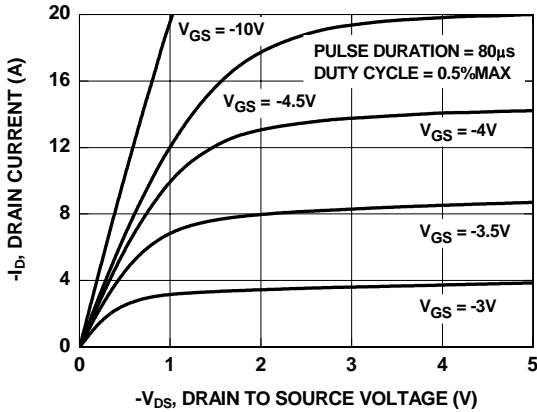
a.  $78^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper on FR-4 board.



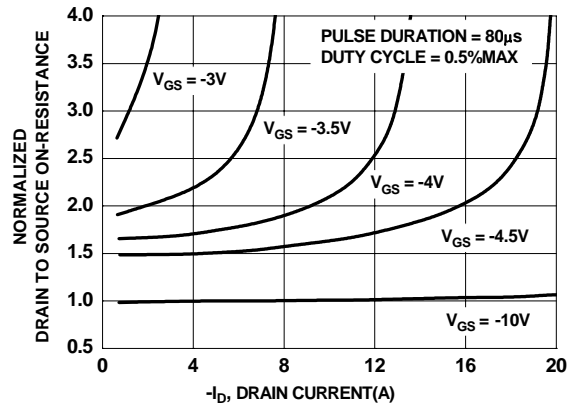
b.  $156^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

- 2: Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty cycle < 2.0%.

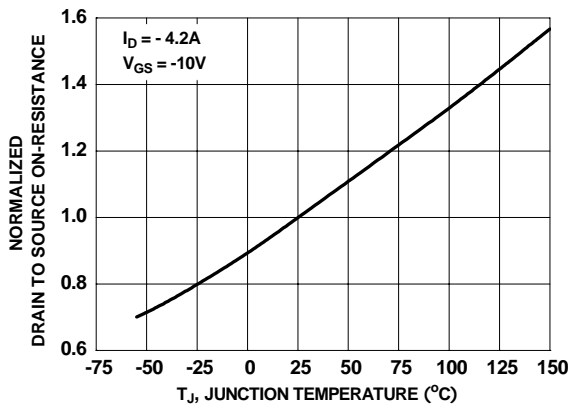
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



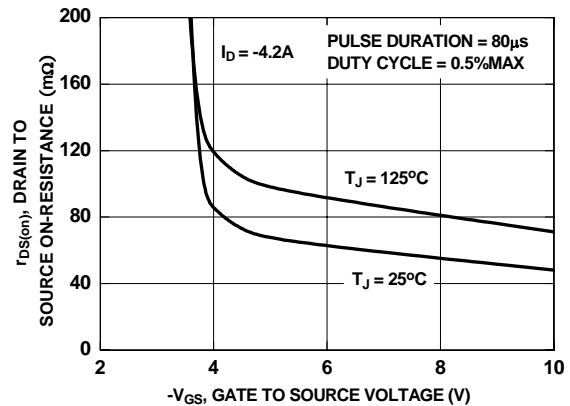
**Figure 1. On-Region Characteristics**



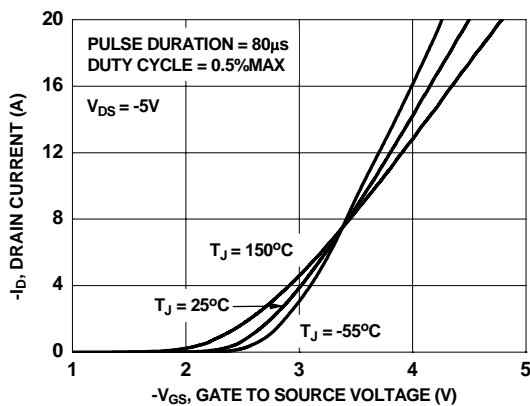
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



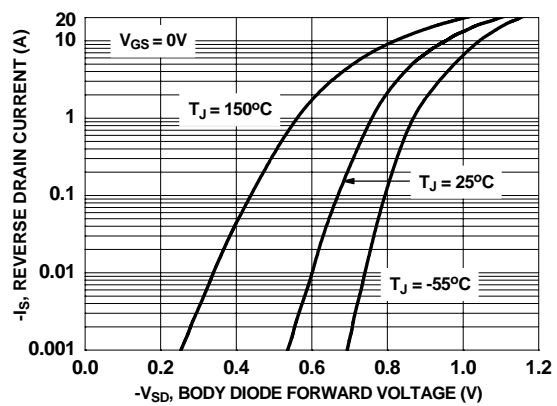
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

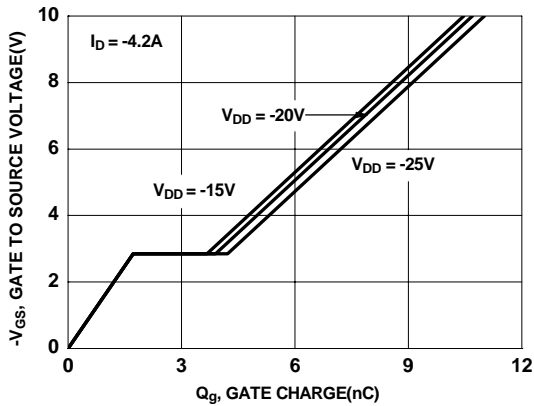


**Figure 5. Transfer Characteristics**

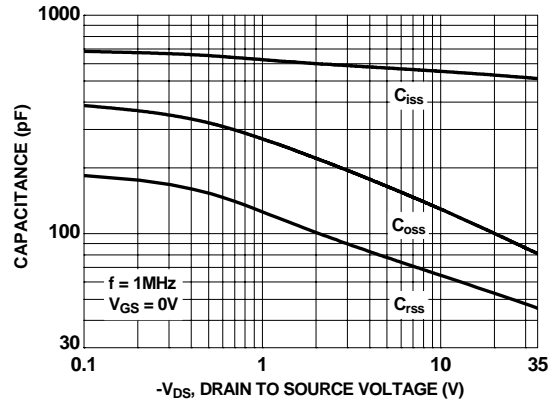


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

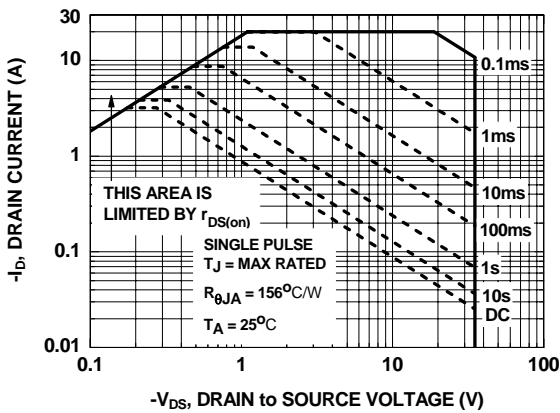
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



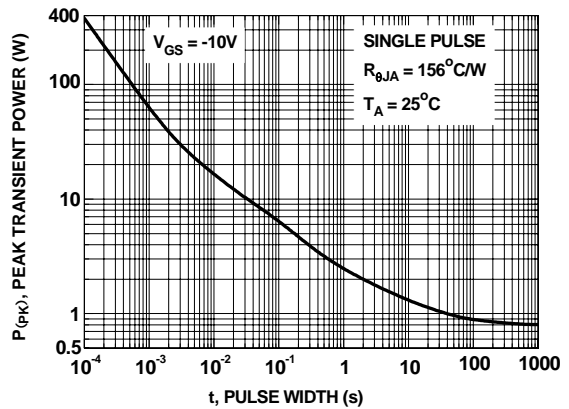
**Figure 7. Gate Charge Characteristics**



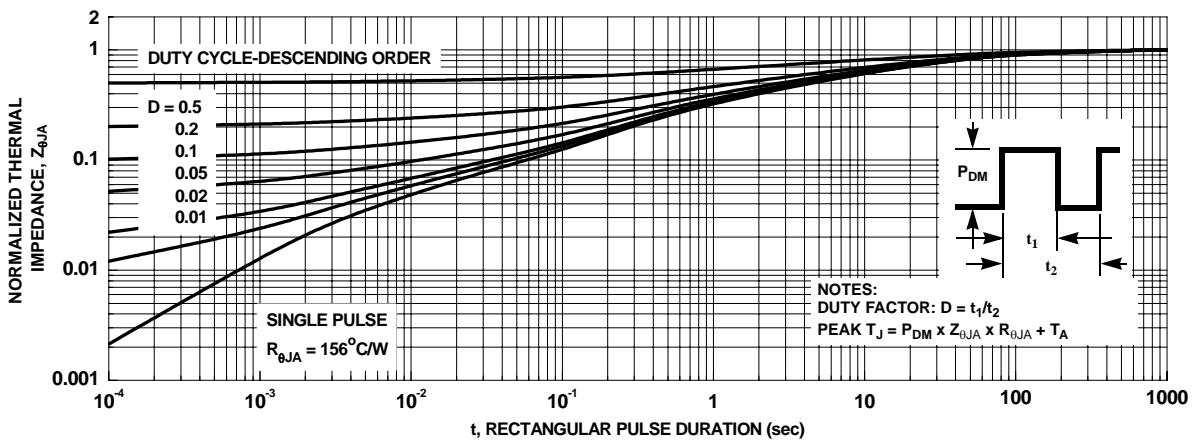
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**

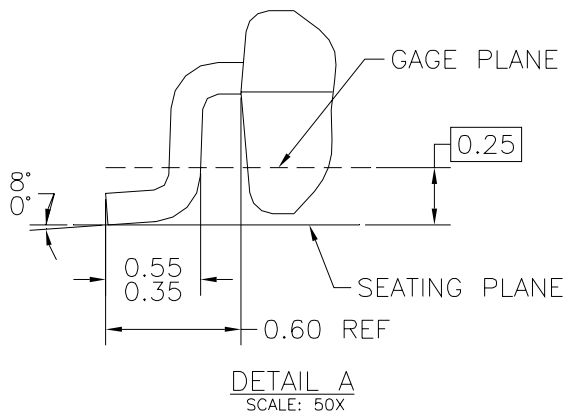
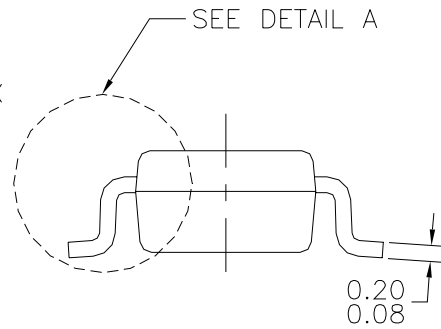
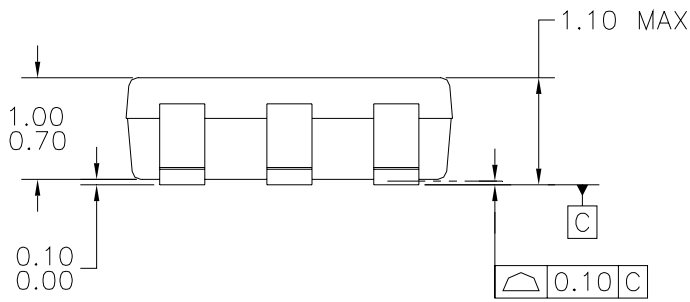
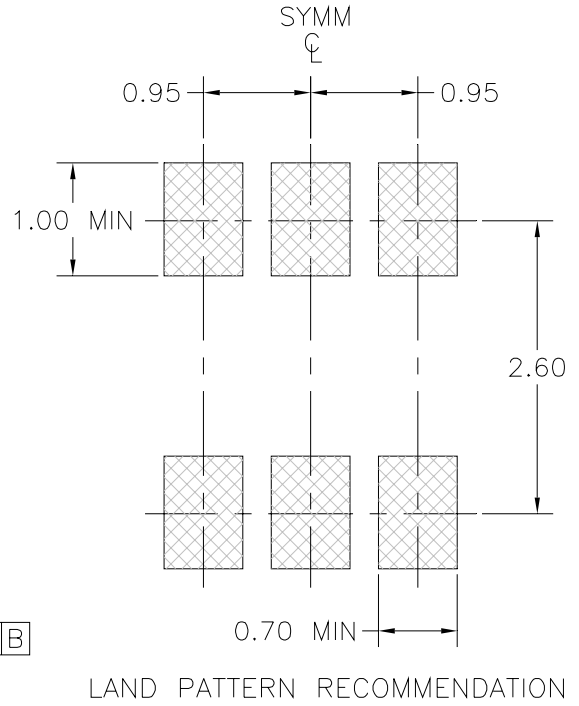
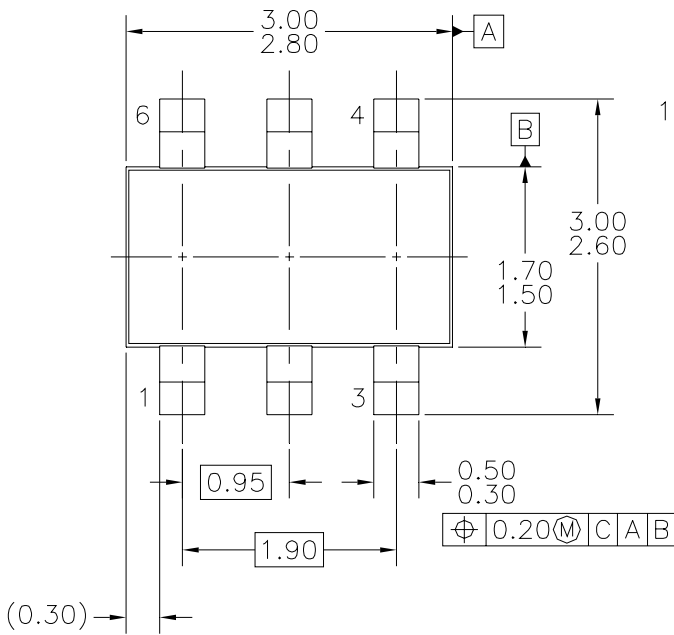


**Figure 10. Single Pulse Maximum Power Dissipation**



**Figure 11. Transient Thermal Response Curve**

### Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MO-193. VAR. AA, ISSUE C, DATED JANUARY 2000.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.

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