

# UNISONIC TECHNOLOGIES CO., LTD

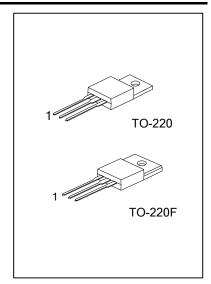
4N50 **Preliminary Power MOSFET** 

# 4 Amps, 500 Volts N-CHANNEL POWER MOSFET

#### **DESCRIPTION**

The UTC 4N50 is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

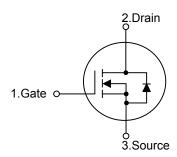
The UTC 4N50 is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.



#### **FEATURES**

- \* 4A, 500V,  $R_{DS(ON)}$ =2.0 $\Omega$  @  $V_{GS}$ =10V
- \* High Switching Speed
- \* 100% Avalanche Tested

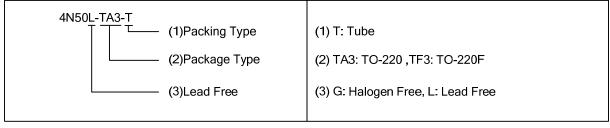
#### **SYMBOL**



#### ORDERING INFORMATION

Ordering Number		Dookogo	Pin Assignment			Dooking	
Lead Free	Halogen Free	Package	1	2	3	Packing	
4N50L-TA3-T	4N50G-TA3-T	TO-220	G	D	S	Tube	
4N50L-TF3-T	4N50G-TF3-T	TO-220F	G	D	S	Tube	

Note: Pin Assignment: G: Gate D: Drain S: Source



## ■ ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT	
Drain-Source Voltage			$V_{DSS}$	500	٧	
Gate-Source Voltage		$V_{GSS}$	±30	٧		
Drain Current Continuous (T <sub>C</sub> =25°C		C)	I <sub>D</sub>	4	Α	
Drain Current	Pulsed (Note 1)		$I_{DM}$	16 *	Α	
Avalanche Current (Note 1)			I <sub>AR</sub>	4	Α	
Avalancha Energy	Single Pulsed (Note 2)		E <sub>AS</sub>	216	mJ	
Avalanche Energy	Repetitive (Note 3)		E <sub>AR</sub>	8.5	mJ	
Peak Diode Recovery dv/dt (Note 3)			dv/dt	4.5	V/ns	
	T <sub>C</sub> =25°C	TO-220	P <sub>D</sub>	85	— W — W/°C	
Dower Dissination		TO-220F		28		
Power Dissipation	Danata ahawa 05°0	TO-220		0.67		
	Derate above 25°C	TO-220F		0.22		
Junction Temperature			$T_J$	+150	°C	
Storage Temperature			T <sub>STG</sub>	-55~+150	°C	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

#### ■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT		
Junction to Ambient	TO-220	0	62.5	°C/W	
Junction to Ambient	TO-220F	$ heta_{JA}$	62.5		
lunction to Coop	TO-220	0	1.47	°C/W	
Junction to Case	TO-220F	$\theta_{JC}$	4.5		

<sup>\*</sup> Drain current limited by maximum junction temperature

### ■ ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C, unless otherwise noted)

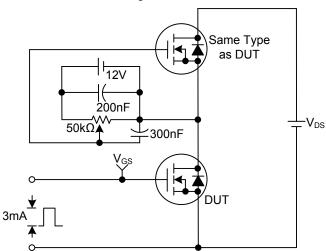
PARAMETER	SYMBOL	TEST CONDITIONS MI		TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	500			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =500V, V <sub>GS</sub> =0V			1	μΑ
Cata Source Lookage Current Forward		V <sub>GS</sub> =+30V, V <sub>DS</sub> =0V			+100	nA
Gate- Source Leakage Current Reverse	I <sub>GSS</sub>	V <sub>GS</sub> =-30V, V <sub>DS</sub> =0V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu A$	2.0		4.0	V
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2A		1.65	2.0	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C <sub>ISS</sub>			485	650	pF
Output Capacitance	Coss	$V_{GS}$ =0V, $V_{DS}$ =25V, f=1.0MHz		65	90	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			5	8	pF
SWITCHING PARAMETERS						
Total Gate Charge	$Q_G$	  -V <sub>GS</sub> =10V, V <sub>DS</sub> =400V, I <sub>D</sub> =4A		11	15	nC
Gate to Source Charge	$Q_GS$	(Note 4, 5)		3		nC
Gate to Drain Charge	$Q_GD$	(Note 4, 5)		5		nC
Turn-ON Delay Time	t <sub>D(ON)</sub>			14	38	ns
Rise Time	t <sub>R</sub>	$V_{DD}$ =250V, $I_{D}$ =4A, $R_{G}$ =25 $\Omega$ (Note 4, 5)		21	52	ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>			27	64	ns
Fall-Time	t <sub>F</sub>			20	50	ns
SOURCE- DRAIN DIODE RATINGS AND	CHARACTERI	STICS				
Maximum Body-Diode Continuous Current	I <sub>S</sub>				4	Α
Maximum Body-Diode Pulsed Current	I <sub>SM</sub>				16	Α
Drain-Source Diode Forward Voltage	$V_{SD}$	I <sub>S</sub> =4A, V <sub>GS</sub> =0V			1.6	V
Body Diode Reverse Recovery Time	t <sub>RR</sub>	I <sub>S</sub> =4A, V <sub>GS</sub> =0V, dI <sub>F</sub> /dt=100A/μs		36		ns
Body Diode Reverse Recovery Charge	$Q_{RR}$	(Note 4)		33		μC

Notes: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

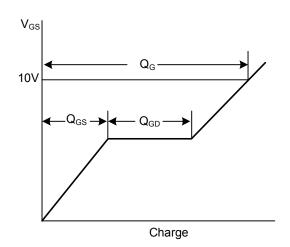
- 2. L = 27mH,  $I_{AS}$  = 4A,  $V_{DD}$  = 50V,  $R_G$  = 25 $\Omega$ , Starting  $T_J$  = 25 $^{\circ}C$
- 3.  $I_{SD} \le 4A$ , di/dt  $\le 200A/\mu s$ ,  $V_{DD} \le BV_{DSS}$ , Starting  $T_J = 25^{\circ}C$
- 4. Pulse Test: Pulse width ≤ 300µs, Duty cycle ≤ 2%
- 5. Essentially independent of operating temperature

#### ■ TEST CIRCUITS AND WAVEFORMS

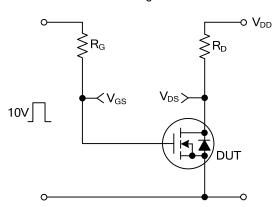
Gate Charge Test Circuit



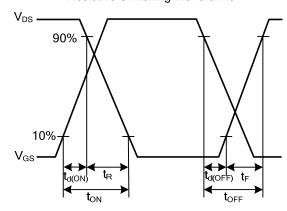
Gate Charge Waveforms



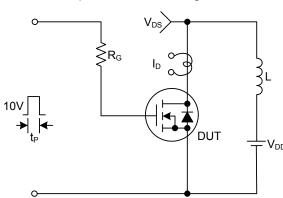
Resistive Switching Test Circuit



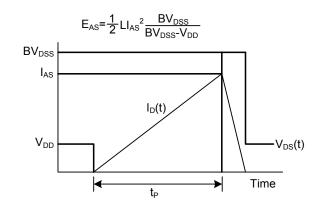
Resistive Switching Waveforms



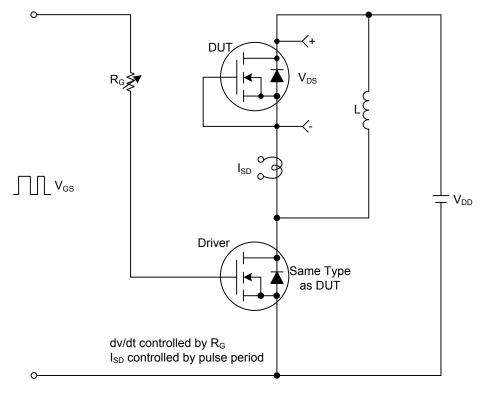
Unclamped Inductive Switching Test Circuit

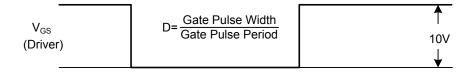


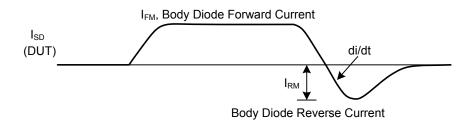
Unclamped Inductive Switching Waveforms

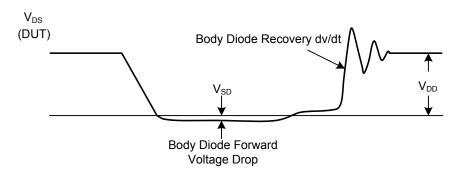


Peak Diode Recovery dv/dt Test Circuit & Waveforms









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