PROTECTION INTERFACE for PMICs with INTEGRATED OVP CONTROL

NEW PRODUCT

Description

AP9050 is designed to protect the latest generation of PMICs for portable applications such as UMPCs, smartphones and others utilizing battery power.

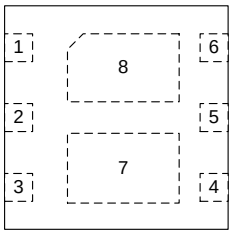
The integrated LDO allows the PMIC to power up and determine whether the connected power supply (USB or AC-DC wall adapter) is valid and a safe operation can be performed.

The PMIC controls the operation of the integrated n-channel MOSFET to either pass the line voltage or disconnect the line from the PMIC to protect its internal circuits in the event of an over-voltage.

The AP9050 is available in a low-profile U-DFN2020-6 package.

Pin Assignments

(Top View)



U-DFN2020-6

Features

- Input Supply Range from 3V to 30V
- Lower Power Dissipation and Higher Efficiency as compared to a Zener Shunt Regulator
- LDO is stable without a bypass capacitor on the output and operates across the temperature range
- Available in a U-DFN2020-6 package with a typical height of 0.575mm

Applications

- Power Interface for New Generation PMICs
- Charger Front End Protection
- Smartphone
- Cell Phone
- Ultra Mobile PC
- Tablets

Note: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.

Typical Application Circuit

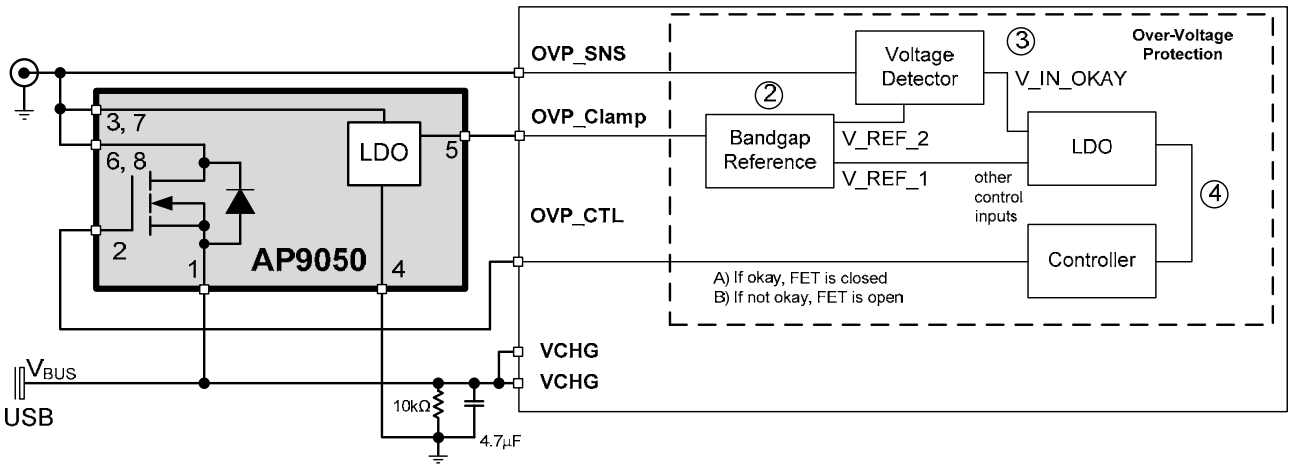


Figure 1. Typical Application Circuit

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Pin Descriptions

Pin #	Name	Description
1	Source	Source of the n-channel power FET. Pass-switch's output pin.
2	Gate	Gate of the FET switch. Pass-switch's control pin.
3, 7	V_{IN}	Input voltage to the internal LDO.
4	Ground	LDO ground connection.
5	V_{OUT}	Output of the LDO.
6, 8	Drain	Drain of the power FET. Pass-switch's input pin.

Functional Block Diagram

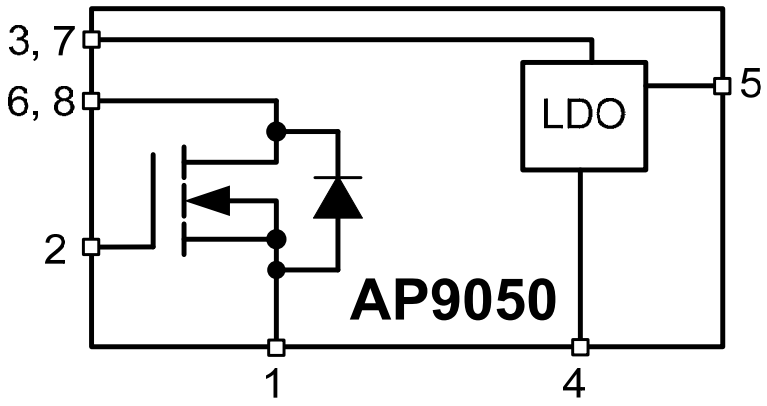

Figure 2. Functional Block Diagram

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Absolute Maximum Ratings (Note 2, 3)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	−0.3 to 30	V
V_{GS}	Gate-to-Source Voltage	±12	V
I_{Dpk}	Drain Current, Peak (10µs pulse)	19	A
I_D	Drain Current, Continuous (Note 4, Steady-State) T_A = 25ºC T_A = 85ºC	 3.7 2.7	A
P_{max}	Total Power Dissipation @ T_A = 25°C (Note 3, 4)	750	mW
T_J	Junction Temperature Range	−40 to +125	°C
T_J	Non-operating Temperature Range	−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes	260	°C

Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Notes: 2. Exceeding these ratings may damage the device.
3. Mounted on FR4 Board using 30 mm^2, 2 oz Cu.
4. Dual die operation (equally−heated).

Thermal Resistance

Symbol	Parameter	Rating	Unit
θ_{JA}	Junction to Ambient (Note 5)	132	°C/W
θ_{JC}	Junction to Case	13	°C/W

Note: 5. Test condition for DFN2020-6: Mounted on FR4 Board using 30 mm^2, 2 oz Cu.

Recommended Operating Conditions (Note 6)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	3	30	V
T_A	Operating Ambient Temperature Range	−40	+85	°C

Note: 6. The device function is not guaranteed outside of the recommended operating conditions.

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Electrical Characteristics (V_{IN} (OVP_SENSE) = 5.0V, T_J = +25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Power FET						
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V T_J = 85°C			1.0 10	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±8V			80	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA	0.62	0.9	1.2	V
$R_{DS(on)}$	Drain-to-Source On-Resistance (Note 7)	V_{GS} = 4.5V, I_D = 2.0A V_{GS} = 2.5V, I_D = 2.0A		41 55	53 68	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5V, ID = 2.0A		8		S
C_{ISS}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		500		pF
C_{OSS}	Output Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		65		pF
C_{RSS}	Reverse Transfer Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		50		pF
LDO (unless otherwise noted, T_J = 25ºC, V_{IN} = 5.0V)						
V_{OUT}	Regulated Output Voltage	V_{IN} = 5.5V, I_{OUT} = 1mA	4.6	5.0	5.3	V
V_{head}	Headroom	V_{IN} − V_{OUT}, I_{OUT} = 1.2mA, V_{IN} = 4.6V			150	mV
		V_{IN} − V_{OUT}, I_{OUT} = 10mA, V_{IN} = 4.8V, T_J = −40 to +125°C			1000	mV
Response to Input Transient						
t_{pulse}	Time signal is above 5.5V	V_{IN} 0 to 30V, < 1µs rise time, 5.0kΩ resistive load (Note 8)			5.0	µs
V_{pk}	Peak Voltage	V_{IN} 0 to 30V, < 1µs rise time, 5.0kΩ resistive load (Note 8)			9.0	V
Total Device						
I_{bias}	Input Bias Current	V_{IN} = 5.5V		110	850	µA
V_{IN_min}	Minimum Operating Voltage				3.0	V

Notes: 7. Pulse test width 300µs, duty cycle 2%
8. Guaranteed by design

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Typical Performance Characteristics

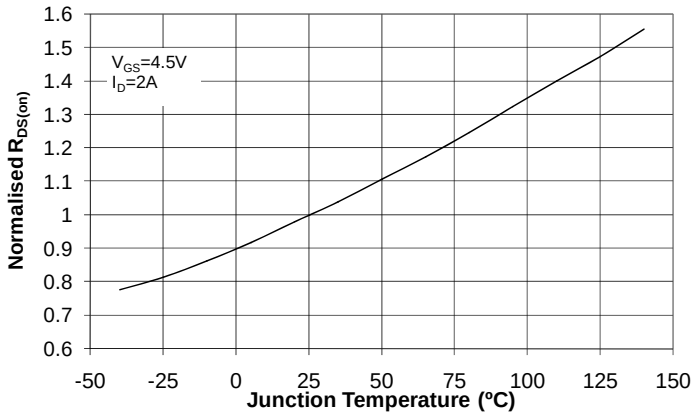

Figure 3. $R_{DS(ON)}$ variation over junction temperature

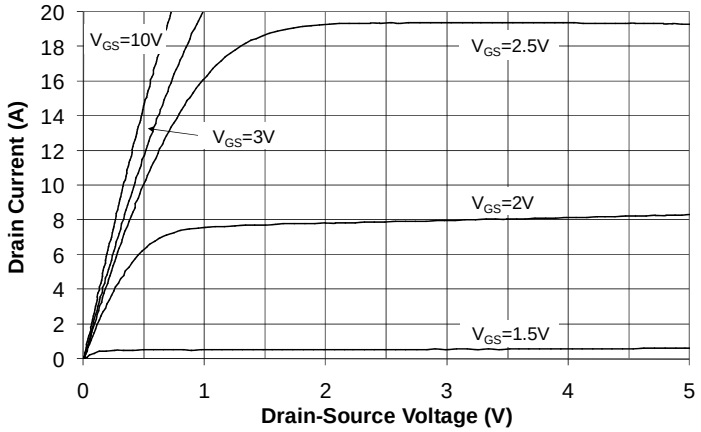

Figure 4. $R_{DS(ON)}$ Characteristics

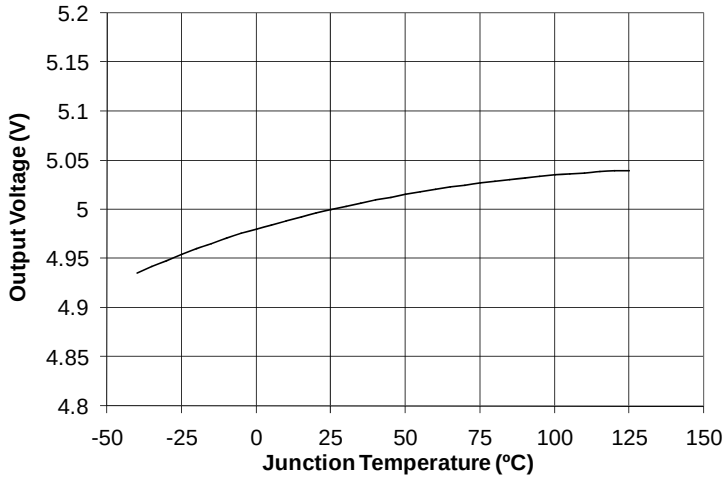

Figure 5. Output voltage variation over junction temperature

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Applications Information

Theory of Operation

The AP9050 was designed to work in close relationship with a PMIC (Power Management IC). To protect the PMIC from an overvoltage situation the AP9050 powers up a detection circuit within the connected PMIC. (See Figure 2 as reference)

This detection circuit determines if a valid input source is connected (ex. V_{IN} < 8V). If a valid input source is detected the power MOSFET will be turned on and the supply current to the PMIC will be turned on. The overvoltage detection is continuous, if an overvoltage occurs at a later state the Power MOSFET will be turned off.

PCB Layout

The AP9050 was designed utilizing two process technologies to provide best performance and a cost effective solution.

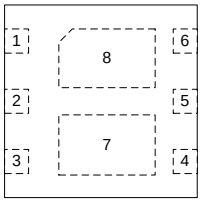

Figure 6. Package Pin Out

Both die are packaged side by side in the U-DFN2020-6 package and are mounted on two separate exposed pads. These pads are not required for electrical functionality, but to aid with the thermal performance of AP9050.

Attention should be paid in the layout of the PCB (Printed Circuit Board) that PAD7 is connected to V_{IN} of the LDO, pin 3, while PAD8 is connected to the Drain of the Power MOSFET, pin 6 of the package. For best thermal performance large copper areas connected to the two exposed pads should be used to transfer heat away from the AP9050.

External Capacitors

AP9050 was specified to reduce board space and external component count, by designing the LDO to be stable without an external bypass capacitor.

A low ESR 1nF to 10nF external capacitor can be used to improve behavior with fast ac transients or other switching currents that might be present.

To improve noise immunity and ac impedance from long input traces a 1nF capacitor can be added to the input V_{IN} of the LDO.

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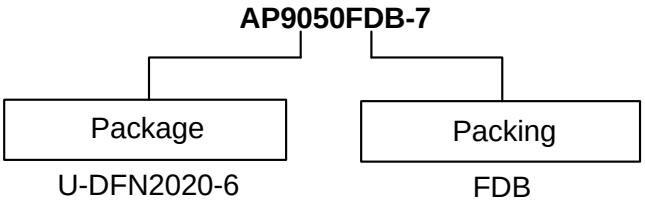
Ordering Information



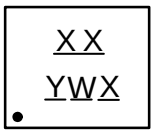
Device	Package Code	Packaging (Note 10)	7" Tape and Reel	
			Quantity	Part Number Suffix
AP9050FDB-7	FDB	U-DFN2020-6	3000/Tape & Reel	-7

Note: 10. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

Marking Information

U-DFN2020-6

(Top View)



XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week; a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Internal code

Device	Package	Identification Code
AP9050FDB	U-DFN2020-6	BZ

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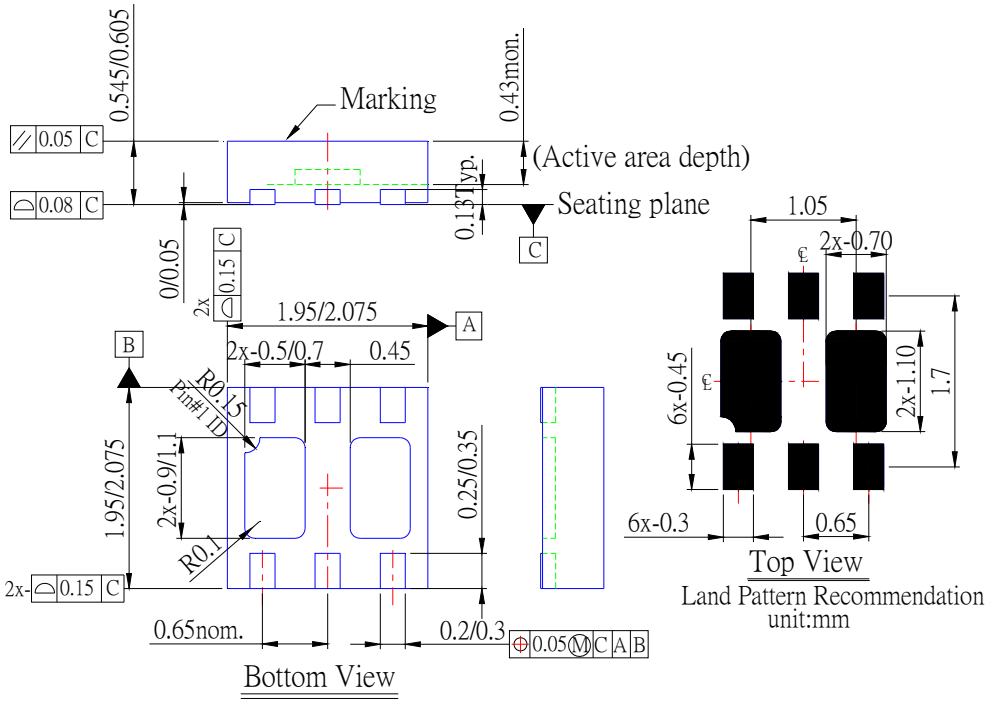
Package Outline Dimensions (All Dimensions in mm)

U-DFN2020-6



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