TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSVI)

TPCA8109

Lithium Ion Battery Applications Power Management Switch Applications

- Small footprint due to small and thin package
- Low drain-source ON-resistance: $RDS(ON) = 7 \text{ m}\Omega$ (typ.)
- Low leakage current: $I_{DSS} = -10 \,\mu\text{A} \,(\text{max}) \,(V_{DS} = -30 \,\text{V})$
- Enhancement mode: $V_{th} = -0.8$ to -2.0 V ($V_{DS} = -10$ V, $I_{D} = -0.5$ mA)

Absolute Maximum Ratings (Ta = 25°C)

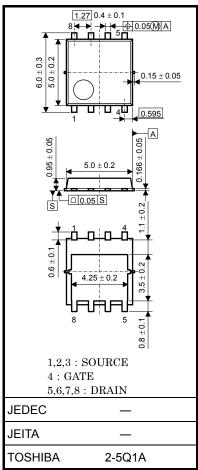
Characte	ristics	Symbol	Rating	Unit	
Drain-source voltage		V_{DSS}	-30	V	
Drain-gate voltage (R	$R_{GS} = 20 \text{ k}\Omega$	V_{DGR}	-30	V	
Gate-source voltage		V _{GSS}	-25/+20	V	
Drain current	DC (Note 1)	ID	-24	Α	
Drain current	Pulsed (Note 1)	I_{DP}	-72	A	
Drain power dissipation (Tc=25°C)		P_{D}	30	W	
Drain power dissipati	on (t = 10 s)	P _D	2.8	W	
	(Note 2a)		2.0		
Drain power dissipation (t = 10 s)		D-	1.6	W	
	(Note 2b)	P_{D}	1.0	VV	
Single pulse avalanche energy		Eas	75	mJ	
	(Note 3)	⊏AS	73	1110	
Avalanche current		I_{AR}	-24	Α	
Channel temperature		T _{ch}	150	°C	
Storage temperature	range	T _{stg}	-55 to 150	°C	

Note: For Notes 1 to 3, refer to the next page.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

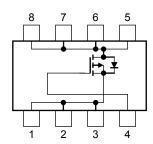
This transistor is an electrostatic sensitive device. Please handle with caution.

Unit: mm



Weight: 0.076 g (typ.)

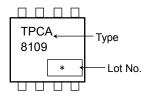
Circuit Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case (Tc=25°C)	R _{th (ch-c)}	4.17	°C/W
Thermal resistance, channel to ambient $(t = 10 \text{ s})$ (Note 2a)	R _{th (ch-a)}	44.6	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	R _{th (ch-a)}	78.1	°C/W

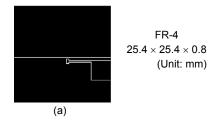
Marking (Note 4)

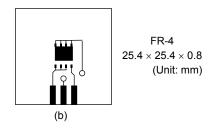


Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a)

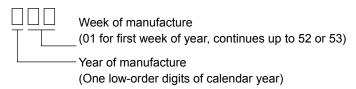
(b) Device mounted on a glass-epoxy board (b)





Note 3: $V_{DD} = -24~V,~T_{ch} = 25^{\circ}C$ (initial), $L = 100 \mu H,~R_G = 25~\Omega,~I_{AR} = -24~A$

Note 4: * Weekly code: (Three digits)



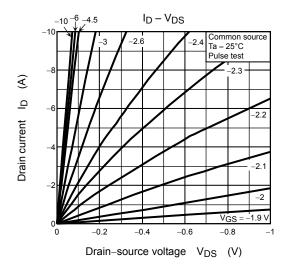
Electrical Characteristics (Ta = 25°C)

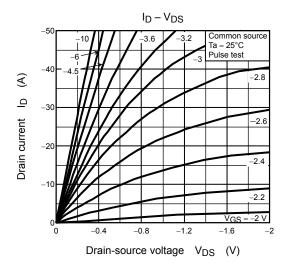
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cur	rent	I _{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±100	nA
Drain cut-OFF cu	rrent	I _{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$	_	_	-10	μА
Drain agurag bro	akdowa voltago	V _{(BR)DSS}	$I_D = -10 \text{ mA}, V_{GS} = 0 \text{ V}$	-30	_	_	V
Dialii-source brea	akuowii voitage	V _{(BR) DSX}	$I_D = -10 \text{ mA}, V_{GS} = 10 \text{ V (Note5)}$	- ±100 - 10 -30 - 1 -30 - 21 -0.8 -2.0 - 10 13 - 7 9 - 2400 - 2400	V		
Gate threshold vo	oltage	V _{th}	$V_{DS} = -10 \text{ V}, I_D = -0.5 \text{ mA}$	-0.8 — -2.0		V	
Drain sauras ON	registance	_	$V_{GS} = -4.5V$, $I_D = -12 A$	_	10	13	m0
Drain-source ON	resistance	KDS (ON)	V _{GS} = -10 V, I _D = -12 A	- ±100 10 -30	mΩ		
Input capacitance	e	C _{iss}		_	2400	_	
Reverse transfer capacitance		C _{rss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	_	400	_	pF
Output capacitance		Coss		_	460	_	
	Rise time	t _r	V _{GS} 0 V 7	_	9.2	_	
	16	_					
Switching time	Fall time	t _f	4.7.5 1.1.2 R _L = 1.	_	58	_	ns
	Turn-off time		100 10 1	_	172	_	
	ource plus gate-drain)		_	56			
Gate-source charge 1		Q _{gs1}		_	5.6		nC
,		Q _{gd}		_	15	_	

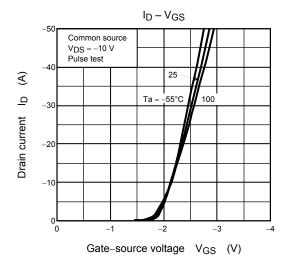
Source-Drain Ratings and Characteristics (Ta = 25°C)

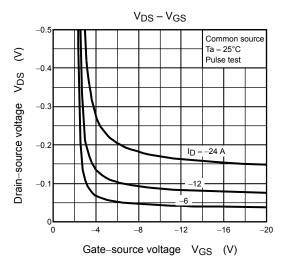
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit	
Drain reverse current	Pulse	(Note 1)	I _{DRP}	_	_	_	-72	Α
Forward voltage (diode)			V_{DSF}	$I_{DR} = -24 \text{ A}, V_{GS} = 0 \text{ V}$	_	_	1.2	V

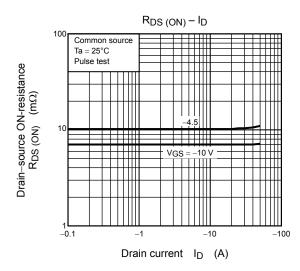
Note 5: $V_{(BR)DSX}$ mode (the application of a plus voltage between gate and source) may cause decrease in maximum rating of drain-source voltage.



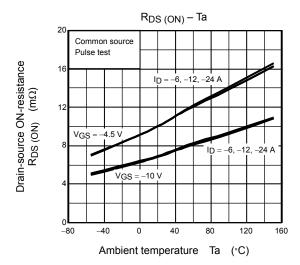


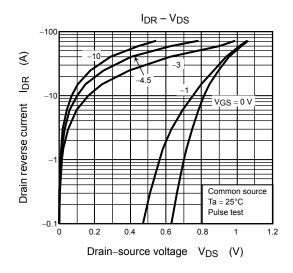


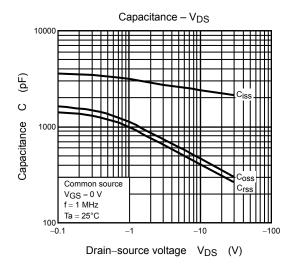


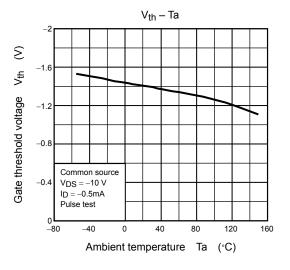


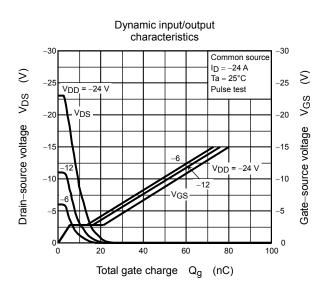
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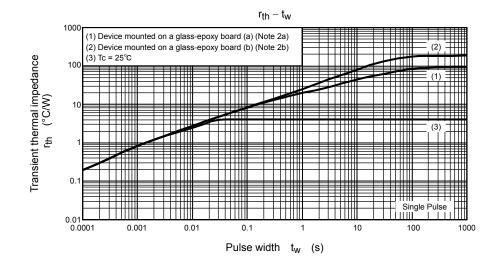


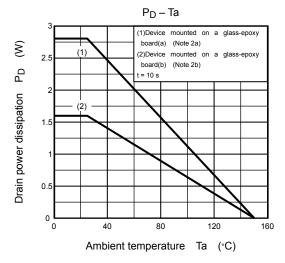


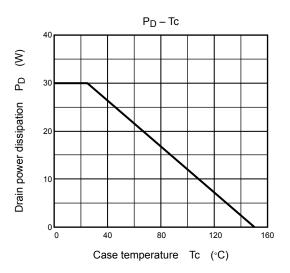


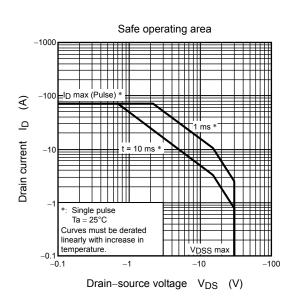


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