AN-6754A

Design Guideline to Replace SG6742 with FAN6754A

Introduction

FAN6754A is a highly integrated PWM controller featuring green mode, frequency hopping, constant power limit, and a number of protection functions. The green-mode function, burst-mode function, and a low operating current maximize the light-load efficiency so that the power supply can meet stringent standby power regulations. Frequency hopping reduces the Electro-Magnetic Emission (EMI) by spreading the frequency spectrum. The constant-power-limit function minimizes the component stress in abnormal conditions and helps optimize the power stage design. Protection functions such as brownout protection, overload / open-loop protection (OLP), over-voltage protection (OVP), sense pin short-circuit protection (SSCP), and over-temperature protection (OTP) are fully integrated to improve the reliability of the switched-mode power supply without increasing system cost. This application note explains how to replace PWM controller SG6742 with FAN6754A. These two devices have the same pin configuration and direct replacement can be achieved without PCB layout change. However, functional improvements to the FAN6754A for higher efficiency and better performance requires several external components to be changed accordingly. Table 1 summarizes the difference between these two devices. The pulse-by-pulse current limit threshold voltage is reduced almost by half to reduce the current sensing loss, which results in 0.4~0.5% efficiency improvement. The operating current is also reduced to achieve less than 100mW standby power consumption for most designs. The typical application circuit and internal block diagram are shown in Figure 1 and Figure 2 , respectively.

Table 1. Comparison of SG6742 and FAN6754A

	SG6742	FAN6754A
Brownout Protection	No	Line Sensing Using HV Pin
Line Voltage Compensation for Pulse-by-Pulse Current Limit ($V_{Limit-L}$ / $V_{Limit-H}$)	Saw-Limit (0.9V / 0.56V)	Adjusted by HV Pin (0.46V / 0.39V)
Sense Pin Short-Circuit Protection	V_{SENSE}<0.15V Longer than 150μs	V_{SENSE}<0.05V Longer than 120μs
Gate Drive Clamping Voltage	18V	13V
FB Impedance (Z_{FB})	5KΩ	15.5KΩ
Operating Current (I_{DD_OP})	2.7mA	1.7mA
Leading-Edge Blanking Time (t_{LEB})	150ns	280ns
Soft-Start	5ms	8ms
Maximum Duty Cycle	65%	89%
V_{FB-G}/V_{FB-N} for Green Mode	2.4V / 3.0V	2.3V / 2.8V
V_{ZDC}/V_{ZDCR} for Burst Mode	1.6V / 1.7V	2.0V / 2.1V

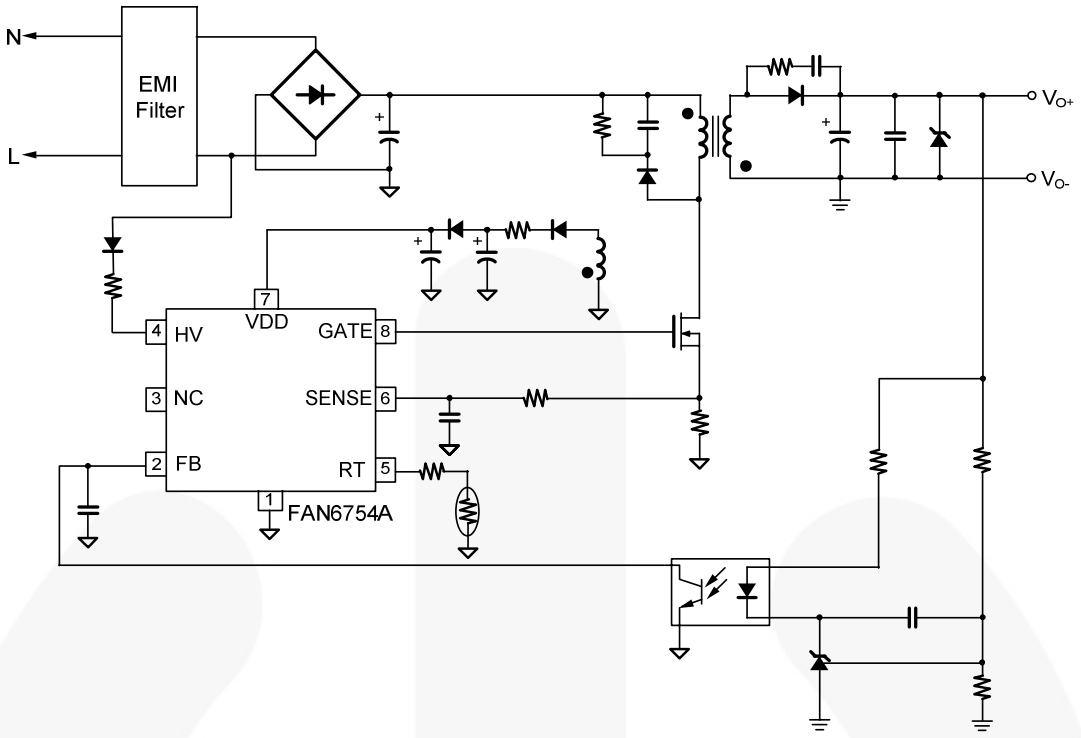

Figure 1. Typical Application

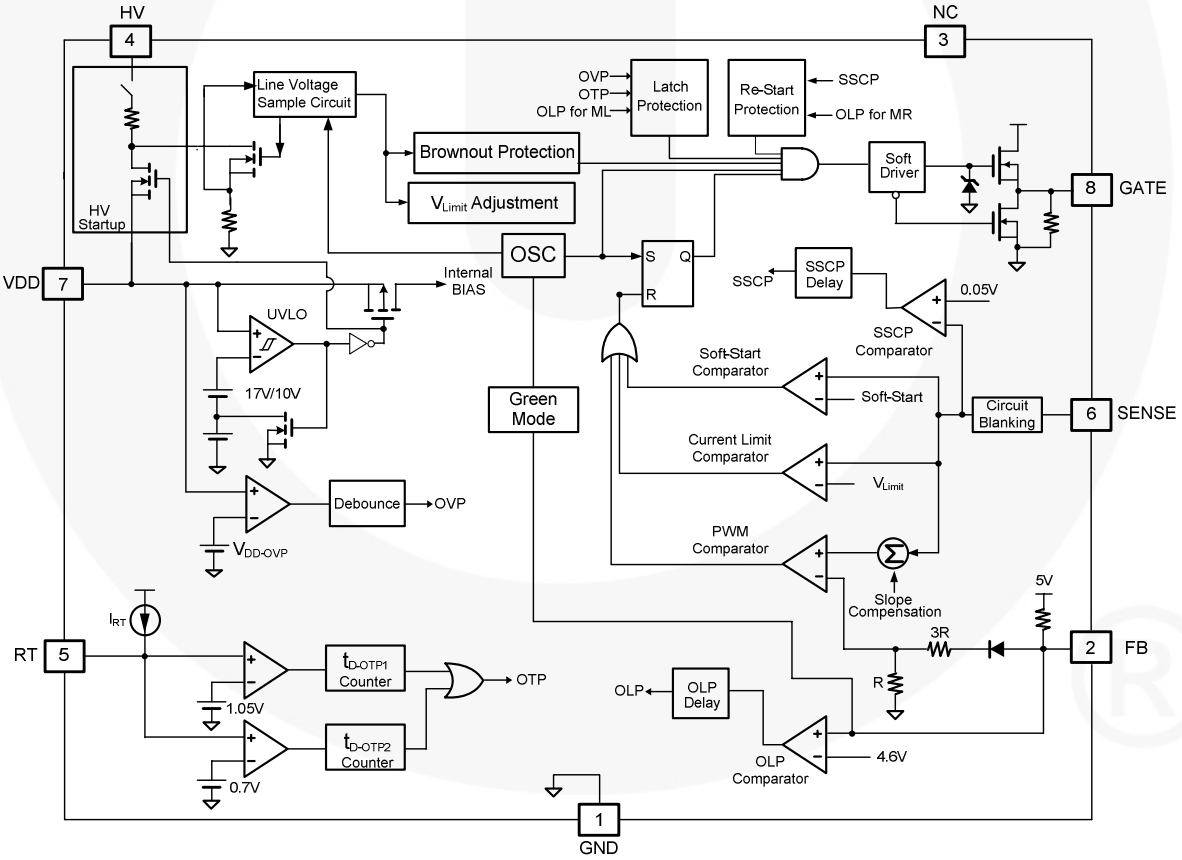

Figure 2. Internal Block Diagram

HV Startup Circuit

Figure 3 shows the simplified schematic for the HV startup circuit. When the AC line is applied to the power supply, the internal high-voltage current source charges the hold-up capacitor C_1 through startup resistor R_{HV}. As the V_{DD} pin voltage reaches the turn-on threshold V_{DD-ON}, the PWM controller is enabled and starts normal operation. Then the high-voltage current source is switched off and the supply current is drawn from the auxiliary winding of the main transformer, as shown in Figure 3. For better line surge immunity on the HV pin, it is typical to use a HV resistor larger than 150kΩ. When a large C1 capacitor is required for V_{DD}, the HV resistor limits the charging current for the V_{DD} capacitor, increasing the startup time. If a shorter startup time is required, a two-stage V_{DD} capacitor circuit, shown in Figure 3, is recommended.

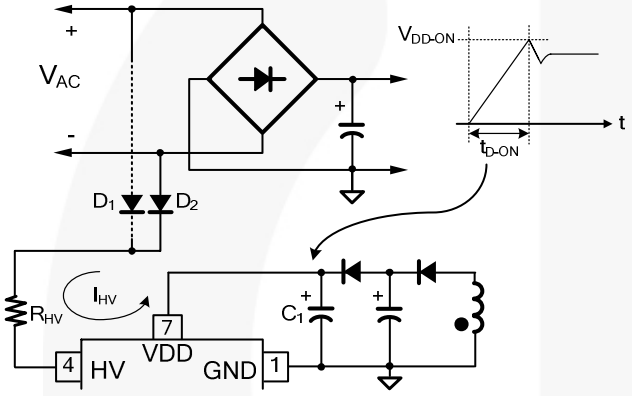

Figure 3. Startup Circuit

Soft-Start

The FAN6754A has an internal soft-start circuit that progressively increases the pulse-by-pulse current limit level as shown in Figure 4. The built-in soft-start circuit significantly reduces the input current overshoot during startup, which also minimizes output voltage overshoot.

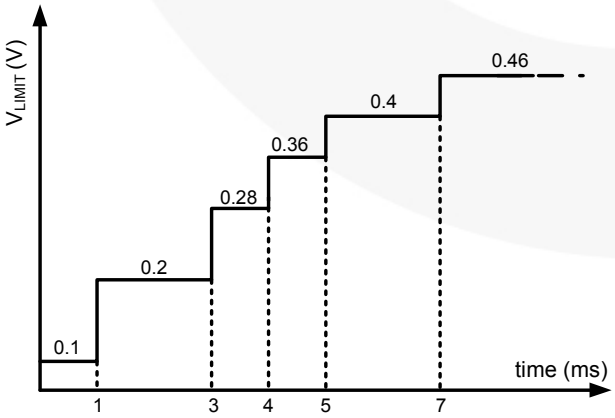

Figure 4. Pulse-by-Pulse Current Limit Level for Soft-Start

Under-Voltage Lockout (UVLO)

The FAN6754A has an under-voltage lockout for V_{DD}. Figure 5 shows the turn-on (V_{DD-ON}) and turn-off (V_{DD-OFF}) threshold levels. Note that there is another V_{DD} turn-off level (V_{DD-OLP}) to minimize the power dissipation of the power stage during the overload protection / open-loop protection condition by extending the V_{DD} discharge time.

If the output short is overloaded or the feedback loop is opened, the FB voltage remains above V_{FB-OLP} for OLP delay time (t_{D-OLP}) until the protection is triggered. During that time, the MOSFET drain-to-source current reaches its pulse-by-pulse current limit level for every switching cycle, causing a large amount of power dissipation to the switching devices and transformer. With the two-step UVLO mechanism, the average input power during overload or open-loop condition is significantly reduced.

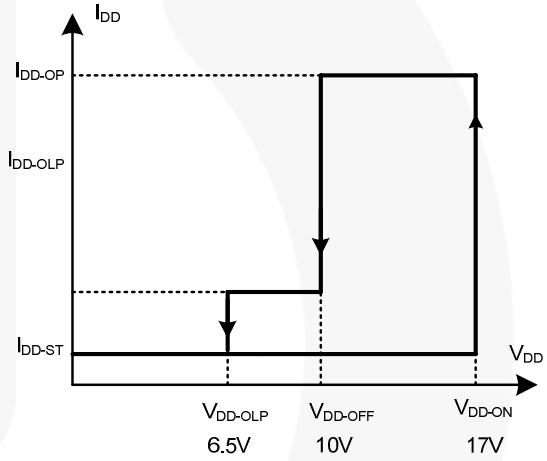

Figure 5. UVLO Specification

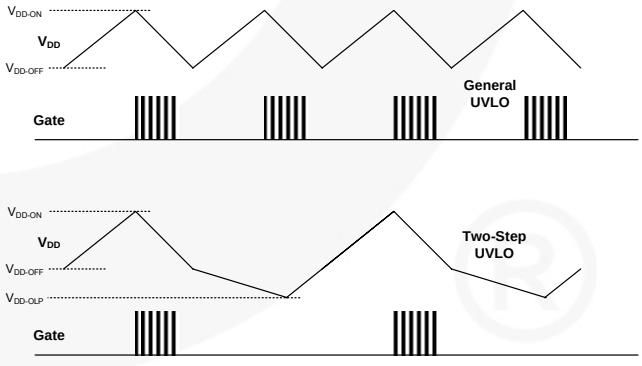

Figure 6. Two-Level UVLO

Green-Mode Operation

The FAN6754A uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 7, such that the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 65KHz. Once V_{FB} decreases below V_{FB-N} (2.8V), the PWM frequency starts to linearly decrease from 65KHz to 22kHz to reduce the switching losses. As V_{FB} decreases below V_{FB-G} (2.3V), the switching frequency is fixed at 22kHz. As V_{FB} decreases below V_{FB-ZDC} (2.0V), the FAN6754A enters burst-mode operation. When V_{FB} drops below V_{FB-ZDC}, the FAN6754A stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above $V_{FB-ZDCR}$, switching resumes. Burst mode alternately enables and disables switching, thereby reducing switching loss in standby mode, as shown in Figure 8.

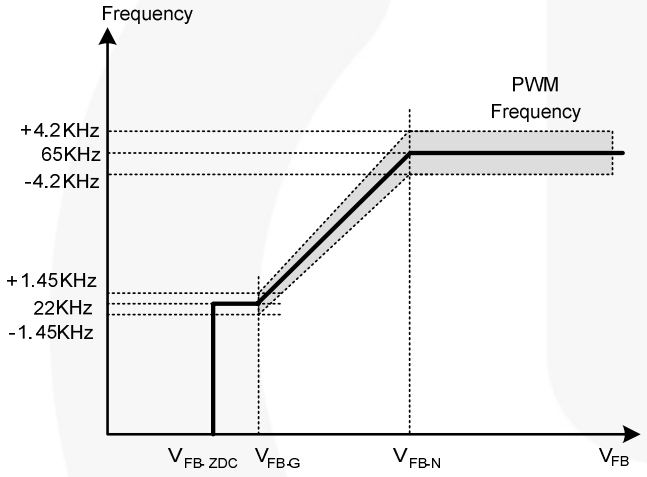

Figure 7. Frequency Modulation

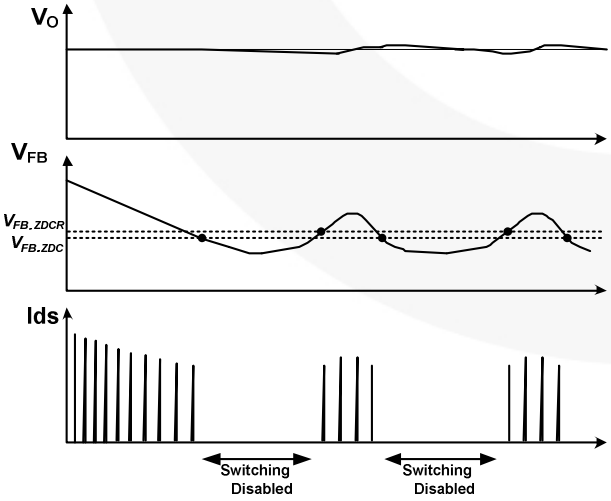

Figure 8. Burst Mode

FB Input

The FAN6754A employs peak-current-mode control as shown in Figure 9. A current-to-voltage conversion is accomplished externally with current-sense resistor R_{CS}.

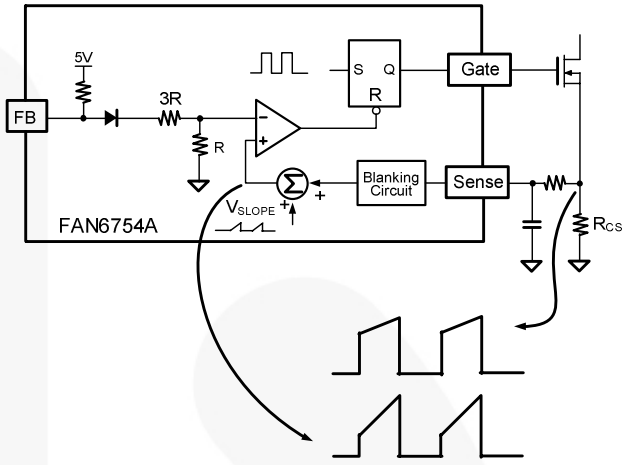

Figure 9. Synchronized Slope Compensation

Figure 10 is a typical feedback circuit mainly consisting of a shunt regulator and an opto-coupler. R1 and R2 form a voltage divider for output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}=10Ω, C_{FB}=1nF) placed between the FB pin and GND pin can increase loop stability substantially. The maximum source current of the FB pin is about 330μA (FB through 15kΩ pulled to 5V reference internally). The phototransistor must be capable of sinking this current to pull the FB level down at no-load condition. Rb and the internal FB pull-up resistor determines the gain feedback loop. The internal pull-up resistor in the SG6742 is 5kΩ, but the FAN6754A has a larger pull-up resistor (15kΩ) to reduce power consumption. Therefore, Rb should be three times the original value when a SG6742 design is replaced with the FAN6754A to have the same loop gain.

Forcing FB by an external voltage is not recommended.

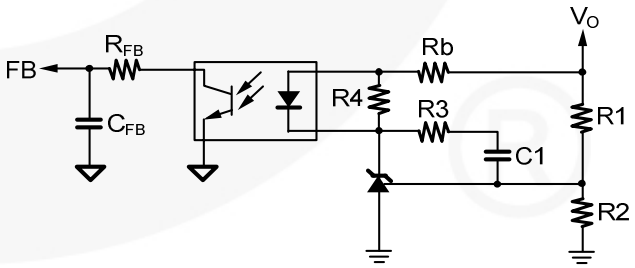

Figure 10. Feedback Circuit

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sense-resistor, R_S in Figure 11, caused by primary-side capacitance and secondary-side rectifier reverse recovery. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period (280ns), the PWM comparator is disabled and cannot switch off the gate driver. Thus, RC filter with a small RC time constant (e.g. 100Ω + 470pF) is enough for current sensing. A non-inductive resistor for R_S is recommended.

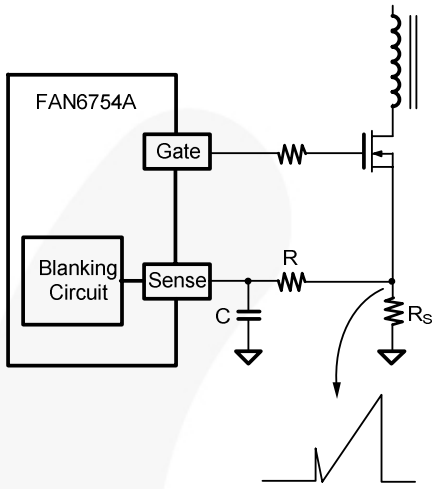

Figure 11. Turn-On Spike

Output Driver / Soft Driving

The output stage is a fast totem-pole gate driver capable of directly driving external MOSFETs. An internal Zener diode, shown in Figure 12, clamps the driver voltage under 13V to protect the MOSFET gate from over voltage. With integrating circuits to control the slew rate of the switch turn-on rise time, the external resistor R_G may not be necessary to reduce switching noise.

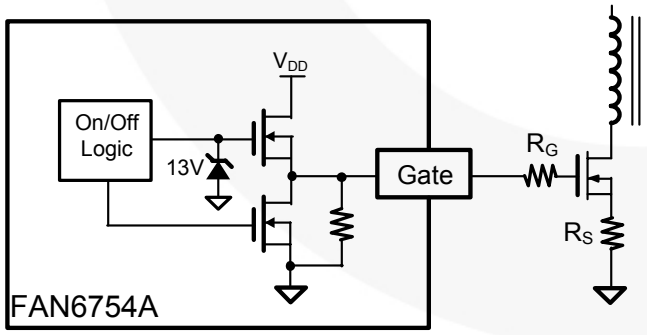

Figure 12. Gate Driver

High/Low Line Compensation in HV Pin

The conventional pulse-by-pulse current limiting scheme has a constant threshold for the current-limit comparator, which results in a higher power limit for high line voltage. The FAN6754A has a current-limit threshold that decreases as line voltage increases to makes the actual power limit level almost constant over different line voltages within a universal input voltage range, as shown in Figure 13. In the FAN6754A, the peak-current limiting threshold is adjusted by the peak voltage of the HV pin. When the internal circuit detailed in Figure 14 samples the line voltage information, an internal 1.62kΩ resistor is connected to the HV pin to scale down the line voltage by forming a voltage divider with resistor R_{HV} and the internal resistor.

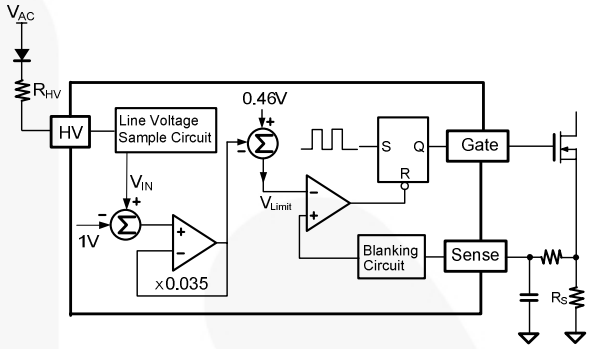

Figure 13. Universal Line Voltage Compensation for Constant Output Power Limit

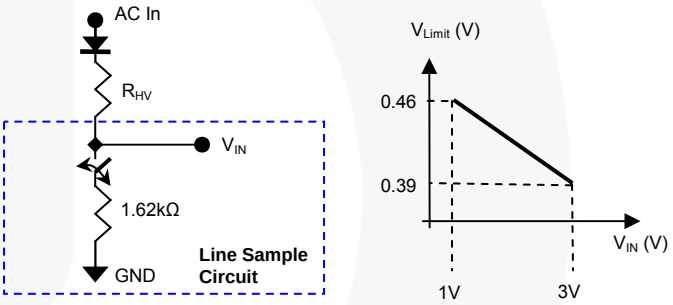

Figure 14. HV Sampling Circuit and V_{Limit} Level vs. V_{IN}

Brownout Protection in HV Pin

As shown in Figure 15, the AC line voltage is monitored by the HV pin using a resistor (R_{HV}), a diode (D_1), and an internal line voltage sample circuit. Figure 16 shows brownout protection behavior when the circuit uses the half-wave of the AC line input (V_{HV}) at the HV pin. When the V_{HV} is larger than the brown-in detection voltage threshold ($V_{AC\text{-}ON}$) and V_{DD} is higher than $V_{DD\text{-}AC}$, the PWM begins to operate without any debounce time. Meanwhile, the PWM stops operating when V_{HV} is less than the detection voltage threshold ($V_{AC\text{-}OFF}$) for longer than debounce time.

The $V_{AC\text{-}ON}$ and $V_{AC\text{-}OFF}$ are calculated using the following equations:

$$V_{AC\text{-}ON}(RMS) = (0.9 \times \frac{R_{HV} + 1.6}{1.6}) / \sqrt{2} \quad (1)$$

$$V_{AC\text{-}OFF}(\text{RMS}) = (0.81 \times \frac{R_{HV} + 1.6}{1.6}) / \sqrt{2} \text{ or where } R_{HV} \text{ is in k}\Omega. \quad (2)$$

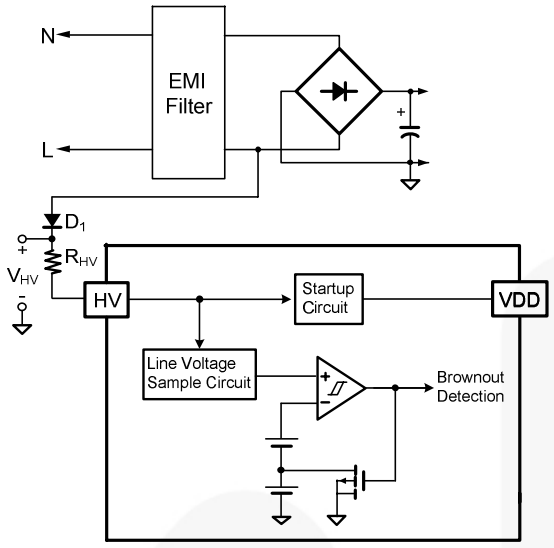

Figure 15. Brownout Circuit

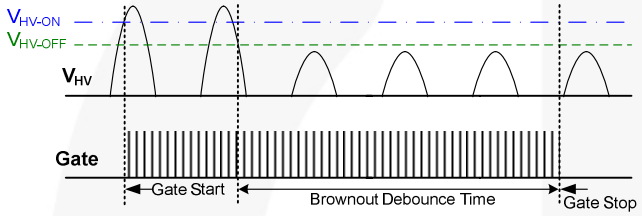

Figure 16. Brownout Protection Behavior

Overload / Open-Loop Protection (OLP)

When output is overloaded, the drain current reaches its pulse-by-pulse current limit level, limiting the input power. Then, the output voltage drops and no current flows through the opto-diode, which causes the feedback voltage to increase above the OLP protection threshold (4.6V). A similar response occurs when the feedback loop is open and no current flows through the opto-diode.

When the feedback voltage is higher than 4.6V for longer than the OLP delay time, the OLP protection is triggered, as shown in Figure 17.

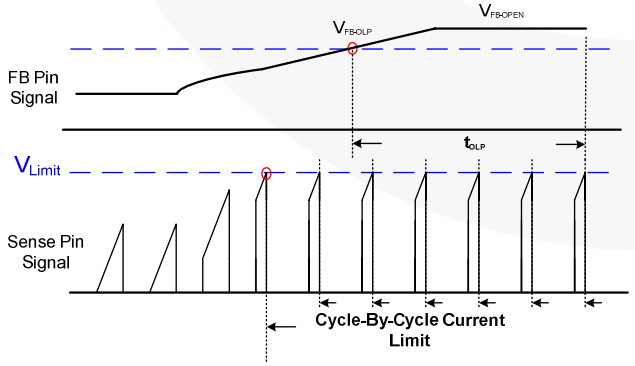

Figure 17. OLP Behavior

V_{DD} Over-Voltage Protection (V_{DD_OVP})

V_{DD} over-voltage protection protects the V_{DD} pin from damage from over-voltage. The V_{DD} voltage rises when an open-feedback loop failure occurs. Once the V_{DD} voltage exceeds 25V (V_{DD-OVP}) for longer than 165µs, the power supply is latched off until V_{DD} is discharged below V_{DD-LH}.

Sense Pin Short-Circuit Protection (SSCP)

This protection is used for Limited Power Source (LPS) safety testing. This test is performed with R_{SENSE} shorted to ground, thus increasing the output power. If the output voltage rating is set to 19V, this protection should be triggered before the output wattage increases to 100W.

Figure 18 shows this detection method. When R_{SENSE} is shorted to ground, the FAN6754A detects the voltage on the SENSE pin during the gate's on time. After debounce time, the gate turns off and V_{DD} goes into hiccup mode.

The sense resistor short-circuit protection is triggered if all of the following occur:

- gate is in a HIGH state; and
- the on-time of gate; $t_{ON-SSCP}$ is over 4.4µs and V_{SENCE}< 50mV; and
- during the debounce time of 120µs, if all pulse conditions are as above or the SSCP counter is reset.

Because of the fixed gate's on-time checking, the peak current of the inductor is different between high line and low line. The FAN6754A sets V_{SENSE} detection levels for all input voltage ranges.

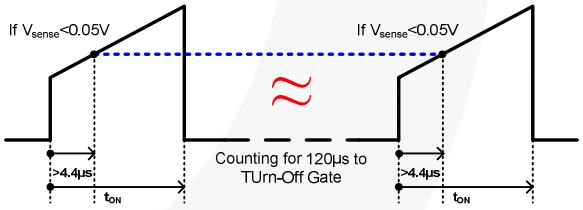

Figure 18. SSCP Detection Method

To prevent miss-triggered protection in normal mode (R_{SENSE} not shorted to ground); especially at lower AC line input voltages and light-load conditions, the transformer's inductance should not be too high in inductance.

The following is a design example;

(1) If the R_{HV} is 200KΩ, the brownout voltage should be $80V_{AC}$; assume the ripple is 15V at light-load condition.
(2) R_{SENSE} is 0.15Ω, and has ±5% tolerance.
(3) The minimum specification of $t_{ON-SSCP}$ is 4µs from the datasheet.
(4) The maximum specification of V_{SSCP-L} is 70mV from the datasheet.

The maximum primary-side inductance of the transformer should be:

$$L_{max} = \frac{(V_{Brownout\_min}) \times t_{ON-SSCP(min)} \times R_{SENSE(min)}}{V_{SSCP-L(max)}} = \frac{(80V \times \sqrt{2} - 15V) \times 4\mu s \times 0.1425\Omega}{70mV} = 799\mu H \quad (3)$$

In general, the manufacturing tolerance of the transformer has ±10%, the system designer should consider this tolerance; don't allow a maximum value over 799µH for this case.

In the FAN6754A, there are two conditions that trigger SSCP in system applications as show below.

(1) Power off on low line input with a heavy load.
If power off during a low input voltage line during a heavy load, then the FAN6754A will trigger the SSCP function as shown in 0 and Figure 1. (SSCP function is re-start behavior.)

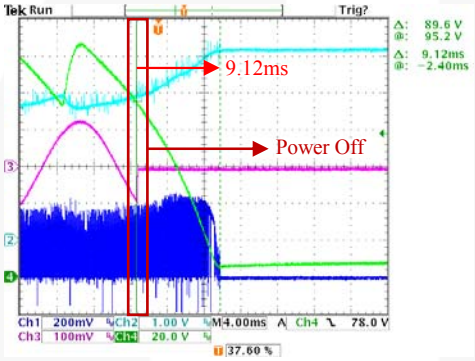

Figure 19.Power Off on 90V$_{AC}$ with Heavy Load (Zoom Out - Ch1:Sense Ch2: FB Ch3:AC Ch4:Bulk)

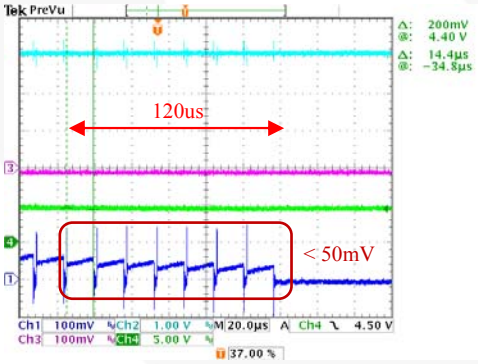

Figure 20. Power Off on 90V$_{AC}$ with Heavy Load (Zoom In - Ch1:Sense Ch2: FB Ch3:AC Ch4:Bulk)

(2) During an AC DIP, wh$_{en}$ the AC DIP cycle is over 30ms (1½ cycle) for 100% drop.
If the bulk voltage slowly droops, the inductor's current slope flattens as shown in Equation 4, this condition triggers the SSCP function. Even when the AC DIP is released, the gate stops going HIGH and V_{DD} restarts again.

$$\frac{V_{Bulk}}{L_P} = \frac{di_L}{dt} \quad (4)$$

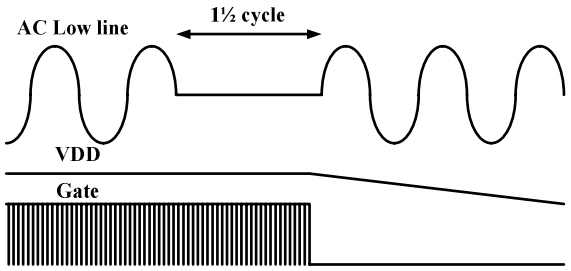

Figure 21. 1½ AC Cycle DIP Test

Thermal Protection

A constant current source I_{RT} (100µA) is connected to the RT pin for over-temperature protection, *(reference Figure 22.)* A NTC thermistor R_{NTC}, in series with resistor R_A, is typically connected between the RT pin and the GND pin. When V_{RT} is less than 1.035V (V_{RTTH1}) and larger than 0.7V, the PWM is disabled after the debounce time $t_{D-OTP-1}$. If V_{RT} is less than 0.7V (V_{RTTH2}), the PWM output is latched off after a very short debounce time of $t_{D-OTP-2}$. This function is used for external protection.

If this thermal protection design is not used, connect a small capacitor (around 0.47nF is recommended) between the RT pin and the GND pin to prevent noise interference. The RT capacitor cannot be larger than 1nF or, thermal protection is triggered during startup. If the RT pin is not connected to a NTC resistor to implement over-temperature protection, add an in-series 100KΩ resistor to ground to prevent noise interference. This pin is limited by internal clamping circuit.

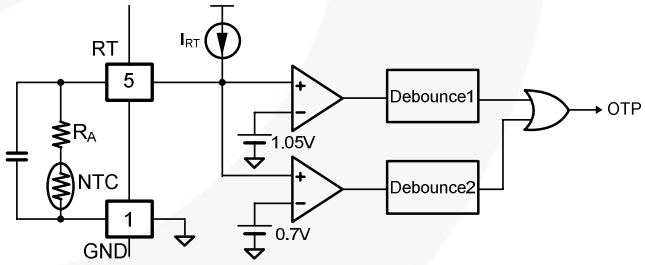

Figure 22. Thermal Protection Circuit

Lab Note

Before rework or solder/de-solder on the power supply, discharge the bulk capacitors in the primary side by an external bleeding resistor. Otherwise, the PWM IC may be damaged by external high voltage during solder/de-solder.

This device is sensitive to ESD discharge. To improve production yield, the production line should be ESD protected according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board (PCB) Layout

High-frequency switching current / voltage makes PCB layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge / ESD tests.

Guidelines:

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier shown in Figure 23 should be connected to capacitor C1 first, then to the switching circuits.
- The high-frequency current loop is in **C1 – Transformer – MOSFET – R_S – C1**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High-voltage traces related to the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, connect this heatsink to ground.
- As indicated by 3, the ground of control circuits should be connected first, then to other circuitry.
- As indicated by 2, the area enclosed by **transformer auxiliary winding, D1, C2, D2, and C3** should also be kept small. Place C3 close to the FAN6754A for good decoupling.

Two suggestions with different pro and cons for ground connections are offered:

- GND3 → 2 → 4 → 1: This could avoid common impedance interference for sense signal.
- GND3→2→1→4: This could be better for ESD testing where the earth ground is not available on the power supply. Regarding the ESD discharge path, the charges go from secondary through the transformer stray capacitance to GND2 first. The charges then go from GND2 to GND1 and back to the mains. Control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and increase ESD immunity.
- Should a Y-cap between primary and secondary be required, connect this Y-cap to the **positive terminal of C1**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of C1 (GND1)** directly. Point discharge of this Y-cap helps ESD. However, the creepage between these two pointed ends should be large enough to satisfy the requirements of applicable standards.

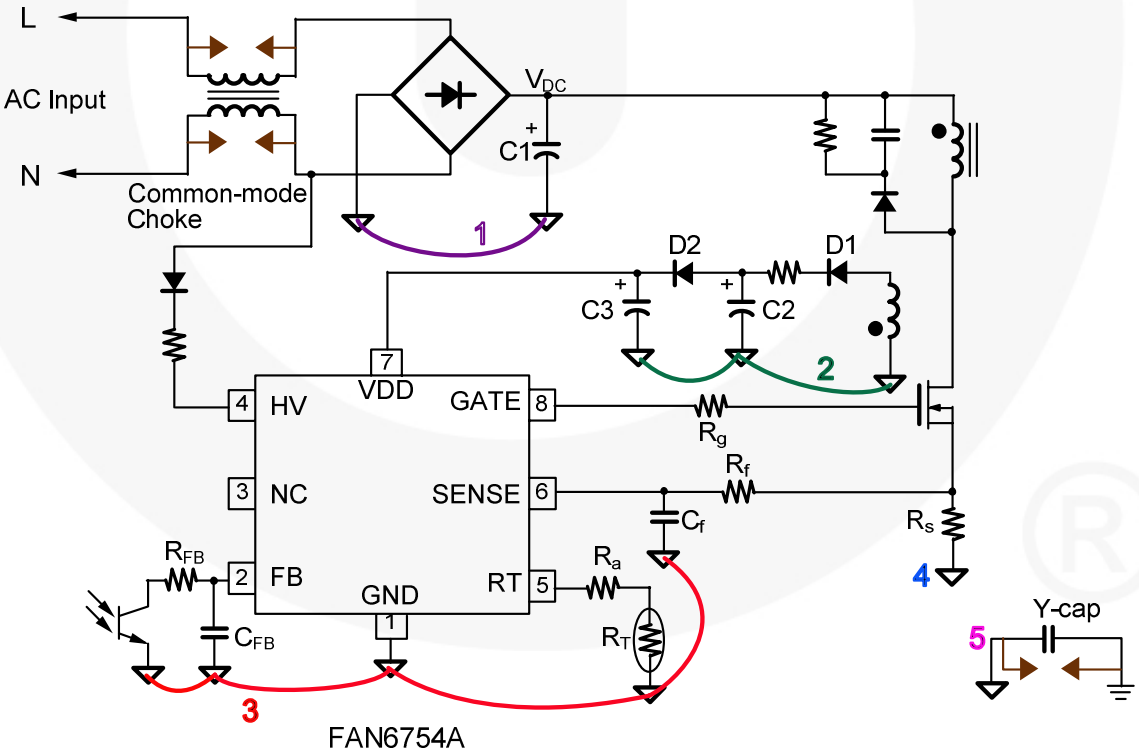

Figure 23. Layout Considerations

Related Datasheets

FAN6754A — Highly Integrated Green-Mode PWM Controller (Brownout and Constant Power Limited by HV Pin)