Am29LV652D

Data Sheet

RETIRED PRODUCT

This product has been retired and is not recommended for designs. For new designs, S29GL128N supersedes Am29LV652D. Please refer to the S29GL-N family data sheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

The following document contains information on Spansion memory products.

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary.

For More Information

Please contact your local sales office for additional information about Spansion memory solutions.

Publication Number 24961 **Revision** E **Amendment** 5 **Issue Date** May 5, 2006

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DATA SHEET

Am29LV652D

128 Megabit (16 M x 8-Bit) CMOS 3.0 Volt-only Uniform Sector Flash Memory with VersatileIO™ Control

This product has been retired and is not recommended for designs. For new designs, S29GL128N supersedes Am29LV652D. Please refer to the S29GL-N family data sheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

DISTINCTIVE CHARACTERISTICS

- **Two 64 Megabit (Am29LV065D) in a single 63-ball 11 x 12 mm FBGA package (Note: Features will be described for each internal Am29LV065D)**
- **Two Chip Enable inputs**
  - Each CE# controls selection of one internal Am29LV065D device
- **Single power supply operation**
  - 3.0 to 3.6 volt read, erase, and program operations
- **VersatileIO™ control**
  - Device generates output voltages and tolerates input voltages on DQ I/Os as determined by the voltage on V_{IO} input
- **High performance**
  - Access times as fast as 90 ns
- **Manufactured on 0.23 µm process technology**
- **CFI (Common Flash Interface) compliant**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Ultra low power consumption (typical values at 3.0 V, 5 MHz) for the part**
  - 9 mA typical active read current
  - 26 mA typical erase/program current
  - 400 nA typical standby mode current
- **Flexible sector architecture**
  - Two hundred fifty-six 64 Kbyte sectors
- **Sector Protection**
  - A hardware method to lock a sector to prevent program or erase operations within that sector
  - Sectors can be locked in-system or via programming equipment
  - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Embedded Algorithms**
  - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Compatibility with JEDEC standards**
  - Except for the added CE2#, the FBGA is pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection
- **Minimum 1 million erase cycle guarantee per sector**
- **63-ball FBGA Package**
- **Erase Suspend/Erase Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program or erase operation completion
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Ready/Busy# output (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Hardware reset input (RESET#)**
  - Hardware method to reset the device for reading array data
- **ACC input**
  - Accelerates programming time for higher throughput during system production
- **Program and Erase Performance (V_{HH} not applied to the ACC input)**
  - Byte program time: 5 µs typical
  - Sector erase time: 1.6 s typical for each 64 Kbyte sector
- **20-year data retention at 125°C**
  - Reliable operation for the life of the system

This Data Sheet states AMD's current technical specifications regarding the Products described herein. This Data Sheet may be revised by subsequent versions or modifications due to changes in technical specifications.

Publication# **24961** Rev: **A** Amendment: **5**
Issue Date: **May 5, 2006**

GENERAL DESCRIPTION

The Am29LV652D is a 128 Mbit, 3.0 Volt (3.0 V to 3.6 V) single power supply flash memory device organized as two Am29LV065D dice in a single 63-ball FBGA package. Each Am29LV065D is a 64 Mbit, 3.0 Volt (3.0 V to 3.6 V) single power supply flash memory device organized as 8,388,608 bytes. Data appears on DQ0-DQ7. The device is designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. A 12.0 volt V_{PP} is not required for program or erase operations. The Am29LV652D is equipped with two CE#s for flexible selection between the two internal 64 Mb devices. The device can also be programmed in standard EPROM programmers.

The Am29LV652D offers access times of 90 and 120 ns and is offered in a 63-ball FBGA package. To eliminate bus contention the Am29LV652D device contains two separate chip enables (CE# and CE2#). Each chip enable (CE# or CE2#) is connected to only one of the two dice in the Am29LV652D package. **To the system, this device is the same as two independent Am29LV065D on the same board. The only difference is that they are now packaged together to reduce board space.**

Each device requires only a **single 3.0 Volt power supply** (3.0 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The **VersatileI/O™** (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on V_{IO}. This allows the device to operate in a 3 V or 5 V system environment as required. For voltage levels below 3 V, contact an AMD representative for more information.

The host system can detect whether a program or erase operation is complete by observing RY/BY#, by reading the DQ7 (Data# Polling), or DQ6 (toggle) **status bits**. After a program or erase cycle is completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET#** terminates any operation in progress and resets the internal state machine to reading array data. RESET# may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The device offers a **standby mode** as a power-saving feature. Once the system places the device into the standby mode power consumption is greatly reduced.

The **accelerated program (ACC)** feature allows the system to program the device at a much faster rate. When ACC is pulled high to V_{HH}, the device enters the Unlock Bypass mode, enabling the user to reduce the time needed to do the program operation. This feature is intended to increase factory throughput during system production, but may also be used in the field if desired.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunnelling. The data is programmed using hot electron injection.

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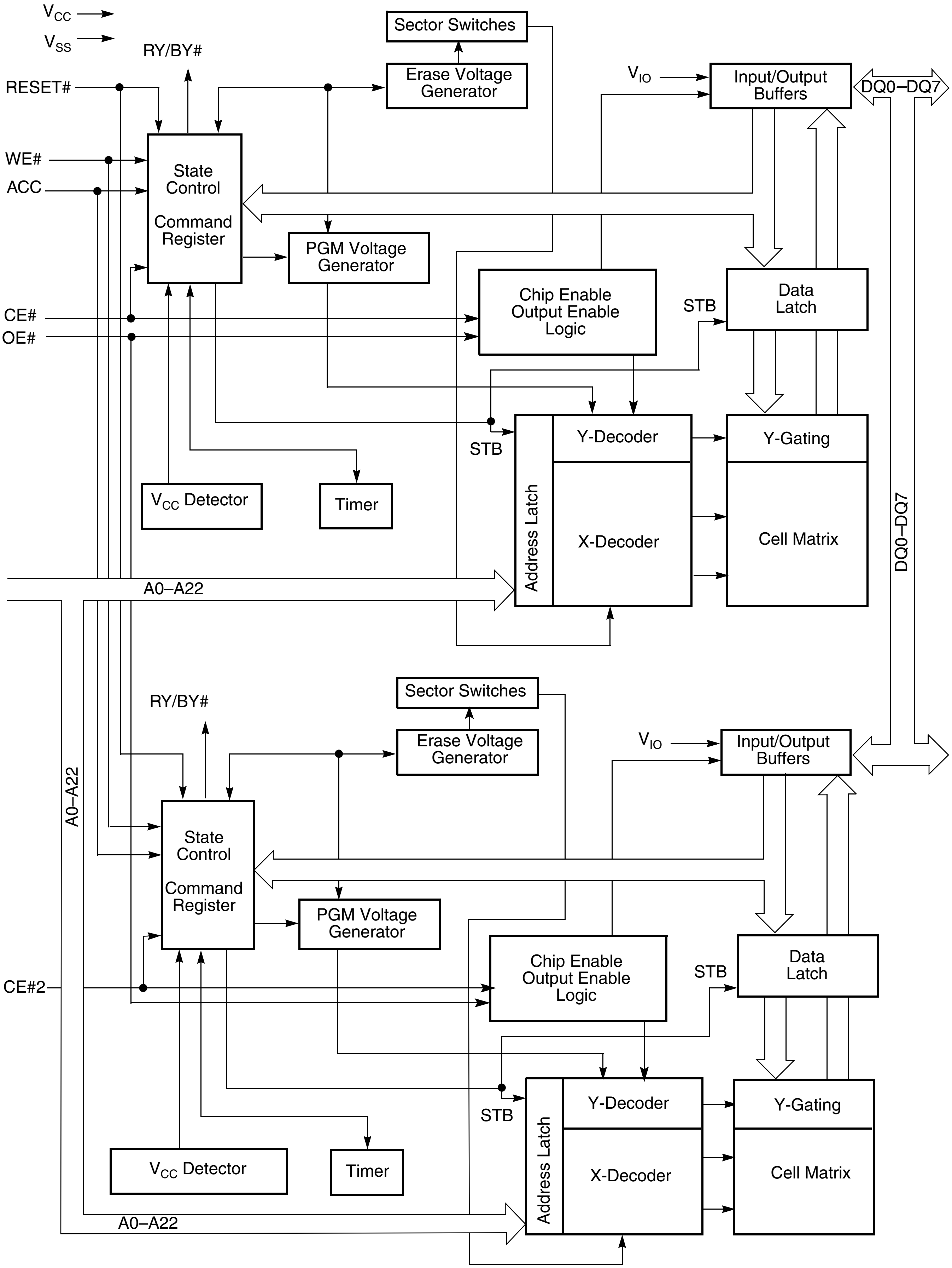
PRODUCT SELECTOR GUIDE

Part Number		Am29LV652D	
Speed Option	Regulated Voltage Range: V_{CC} = 3.0–3.6 V	**90R**	**12R**
Max Access Time (ns)		90	120
CE# Access Time (ns)		90	120
OE# Access Time (ns)		35	50

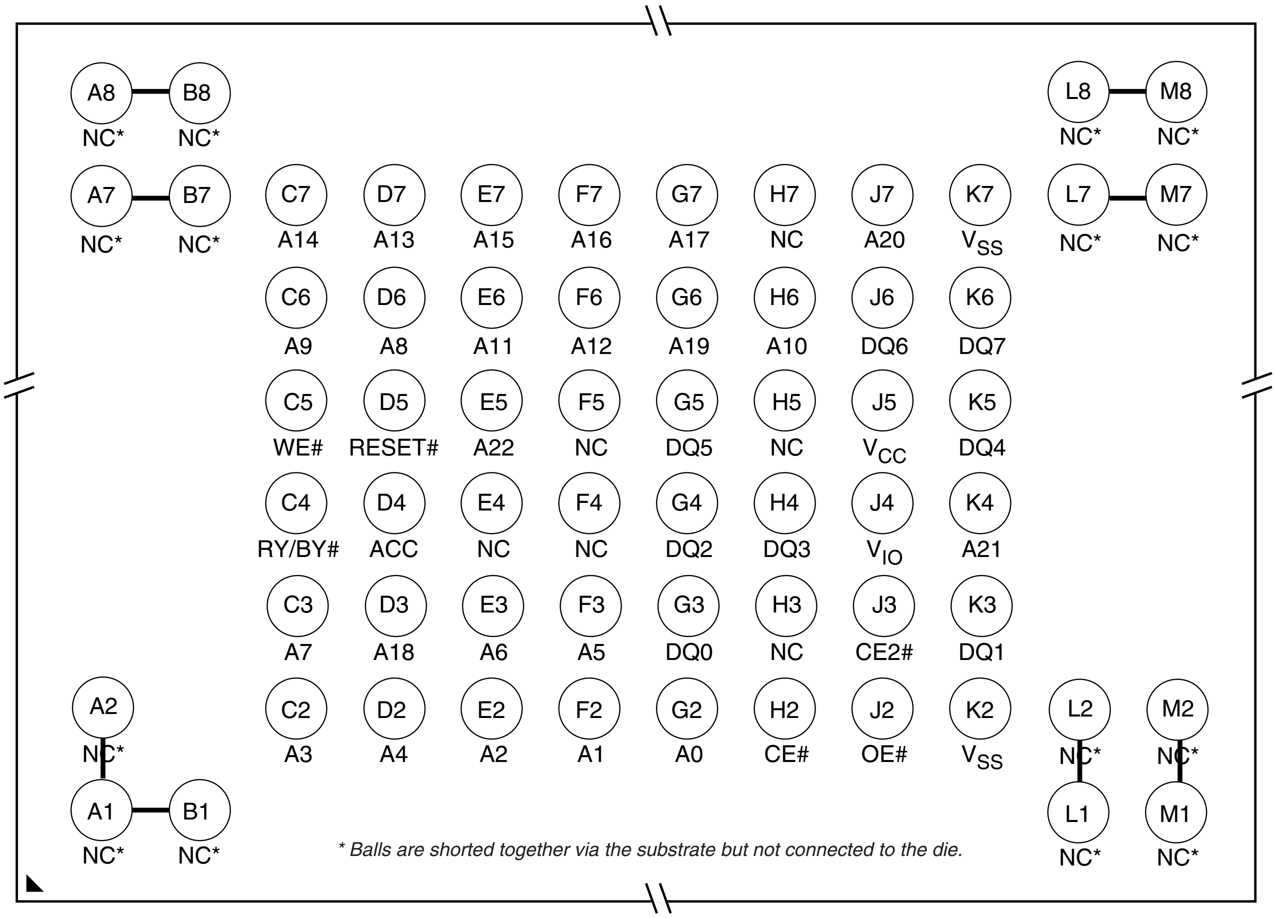
Note: *See* *“AC Characteristics” on page 39* *for full specifications.*

BLOCK DIAGRAM



CONNECTION DIAGRAM

63-Ball FBGA
Top View, Balls Facing Down



Special Handling Instructions for FBGA Package

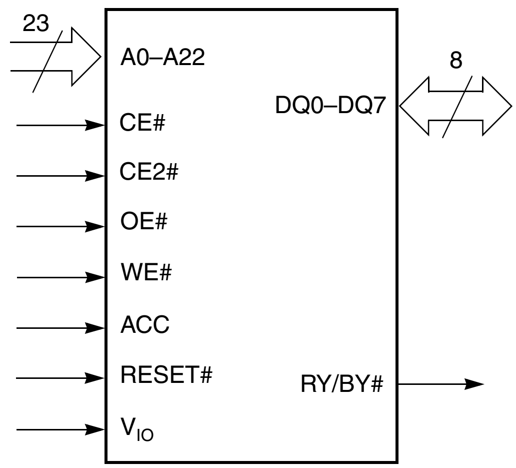
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A0–A22	=	23 Addresses inputs
DQ0–DQ7	=	8 Data inputs/outputs
CE#	=	Chip Enable input
CE2#	=	Chip Enable input for second die
OE#	=	Output Enable input
WE#	=	Write Enable input
ACC	=	Acceleration Input
RESET#	=	Hardware Reset Pin input
RY/BY#	=	Ready/Busy output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{IO}	=	Output Buffer power
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29LV652D U 90R MA I

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)
F = Industrial (-40°C to +85°C) with Pb-free Package
K = Extended (-55°C to +125°C) with Pb-free Package

PACKAGE TYPE
MA = 63-Ball Fine-Pitch Ball Grid Array (FBGA)
0.80 mm pitch, 11 x 12 mm package (FSA063)

SPEED OPTION
See Product Selector Guide and Valid Combinations

SECTOR ARCHITECTURE
U = Uniform sector device

DEVICE NUMBER/DESCRIPTION
Am29LV652D
128 Megabit (2 x 8 M x 8-Bit) CMOS Uniform Sector Flash Memory with VersatileIO™ Control
3.0 Volt-only Read, Program, and Erase

Valid Combinations for FBGA Packages				Speed/ V_{IO} Range
Order Number		Package Marking		
Am29LV652DU90R	MAF, MAI	L652DU90R	F, I	90 ns, V_{IO} = 3.0 V – 5.0 V
Am29LV652DU12R	MAI, MAE MAF, MAK	L652DU12R	I, E, F, K	120 ns, V_{IO} = 3.0 V – 5.0 V

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29LV652D Device Bus Operations

Operation	CE# (Note 1)	OE#	WE#	RESET#	ACC	Addresses (Note 2)	DQ0–DQ7
Read	L	L	H	H	X	A_{IN}	D_{OUT}
Write (Program/Erase)	L	H	L	H	X	A_{IN}	(Note 3)
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 3)
Standby	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V	H	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z
Reset	X	X	X	L	X	X	High-Z
Sector Group Protect (Note 4)	L	H	L	V_{ID}	X	SA, A6 = L, A1 = H, A0 = L	(Note 3)
Sector Group Unprotect (Note 4)	L	H	L	V_{ID}	X	SA, A6 = H, A1 = H, A0 = L	(Note 3)
Temporary Sector Group Unprotect	X	X	X	V_{ID}	X	A_{IN}	(Note 3)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 8.5–12.5 V, V_{HH} = 11.5–12.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *CE# can be replaced with CE2# when referring to the second die in the package. CE# and CE2# must not both be driven at the same time.*
2. *Addresses are A22:A0. Sector addresses are A22:A16.*
3. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 2).*
4. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Unprotection" section.*
5. *All sectors are unprotected when shipped from the factory.*

VersatileIO™ (V_{IO}) Control

The VersatileIO (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on V_{IO}. This allows the device to operate in a 3 V or 5 V system environment as required. For voltage levels below 3 V, contact an AMD representative for more information.

For example, a $V_{I/O}$ of 4.5–5.0 volts allows for I/O at the 5 volt level, driving and receiving signals to and from other 5 V devices on the same data bus.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive CE# or CE2# and OE# to V_{IL}. CE# or CE2# is the power control and selects the device. OE# is the output control and gates array data to the outputs. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "VersatileIO‰ (VIO) Control" for more information. Refer to the AC "Read-Only Operations" on page 39 table for timing specifications and to Figure 13, on page 39 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# (or CE2#) to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a byte, instead of four. The "Byte Program Command Sequence" on page 26 section contains details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2, on page 11 indicates the address space that each sector occupies.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput during system production.

If the system asserts V_{HH} on ACC, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from ACC returns the device to normal operation. *Note that ACC must not be at V_{HH} for operations other than accelerated programming, or device damage may result.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" on page 19 and "Autoselect Command Sequence" on page 26 sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE#, CE2#, and RESET# are all held at V_{CC} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE#, CE2#, and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3 V, the device is in the standby mode, but the standby current is greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics (for two Am29LV065 devices) table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, CE2#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics (for two Am29LV065 devices) table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

RESET# provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS} ± 0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL}, but not within V_{SS} ± 0.3 V, the standby current is greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, RY/BY# remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after RESET# returns to V_{IH}.

Refer to the “AC Characteristics” on page 39 tables for RESET# parameters and to Figure 14, on page 40 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

Table 2. Sector Address Table for CE# (Sheet 1 of 4)

Sector	A22	A21	A20	A19	A18	A17	A16	8-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	000000–00FFFF
SA1	0	0	0	0	0	0	1	010000–01FFFF
SA2	0	0	0	0	0	1	0	020000–02FFFF
SA3	0	0	0	0	0	1	1	030000–03FFFF
SA4	0	0	0	0	1	0	0	040000–04FFFF
SA5	0	0	0	0	1	0	1	050000–05FFFF
SA6	0	0	0	0	1	1	0	060000–06FFFF
SA7	0	0	0	0	1	1	1	070000–07FFFF
SA8	0	0	0	1	0	0	0	080000–08FFFF
SA9	0	0	0	1	0	0	1	090000–09FFFF
SA10	0	0	0	1	0	1	0	0A0000–0AFFFF
SA11	0	0	0	1	0	1	1	0B0000–0BFFFF
SA12	0	0	0	1	1	0	0	0C0000–0CFFFF
SA13	0	0	0	1	1	0	1	0D0000–0DFFFF
SA14	0	0	0	1	1	1	0	0E0000–0EFFFF
SA15	0	0	0	1	1	1	1	0F0000–0FFFFF
SA16	0	0	1	0	0	0	0	100000–10FFFF
SA17	0	0	1	0	0	0	1	110000–11FFFF
SA18	0	0	1	0	0	1	0	120000–12FFFF
SA19	0	0	1	0	0	1	1	130000–13FFFF
SA20	0	0	1	0	1	0	0	140000–14FFFF
SA21	0	0	1	0	1	0	1	150000–15FFFF
SA22	0	0	1	0	1	1	0	160000–16FFFF
SA23	0	0	1	0	1	1	1	170000–17FFFF
SA24	0	0	1	1	0	0	0	180000–18FFFF
SA25	0	0	1	1	0	0	1	190000–19FFFF
SA26	0	0	1	1	0	1	0	1A0000–1AFFFF

Table 2. Sector Address Table for CE# (Sheet 2 of 4)

Sector	A22	A21	A20	A19	A18	A17	A16	8-bit Address Range (in hexadecimal)
SA27	0	0	1	1	0	1	1	1B0000–1BFFFF
SA28	0	0	1	1	1	0	0	1C0000–1CFFFF
SA29	0	0	1	1	1	0	1	1D0000–1DFFFF
SA30	0	0	1	1	1	1	0	1E0000–1EFFFF
SA31	0	0	1	1	1	1	1	1F0000–1FFFFF
SA32	0	1	0	0	0	0	0	200000–20FFFF
SA33	0	1	0	0	0	0	1	210000–21FFFF
SA34	0	1	0	0	0	1	0	220000–22FFFF
SA35	0	1	0	0	0	1	1	230000–23FFFF
SA36	0	1	0	0	1	0	0	240000–24FFFF
SA37	0	1	0	0	1	0	1	250000–25FFFF
SA38	0	1	0	0	1	1	0	260000–26FFFF
SA39	0	1	0	0	1	1	1	270000–27FFFF
SA40	0	1	0	1	0	0	0	280000–28FFFF
SA41	0	1	0	1	0	0	1	290000–29FFFF
SA42	0	1	0	1	0	1	0	2A0000–2AFFFF
SA43	0	1	0	1	0	1	1	2B0000–2BFFFF
SA44	0	1	0	1	1	0	0	2C0000–2CFFFF
SA45	0	1	0	1	1	0	1	2D0000–2DFFFF
SA46	0	1	0	1	1	1	0	2E0000–2EFFFF
SA47	0	1	0	1	1	1	1	2F0000–2FFFFF
SA48	0	1	1	0	0	0	0	300000–30FFFF
SA49	0	1	1	0	0	0	1	310000–31FFFF
SA50	0	1	1	0	0	1	0	320000–32FFFF
SA51	0	1	1	0	0	1	1	330000–33FFFF
SA52	0	1	1	0	1	0	0	340000–34FFFF
SA53	0	1	1	0	1	0	1	350000–35FFFF
SA54	0	1	1	0	1	1	0	360000–36FFFF
SA55	0	1	1	0	1	1	1	370000–37FFFF
SA56	0	1	1	1	0	0	0	380000–38FFFF
SA57	0	1	1	1	0	0	1	390000–39FFFF
SA58	0	1	1	1	0	1	0	3A0000–3AFFFF
SA59	0	1	1	1	0	1	1	3B0000–3BFFFF
SA60	0	1	1	1	1	0	0	3C0000–3CFFFF
SA61	0	1	1	1	1	0	1	3D0000–3DFFFF

Table 2. Sector Address Table for CE# (Sheet 3 of 4)

Sector	A22	A21	A20	A19	A18	A17	A16	8-bit Address Range (in hexadecimal)
SA62	0	1	1	1	1	1	0	3E0000–3EFFFF
SA63	0	1	1	1	1	1	1	3F0000–3FFFFF
SA64	1	0	0	0	0	0	0	400000–40FFFF
SA65	1	0	0	0	0	0	1	410000–41FFFF
SA66	1	0	0	0	0	1	0	420000–42FFFF
SA67	1	0	0	0	0	1	1	430000–43FFFF
SA68	1	0	0	0	1	0	0	440000–44FFFF
SA69	1	0	0	0	1	0	1	450000–45FFFF
SA70	1	0	0	0	1	1	0	460000–46FFFF
SA71	1	0	0	0	1	1	1	470000–47FFFF
SA72	1	0	0	1	0	0	0	480000–48FFFF
SA73	1	0	0	1	0	0	1	490000–49FFFF
SA74	1	0	0	1	0	1	0	4A0000–4AFFFF
SA75	1	0	0	1	0	1	1	4B0000–4BFFFF
SA76	1	0	0	1	1	0	0	4C0000–4CFFFF
SA77	1	0	0	1	1	0	1	4D0000–4DFFFF
SA78	1	0	0	1	1	1	0	4E0000–4EFFFF
SA79	1	0	0	1	1	1	1	4F0000–4FFFFF
SA80	1	0	1	0	0	0	0	500000–50FFFF
SA81	1	0	1	0	0	0	1	510000–51FFFF
SA82	1	0	1	0	0	1	0	520000–52FFFF
SA83	1	0	1	0	0	1	1	530000–53FFFF
SA84	1	0	1	0	1	0	0	540000–54FFFF
SA85	1	0	1	0	1	0	1	550000–55FFFF
SA86	1	0	1	0	1	1	0	560000–56FFFF
SA87	1	0	1	0	1	1	1	570000–57FFFF
SA88	1	0	1	1	0	0	0	580000–58FFFF
SA89	1	0	1	1	0	0	1	590000–59FFFF
SA90	1	0	1	1	0	1	0	5A0000–5AFFFF
SA91	1	0	1	1	0	1	1	5B0000–5BFFFF
SA92	1	0	1	1	1	0	0	5C0000–5CFFFF
SA93	1	0	1	1	1	0	1	5D0000–5DFFFF
SA94	1	0	1	1	1	1	0	5E0000–5EFFFF
SA95	1	0	1	1	1	1	1	5F0000–5FFFFF
SA96	1	1	0	0	0	0	0	600000–60FFFF

Table 2. Sector Address Table for CE# (Sheet 4 of 4)

Sector	A22	A21	A20	A19	A18	A17	A16	8-bit Address Range (in hexadecimal)
SA97	1	1	0	0	0	0	1	610000–61FFFF
SA98	1	1	0	0	0	1	0	620000–62FFFF
SA99	1	1	0	0	0	1	1	630000–63FFFF
SA100	1	1	0	0	1	0	0	640000–64FFFF
SA101	1	1	0	0	1	0	1	650000–65FFFF
SA102	1	1	0	0	1	1	0	660000–66FFFF
SA103	1	1	0	0	1	1	1	670000–67FFFF
SA104	1	1	0	1	0	0	0	680000–68FFFF
SA105	1	1	0	1	0	0	1	690000–69FFFF
SA106	1	1	0	1	0	1	0	6A0000–6AFFFF
SA107	1	1	0	1	0	1	1	6B0000–6BFFFF
SA108	1	1	0	1	1	0	0	6C0000–6CFFFF
SA109	1	1	0	1	1	0	1	6D0000–6DFFFF
SA110	1	1	0	1	1	1	0	6E0000–6EFFFF
SA111	1	1	0	1	1	1	1	6F0000–6FFFFF
SA112	1	1	1	0	0	0	0	700000–70FFFF
SA113	1	1	1	0	0	0	1	710000–71FFFF
SA114	1	1	1	0	0	1	0	720000–72FFFF
SA115	1	1	1	0	0	1	1	730000–73FFFF
SA116	1	1	1	0	1	0	0	740000–74FFFF
SA117	1	1	1	0	1	0	1	750000–75FFFF
SA118	1	1	1	0	1	1	0	760000–76FFFF
SA119	1	1	1	0	1	1	1	770000–77FFFF
SA120	1	1	1	1	0	0	0	780000–78FFFF
SA121	1	1	1	1	0	0	1	790000–79FFFF
SA122	1	1	1	1	0	1	0	7A0000–7AFFFF
SA123	1	1	1	1	0	1	1	7B0000–7BFFFF
SA124	1	1	1	1	1	0	0	7C0000–7CFFFF
SA125	1	1	1	1	1	0	1	7D0000–7DFFFF
SA126	1	1	1	1	1	1	0	7E0000–7EFFFF
SA127	1	1	1	1	1	1	1	7F0000–7FFFFF

Note: *All sectors are 64 Kbytes in size.*

Table 3. Sector Address Table for CE2# (Sheet 1 of 4)

Sector	A22	A21	A20	A19	A18	A17	A16	8-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	000000–00FFFF
SA1	0	0	0	0	0	0	1	010000–01FFFF
SA2	0	0	0	0	0	1	0	020000–02FFFF
SA3	0	0	0	0	0	1	1	030000–03FFFF
SA4	0	0	0	0	1	0	0	040000–04FFFF
SA5	0	0	0	0	1	0	1	050000–05FFFF
SA6	0	0	0	0	1	1	0	060000–06FFFF
SA7	0	0	0	0	1	1	1	070000–07FFFF
SA8	0	0	0	1	0	0	0	080000–08FFFF
SA9	0	0	0	1	0	0	1	090000–09FFFF
SA10	0	0	0	1	0	1	0	0A0000–0AFFFF
SA11	0	0	0	1	0	1	1	0B0000–0BFFFF
SA12	0	0	0	1	1	0	0	0C0000–0CFFFF
SA13	0	0	0	1	1	0	1	0D0000–0DFFFF
SA14	0	0	0	1	1	1	0	0E0000–0EFFFF
SA15	0	0	0	1	1	1	1	0F0000–0FFFFF
SA16	0	0	1	0	0	0	0	100000–10FFFF
SA17	0	0	1	0	0	0	1	110000–11FFFF
SA18	0	0	1	0	0	1	0	120000–12FFFF
SA19	0	0	1	0	0	1	1	130000–13FFFF
SA20	0	0	1	0	1	0	0	140000–14FFFF
SA21	0	0	1	0	1	0	1	150000–15FFFF
SA22	0	0	1	0	1	1	0	160000–16FFFF
SA23	0	0	1	0	1	1	1	170000–17FFFF
SA24	0	0	1	1	0	0	0	180000–18FFFF
SA25	0	0	1	1	0	0	1	190000–19FFFF
SA26	0	0	1	1	0	1	0	1A0000–1AFFFF
SA27	0	0	1	1	0	1	1	1B0000–1BFFFF
SA28	0	0	1	1	1	0	0	1C0000–1CFFFF
SA29	0	0	1	1	1	0	1	1D0000–1DFFFF
SA30	0	0	1	1	1	1	0	1E0000–1EFFFF
SA31	0	0	1	1	1	1	1	1F0000–1FFFFF
SA32	0	1	0	0	0	0	0	200000–20FFFF
SA33	0	1	0	0	0	0	1	210000–21FFFF

Table 3. Sector Address Table for CE2# (Sheet 2 of 4)

Sector	A22	A21	A20	A19	A18	A17	A16	8-bit Address Range (in hexadecimal)
SA34	0	1	0	0	0	1	0	220000–22FFFF
SA35	0	1	0	0	0	1	1	230000–23FFFF
SA36	0	1	0	0	1	0	0	240000–24FFFF
SA37	0	1	0	0	1	0	1	250000–25FFFF
SA38	0	1	0	0	1	1	0	260000–26FFFF
SA39	0	1	0	0	1	1	1	270000–27FFFF
SA40	0	1	0	1	0	0	0	280000–28FFFF
SA41	0	1	0	1	0	0	1	290000–29FFFF
SA42	0	1	0	1	0	1	0	2A0000–2AFFFF
SA43	0	1	0	1	0	1	1	2B0000–2BFFFF
SA44	0	1	0	1	1	0	0	2C0000–2CFFFF
SA45	0	1	0	1	1	0	1	2D0000–2DFFFF
SA46	0	1	0	1	1	1	0	2E0000–2EFFFF
SA47	0	1	0	1	1	1	1	2F0000–2FFFFF
SA48	0	1	1	0	0	0	0	300000–30FFFF
SA49	0	1	1	0	0	0	1	310000–31FFFF
SA50	0	1	1	0	0	1	0	320000–32FFFF
SA51	0	1	1	0	0	1	1	330000–33FFFF
SA52	0	1	1	0	1	0	0	340000–34FFFF
SA53	0	1	1	0	1	0	1	350000–35FFFF
SA54	0	1	1	0	1	1	0	360000–36FFFF
SA55	0	1	1	0	1	1	1	370000–37FFFF
SA56	0	1	1	1	0	0	0	380000–38FFFF
SA57	0	1	1	1	0	0	1	390000–39FFFF
SA58	0	1	1	1	0	1	0	3A0000–3AFFFF
SA59	0	1	1	1	0	1	1	3B0000–3BFFFF
SA60	0	1	1	1	1	0	0	3C0000–3CFFFF
SA61	0	1	1	1	1	0	1	3D0000–3DFFFF
SA62	0	1	1	1	1	1	0	3E0000–3EFFFF
SA63	0	1	1	1	1	1	1	3F0000–3FFFFF
SA64	1	0	0	0	0	0	0	400000–40FFFF
SA65	1	0	0	0	0	0	1	410000–41FFFF
SA66	1	0	0	0	0	1	0	420000–42FFFF
SA67	1	0	0	0	0	1	1	430000–43FFFF
SA68	1	0	0	0	1	0	0	440000–44FFFF

Table 3. Sector Address Table for CE2# (Sheet 3 of 4)

Sector	A22	A21	A20	A19	A18	A17	A16	8-bit Address Range (in hexadecimal)
SA69	1	0	0	0	1	0	1	450000–45FFFF
SA70	1	0	0	0	1	1	0	460000–46FFFF
SA71	1	0	0	0	1	1	1	470000–47FFFF
SA72	1	0	0	1	0	0	0	480000–48FFFF
SA73	1	0	0	1	0	0	1	490000–49FFFF
SA74	1	0	0	1	0	1	0	4A0000–4AFFFF
SA75	1	0	0	1	0	1	1	4B0000–4BFFFF
SA76	1	0	0	1	1	0	0	4C0000–4CFFFF
SA77	1	0	0	1	1	0	1	4D0000–4DFFFF
SA78	1	0	0	1	1	1	0	4E0000–4EFFFF
SA79	1	0	0	1	1	1	1	4F0000–4FFFFF
SA80	1	0	1	0	0	0	0	500000–50FFFF
SA81	1	0	1	0	0	0	1	510000–51FFFF
SA82	1	0	1	0	0	1	0	520000–52FFFF
SA83	1	0	1	0	0	1	1	530000–53FFFF
SA84	1	0	1	0	1	0	0	540000–54FFFF
SA85	1	0	1	0	1	0	1	550000–55FFFF
SA86	1	0	1	0	1	1	0	560000–56FFFF
SA87	1	0	1	0	1	1	1	570000–57FFFF
SA88	1	0	1	1	0	0	0	580000–58FFFF
SA89	1	0	1	1	0	0	1	590000–59FFFF
SA90	1	0	1	1	0	1	0	5A0000–5AFFFF
SA91	1	0	1	1	0	1	1	5B0000–5BFFFF
SA92	1	0	1	1	1	0	0	5C0000–5CFFFF
SA93	1	0	1	1	1	0	1	5D0000–5DFFFF
SA94	1	0	1	1	1	1	0	5E0000–5EFFFF
SA95	1	0	1	1	1	1	1	5F0000–5FFFFF
SA96	1	1	0	0	0	0	0	600000–60FFFF
SA97	1	1	0	0	0	0	1	610000–61FFFF
SA98	1	1	0	0	0	1	0	620000–62FFFF
SA99	1	1	0	0	0	1	1	630000–63FFFF
SA100	1	1	0	0	1	0	0	640000–64FFFF
SA101	1	1	0	0	1	0	1	650000–65FFFF
SA102	1	1	0	0	1	1	0	660000–66FFFF
SA103	1	1	0	0	1	1	1	670000–67FFFF

Table 3. Sector Address Table for CE2# (Sheet 4 of 4)

Sector	A22	A21	A20	A19	A18	A17	A16	8-bit Address Range (in hexadecimal)
SA104	1	1	0	1	0	0	0	680000–68FFFF
SA105	1	1	0	1	0	0	1	690000–69FFFF
SA106	1	1	0	1	0	1	0	6A0000–6AFFFF
SA107	1	1	0	1	0	1	1	6B0000–6BFFFF
SA108	1	1	0	1	1	0	0	6C0000–6CFFFF
SA109	1	1	0	1	1	0	1	6D0000–6DFFFF
SA110	1	1	0	1	1	1	0	6E0000–6EFFFF
SA111	1	1	0	1	1	1	1	6F0000–6FFFFF
SA112	1	1	1	0	0	0	0	700000–70FFFF
SA113	1	1	1	0	0	0	1	710000–71FFFF
SA114	1	1	1	0	0	1	0	720000–72FFFF
SA115	1	1	1	0	0	1	1	730000–73FFFF
SA116	1	1	1	0	1	0	0	740000–74FFFF
SA117	1	1	1	0	1	0	1	750000–75FFFF
SA118	1	1	1	0	1	1	0	760000–76FFFF
SA119	1	1	1	0	1	1	1	770000–77FFFF
SA120	1	1	1	1	0	0	0	780000–78FFFF
SA121	1	1	1	1	0	0	1	790000–79FFFF
SA122	1	1	1	1	0	1	0	7A0000–7AFFFF
SA123	1	1	1	1	0	1	1	7B0000–7BFFFF
SA124	1	1	1	1	1	0	0	7C0000–7CFFFF
SA125	1	1	1	1	1	0	1	7D0000–7DFFFF
SA126	1	1	1	1	1	1	0	7E0000–7EFFFF
SA127	1	1	1	1	1	1	1	7F0000–7FFFFF

Note: *All sectors are 64 Kbytes in size.*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (8.5 V to 12.5 V) on address A9. Addresses A6, A1, and A0 must be as shown in Table 4, on page 19. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 2, on page 11 and Table 3, on page 15). Table 4 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 10, on page 30. This method does not require V_{ID}. Refer to the "Autoselect Command Sequence" on page 26 section for more information.

Table 4. Am29LV652D Autoselect Codes, (High Voltage Method)

Description	CE#	OE#	WE#	A22 to A16	A15 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	L	X	L	L	01h
Device ID: Am29LV652D	L	L	H	X	X	V_{ID}	X	L	X	L	H	93h
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01h (protected), 00h (unprotected)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.*

Notes:

1. *CE# can be replaced with CE2# when referring to the second die in the package.*
2. *The device ID's used for the Am29LV652 are the same as the Am29LV065, because the Am29LV652 uses two Am29LV065 dice and appears to the system as two Am29LV065 devices.*

Sector Group Protection and Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Table 5). The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection can be implemented via two methods.

The primary method requires V_{ID} on RESET# only, and can be implemented either in-system or via programming equipment. Figure 2, on page 22 shows the algorithms and Figure 22, on page 47 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector group unprotect, all unprotected sector groups must first be protected prior to the first sector group unprotect write cycle.

Some earlier 3.0 volt-only AMD flash devices used a sector protection/unprotection method intended only for programming equipment, and required V_{ID} on address A9 and OE#. If this earlier method is required for the intended application, contact AMD for further details.

The device is shipped with all sector groups unprotected. AMD offers the option of programming and protecting sector groups at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector group is protected or unprotected. See the "Autoselect Mode" on page 19 section for details.

Table 5. Sector Group Protection/Unprotection Address Table

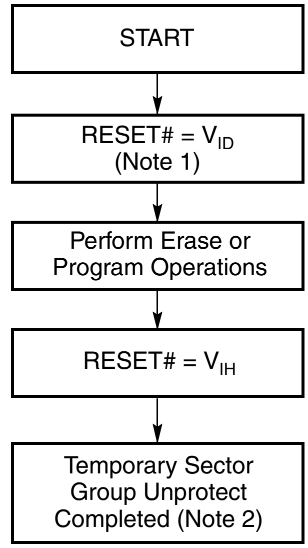
Sector Group	A22–A18
SA0–SA3	00000
SA4–SA7	00001
SA8–SA11	00010
SA12–SA15	00011
SA16–SA19	00100
SA20–SA23	00101
SA24–SA27	00110
SA28–SA31	00111
SA32–SA35	01000
SA36–SA39	01001
SA40–SA43	01010
SA44–SA47	01011
SA48–SA51	01100
SA52–SA55	01101
SA56–SA59	01110
SA60–SA63	01111
SA64–SA67	10000
SA68–SA71	10001
SA72–SA75	10010
SA76–SA79	10011
SA80–SA83	10100
SA84–SA87	10101
SA88–SA91	10110
SA92–SA95	10111
SA96–SA99	11000
SA100–SA103	11001
SA104–SA107	11010
SA108–SA111	11011
SA112–SA115	11100
SA116–SA119	11101
SA120–SA123	11110
SA124–SA127	11111

Note: *All sector groups are 256 Kbytes in size.*

Temporary Sector Group Unprotect

*(**Note:** In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Table 5, on page 20)).*

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting RESET# to V_{ID} (8.5 V – 12.5 V). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once V_{ID} is removed from RESET#, all the previously protected sector groups are protected again. Figure 1, on page 21 shows the algorithm, and Figure 21, on page 46 shows the timing diagrams, for this feature.



Notes:
1. *All protected sector groups unprotected.*
2. *All previously protected sector groups are protected once again.*

Figure 1. Temporary Sector Group Unprotect Operation

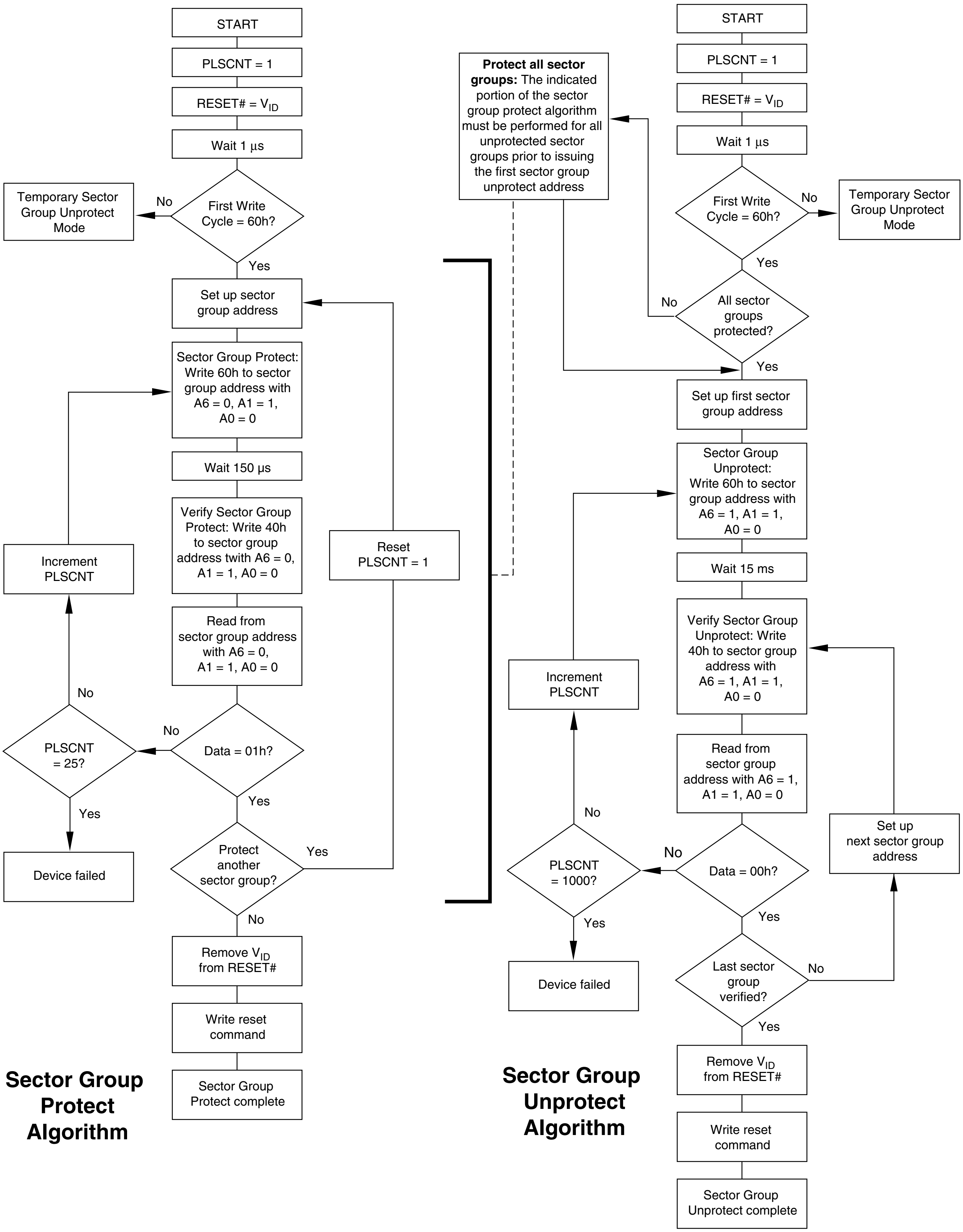


Figure 2. In-System Sector Group Protect/Unprotect Algorithms

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 10, on page 30 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE#, CE2#, or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH}, CE2# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# (or CE2#), and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = CE2# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

The Am29LV652 is a two die solution which appears as two 64 Mbit Am29LV065 devices in the system. This allows the same CFI information to be used because the system "sees" two 64 Mbit devices, not a single 128 Mbit device.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, any time the device is ready to read array data (addresses are don't care). The system can read CFI information at the addresses given in Table 6, on page 23 to Table 9, on page 25. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 6, on page 23 to Table 9, on page 25. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/products/nvd/overview/cfi.html. Alternatively, contact an AMD representative for copies of these documents.

Table 6. CFI Query Identification String

Addresses (x8)	Data	Description
10h 11h 12h	51h 52h 59h	Query Unique ASCII string "QRY"
13h 14h	02h 00h	Primary OEM Command Set
15h 16h	40h 00h	Address for Primary Extended Table
17h 18h	00h 00h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	00h 00h	Address for Alternate OEM Extended Table (00h = none exists)

Table 7. System Interface String

Addresses (x8)	Data	Description
1Bh	27h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	36h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	00h	V_{PP} Min. voltage (00h = no V_{PP} input present)
1Eh	00h	V_{PP} Max. voltage (00h = no V_{PP} input present)
1Fh	04h	Typical timeout per single byte write 2^N µs
20h	00h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0Ah	Typical timeout per individual block erase 2^N ms
22h	00h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	05h	Max. timeout for byte write 2^N times typical
24h	00h	Max. timeout for buffer write 2^N times typical
25h	04h	Max. timeout per individual block erase 2^N times typical
26h	00h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 8. Device Geometry Definition

Addresses (x8)	Data	Description
27h	17h	Device Size = 2^N byte
28h 29h	00h 00h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	00h 00h	Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	01h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	7Fh 00h 00h 01h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	00h 00h 00h 00h	Erase Block Region 2 Information (refer to CFI publication 100)
35h 36h 37h 38h	00h 00h 00h 00h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	00h 00h 00h 00h	Erase Block Region 4 Information (refer to CFI publication 100)

Table 9. Primary Vendor-Specific Extended Query

Addresses (x8)	Data	Description
40h 41h 42h	50h 52h 49h	Query-unique ASCII string “PRI”
43h	31h	Major version number, ASCII
44h	31h	Minor version number, ASCII
45h	01h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	02h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	04h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	01h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	04h	Sector Protect/Unprotect scheme 04 = 29LV800 mode
4Ah	00h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors in Bank
4Bh	000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	00h	Page Mode Type 00 = Not Supported
4Dh	B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	00h	Top/Bottom Boot Sector Flag 02h = Bottom Boot Device, 03h = Top Boot Device

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 10, on page 30 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE# (or CE2#), whichever happens later. All data is latched on the rising edge of WE# or CE# (or CE2#), whichever happens first. Refer to “AC Characteristics” on page 39 for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See “Erase Suspend/Erase Resume Commands” on page 28 for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, "Reset Command", for more information.

See also "VersatileIO‰ (VIO) Control" on page 9 for more information. The Read-Only Operations table provides the read parameters, and Figure 13, on page 39 shows the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 10, on page 30 shows the address and data requirements. This method is an alternative to that shown in Table 4, on page 19, which is intended for PROM programmers and requires V_{ID} on address A9. The autoselect command sequence may be written to an address that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence:

- A read cycle at address XX00h returns the manufacturer code.
- A read cycle at address XX01h returns the device code.
- A read cycle to an address containing a sector group address (SA), and the address 02h on A7–A0 returns 01h if the sector group is protected, or 00h if it is unprotected. (Refer to Table 5, on page 20 for valid sector addresses).

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Byte Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 10, on page 30 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the "Write Operation Status" on page 31 section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device returns to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read shows that the data is still "0." Only erase operations can convert a "0" to a "1."

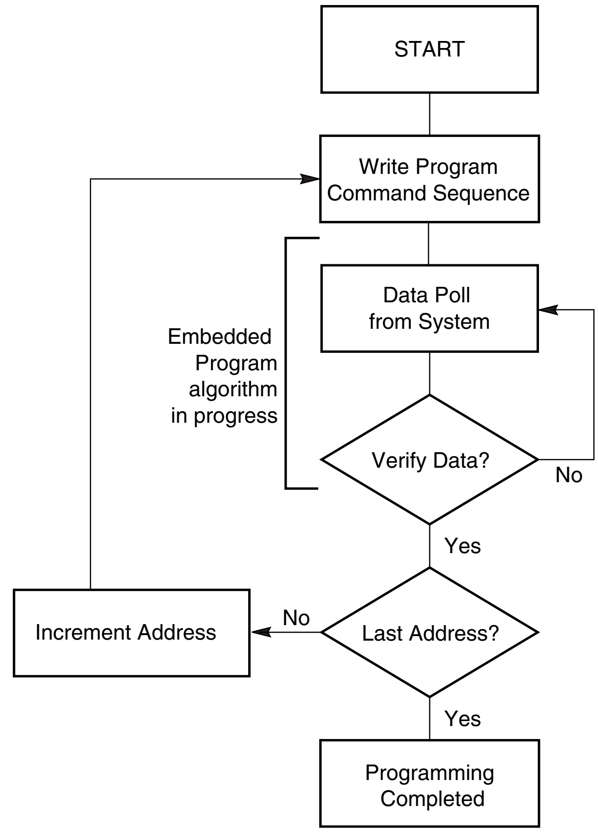
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 10, on page 30 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle must contain the data 00h. The device then returns to the read mode.

The device offers accelerated program operations through ACC. When the system asserts V_{HH} on ACC, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on ACC to accelerate the operation. *Note that ACC must not be at V_{HH} for operations other than accelerated programming, or device damage may result.*

Figure 3, on page 27 illustrates the algorithm for the program operation. Refer to the "Erase and Program Operations" on page 41 table in the AC Characteristics section for parameters, and Figure 15, on page 42 for timing diagrams.



Note: *See Table 10, on page 30 for program command sequence.*

Figure 3. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 10, on page 30 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to “Write Operation Status” on page 31 for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

Figure 4, on page 29 illustrates the algorithm for the erase operation. Refer to the “Erase and Program Operations” on page 41 tables in the AC Characteristics section for parameters, and Figure 17, on page 43 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 10, on page 30 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See “DQ3: Sector Erase Timer” on page 33.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing sector. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing sector. Refer to “Write Operation Status” on page 31 for information on these status bits.

Once the sector erase operation begins, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

Figure 4, on page 29 illustrates the algorithm for the erase operation. Refer to the “Erase and Program Operations” on page 41 tables in the AC Characteristics section for parameters, and Figure 17, on page 43 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

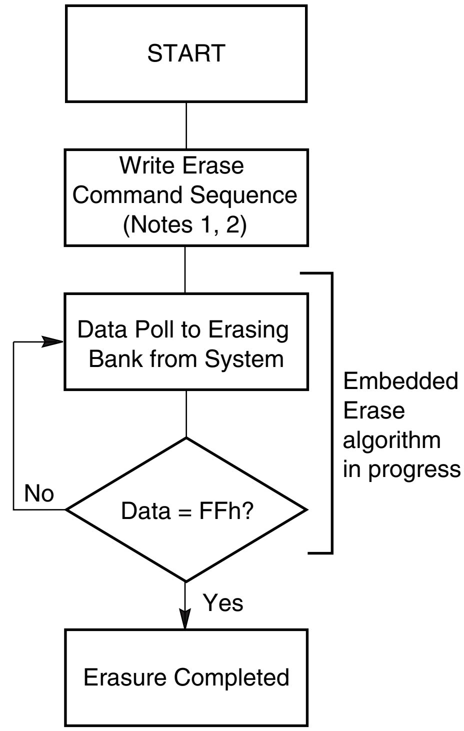
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation is suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to “Write Operation Status” on page 31 for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard byte program operation. Refer to "Write Operation Status" on page 31 for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the "Autoselect Mode" on page 19 and "Autoselect Command Sequence" on page 26 sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip resumes erasing.



Notes:

1. *See Table 10, on page 30 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 4. Erase Operation

Command Definitions

Table 10. Am29LV652D Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	XXX	AA	XXX	55	XXX	90	X00	01				
	Device ID	4	XXX	AA	XXX	55	XXX	90	X01	93				
	Sector Group Protect Verify (Note 8)	4	XXX	AA	XXX	55	XXX	90	(SA)X02	00/01				
Program		4	XXX	AA	XXX	55	XXX	A0	PA	PD				
Unlock Bypass		3	XXX	AA	XXX	55	XXX	20						
Unlock Bypass Program (Note 9)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 10)		2	XXX	90	XXX	00								
Chip Erase		6	XXX	AA	XXX	55	XXX	80	XXX	AA	XXX	55	XXX	10
Sector Erase		6	XXX	AA	XXX	55	XXX	80	XXX	AA	XXX	55	SA	30
Erase Suspend (Note 11)		1	BA	B0										
Erase Resume (Note 12)		1	BA	30										
CFI Query (Note 13)		1	XX	98										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# (or CE2#) pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# (or CE2#) pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A22–A16 uniquely select any sector.

Notes:

1. *See Table 1, on page 9 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Unless otherwise noted, address bits A22–A12 are don't cares.*
5. *No unlock or command cycles required when device is in read mode.*
6. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high (while the device is providing status information).*
7. *The fourth cycle of the autoselect command sequence is a read cycle. See the Autoselect Command Sequence section for more information.*
8. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
9. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
10. *The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.*
11. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
12. *The Erase Resume command is valid only during the Erase Suspend mode.*
13. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 11, on page 34 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or is completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

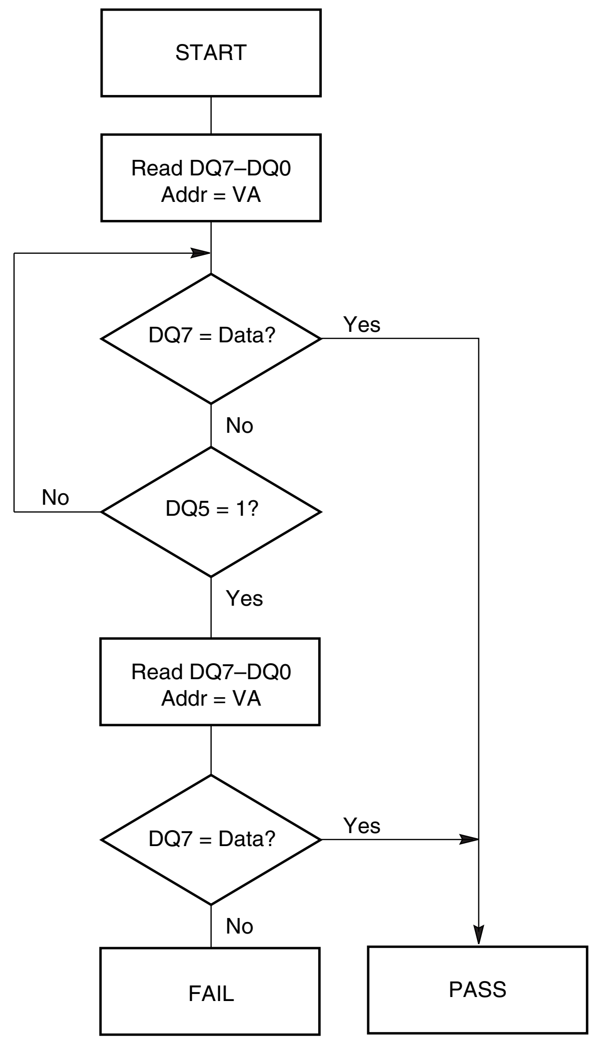
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device completes the program or erase operation and DQ7 contains valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 appears on successive read cycles.

“Write Operation Status” on page 34 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 18, on page 44 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY#s can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or the device is in the erase-suspend-read mode.

Table 11, on page 34 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# (or CE2#) to control the read cycles. When the operation is complete, DQ6 stops toggling.

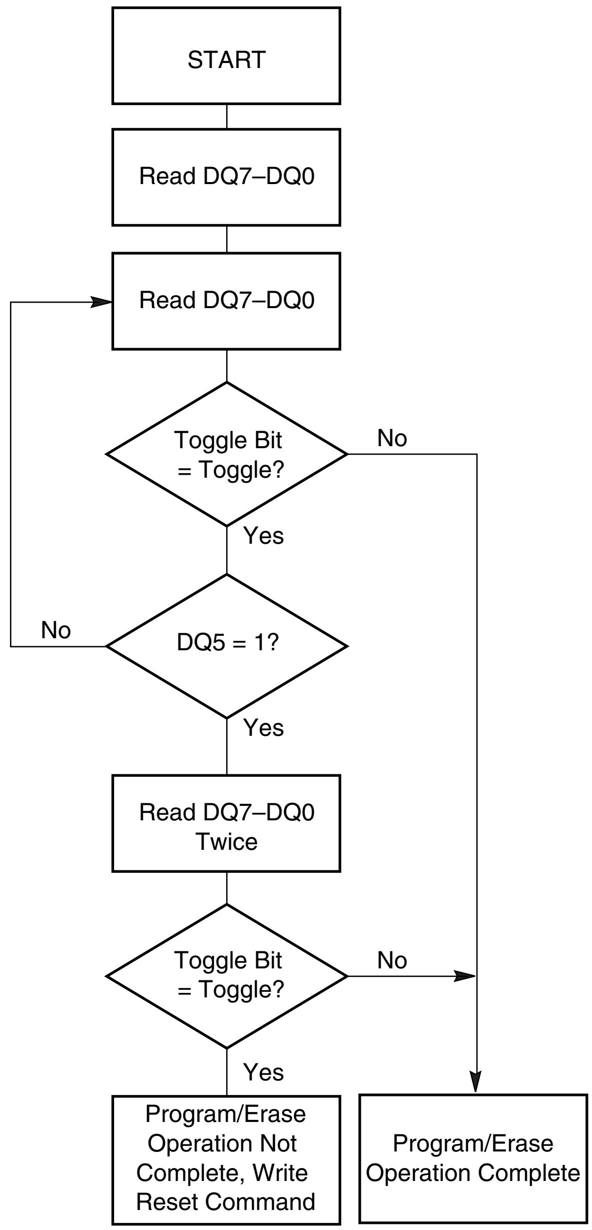
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on "DQ7: Data# Polling" on page 31).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 11, on page 34 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm. Figure 19, on page 45 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 20, on page 45 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection "DQ2: Toggle Bit II" on page 33.



***Note:** The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 6. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# or CE2# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 11, on page 34 to compare outputs for DQ2 and DQ6.

Figure 6, on page 32 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 19, on page 45 shows the toggle bit timing diagram. Figure 20, on page 45 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 6, on page 32 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6, on page 32).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit is exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure began. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also "Sector Erase Command Sequence" on page 28

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device accepts additional sector erase commands. To ensure the command is accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 11, on page 34 shows the status of DQ3 relative to the other status bits.

Table 11. Write Operation Status

<table>
<tr><th colspan="3">Status</th><th>DQ7 (Note 2)</th><th>DQ6</th><th>DQ5 (Note 1)</th><th>DQ3</th><th>DQ2 (Note 2)</th><th>RY/BY#</th></tr>
<tr><td rowspan="2">Standard Mode</td><td colspan="2">Embedded Program Algorithm</td><td>DQ7#</td><td>Toggle</td><td>0</td><td>N/A</td><td>No toggle</td><td>0</td></tr>
<tr><td colspan="2">Embedded Erase Algorithm</td><td>0</td><td>Toggle</td><td>0</td><td>1</td><td>Toggle</td><td>0</td></tr>
<tr><td rowspan="3">Erase Suspend Mode</td><td rowspan="2">Erase-Suspend-Read</td><td>Erase Suspended Sector</td><td>1</td><td>No toggle</td><td>0</td><td>N/A</td><td>Toggle</td><td>1</td></tr>
<tr><td>Non-Erase Suspended Sector</td><td>Data</td><td>Data</td><td>Data</td><td>Data</td><td>Data</td><td>1</td></tr>
<tr><td colspan="2">Erase-Suspend-Program</td><td>DQ7#</td><td>Toggle</td><td>0</td><td>N/A</td><td>N/A</td><td>0</td></tr>
</table>

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . .–0.5 V to +4.0 V

V_{IO}. . . . .–0.5 V to +5.5 V

A9, OE#, ACC, and RESET#
(Note 2). . . . .–0.5 V to +12.5 V

All others (Note 1). . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, input or I/Os may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/Os is V_{CC} +0.5 V. See Figure 7, on page 35. During voltage transitions, input or I/Os may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8, on page 35.*
2. *Minimum DC input voltage on A9, OE#, ACC, and RESET# is –0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7, on page 35. Maximum DC input voltage on A9, OE#, ACC, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A). . . . .–40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A). . . . .–55°C to +125°C

Supply Voltages

V_{CC} . . . . .3.0 V–3.6 V

V_{IO}. . . . . .3.0 V–5.0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

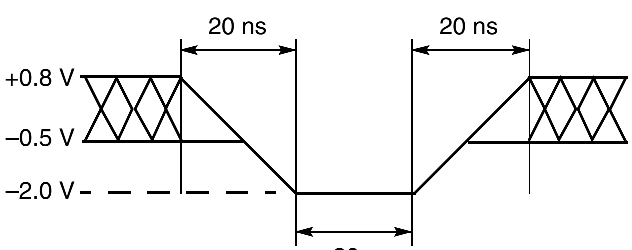


Figure 7. Maximum Negative Overshoot Waveform

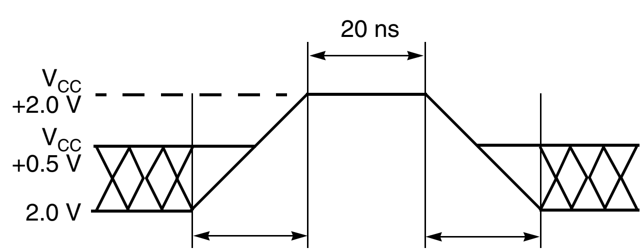


Figure 8. Maximum Positive Overshoot Waveform

DC CHARACTERISTICS (For Two Am29LV065 Devices)

CMOS Compatible

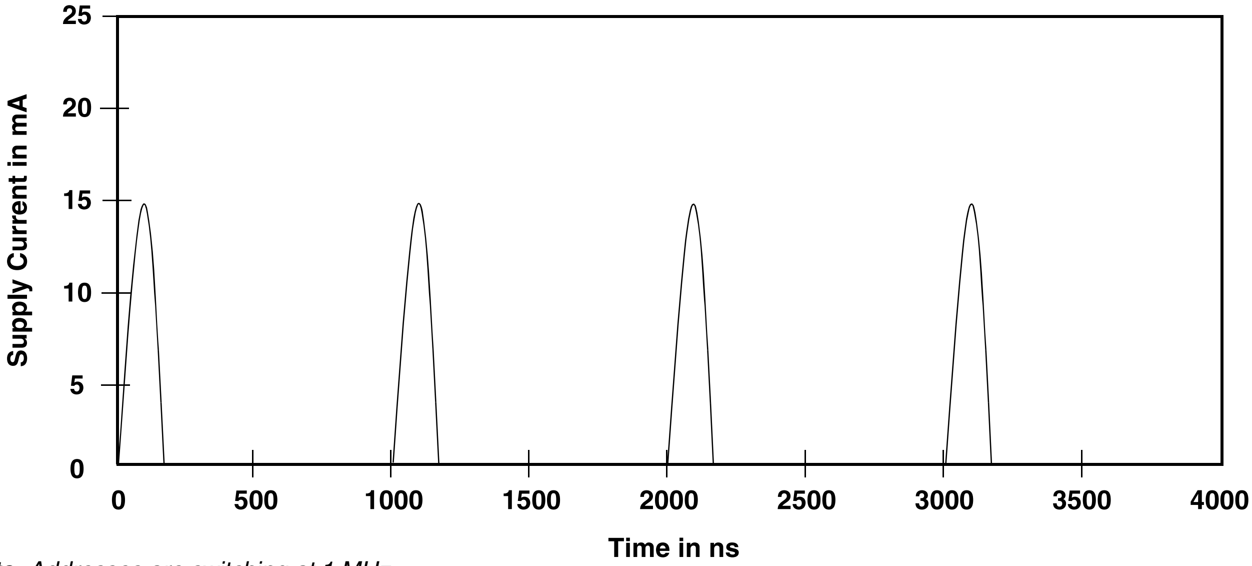
Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, ACC Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				70	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# (or CE2#) = V_{IL}, OE# = V_{IH}	5 MHz		9	16	mA
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3, 4)	CE# (or CE2#) = V_{IL}, OE# = V_{IH}			26	30	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, CE2#, RESET# = $V_{CC} \pm 0.3$ V			0.4	10	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = $V_{SS} \pm 0.3$ V			0.4	10	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 5)	$V_{IH} = V_{CC} \pm 0.3$ V; $V_{IL} = V_{SS} \pm 0.3$ V			0.4	10	µA
I_{ACC}	ACC Accelerated Program Current (Note 4)	CE# = V_{IL}, OE# = V_{IH}	ACC		5	10	mA
			V_{CC}		15	30	mA
V_{IL}	Input Low Voltage (Note 6)			–0.5		0.8	V
V_{IH}	Input High Voltage (Note 6)			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 V ± 10%		8.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage (Note 7)	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 V_{IO}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{IO}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 7)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Assumes only one Am29LV065 die being programmed at the same time.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 400 nA.*
6. *If $V_{IO} < V_{CC}$, maximum V_{IL} for CE# (or CE2#) is 0.3 V_{IO}. If $V_{IO} < V_{CC}$, minimum V_{IH} for CE# (or CE2#) is 0.3 V_{IO}.*
7. *Not 100% tested.*
8. *CE# can be replaced with CE2# when referring to the second device within the package.*
9. *Specifications in the table are for the Am29LV652 i.e. two Am29LV065 dice.*

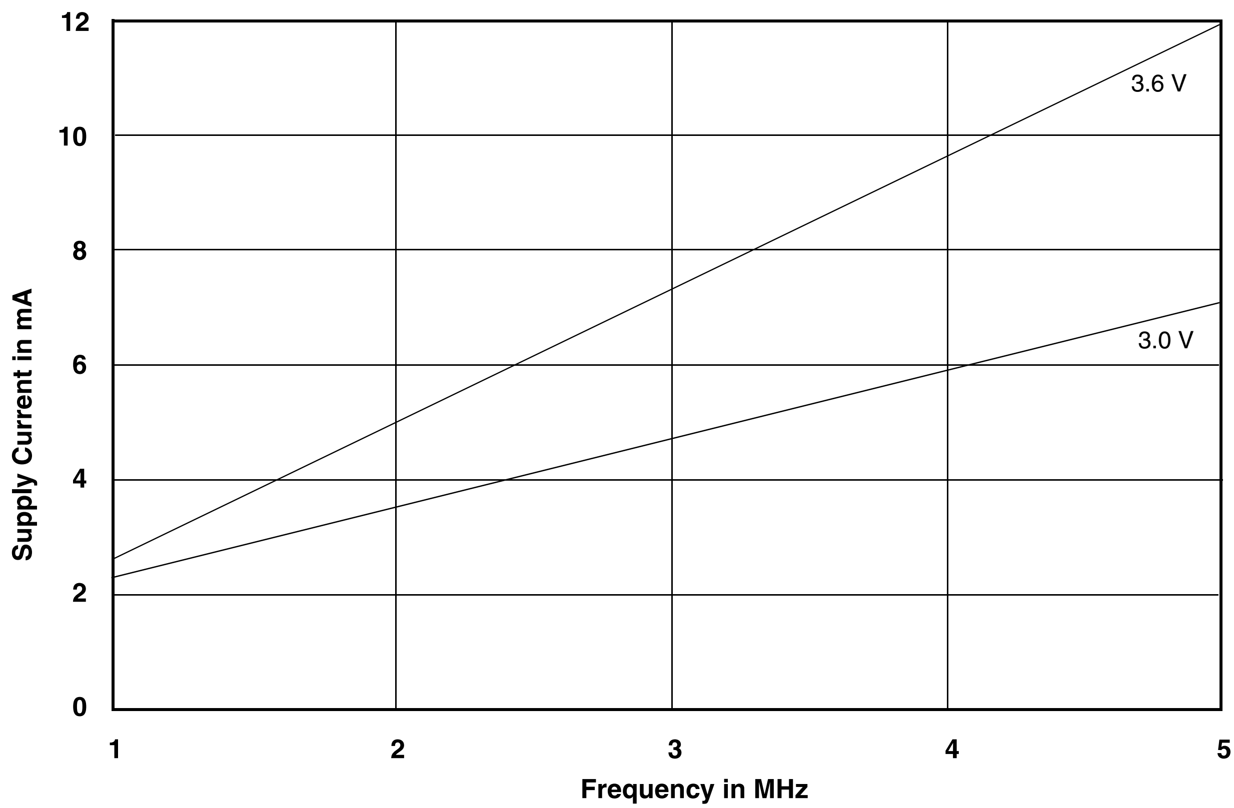
DC CHARACTERISTICS

Zero-Power Flash



Note: *Addresses are switching at 1 MHz*

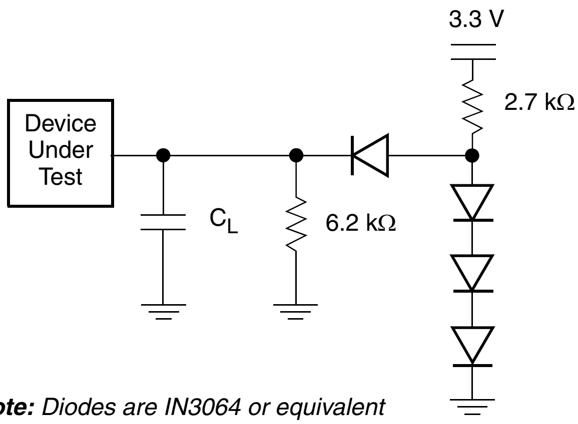
Figure 9. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

Figure 10. Typical I_{CC1} vs. Frequency

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 11. Test Setup

Table 12. Test Specifications

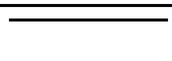
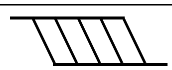
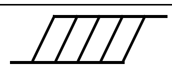
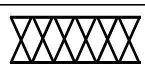
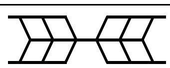
Test Condition	90R	12R	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels (See Note)	1.5		V
Output timing measurement reference levels	0.5 V_{IO}		V

Note: *If $V_{IO} < V_{CC}$, the reference level is 0.5 V_{IO}.*

Note: *If $V_{IO} < V_{CC}$, the input measurement reference level is 0.5 V_{IO}.*

Figure 12. Input Waveforms and Measurement Levels

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

AC CHARACTERISTICS

Read-Only Operations

Parameter		Description	Test Setup (Note 1)		Speed Options		Unit
JEDEC	Std.				90R	12R	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 2)		Min	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	CE#, OE# = V_{IL}	Max	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	Max	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 2)		Max	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 2)		Max	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First		Min	0		ns
	t_{OEH}	Output Enable Hold Time (Note 2): Read		Min	0		ns
		Output Enable Hold Time (Note 2): Toggle and Data# Polling		Min	10		ns

Notes:

1. *All test setups assume $V_{IO} = V_{CC}$.*
2. *Not 100% tested.*
3. *See Figure 11, on page 38 and Table 12, on page 38 for test specifications*
4. *CE# can be replaced with CE2# when referring to the second device within the package.*

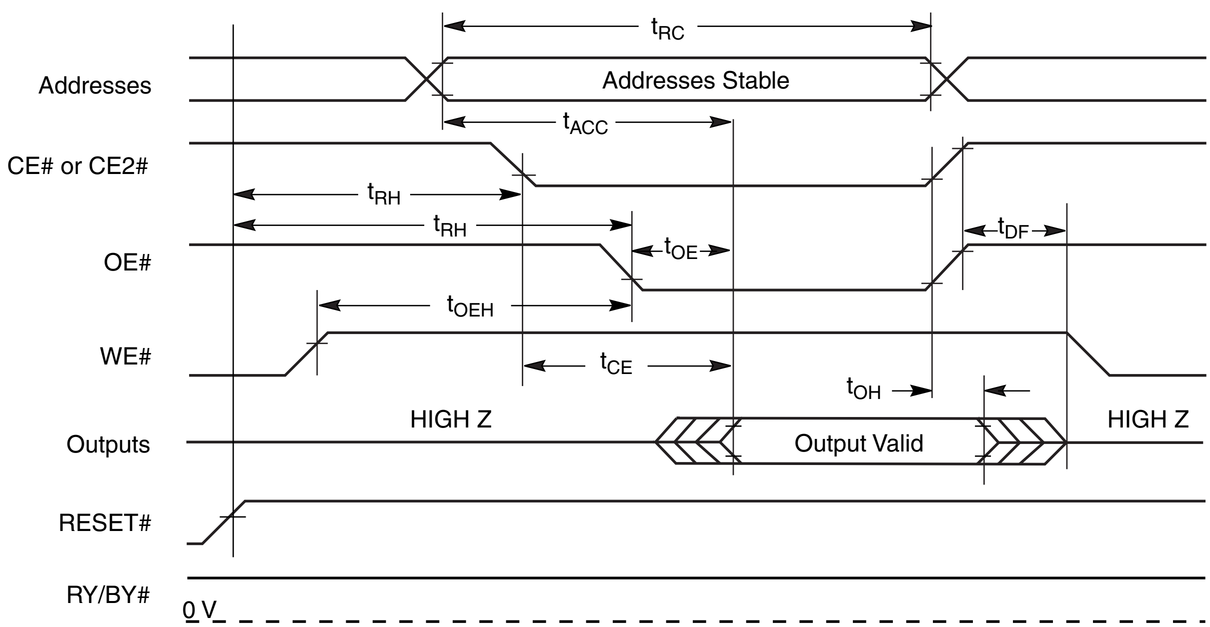


Figure 13. Read Operation Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

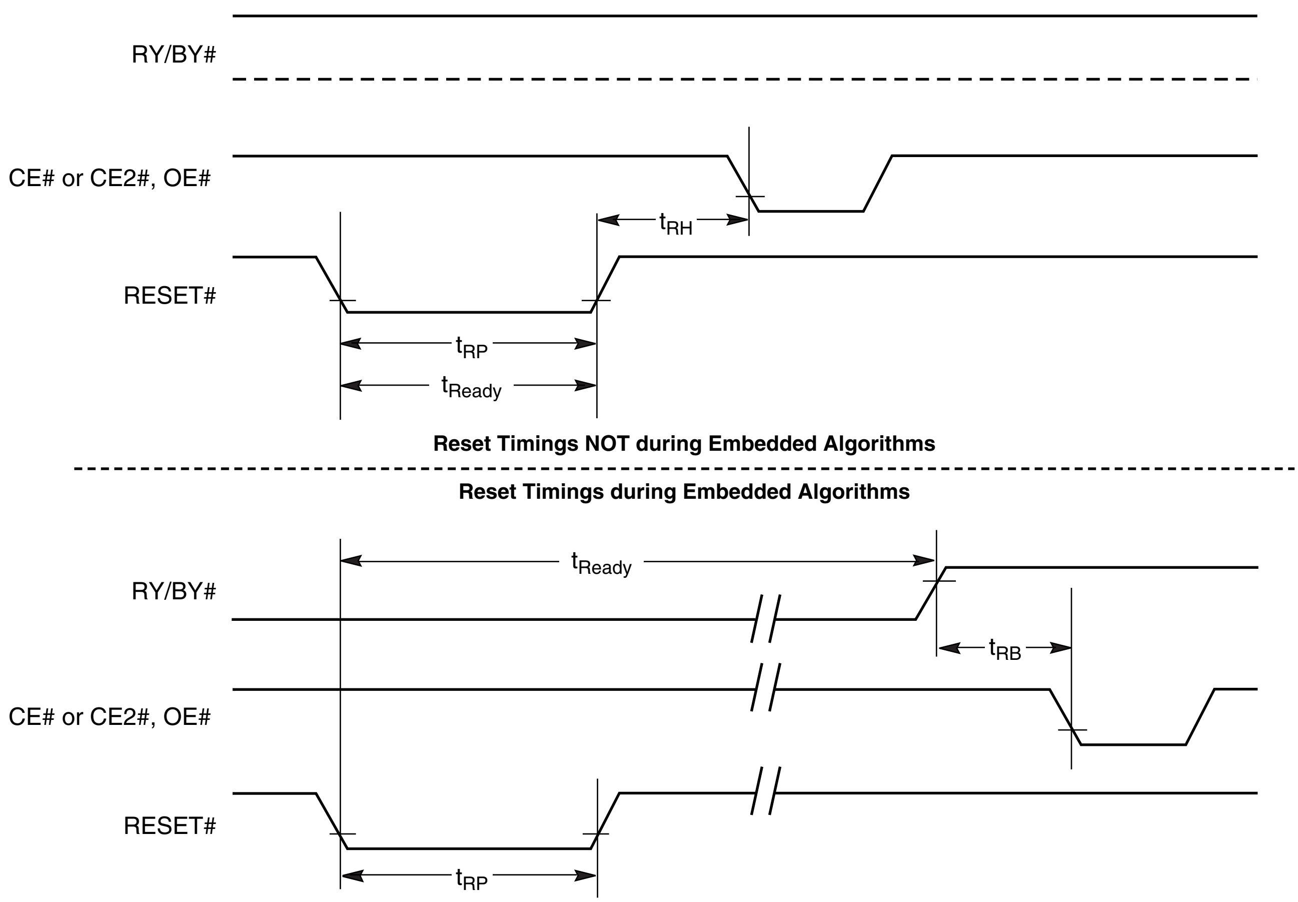


Figure 14. Reset Timings

AC CHARACTERISTICS

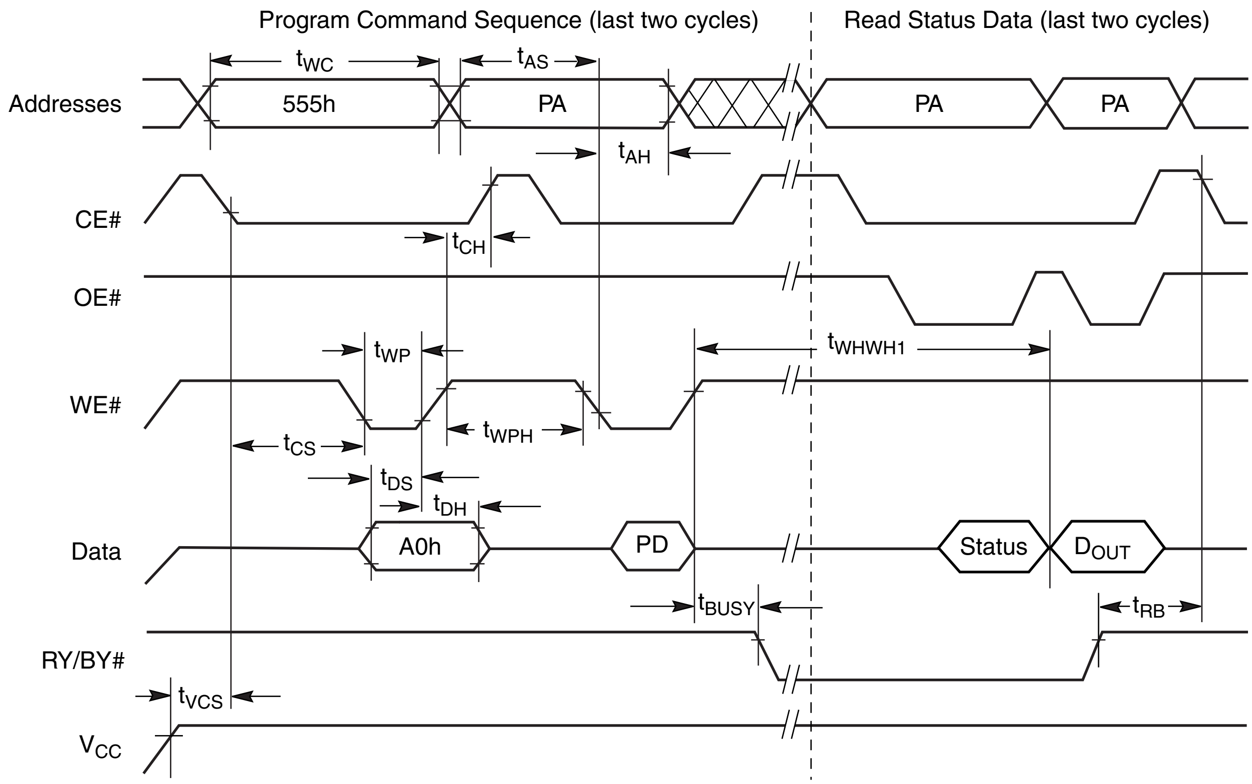
Erase and Program Operations

Parameter				Speed Options		
JEDEC	Std.	Description		90R	12R	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0		ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	15		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	50	ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling	Min	0		ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0		ns
	t_{OEPH}	Output Enable High during toggle bit polling	Min	20		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	50	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	30		ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Typ	5		µs
t_{WHWH1}	t_{WHWH1}	Accelerated Byte Programming Operation (Note 2)	Typ	4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	1.6		sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)	Min	250		ns
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50		µs
	t_{RB}	Write Recovery Time from RY/BY#	Min	0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Min	90		ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" on page 50 section for more information.*
3. *CE# can be replaced with CE2# when referring to the second device within the package.*

AC CHARACTERISTICS



Note: *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*

Figure 15. Program Operation Timings

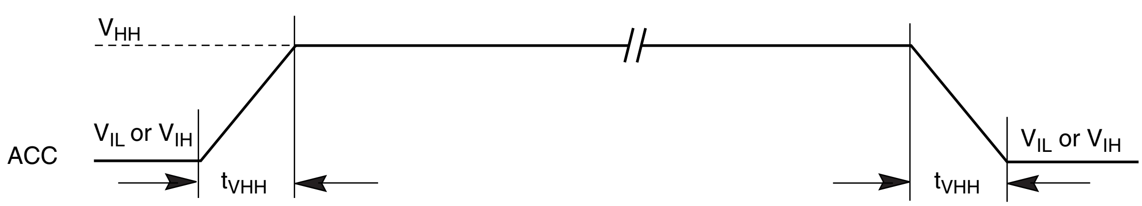
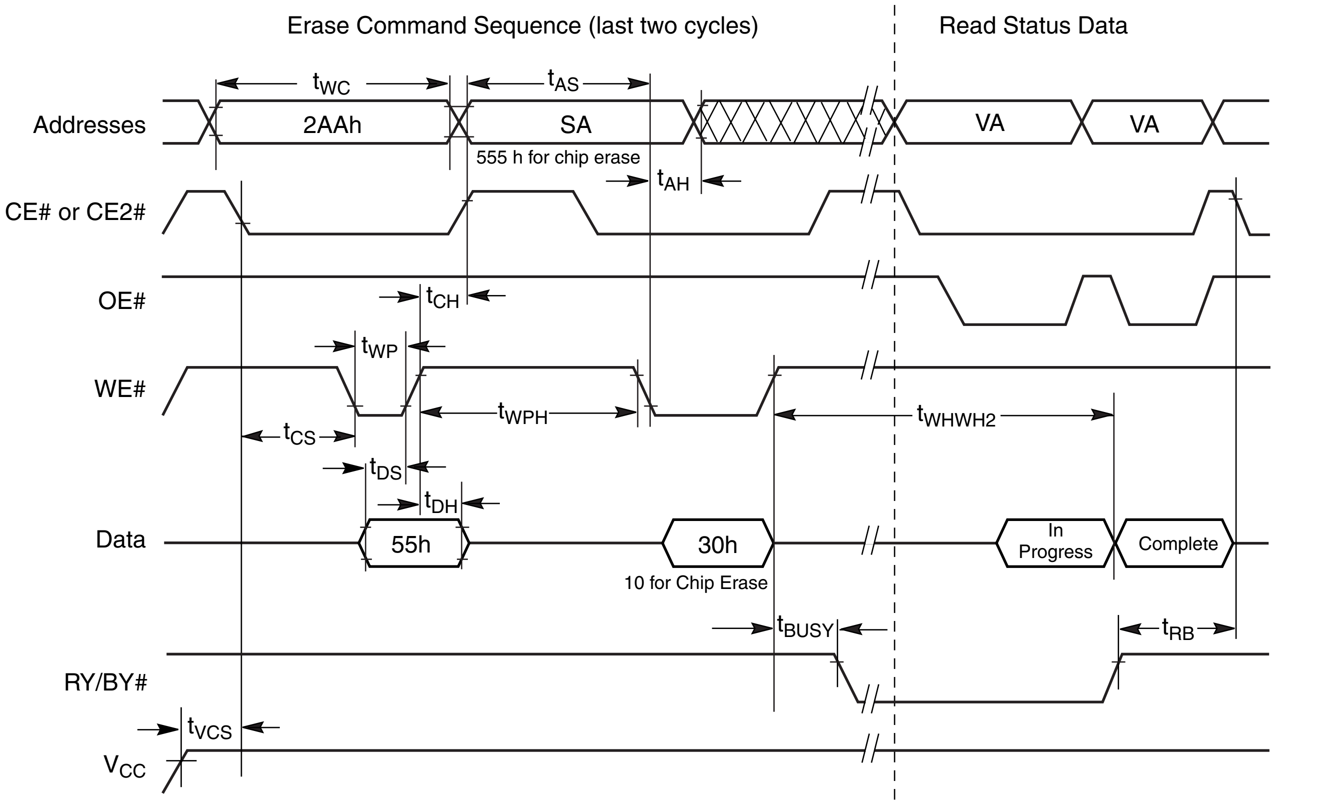


Figure 16. Accelerated Program Timing Diagram

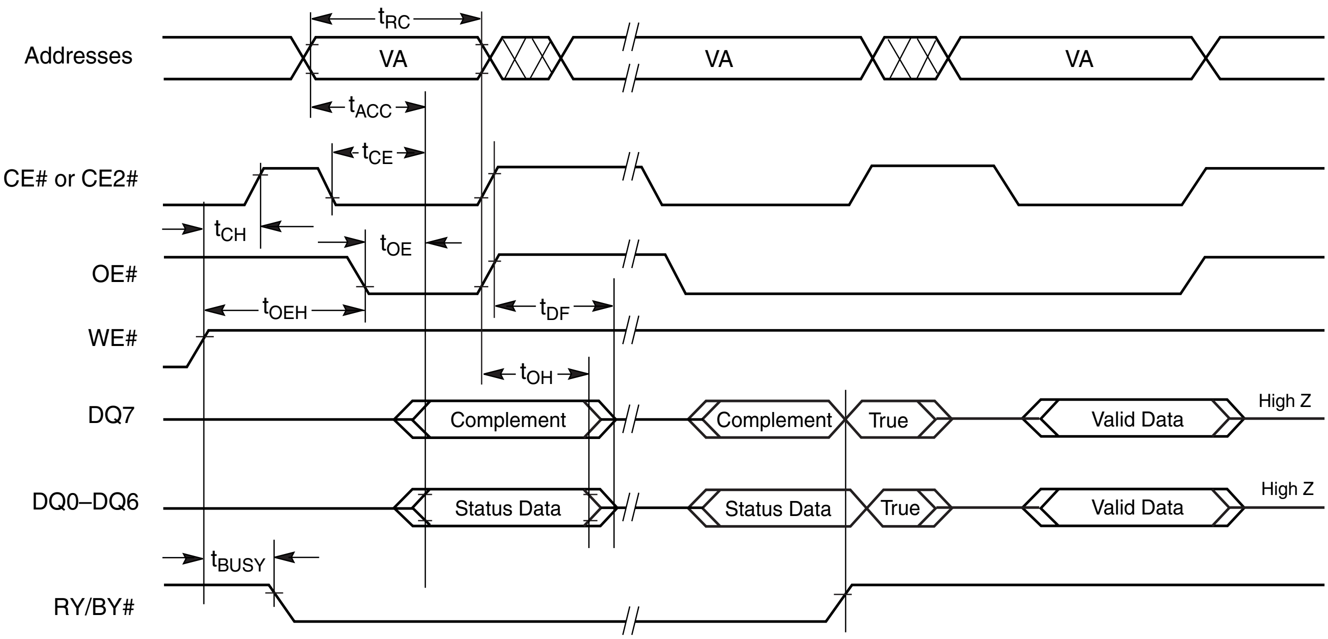
AC CHARACTERISTICS



Note: *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see “Write Operation Status” on page 31*

Figure 17. Chip/Sector Erase Operation Timings

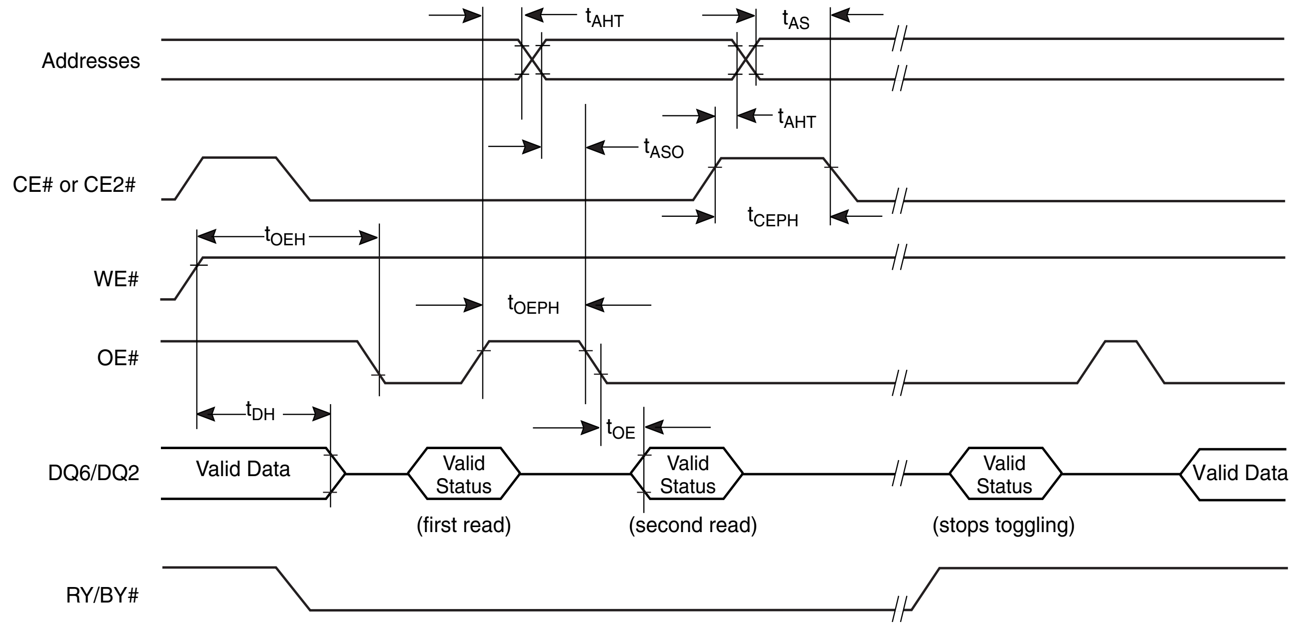
AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

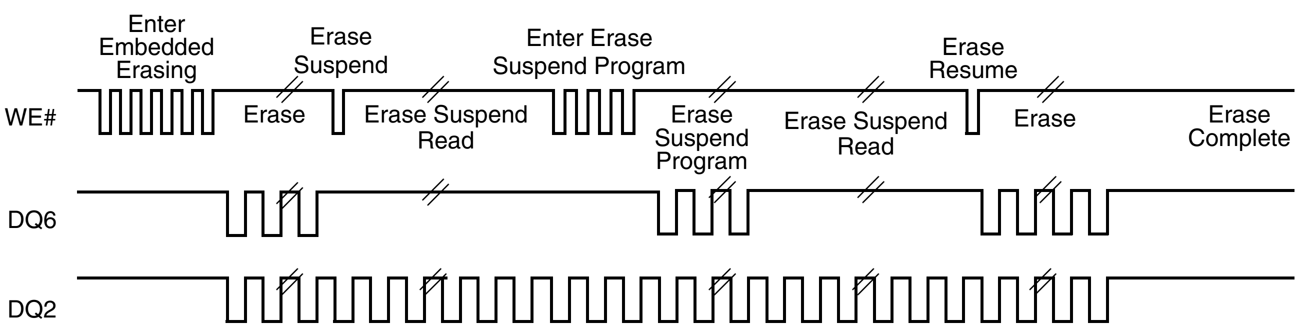
Figure 18. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



***Note:** VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 19. Toggle Bit Timings (During Embedded Algorithms)



***Note:** DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 20. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Group Unprotect	Min	4	µs

Note: *Not 100% tested.*

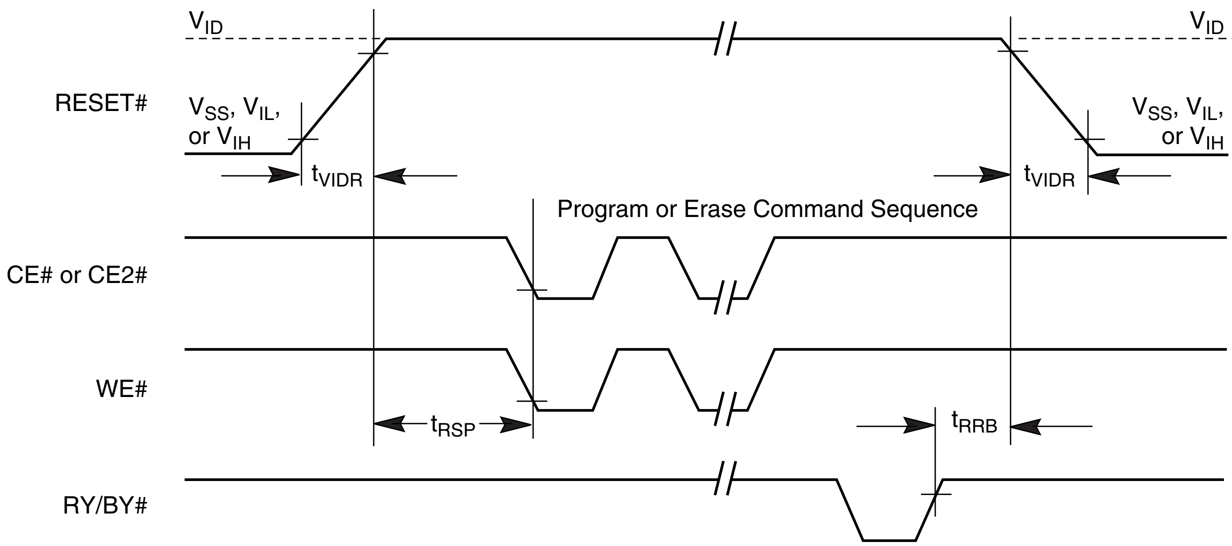
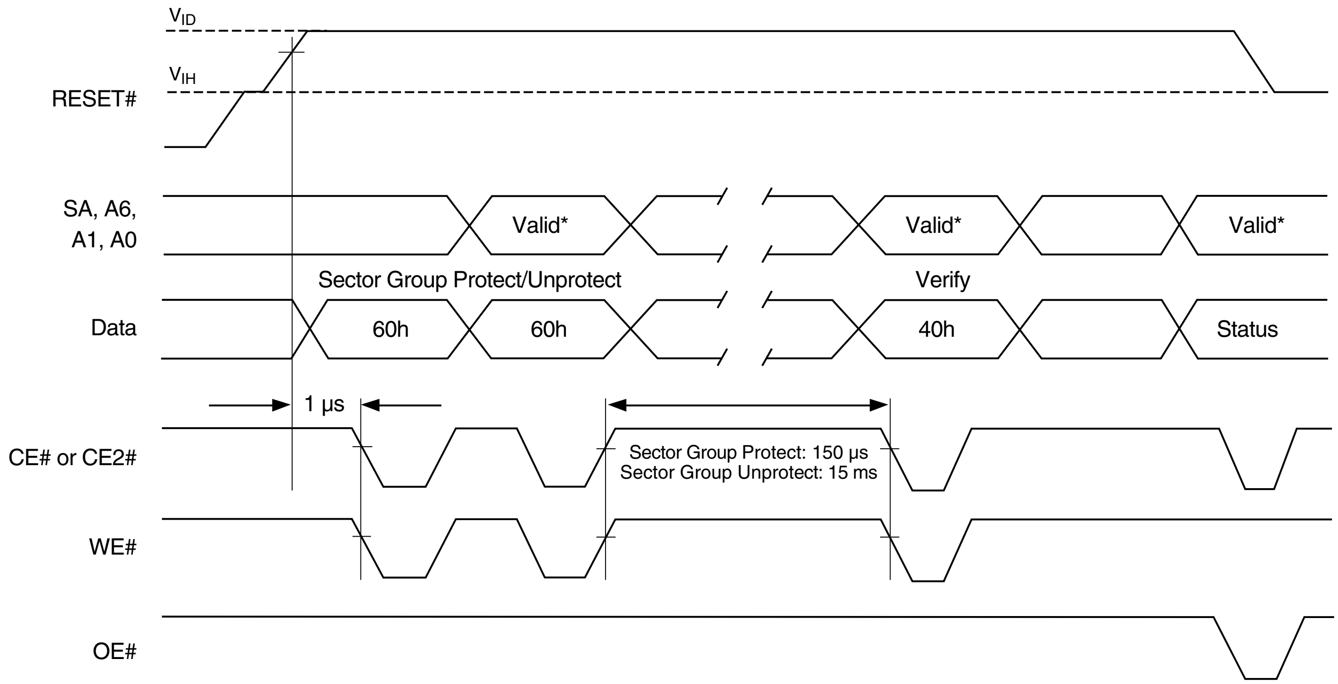


Figure 21. Temporary Sector Group Unprotect Timing Diagram

AC CHARACTERISTICS



* *For sector group protect, A6 = 0, A1 = 1, A0 = 0. For sector group unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 22. Sector Group Protect and Unprotect Timing Diagram

AC CHARACTERISTICS

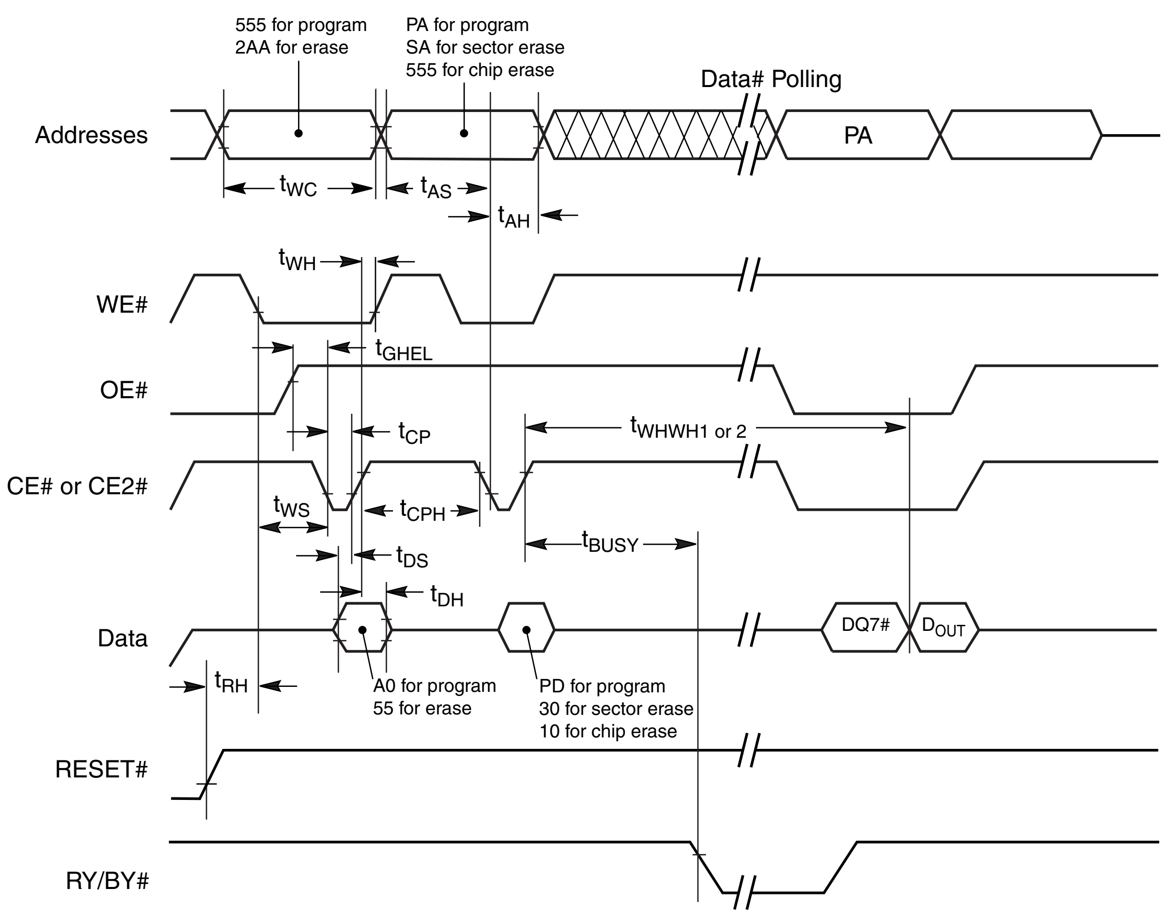
Alternate CE# Controlled Erase and Program Operations

Parameter		Description		Speed Options		Unit
JEDEC	Std			90R	12R	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	45	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	30		ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Typ	5		µs
t_{WHWH1}	t_{WHWH1}	Accelerated Byte Programming Operation (Note 2)	Typ	4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	1.6		sec

Notes:

1. *Not 100% tested.*
2. *See the “Erase And Programming Performance” section for more information.*
3. *CE# can be replaced with CE2# when referring to the second device within the package.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*

Figure 23. Alternate CE# Controlled Write (Erase/Program) Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	1.6	15	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	205		sec	
Byte Program Time	5	150	µs	Excludes system level overhead (Note 5)
Accelerated Byte Program Time	4	120	µs	
Chip Program Time (Note 3)	42	126	sec	

Notes:
1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 3.0 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 10, on page 30 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all device connections (including A9, OE#, and RESET#) except I/Os	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/Os	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all connections except V_{CC}. Test conditions: V_{CC} = 3.0 V, one connection at a time.*

INPUT/OUTPUT CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	12	16	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	12	16	pF
C_E/C_{E2}	Control Pin Capacitance	$V_{IN} = 0$	6	8	pF

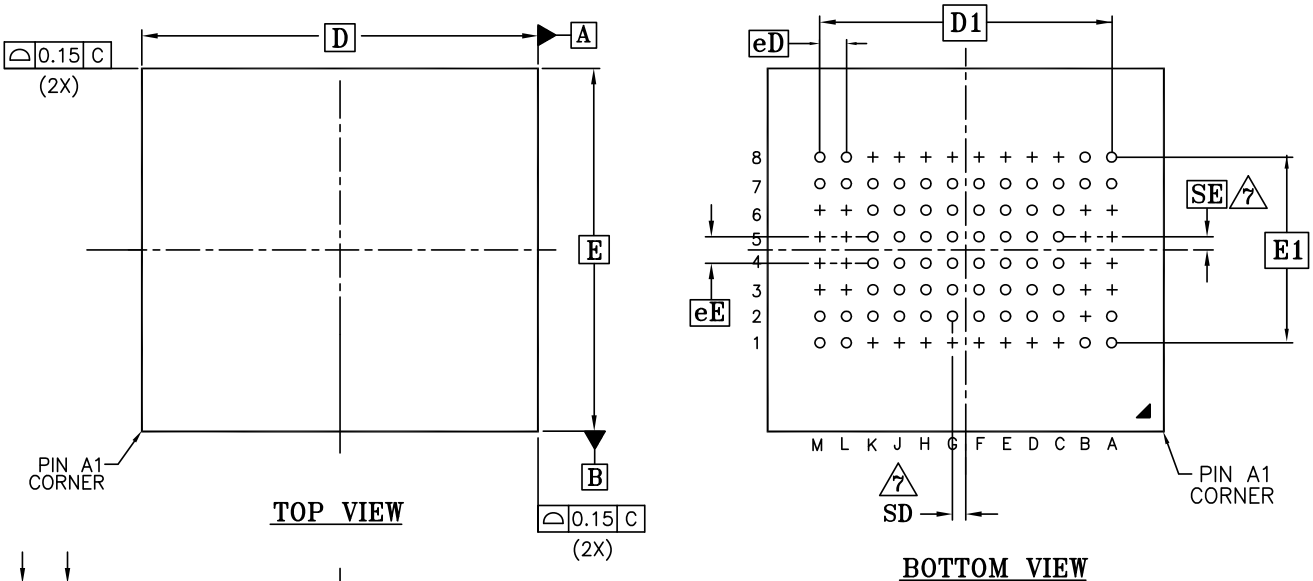
Notes:
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

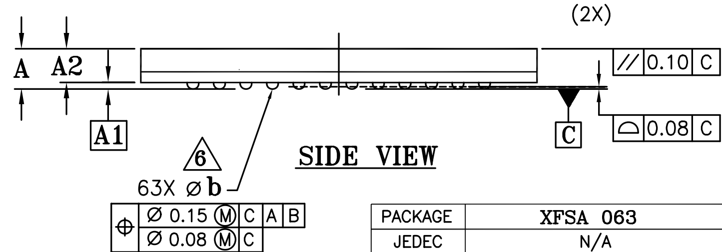
DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

FSA063—63-Ball Fine-Pitch Ball Grid Array (FBGA) 11 x 12 mm package





PACKAGE	XFSA 063			NOTE
JEDEC	N/A			
	11.00mm X 12.00mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	--	--	1.70	PROFILE
A1	0.35	--	--	BALL HEIGHT
A2	1.15	--	1.25	BODY THICKNESS
D	11.95 BSC			BODY SIZE
E	10.95 BSC			BODY SIZE
D1	8.80 BSC			MATRIX FOOTPRINT
E1	5.60 BSC			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	63			BALL COUNT
⌀b	0.40	0.45	0.50	BALL DIAMETER
eE	0.80 BSC			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT
	A3,A4,A5,A6,B2,B3,B4,B5,B6 C1,C8,D1,D8,E1,E8,F1,F8 G1,G8,H1,H8,J1,J8,K1,K8 L3,L4,L5,L6,M3,M4,M5,M6			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

REVISION SUMMARY

Revision A (May 24, 2001)

Initial release.

Revision A+1 (July 31, 2001)

AC Characteristics—Alternate CE# Controlled Erase and Program Table

t_{WHWH1}—*Byte Programming Operation:* Changed typical value from 11 µs to 5 µs.

t_{WHWH1}—*Accelerated Byte Programming Operation:* Changed typical value from 7 µs to 4 µs.

Revision A+2 (August 14, 2001)

Global

Removed the speed options for 100 ns with V_{IO} = 1.8 V – 2.9 V and 120 ns with V_{IO} = 1.8 V – 2.9 V. Changed the speed option for 120 ns with V_{IO} = 3.0 V – 5.0 V from 120R to 12R.

General Description and Device Bus Operations

Added "For voltage levels below 3 V, contact an AMD representative for more information." to VersatileI/O™ text.

Ordering Information

Removed the Optional Processing from the order number.

Revision A+3 (January 10, 2002)

Global

Clarified description of VersatileIO (V_{IO}) in the following sections: Distinctive Characteristics; General Description; VersatileIO (V_{IO}) Control; Operating Ranges; DC Characteristics; CMOS compatible.

Revision A+4 (October 29, 2004)

Global

Added Spansion Cover Sheet

Added reference links to page numbers

Added Colophon

Ordering Information

Added two package types to temperature range.

Valid Combination for FBGA Packages

Added MAF and MAK to order number.

Added F and K to Package Marking.

Revision A5 (May 5, 2006)

Added migration/obsolescence notices.

Colophon

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