PRELIMINARY

AMD

Am79C988A

Quad Integrated Ethernet Transceiver (QuIET™)

DISTINCTIVE CHARACTERISTICS

- **Four independent 10BASE-T transceivers compliant with IEEE 802.3 Section 14 (10BASE-T MAUs)**
- **Direct interface with AMD's Am79C983A IMR2™ repeater device**
- **On-chip filtering**
  - — Eliminates external transmit and receive filters
  - — Meets IEEE 802.3 (Section 14.3) electrical requirements
  - — Enables port switching when used with the IMR2 device
- **Automatic polarity detection and correction**
- **Serial management interface allows transfer of command and status data between the QuIET device and a controller (IMR2 or other device)**
- **Standard Ethernet (Normal) and Full-Duplex modes**
- **Extended distance option to accommodate lines longer than 100 meters**
- **Test functions provided for Loopback, Link Test, Reverse Polarity, and Jabber**
- **44-pin PLCC CMOS device with a single 5-V supply**

GENERAL DESCRIPTION

The Am79C988A Quad Integrated Ethernet Transceiver (QuIET) device consists of four independent 10BASE-T transceivers which are compliant with the IEEE 802.3 Section 14 (*Medium Attachment Unit for 10BASE-T Cabling*) standard. When combined with AMD's Integrated Multiport Repeater 2 (IMR2™) chip, the QuIET device provides a system-level solution to designing a managed 10BASE-T repeater.

The QuIET device includes on-chip filtering for both transmit and receive functions, thus eliminating the need for external filters. On-chip filtering meets IEEE 802.3 (Section 14.3) electrical requirements. The QuIET device provides automatic polarity detection and correction and can operate in either normal or full-duplex mode.

The QuIET device interfaces directly with the Pseudo AUI (PAUI™) ports on the IMR2 (Am79C983A) device and can also be connected to standard AUI ports. Command and status data are exchanged with the IMR2 device via a serial management interface. Port switching can be easily implemented with the IMR2/QuIET chipset to move individual ports between multiple Ethernet segments under software control.

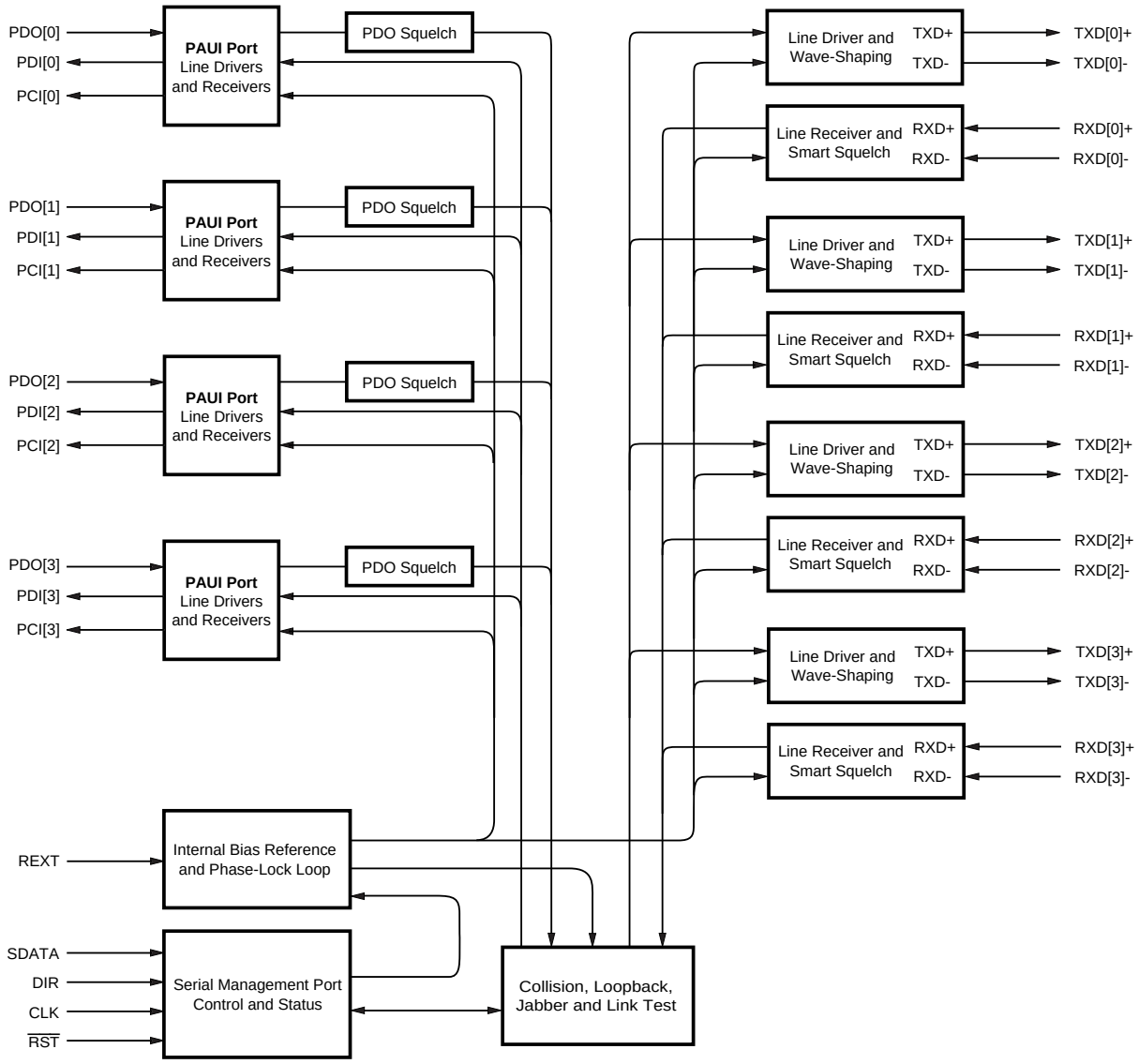
For application examples on building fully-managed repeaters using the QuIET and IMR2 devices, refer to AMD's *IMR2 Technical Manual* (PID 19898A).

The QuIET chip is packaged in a 44-pin plastic leaded chip carrier (PLCC). The device is fabricated in CMOS technology and requires a single 5-V supply.

Publication# **19880** Rev: **B** Amendment/**+2**
Issue Date: **November 1997**

BLOCK DIAGRAM

QuIET Device



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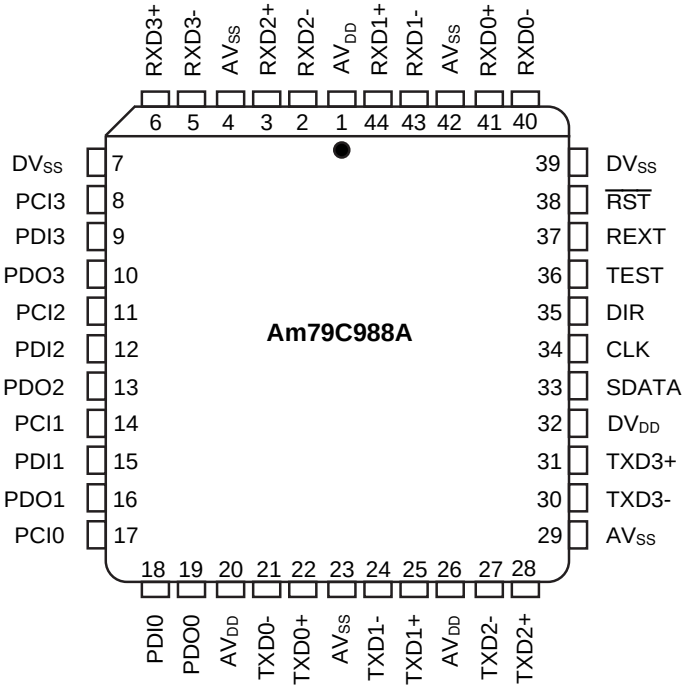
RELATED AMD PRODUCTS

Part No.	Description
Am79C981	Integrated Multiport Repeater+ (IMR+™)
Am79C982	*b*asic Integrated Multiport Repeater (*b*IMR™)
Am79C983A	Integrated Multiport Repeater 2 (IMR2™)
Am79C987	Hardware Implemented Management Information Base (HIMIB™)
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7996	IEEE 802.3/Ethernet/Cheapernet Transceiver
Am79C90	CMOS Local Area Network Controller for Ethernet (C-LANCE)
Am79C98	Twisted Pair Ethernet Transceiver (TPEX)
Am79C100	Twisted Pair Ethernet Transceiver Plus (TPEX+)
Am79C900	Integrated Local Area Communications Controller (ILACC™)
Am79C940	Media Access Controller for Ethernet (MACE™)
Am79C960	PCnet™-ISA Single-Chip Ethernet Controller (for ISA bus)
Am79C961	PCnet™-ISA+ Single-Chip Ethernet Controller for ISA (with Microsoft® Plug n' Play® Support)
Am79C961A	PCnet™-ISA II Full Duplex Single-Chip Ethernet Controller for ISA
Am79C965	PCnet™-32 Single-Chip 32-Bit Ethernet Controller
Am79C970	PCnet™-PCI Single-Chip Ethernet Controller (for PCI bus)
Am79C970A	PCnet™-PCI II Full Duplex Single-Chip Ethernet Controller (for PCI bus)
Am79C974	PCnet™-SCSI Combination Ethernet and SCSI Controller for PCI Systems

CONNECTION DIAGRAM



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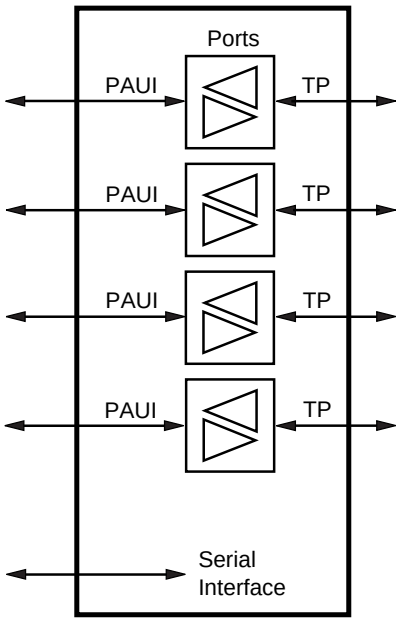
LOGIC DIAGRAM



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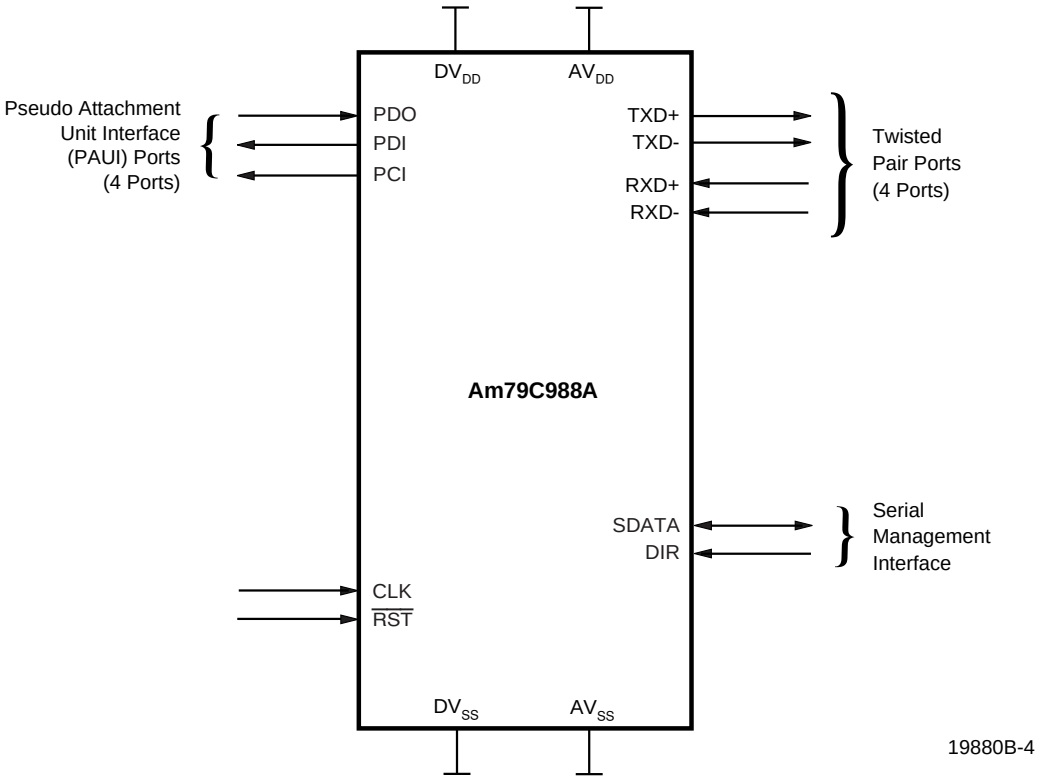
LOGIC SYMBOL

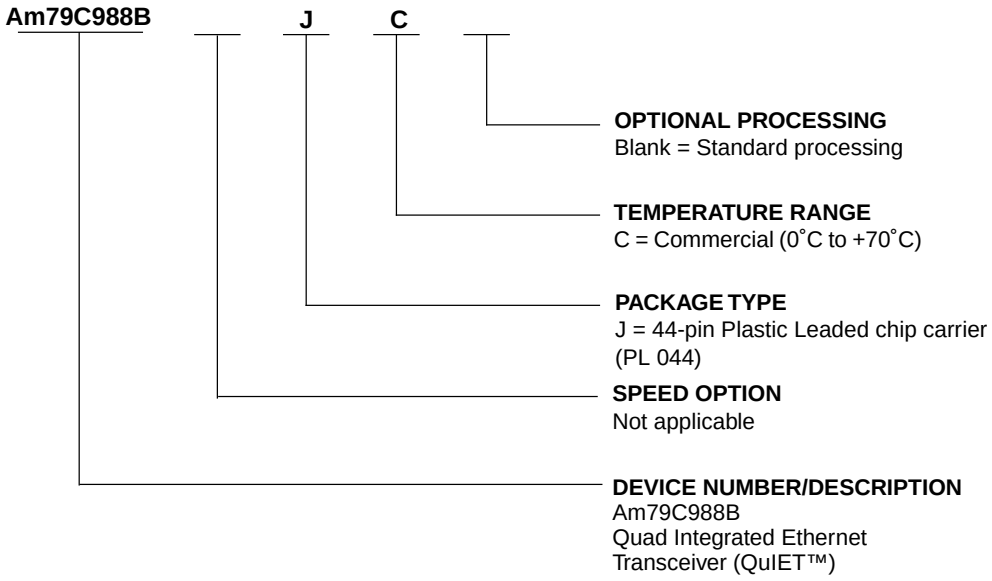


19880B-4

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
Am79C988B	JC\T

Valid Combinations

Valid Combinations table list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

Analog

PDO_{0-3}
Pseudo AUI Data Output
Input
Single-ended receiver. Data input from the IMR2 device.

PDI_{0-3}
Pseudo AUI Data Input
Output

Single-ended output driver. Data output to the IMR2 device.

PCI_{0-3}
Pseudo AUI Collision Input
Output

Single-ended output driver. Collision output to the IMR2 device.

$TXD+_{0-3}$, $TXD-_{0-3}$
Transmit Data
Output

10BASE-T port differential drivers.

$RXD+_{0-3}$, $RXD-_{0-3}$
Receive Data
Input

10BASE-T port differential receivers.

REXT
External Resistor
Input

REXT must be tied to AV_{DD} through a 13 kΩ ±1% resistor.This provides the current reference for all internal analog functions.

AV_{DD}

Analog Power
Power Pin

These pins supply +5-V power to the analog portion of the device. These pins should be decoupled and kept separate from the digital power plane.

AV_{SS}
Analog Ground
Ground Pin

These pins provide the ground reference for the analog portions of the QuIET circuitry.

Digital

SDATA
Serial Data
Input/Output

Transfers command and status data between the QuIET device and the IMR2 chip.

DIR
Direction
Input

Selects the direction of command data and status data transfer between the QuIET device and the IMR2 chip.

$\overline{RST}$
Reset
Input, Active Low

Resets the internal registers of the QuIET device.

CLK
Clock
Input

20-Mhz clock signal. The clock signal should be the same one that is used by all IMR2 devices connected to the QuIET chip.

TEST
Input, Active High

Reserved for factory use only. This pin does have an internal pull-down, but should be tied LOW for normal operation.

DV_{DD}
Digital Power
Power Pin

These pins supply +5-V power to the digital portion of the device. These pins should be decoupled and kept separate from the analog power plane.

DV_{SS}
Digital Ground
Ground Pin

These pins provide the ground reference for the digital portions of the QuIET circuitry.

Note: *All digital I/O pins are CMOS and TTL compatible.*

FUNCTIONAL DESCRIPTION

Overview

The Am79C988A Quad Integrated Ethernet Transceiver (QuIET™) device consists of four independent 10BASE-T transceivers which are compliant with the IEEE 802.3 Section 14 (*Medium Attachment Unit for 10BASE-T Cabling*) standard. The QuIET device includes on-chip filtering for both transmit and receive functions, thus eliminating the need for external filters. It provides automatic polarity detection and correction and can operate in either normal or full-duplex mode.

The QuIET device interfaces directly with the Pseudo AUI (PAUI™) ports on the IMR2 (Am79C983A) device. PAUI ports are functionally equivalent to the AUI interface as described in IEEE 802.3 Section 7, but are single-ended and do not have the drive capability specified in the standard. The QuIET device can also be connected to standard AUI ports. Command and status data is exchanged with the IMR2 device via a serial management interface.

Twisted Pair Transmitters

Each TXD port is a differential twisted pair driver. When properly terminated, TXD meets the 10BASE-T transmitter electrical requirements as specified in IEEE 802.3 Section 14.3.1.2. Proper termination, Figure 1, consists of a single 110 ohm ±1% resistor across TXD+ and TXD- and a 1:1 standard Ethernet transformer. A common mode may be required for EMI considerations. An external capacitor is not required. The load is a twisted pair cable that meets IEEE 802.3, Section 14.4 requirements. The cable is terminated at the other end by a 100 ohm load.

The TXD signal is filtered on the chip to reduce harmonic content per IEEE 802.3 Section 14.3.2.1 (10BASE-T). Since filtering is performed by the QuIET device, the TXD signal can be connected directly to a standard transformer. External filter modules are not required.

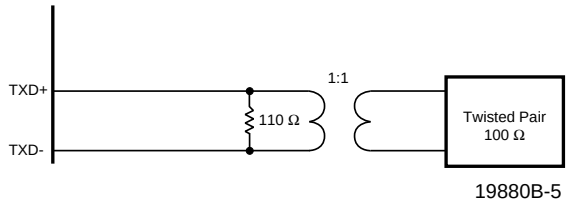


Figure 1. TXD Termination

Twisted Pair Receivers

Each RXD port is a differential twisted-pair receiver. When properly terminated, RXD ports will meet the electrical requirements for 10BASE-T receivers as specified in IEEE 802.3, Section 14.3.1.3. Proper termination is shown in Figure 2. Each receiver has internal filtering and does not require external filter modules.

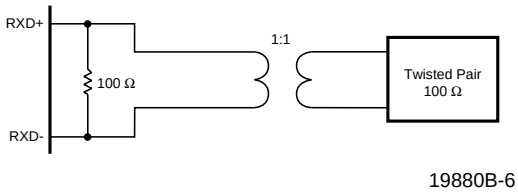


Figure 2. RXD Termination

Receive squelch threshold voltage can be programmed for extended distance mode. In this mode, the differential receive threshold is reduced to allow cable lengths greater than the 100 meters specified in the IEEE 802.3 Standard.

Polarity Detection and Reversal

The receive function includes the ability to invert the polarity of the signals appearing at the RXD± pair if the polarity of the received signal is reversed (such as in the case of a wiring error). The polarity detection function is activated following Reset or Link Fail, and will reverse the receive polarity based on both the polarity of any previous Link Test Pulses and the polarity of subsequent packets with a valid End Transmit Delimiter (ETD).

When in the Link Fail State, the QuIET device will recognize Link Test Pulses of either positive or negative polarity. Exit from the Link Fail state is caused by the reception of five-to-seven consecutive Link Test Pulses of identical polarity. Both Link Test Pulses and packets are used to determine the initial receive polarity. Once correct polarity is established, the receiver subsequently accepts only Link Test Pulses that are recognized as TRUE rather than inverted.

The Link Test pulse follows the template of Figure 14-12 of the IEEE 802.3 10BASE-T standard.

Link Test Function

The Link Test function is implemented as specified in the IEEE 802.3 10BASE-T standard. A Link Test pulse is transmitted if a port has been idle for a period of more than approximately 16 (+/-8) milliseconds (ms).

The QuIET device monitors the 10BASE-T ports for packet and Link Pulse activity. If neither a packet nor a Link Test pulse is received for 79 ms to 102 ms, the port will enter the Link Test Fail State and the QuIET device will inhibit the transmit and receive functions for that port. Link pulses are transmitted when idle conditions are met. When a packet or five-to-seven consecutive Link Test pulses is received, the port exits the Link Fail State and transmit/receive functions are restored.

PAUI Ports

The PAUI ports are functionally equivalent to AUI ports as described in IEEE 802.3, Section 7. However, they are single ended and, therefore, are not an exact match with the electrical specifications.

PDO, PDI, and PCI are functionally similar to DO, DI, and CI, respectively. PDO is the PAUI input from the IMR2 device. This signal is transmitted by the corresponding TXD port. PDI is the data output to the IMR2 device and is the data received by the corresponding RXD port. PDI also loops back data received by PDO to the IMR2 device. PCI is the collision output to the IMR2 device and indicates either a collision on the corresponding port or an excessive continuous data stream on the corresponding PDO. PCI sends a 10-MHz square wave during collision and jabber.

Collision Handling

Collision is defined for the QuIET device as data being simultaneously transmitted and received at the corresponding TXD and RXD pins. When a collision is detected, the QuIET device sends a 10 MHz signal over the corresponding PCI pin. This is the only action taken by the QuIET device. The generation of the JAM signal is performed by the IMR2 device.

Jabber Protection

The Jabber function inhibits the twisted pair transmit function of the port if the PDO circuit is active for an excessive period (> 30 ms). If the maximum transmit time is exceeded, the transmitter circuitry is disabled, PDO to PDI loopback is disabled, and a 10 MHz signal is transmitted by PCI. Once the data stream is removed from PDO, 350 ms will elapse before PCI stops transmitting the 10 MHz signal and the TXD circuitry is enabled again. Note that a properly functioning repeater device will never jabber because of the MAU Jabber Lockup Protection (MJLP).

Transceiver Modes

The QuIET transceivers have two modes of operation: Normal and Full Duplex. In Normal mode, the data flows only in one direction at a time. In Full-Duplex mode, the collision circuitry and the loopback circuitry are disabled. Therefore, transmit and receive can occur simultaneously. The transceiver mode is selected through the serial management interface, which is explained further in the *Management Commands* and *Transceiver Mode Selection* sections.

Normal Mode

The QuIET device defaults to the Normal mode at power up and reset. In this mode, no twisted pair port can transmit and receive data simultaneously. If a port receives data when it is transmitting, the QuIET device sends a collision signal to the IMR2 device via the corresponding PCI pin.

Note: *The IMR2 device only supports Normal operation.*

Full-Duplex Mode

In Full-Duplex mode a port can transmit and receive simultaneously, and Collision and PAUI Loopback functions are disabled. The normal loopback of PDO to PDI is disabled to allow the RXD signal to be transmitted on PDI.

PCI is disabled and Jabber status is only available to the controller through the serial management interface. The serial management interface also transmits Jabber status when the QuIET device is in Normal mode.

Serial Management Interface

Command and status data are transferred between the QuIET device and the IMR2 device via SDATA. (See Figure 4 for proper interconnections.) The direction of SDATA is set by DIR. All activity on SDATA starts at the edge (rising or falling) of DIR.

The DIR pin of the QuIET device connects to DIR[1] of the IMR2 device. The IMR2 device continually cycles DIR[1] LOW and HIGH. LOW is status reporting (SDATA Write) and HIGH is management commands (SDATA Read). The controller (IMR2 device) should keep DIR at one level for the entire bit stream. The status bit stream is described in the *Status Reporting* section, and the command bit stream is described in the *Management Commands* section. Each bit on SDATA is held for 2-bit times (200 ns).

Status Reporting

When DIR switches from HIGH to LOW, the QuIET device drives SDATA with status information (left to right) in the format shown below. After the 29th bit, the SDATA driver turns off. The SDATA driver also turns off if DIR switches HIGH before the 29th bit.

Status Information Format

$01010A_0A_1A_2A_3B_0B_1B_2B_3C_0C_1C_2C_3D_0D_1D_2D_3SSSSSSSS$

01010	Preamble
A_n	QuIET device ID (0000 for QuIET device)
B_n	0 Link Fail 1 Link Pass
C_n	0 Received Polarity Reversed 1 Received Polarity Correct
D_n	0 No Jabber 1 Jabber
S	Not used, logic HIGH

Preamble

The 01010 preamble is an indication to the IMR2 that the transceiver is a QuIET device.

QuIET Device ID

$A_0A_1A_2A_3$

The QuIET device returns 0000.

Link Status

$B_0B_1B_2B_3$

The QuIET device reports the Link Status of each port. If Link Test is disabled, Link Status indicates a Link Pass.

B_n	0	Link Fail
	1	Link Pass

Receive Polarity Status

$C_0C_1C_2C_3$

The QuIET device reports the polarity status of each port.

C_n	0	Reversed Polarity
	1	True Polarity

Jabber Condition

$D_0D_1D_2D_3$

The QuIET device reports the Jabber Condition status for each port. Jabber is defined as continuous transmissions by a port for more than 30 ms.

D_n	0	No Jabber
	1	Jabber

Management Commands

When DIR switches from LOW to HIGH, the QuIET device reads the command sequence over SDATA. Each management command character is held for 2-bit times (200 ns). The command format is as follows.

Management Command Format

$0E_0E_1E_2E_3F_0F_1F_2F_3G_0G_1G_2G_3H_0H_1H_2H_3I\ J_0J_1J_2J_3KSSSSSSS$

E_n	Extended Distance	0 Disabled 1 Enabled
F_n	Link Test	0 Disabled 1 Enabled
G_n	Transmit Link Test Pulses	0 Disabled 1 Enabled
H_n	Enable Polarity Correction	0 Enabled 1 Disabled
I	Loopback Test (All Ports)	0 Enabled 1 Disabled
J_n	Transceiver Mode	0 Full Duplex 1 Normal (Default condition - IMR2 only supports Normal)
K	CMOS/PAUI Mode	0 CMOS Mode 1 PAUI Mode
S	Not used	Logic HIGH

Note: *The QuIET device requires DIR to be high for a minimum of 29 data bits (one bit is four MCLKs), which automatically occurs with the IMR2 device. If any other type of controller is used, DIR must still be high at least 29-bit times. After I, SDATA can be all ones.*

Extended Distance Option

$E_0E_1E_2E_3$

This command modifies the RXD circuit of the transceiver to accommodate signal-attenuation lines longer than 100 meters.

E_n	0	Disable Extended Distance Option
	1	Enable Extended Distance Option

Link Test Enable

$F_0F_1F_2F_3$

This command enables the corresponding port to perform a Link Test. Link Status will report Link Pass if the Link Test is disabled.

F_n	0	Disable Link Test
	1	Enable Link Test

Transmit Link Pulse Enable

$G_0G_1G_2G_3$

This command enables the corresponding port to transmit a Link Pulse. The pulse will be transmitted if either a packet or a pulse has not been transmitted for 16 ms. Note that Link Pulses are transmitted when ports are in Link Test Fail.

G_n	0	Disable Link Pulse Transmit
	1	Enable Link Pulse Transmit

Auto Polarity Correction Enable

$H_0H_1H_2H_3$

This command allows the QuIET device to detect and correct the polarity of signals at RXD.

H_n	0	Enable Auto Polarity
	1	Disable Auto Polarity

Loopback Test Enable

This command enables or disables the loopback test for the twisted pair ports. When enabled, the signal on RXD is retransmitted on TXD. The default condition is loopback test disabled. Note that the TXD drivers have on-chip filtering, which may cause the TXD output to be different from the corresponding RXD input during this test.

I	0	Enable Loopback Test
	1	Disable Loopback Test

Transceiver Mode Selection

$J_0J_1J_2J_3$

This command sets the QuIET device either in Full-Duplex or Normal mode. The default is Normal mode.

J_n	0	Full Duplex
	1	Normal

CMOS/PAUI Mode Selection

This command sets the QuIET interface drivers (PDO, PDI, PCI) to be driven at normal PAUI signal levels or CMOS voltage levels. The default is PAUI levels. Refer to the DC Characteristics table for voltage levels.

K	0	CMOS Levels
	1	PAUI Levels

Reset Function

The QuIET device enters the reset state when the reset pin ($\overline{RST}$) is held LOW. All ports, status registers, and command registers are put into their default state. When powering up the device, the $\overline{RST}$ pin should be held LOW for 150 microseconds (µs). At other times, the $\overline{RST}$ pin should be held LOW for a minimum of 4 µs. The default conditions are detailed below.

Command and Status Default Conditions

Command	Default
Extended Distance	Disabled
Link Test	Enabled
Link Pulse Transmit	Enabled
Correct Polarity	Disabled
Loopback Test	Disabled
Transceiver Mode Selection	Normal
CMOS/PAUI Mode	PAUI Mode

Status	Default
Device	QuIET
Link	Fail
Polarity	Correct
Jabber	No Error

SYSTEMS APPLICATIONS

10BASE-T Repeaters

The IMR2/QuIET chipset provides a system solution to designing 10BASE-T repeaters. Figure 3 shows the necessary connections between the IMR2 device and the QuIET device. Although only one QuIET device is shown for clarity, three QuIET devices are required to build a 12-port 10BASE-T repeater.

Port Switching

The IMR2/QuIET chipset supports port switching, which is the ability to move individual ports to any one of multiple Ethernet backplanes under software control. To implement port switching, each port on the QuIET device is connected to two or more IMR2 devices in parallel. Each IMR2 device defines a different logical repeater and constitutes a separate Ethernet collision domain. For each port on the QuIET device, only one corresponding port on the IMR2 devices is enabled at any one time.

Figure 4 shows the IMR2 device-to-QuIET device connections necessary for port switching. Note that only one QuIET device is shown for clarity. A full implementation would use three QuIET devices to provide 12 10BASE-T ports that can be individually switched between three Ethernet collision domains.

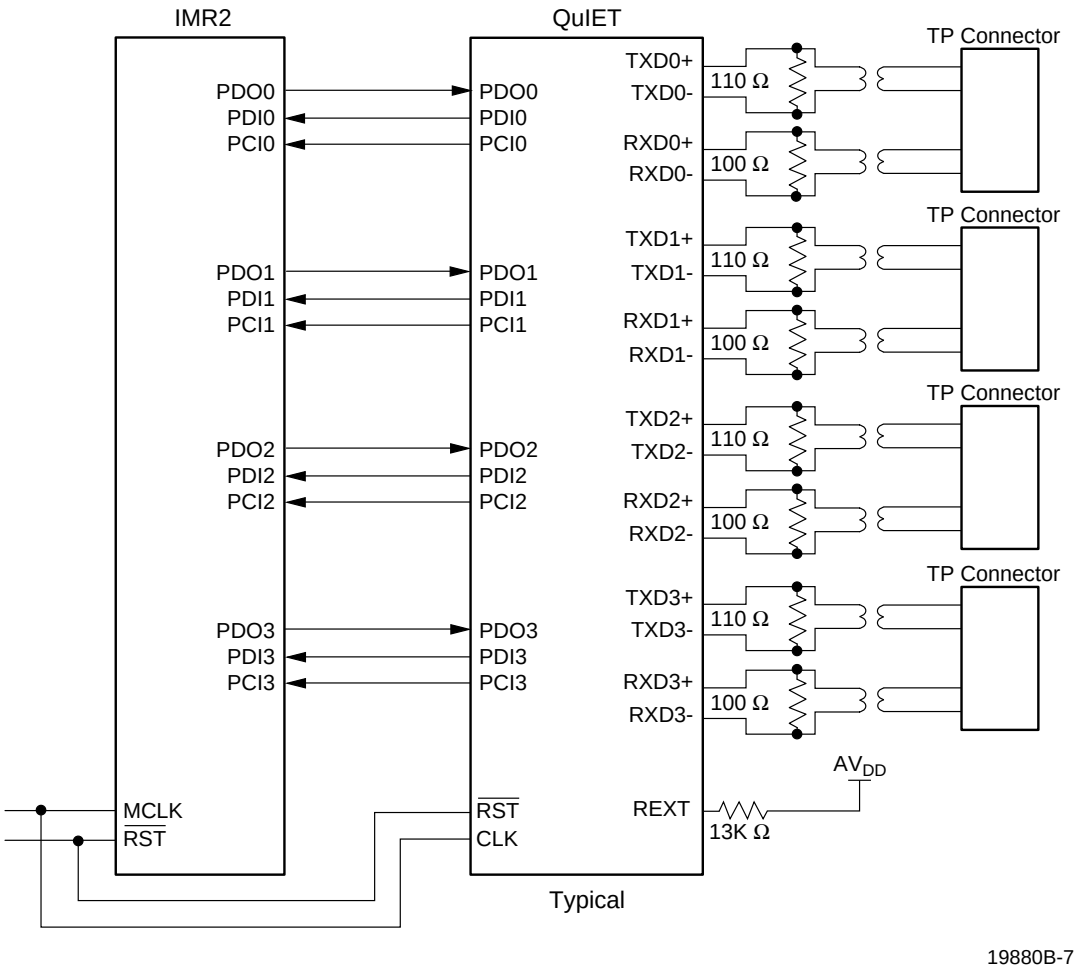
The IMR2 and QuIET devices must share a common ground plane and a common power plane. Failure to meet this design requirement may result in false assertion of internal carrier sense or inability to unsquelch in either PDI (for IMR2) or PDO (for QuIET).

Connection to Standard AUI Port

The PAUI ports on the QuIET device can also be connected to standard AUI ports when used with devices other than the IMR2 chip. Connection to a standard AUI port is not meant to support a full length AUI cable. The AUI connection should remain on the same board as shown in Figure 6.

Connection to CMOS Circuits

The PAUI ports on the QuIET device can also drive CMOS loads for other devices, including switches. The PDO, PDI, and PCI signals connect directly to the CMOS device. Note that CMOS mode must be selected in the Management Command Frame.



***Note**: Common mode chokes may be required.*

Figure 3. IMR2 Device to QuIET Device Connection

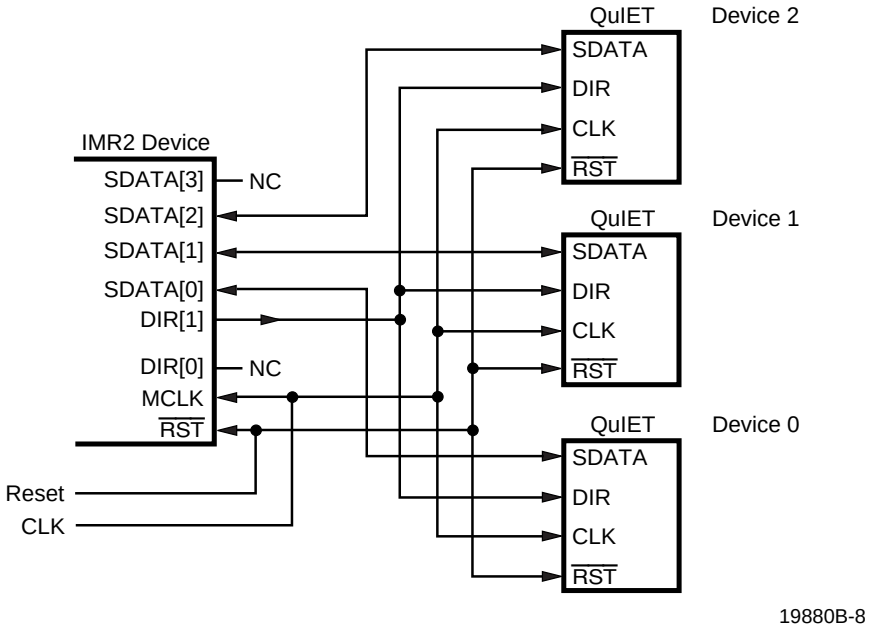


Figure 4. IMR2 Device To QuIET Device Serial Interface

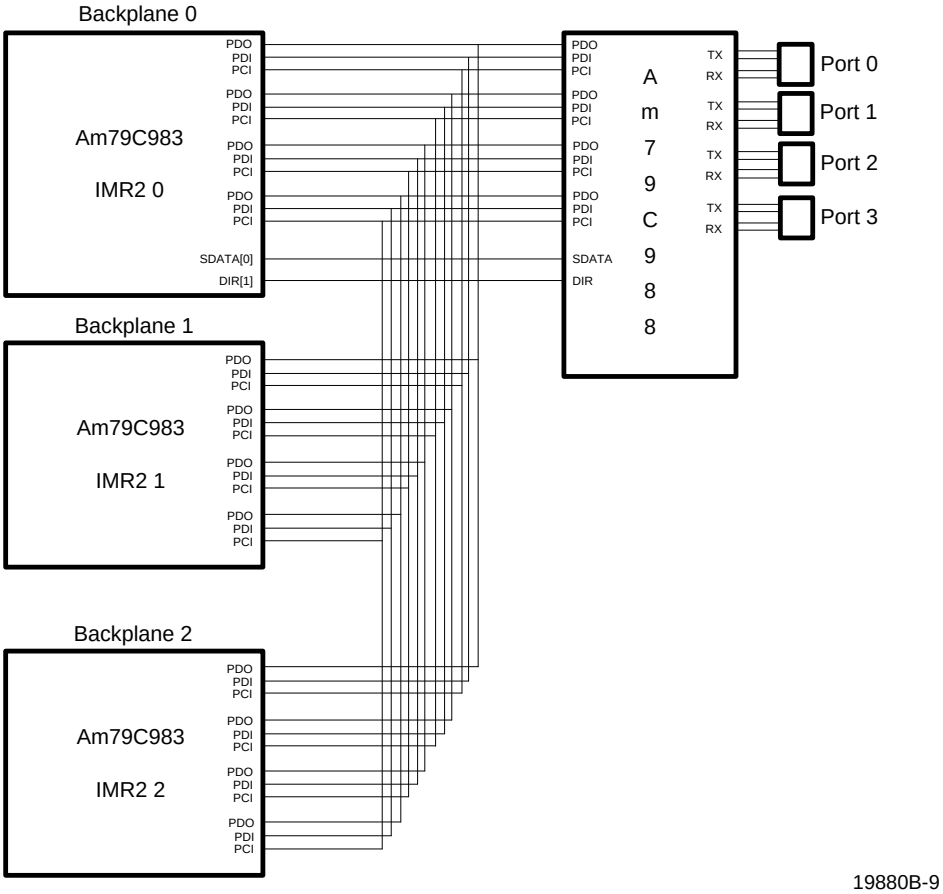


Figure 5. Port Switching

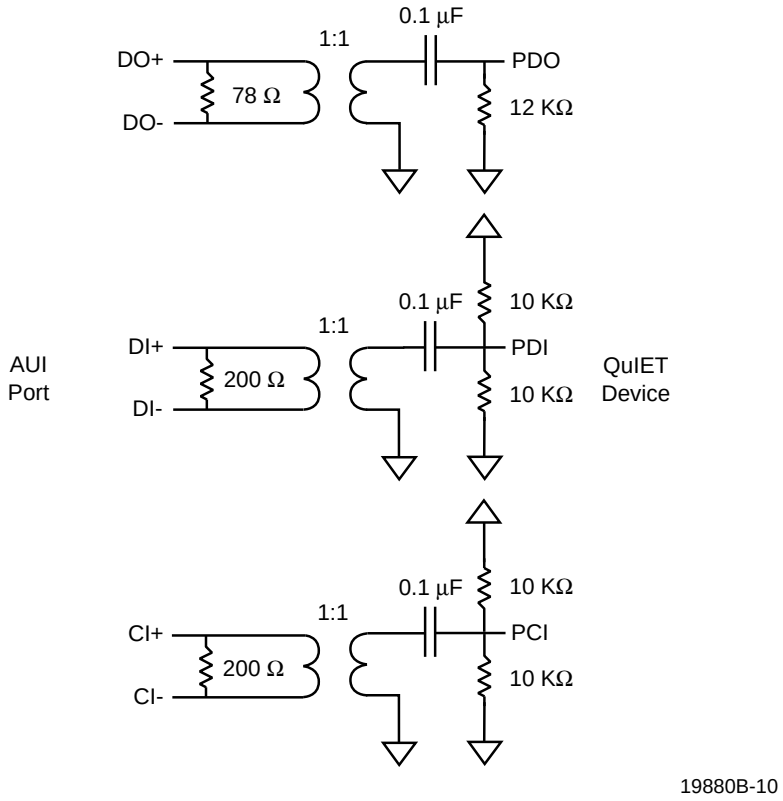


Figure 6. AUI to PAUI Connections

ABSOLUTE MAXIMUM RATINGS

Storage Temperature. . . . . –65°C to +150°C

Ambient Temperature Under Bias. . . . . 0 to 70°C

Supply Voltage referenced to

AV_{SS} or DV_{SS} (AV_{DD}, DV_{DD}) . . . . . .–0.3 to +6V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (TA) . . . . . .0°C to + 70° C

Supply Voltages (V_{DD}). . . . . +5 V ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Digital I/O					
V_{IL}	Input LOW Voltage	DV_{SS} = 0.0 V	-0.5	0.8	V
V_{IH}	Input HIGH Voltage		2.0	DV_{DD} +0.5	V
V_{OL}	Output LOW Voltage	I_{OL}=4.0 mA	-	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} =-0.4 mA	2.4	-	V
I_{IH}	Input Leakage Current HIGH (DIR, SDATA, CLK, $\overline{RST}$)	$0<V_{IN}<DV_{DD}$	-	10	µA
I_{IL}	Input Leakage Current LOW (DIR, SDATA, CLK, TEST)	$0V<V_{IN}<DV_{DD}$	-	-10	µA
I_{ILDH}	Input Leakage Current HIGH ($\overline{TEST}$)	$0<V_{IN}<DV_{DD}$	-	500	µA
I_{ILDL}	Input Leakage Current LOW ($\overline{RST}$)	$0V<V_{IN}<DV_{DD}$	-	-500	µA
PAUI Ports					
V_{POH}	Output HIGH Voltage	PAUI Mode	$V_{DD/2}$ + 0.45	-	V
V_{POL}	Output LOW Voltage	PAUI Mode	-	$V_{DD/2}$ - 0.45	V
V_{PIH}	Input HIGH Voltage	PAUI Mode	$V_{DD/2}$ + 0.45	-	V
V_{PIL}	Input LOW Voltage	PAUI Mode	-	$V_{DD/2}$ - 0.45	V
I_{PILH}	Input Leakage Current HIGH	AV_{DD} = MAX	-	10	µA
I_{PILL}	Input Leakage Current LOW	AV_{DD} = MAX	-	-10	µA
V_{PASQ}	PDO Squelch (the value PDO must go to before internal PDO carrier sense can be turned on)		$V_{DD/2}$ - 0.400	$V_{DD/2}$ - 0.175	mV
Twisted Pair Ports					
I_{IRXD}	Input Current at RXD±	$AV_{SS}<V_{IN}<AV_{DD}$	-500	500	µA
R_{RXD}	RXD Differential Input Resistance	(Note 1)	10	-	kΩ
V_{TIVB}	RXD±, Open Circuit Input Voltage (Bias)	I_{IN} = 0 mA	AV_{DD}-3.0	AV_{DD}-1.5	V
V_{TIDV}	Differential Mode Input Voltage Range (RXD)	AV_{DD} = 5.0 V	-3.1	3.1	V
V_{TSQ+}	RXD Positive Squelch Threshold (Peak)	Sinusoid 5 MHz <f< 10 MHz	300	520	mV
V_{TSQ-}	RXD Negative Squelch Threshold (Peak)	Sinusoid 5 MHz <f< 10 MHz	-520	-300	mV
V_{THS+}	RXD Post-Squelch Positive Threshold (Peak)	Sinusoid 5 MHz <f< 10 MHz	120	293	mV
V_{THS-}	RXD Post-Squelch Negative Threshold (Peak)	Sinusoid 5 MHz <f< 10 MHz	-293	-120	mV

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{LTSQ+}	RXD Positive Squelch Threshold Extended Distance Mode	Sinusoid 5 MHz <f< 10 MHz	180	312	mV
V_{LTSQ-}	RXD Positive Squelch Threshold Extended Distance Mode	Sinusoid 5 MHz <f< 10 MHz	-312	-180	mV
V_{LTHS+}	RXD Post-Squelch Positive Threshold Extended Distance Mode	Sinusoid 5 MHz <f< 10 MHz	80	175	mV
V_{LTHS-}	RXD Post-Squelch Negative Threshold Extended Distance Mode	Sinusoid 5 MHz <f< 10 MHz	-175	-80	mV
V_{RXDTH}	RXD Switching Threshold	(Note 1)	-60	+60	mV
V_{TXI}	TXD± Differential Output Voltage Imbalance		-40	+40	mV
I_{TXOFF}	TXD± Idle Output Current	DV_{DD} = 5V (Note 2)	-2	2	µA
Power Supply Current					
I_{DDTX}	Power Supply Current (All 4 ports Transmitting Including TXD current)	F = 20 MHz $V_{DD} = V_{MAX}$ (Uses Twisted Pair Switching Test Current)	-	380	mA
I_{DDI}	Power Supply Current Idle	F= 20 MHz $V_{DD} = V_{MAX}$	-	120	mA

Note:

1. CMOS Mode on PAUI signals is guaranteed by design and is compatible with normal CMOS levels present on other QuIET device pins.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Clock and Reset Timing					
t_{CLK}	CLK Clock Period	(Note 1)	49.995	50.005	ns
t_{CLKH}	CLK Clock High		20	30	ns
t_{CLKL}	CLK Clock Low		20	30	ns
t_{CLKR}	CLK Rise Time	(Note 1)	-	10	ns
t_{CLKF}	CLK Fall Time	(Note 1)	-	10	ns
t_{RST}	Reset Pulse Width ($\overline{RST}$ pin LOW)		4	-	µs
t_{PRST}	Reset Pulse Width at Power Up		150	-	µs
Transmit Timing					
t_{PWODO}	PDO Pulse Width Accept/ Reject Threshold	Input > V_{ASQ} (Max) (Note 3)	15	35	ns
t_{PWKDO}	PDO Pulse Width Maintain/Turn-Off Threshold	Input > V_{ASQ} (Max) (Note 4)	110	200	ns
t_{TON}	Transmit Start-Up Delay		-	300	ns
t_{TSD}	Transmit Static Propagation Delay (PDO to TXD)		-	200	ns
t_{TETD}	Transmit End of Transmission (for TXD)		250	450	ns
t_{PERLP}	Idle Signal Period	(Note 7)	8	24	ms
t_{PWLP}	Link Pulse Width	(Note 1)	75	120	ns
t_{JA}	Transmit Jabber Activation Time	(Note 7)	20	150	ms
t_{JR}	Transmit Jabber Reset Time	(Note 7)	250	750	ms
t_{JREC}	Transmit Jabber Recovery Time (Minimum time gap between packets to prevent Jabber activation)	(Note 1)	1.0	-	µs
t_{DODION}	PDO to PDI Start-up Delay			300	ns
t_{DODISD}	PDO to PDI Static Propagation Delay		-	100	ns
Receive Timing					
t_{PWORD}	RXD Pulse Width Accept/Reject Threshold	(Note 5)	5	35	ns
t_{PWKRD}	RXD Pulse Width Maintain/Turn-Off Threshold	(Note 6)	136	200	ns
t_{RON}	Receiver Start-up Delay (RXD to PDI)		200	400	ns
t_{RVD}	First Validly Timed Bits		-	t_{RON} +100	ns
t_{RSD}	Receiver Static Propagation Delay (RXD to PDI)		-	70	ns
t_{RETD}	PDI End of Transmission		200	-	ns
t_{RR}	PDI, PCI Rise Time	(Note 1)	-	10	ns
t_{RF}	PDI, PCI Fall Time	(Note 1)	-	10	ns
t_{RM}	PDI, PCI Rise and Fall Time Mismatch (t_{RR} - t_{RF})	(Note 1)	-	5	ns
Collision Timing					
t_{CON}	Collision Turn On Delay		-	500	ns
t_{COFF}	Collision Turn Off Delay		-	500	ns
t_{CPER}	Collision Period	(Note 1)	87	117	ns
t_{CPW}	Collision Output Pulse Width	(Note 1)	40	60	ns
Serial Interface Timing					
t_{SDSU}	CLK to DIR Setup Time	(Note 7)	10	-	ns
t_{SDHD}	DIR Hold Time	(Note 7)	10	-	ns
t_{SSSU}	CLK to SDATA Setup Time	(Note 7)	10	-	ns
t_{SSHD}	CLK to SDATA Hold Time	(Note 7)	10	-	ns
t_{SSDO}	CLK to Output Delay		-	40	ns

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
t_{SSDOZ}	Clock to High Impedance Output		-	40	ns
t_{SDS}	DIR going HIGH to SDATA Input Valid	(Note 7)	-50	100	ns
t_{DDS}	DIR going LOW to SDATA Output Valid	(Note 7)	100	150	ns

***Notes**:*

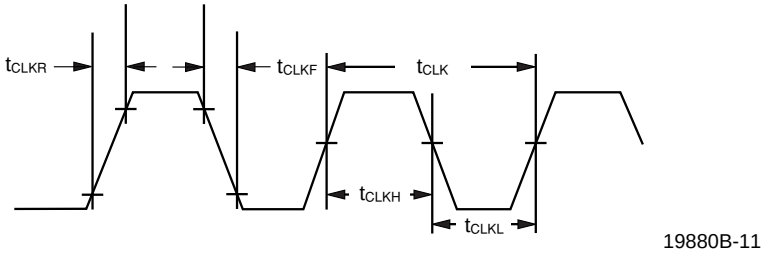
1. *Parameter is not tested.*
2. *Uses switching test load.*
3. *PDO pulses narrower than t_{PWODO} (min) will be rejected; PDO pulses wider than t_{PWODO} (max) will turn internal PDO carrier sense on.*
4. *PDO pulses narrower than t_{PWKDO} (min) will maintain internal PDO carrier sense on; PDO pulses longer than t_{PWKDO} (max) will turn internal PDO carrier sense off.*
5. *RXD pulses narrower than t_{PWORD} (min) will be rejected; RXD pulses longer than t_{PWORD} (max) will turn internal RXD carrier sense on.*
6. *RXD pulses narrower than t_{PWKRD} (min) will maintain internal RXD carrier sense; RXD pulses longer than t_{PWKRD} (max) will turn internal RXD carrier sense off.*
7. *Parameter tested functionally.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

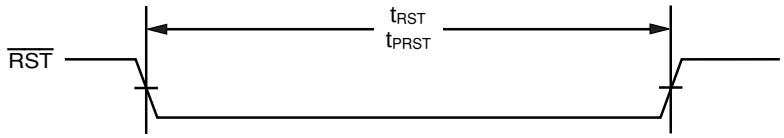
KS00010

SWITCHING WAVEFORMS



19880B-11

Figure 7. Clock (CLK) Timing



19880B-12

Figure 8. Reset Pulse

SWITCHING WAVEFORMS

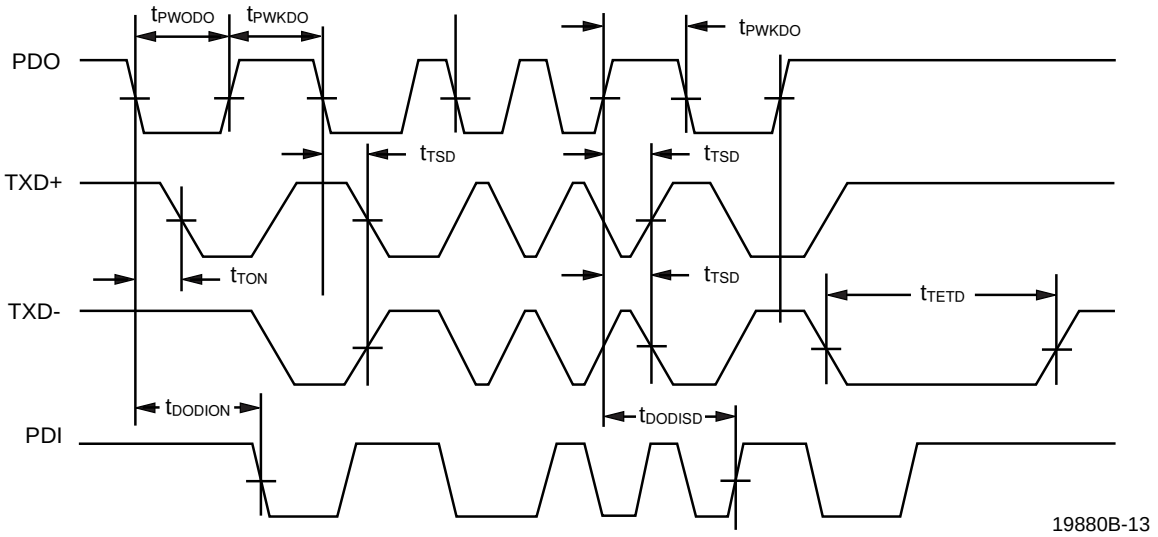


Figure 9. Transmit Signals

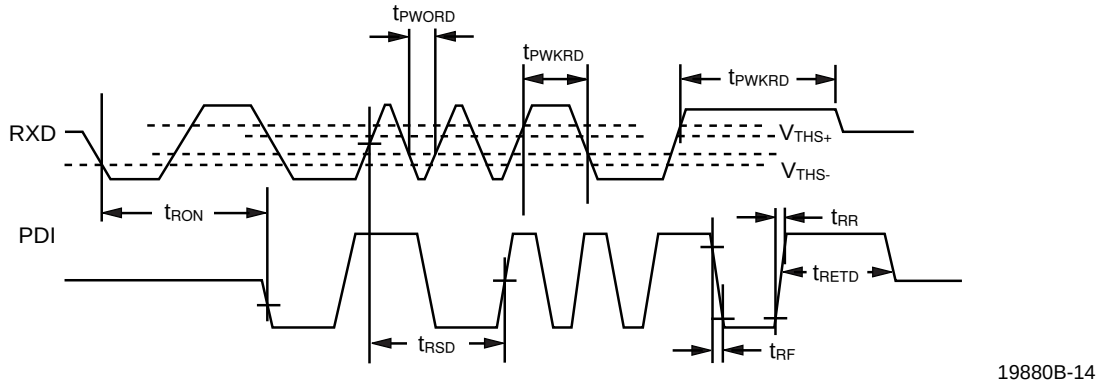


Figure 10. Receive Signals

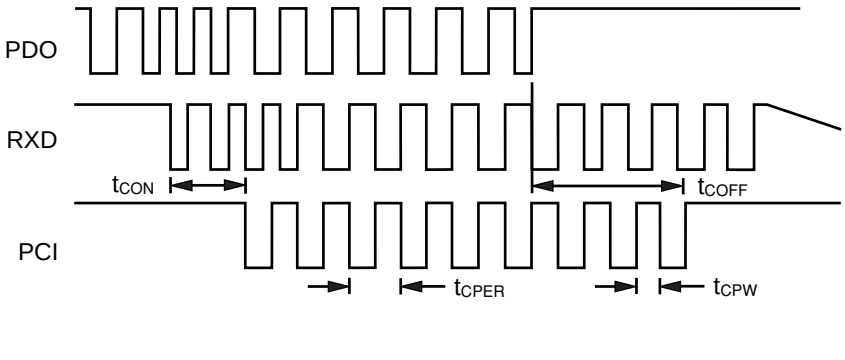


Figure 11. Collision Signals

SWITCHING WAVEFORMS

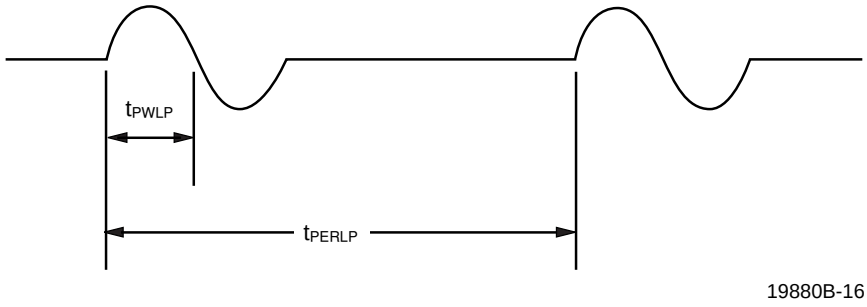


Figure 12. Transmit Link Beat Pulse

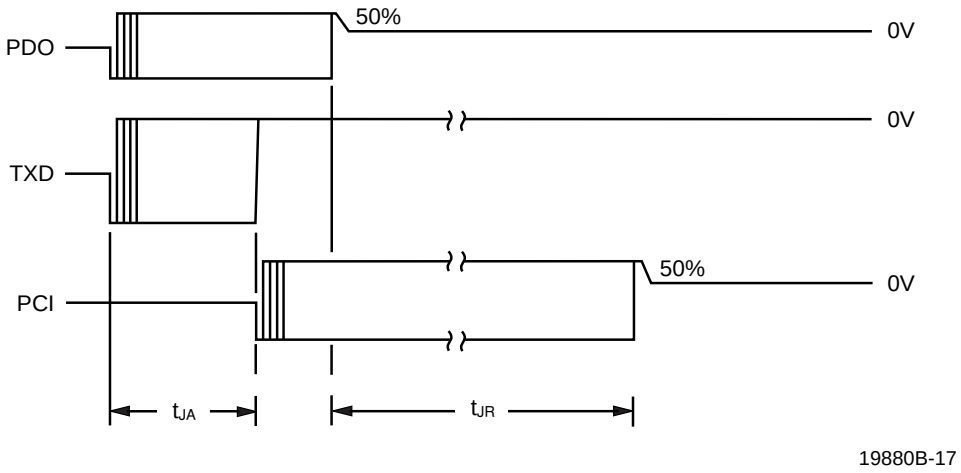


Figure 13. Jabber Function

SWITCHING WAVEFORMS

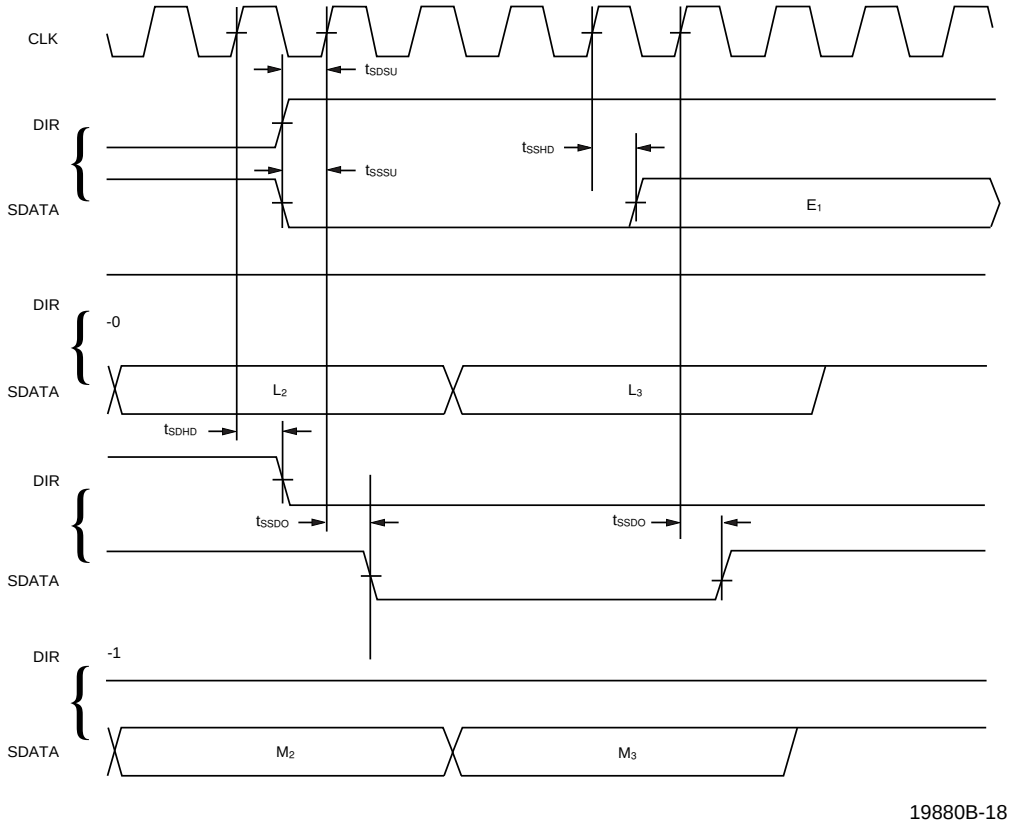


Figure 14. Serial Interface Waveforms

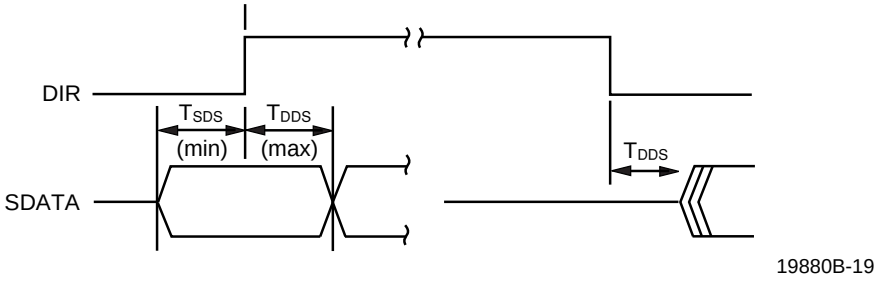


Figure 15. Serial Interface SDATA Transmit and Start Receive

SWITCHING TEST CIRCUITS

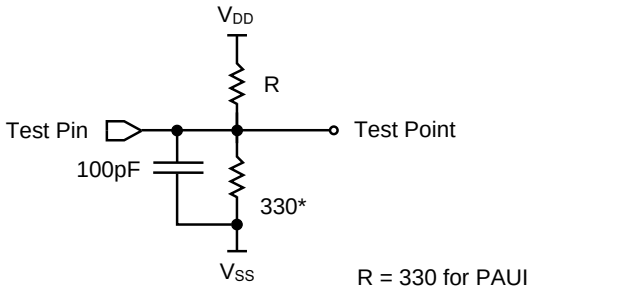


Figure 16. Switching Test Circuit

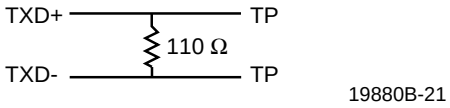
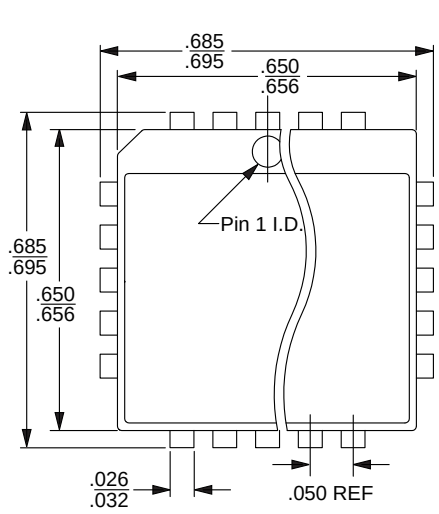


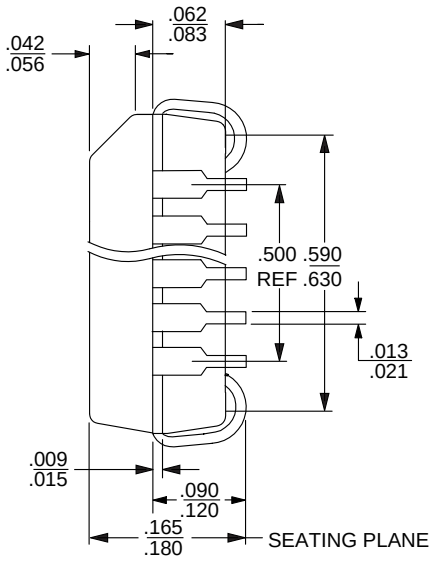
Figure 17. Twisted Pair Switching Test Circuit

PHYSICAL DIMENSIONS*

PL 044
44-Pin Plastic Leaded Chip Carrier (Measured in inches)



TOP VIEW



SIDE VIEW

16-038-SQ
PL 044
EC80
11.3.97 lv

REVISION SUMMARY

This revision (B) reflects changes to Figures 3, 6, and 17. Changes have also been made to the Ordering Information page, and the DC Characteristics and Switching Characteristics tables. No other technical changes have been made.