

CMOS single-chip 8-bit microcontrollers

87C51FA/87C51FB

DESCRIPTION

The 87C51FA and 87C51FB Single-Chip 8-Bit Microcontrollers are manufactured in an advanced CMOS process and are derivatives of the 80C51 microcontroller family. The 87C51FA/FB has the same instruction set as the 80C51.

This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 87C51FA contains $8k \times 8$ memory, and the 87C51FB contains $16k \times 8$ memory. They both contain a volatile 256×8 read/write data memory, four 8-bit I/O ports, three 16-bit timer/event counters, a Programmable Counter Array (PCA), a multi-source, two-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C51FA/FB can be expanded using standard TTL compatible memories and logic.

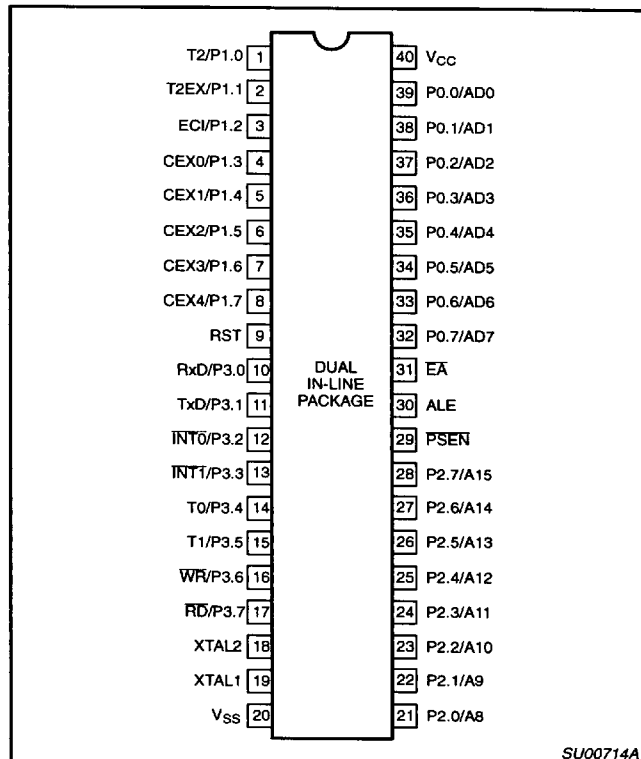
Its added features make it an even more powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multiprocessor communications.

See 83C51FA/83C51FB/83C51FC/80C51FA datasheet for ROM and ROMless devices.

FEATURES

- 80C51 central processing unit
- 87C51FA: $8k \times 8$ EPROM
87C51FB: $16k \times 8$ EPROM
 - expandable externally to 64k bytes
 - Quick Pulse programming algorithm
 - Two level program security system
- 256×8 RAM, expandable externally to 64k bytes
- Three 16-bit timer/counters
 - T2 is an up/down counter
- Programmable Counter Array (PCA)
 - High speed output
 - Capture/compare
 - Pulse Width Modulator
 - Watchdog Timer
- Four 8-bit I/O ports
- Full-duplex enhanced UART
 - Framing error detection
 - Automatic address recognition
- Power control modes
 - Idle mode
 - Power-down mode
- Once (On Circuit Emulation) Mode
- Five package styles
- OTP package available

PIN CONFIGURATIONS



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ORDERING INFORMATION

8k × 8 EPROM ¹	16k × 8 EPROM ¹		TEMPERATURE RANGE °C AND PACKAGE	FREQ. (MHz)	DRAWING NUMBER
S87C51FA-4N40	S87C51FB-4N40	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	3.5 to 16	SOT129-1
S87C51FA-4F40	S87C51FB-4F40	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 16	0590B
S87C51FA-4A44	S87C51FB-4A44	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	3.5 to 16	SOT187-2
S87C51FA-4K44	S87C51FB-4K44	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 16	1472A
S87C51FA-4B44	S87C51FB-4B44	OTP	0 to +70, 44-Pin Plastic Quad Flat Pack	3.5 to 16	SOT307-2
S87C51FA-5N40	S87C51FB-5N40	OTP	-40 to +85, 40-Pin Plastic Dual In-line Package	3.5 to 16	SOT129-1
S87C51FA-5F40	S87C51FB-5F40	UV	-40 to +85, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 16	0590B
S87C51FA-5A44	S87C51FB-5A44	OTP	-40 to +85, 44-Pin Plastic Leaded Chip Carrier	3.5 to 16	SOT187-2
S87C51FA-5B44	S87C51FB-5B44	OTP	-40 to +85, 44-Pin Plastic Quad Flat Pack	3.5 to 16	SOT307-2
S87C51FA-AN40	S87C51FB-AN40	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	3.5 to 24	SOT129-1
S87C51FA-AF40	S87C51FB-AF40	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 24	0590B
S87C51FA-AA44	S87C51FB-AA44	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	3.5 to 24	SOT187-2
S87C51FA-AK44	S87C51FB-AK44	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 24	1472A
S87C51FA-BN40	S87C51FB-BN40	OTP	-40 to +85, 40-Pin Plastic Dual In-line Package	3.5 to 24	SOT129-1
S87C51FA-BF40	S87C51FB-BF40	UV	-40 to +85, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 24	0590B
S87C51FA-BA44	S87C51FB-BA44	OTP	-40 to +85, 44-Pin Plastic Leaded Chip Carrier	3.5 to 24	SOT187-2

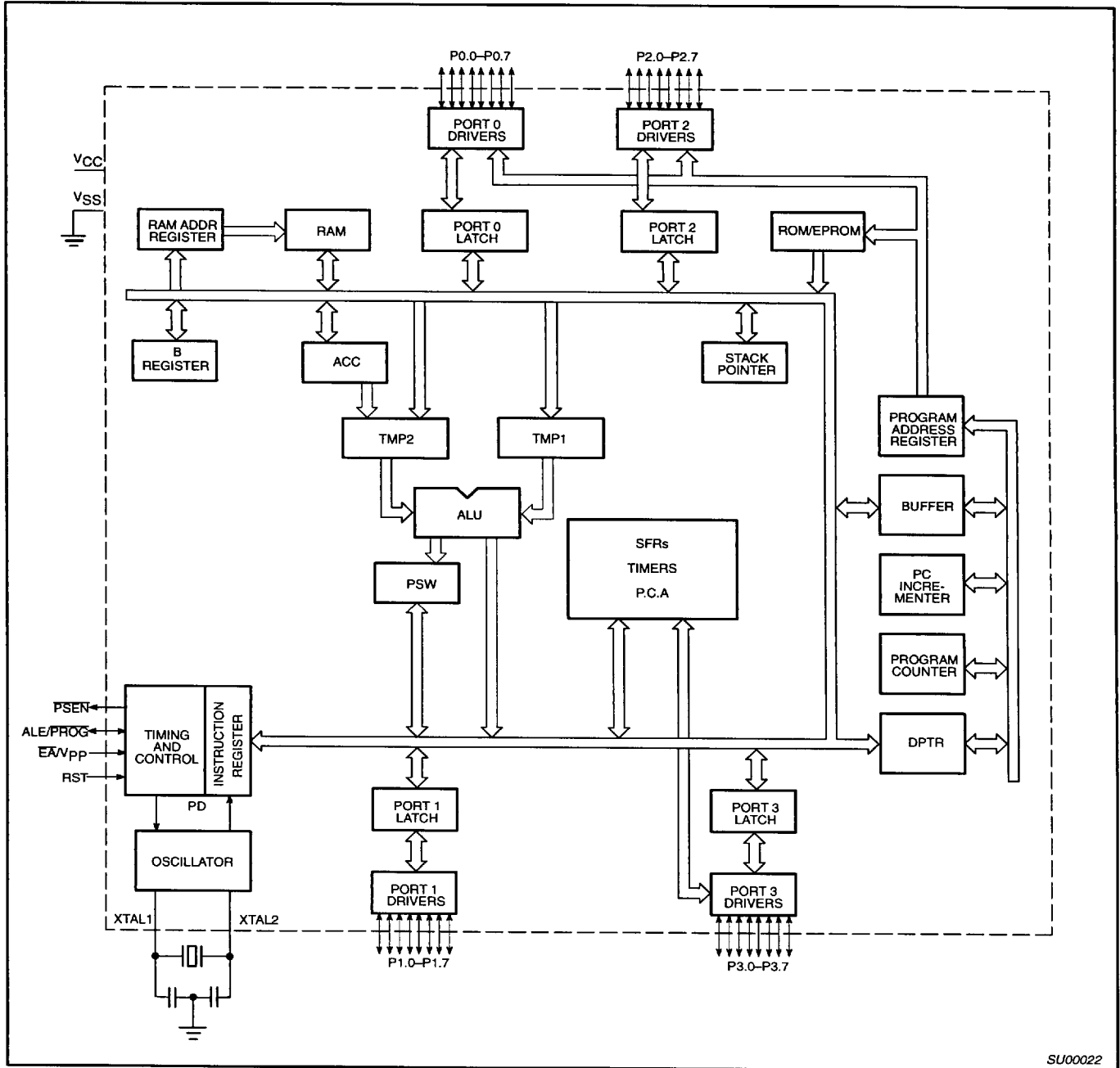
NOTE:

1. OTP = One Time Programmable EPROM. UV = Erasable EPROM.

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BLOCK DIAGRAM



SU00022

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Table 1. 87C51FA/87C51FB Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB				LSB				
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	-	-	-	-	-	-	-	AO	xxxxxxx0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
CCAP0H#	Module 0 Capture High	FAH									xxxxxxxB
CCAP1H#	Module 1 Capture High	FBH									xxxxxxxB
CCAP2H#	Module 2 Capture High	FCH									xxxxxxxB
CCAP3H#	Module 3 Capture High	FDH									xxxxxxxB
CCAP4H#	Module 4 Capture High	FEH									xxxxxxxB
CCAP0L#	Module 0 Capture Low	EAH									xxxxxxxB
CCAP1L#	Module 1 Capture Low	EBH									xxxxxxxB
CCAP2L#	Module 2 Capture Low	ECH									xxxxxxxB
CCAP3L#	Module 3 Capture Low	EDH									xxxxxxxB
CCAP4L#	Module 4 Capture Low	EEH									xxxxxxxB
CCAPM0#	Module 0 Mode	DAH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x000000B
CCAPM1#	Module 1 Mode	DBH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x000000B
CCAPM2#	Module 2 Mode	DCH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x000000B
CCAPM3#	Module 3 Mode	DDH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x000000B
CCAPM4#	Module 4 Mode	DEH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x000000B
CCON*#	PCA Counter Control	D8H	DF	DE	DD	DC	DB	DA	D9	D8	00x0000B 00H 00H
CH#	PCA Counter High	F9H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	
CL#	PCA Counter Low	E9H									
CMOD#	PCA Counter Mode	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx00B
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
IE*	Interrupt Enable	A8H	AF	AE	AD	AC	AB	AA	A9	A8	00H
			EA	EC	ET2	ES	ET1	EX1	ET0	EX0	
IP*	Interrupt Priority	B8H	BF	BE	BD	BC	BB	BA	B9	B8	x000000B
			-	PPC	PT2	PS	PT1	PX1	PT0	PX0	
P0*	Port 0	80H	87	86	85	84	83	82	81	80	FFH
			AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
P1*	Port 1	90H	97	96	95	94	93	92	91	90	FFH
			CEX4	CEX3	CEX2	CEX1	CEX0	ECl	T2EX	T2	
P2*	Port 2	A0H	A7	A6	A5	A4	A3	A2	A1	A0	FFH
			AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
			RD	WR	T1	T0	INT1	INT0	TxD	RxD	
PCON#	Power Control	87H	SMOD1	SMOD0	-	POF1	GF1	GF0	PD	IDL	00xxx00B

* SFRs are bit addressable.

SFRs are modified from or added to the 80C51 SFRs.

1. Reset value depends on reset source.

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Table 1. 87C51FA/87C51FB Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB							LSB	
PSW*	Program Status Word	D0H	D7	D6	D5	D4	D3	D2	D1	D0	00H
			CY	AC	F0	RS1	RS0	OV	-	P	
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxx0B
SCON*	Serial Control	98H									9F
SP	Stack Pointer	81H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
											07H
TCON*	Timer Control	88H	8F	8E	8D	8C	8B	8A	89	88	00H
			TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
T2CON*	Timer 2 Control	C8H	CF	CE	CD	CC	CB	CA	C9	C8	00H
			TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	
T2MOD#	Timer 2 Mode Control	C9H	-	-	-	-	-	-	T2OE ²	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH	00H								
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H

* SFRs are bit addressable.

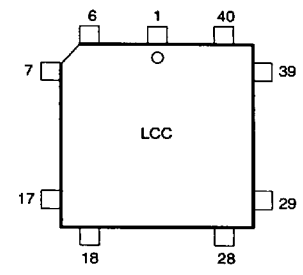
SFRs are modified from or added to the 80C51 SFRs.

2. T2OE – see Programmable Clock-Out.

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CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

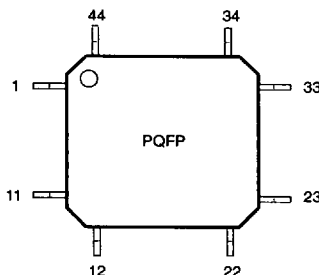


Pin	Function	Pin	Function	Pin	Function
1	NC*	16	P3.4/T0	31	P2.7/A15
2	P1.0/T2	17	P3.5/T1	32	PSEN
3	P1.1/T2EX	18	P3.6/WR	33	ALE
4	P1.2/ECI	19	P3.7/RD	34	NC*
5	P1.3/CEX0	20	XTAL2	35	EA
6	P1.4/CEX1	21	XTAL1	36	P0.7/AD7
7	P1.5/CEX2	22	V _{SS}	37	P0.6/AD6
8	P1.6/CEX3	23	NC*	38	P0.5/AD5
9	P1.7/CEX4	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/INT0	29	P2.5/A13	44	V _{CC}
15	P3.3/INT1	30	P2.6/A14		

* DO NOT CONNECT

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PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function	Pin	Function
1	P1.5/CEX2	16	V _{SS}	31	P0.6/AD6
2	P1.6/CEX3	17	NC*	32	P0.5/AD5
3	P1.7/CEX4	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	P3.0/RxD	20	P2.2/A10	35	P0.2/AD2
6	NC*	21	P2.3/A11	36	P0.1/AD1
7	P3.1/TxD	22	P2.4/A12	37	P0.0/AD0
8	P3.2/INT0	23	P2.5/A13	38	V _{CC}
9	P3.3/INT1	24	P2.6/A14	39	NC*
10	P3.4/T0	25	P2.7/A15	40	P1.0/T2
11	P3.5/T1	26	PSEN	41	P1.1/T2EX
12	P3.6/WR	27	ALE	42	P1.2/ECI
13	P3.7/RD	28	NC*	43	P1.3/CEX0
14	XTAL2	29	EA	44	P1.4/CEX1
15	XTAL1	30	P0.7/AD7		

* DO NOT CONNECT

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PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
V _{SS}	20	22	16	I	Ground: 0V reference.
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and receives code bytes during EPROM programming. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include: T2 (P1.0): Timer/Counter 2 external count input/Clockout (See Programmable Clock-Out.) T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control ECI (P1.2): External Clock Input to the PCA CEX0 (P1.3): Capture/Compare External I/O for PCA module 0 CEX1 (P1.4): Capture/Compare External I/O for PCA module 1 CEX2 (P1.5): Capture/Compare External I/O for PCA module 2 CEX3 (P1.6): Capture/Compare External I/O for PCA module 3 CEX4 (P1.7): Capture/Compare External I/O for PCA module 4
	1	2	40	I	
	2	3	41	I	
	3	4	42	I	
	4	5	43	I/O	
	5	6	44	I/O	
	6	7	1	I/O	
	7	8	2	I/O	
8	9	3	I/O		
P2.0–P2.7	21–28	24–31	18–25	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during EPROM programming and verification.

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PIN DESCRIPTIONS (Continued)

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 80C51 family, as listed below: RxD (P3.0): Serial input port TxD (P3.1): Serial output port INT0 (P3.2): External interrupt INT1 (P3.3): External interrupt T0 (P3.4): Timer 0 external input T1 (P3.5): Timer 1 external input WR (P3.6): External data memory write strobe RD (P3.7): External data memory read strobe
RST	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{CC} .
ALE/PROG	30	33	27	I/O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.
PSEN	29	32	26	O	Program Store Enable: The read strobe to external program memory. When the 87C51FA/FB is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
E _A /V _{PP}	31	35	29	I	External Access Enable/Programming Supply Voltage: E _A must be externally held low to enable the device to fetch code from external program memory locations 0000H to 1FFFH. If E _A is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming. If security bit 1 is programmed, E _A will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier.

NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5V or V_{SS} - 0.5V, respectively.

TIMER 2

This is a 16-bit up or down counter, which can be operated as either a timer or event counter. It can be operated in one of three different modes (autoreload, capture or as the baud rate generator for the UART).

In the autoreload mode the Timer can be set to count up or down by setting or clearing the bit DCEN in the T2CON Special Function Register. The SFR's RCAP2H and RCAP2L are used to reload the Timer upon overflow or a 1-to-0 transition on the T2EX input (P1.1).

In the Capture mode Timer 2 can either set TF2 and generate an interrupt or capture its value. To capture Timer 2 in response to a 1-to-0 transition on the T2EX input, the EXEN2 bit in the T2CON must be set. Timer 2 is then captured in SFR's RCAP2H and RCAP2L.

As the baud rate generator, Timer 2 is selected by setting TCLK and/or RCLK in T2CON. As the baud rate generator Timer 2 is incremented at 1/2 the oscillator frequency.

POWER OFF FLAG

The Power Off Flag (POF) is set by on-chip circuitry when the V_{CC} level on the 87C51FA/FB rises from 0 to 5V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The V_{CC} level must remain above 3V for the POF to remain unaffected by the V_{CC} level.



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OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

Idle Mode

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 87C51FA/FB either a hardware reset or external interrupt can use an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 87C51FA/FB without the 87C51FA/FB having to be removed from the circuit. The ONCE Mode is invoked by:

- Pull ALE low while the device is in reset and PSEN is high;
- Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and PSEN are weakly pulled high. The oscillator circuit remains active. While the 87C51FA/FB is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Programmable Clock-Out

The 87C51FA/FB has a new feature. A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed (1) to input the external clock for Timer/Counter 2 or (2) to output a 50% duty cycle clock ranging from 61Hz to 4MHz at a 16MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H}, \text{RCAP2L})}$$

In the Clock-Out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

Table 2. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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Programmable Counter Array (PCA)

The Programmable Counter Array is a special Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3(CEX0), module 1 to P1.4(CEX1), etc. The basic PCA configuration is shown in Figure 1.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/12 the oscillator frequency, 1/4 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 4):

CPS1	CPS0	PCA Timer Count Source
0	0	1/12 oscillator frequency
0	1	1/4 oscillator frequency
1	0	Timer 0 overflow
1	1	External Input at ECI pin

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag, CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 2.

The watchdog timer function is implemented in module 4 as implemented in other parts that have a PCA that are available on the market. However, if a watchdog timer is required in the target application, it is recommended to use the hardware watchdog timer that is implemented on the 87C51FA/FB separately from the PCA (see Figure 12).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 5). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system shown in Figure 3.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 6). The registers contain the bits that control the mode in which each module will operate. The ECCFn bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 7 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated. Refer to Figure 8.

16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (see Figure 9).

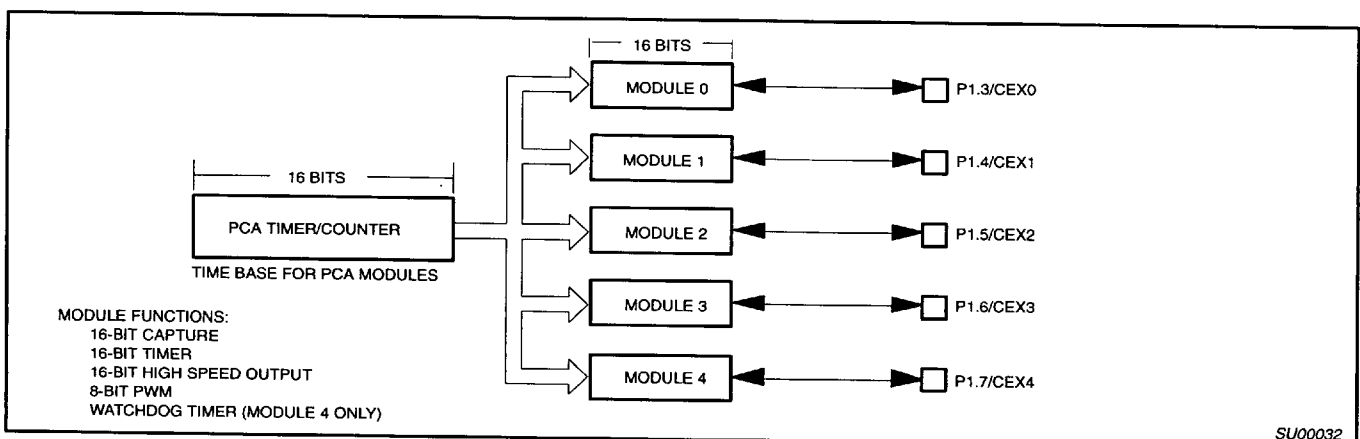


Figure 1. Programmable Counter Array (PCA)

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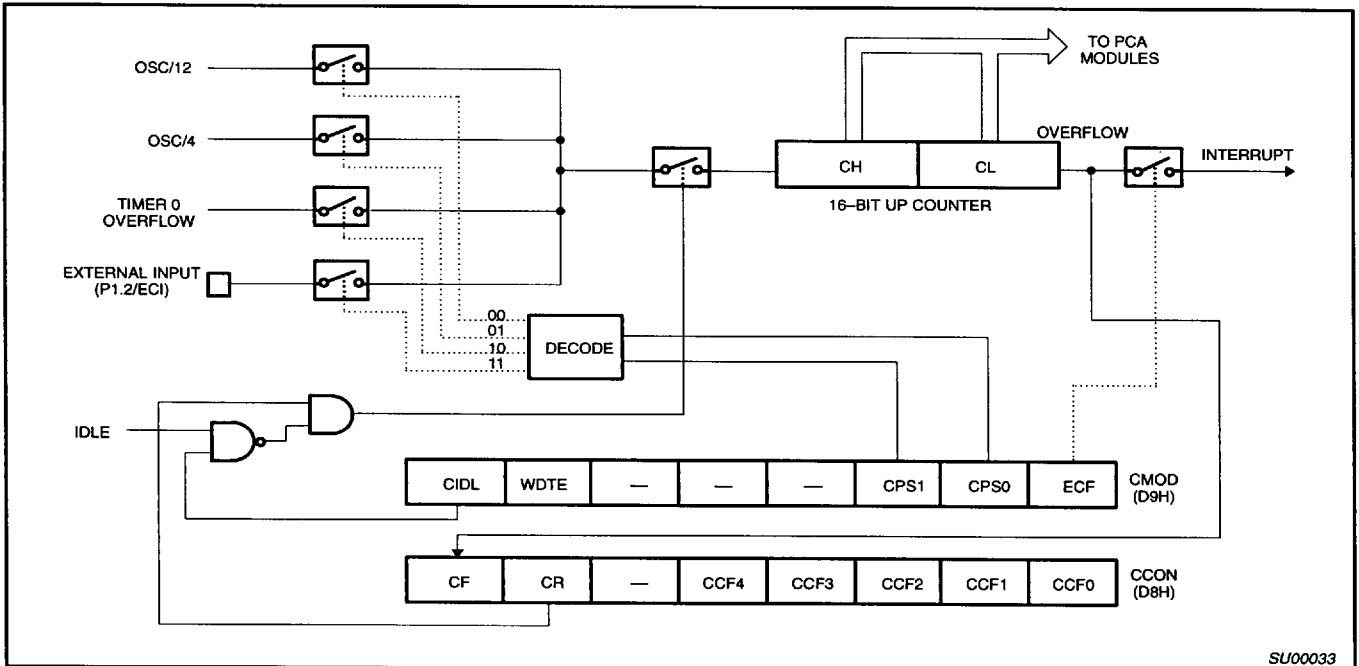


Figure 2. PCA Timer/Counter

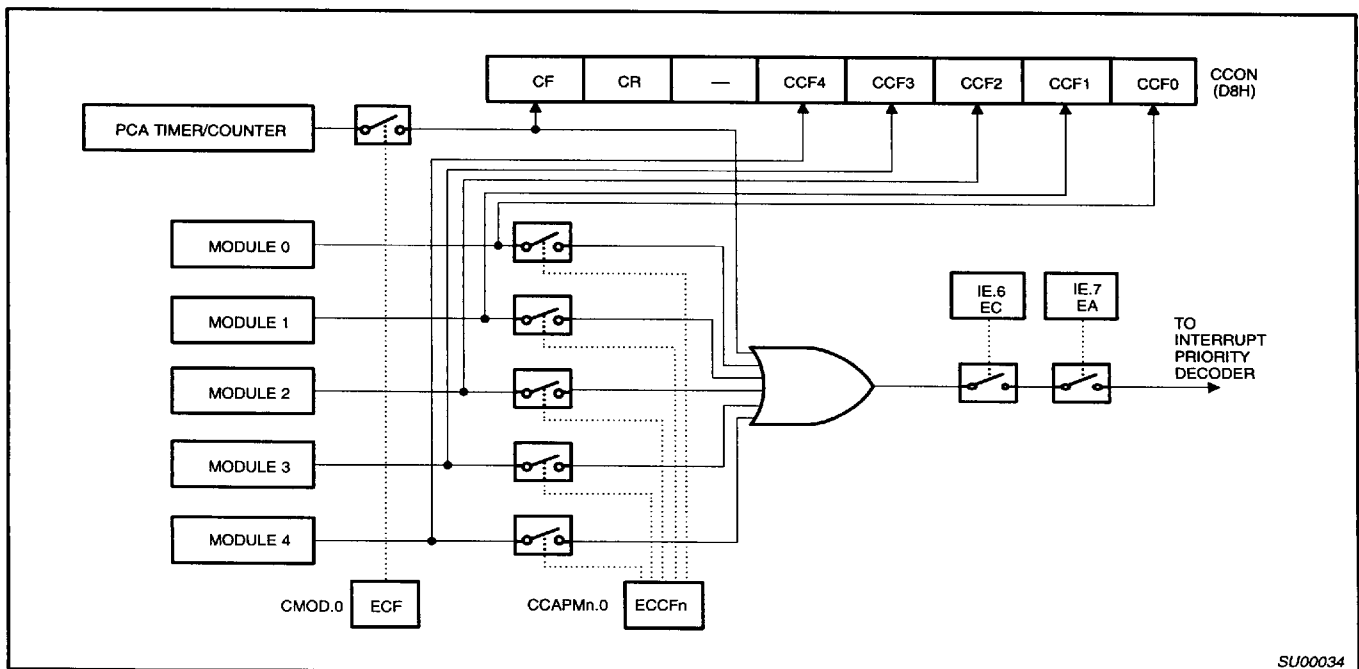


Figure 3. PCA Interrupt System

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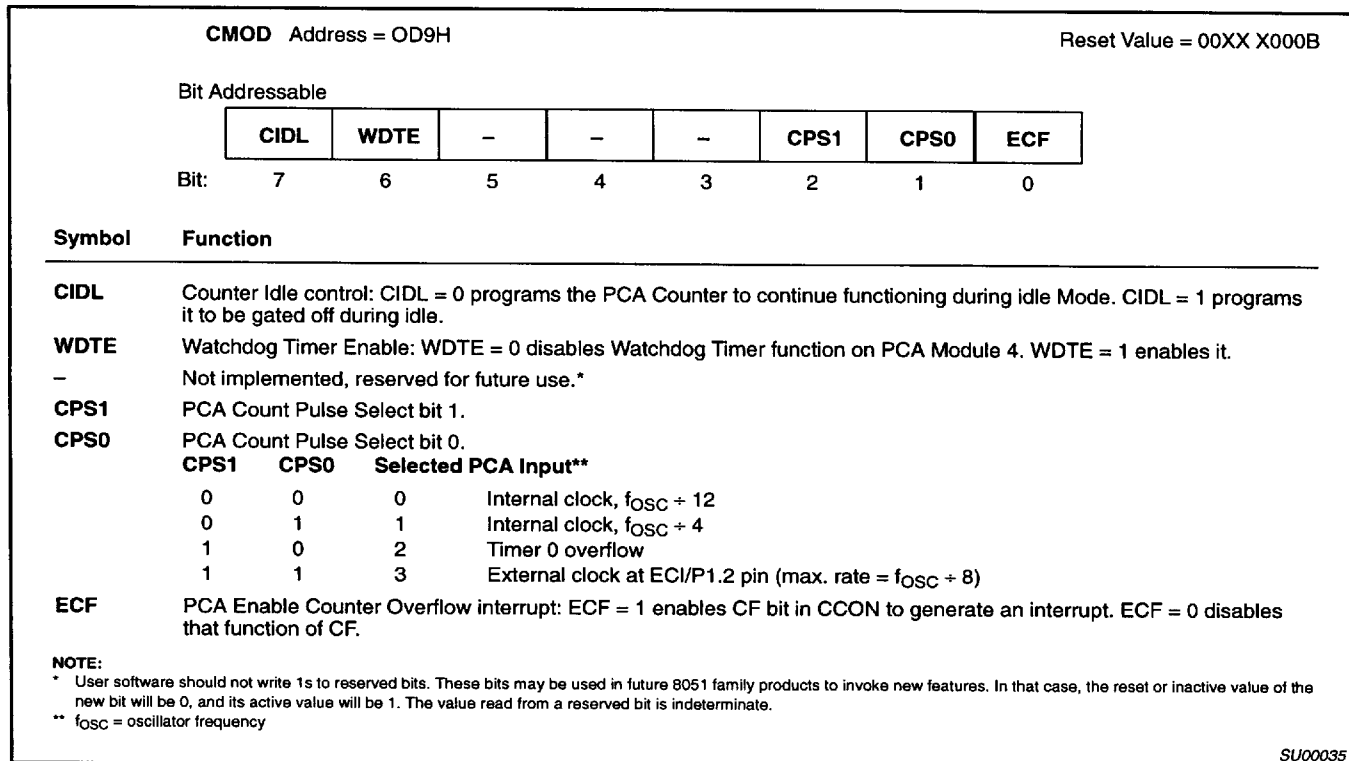


Figure 4. CMOD: PCA Counter Mode Register

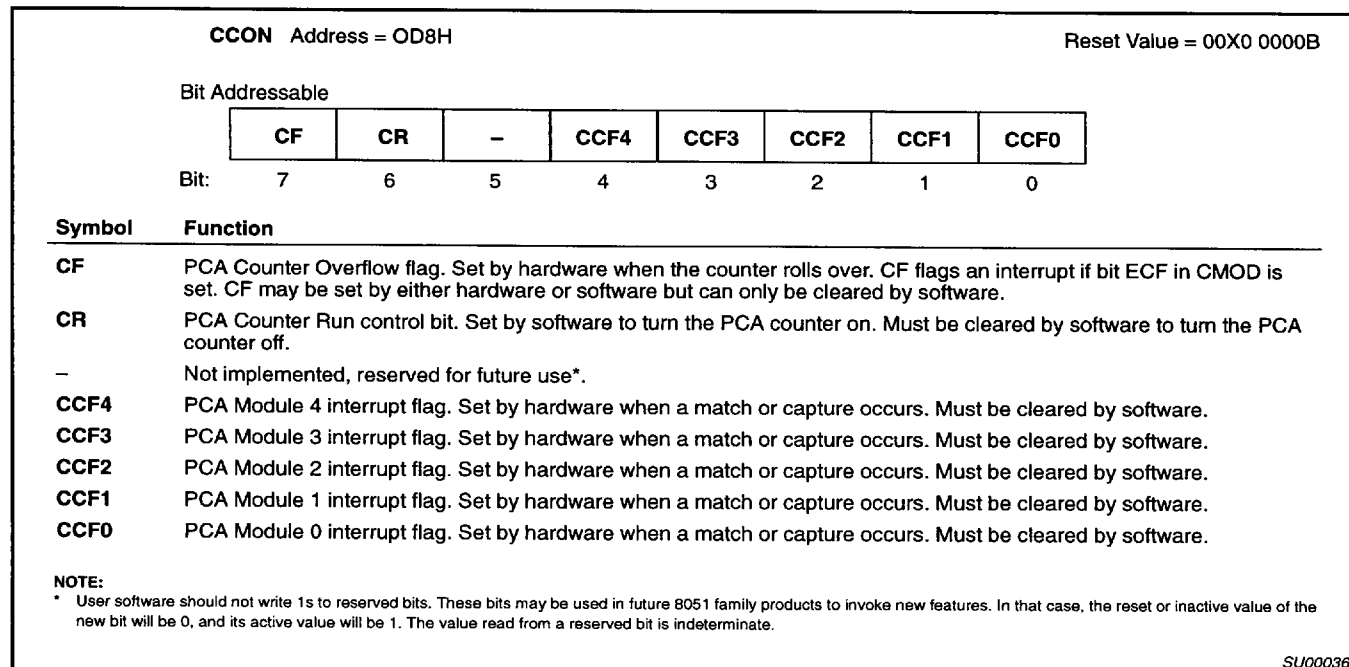


Figure 5. CCON: PCA Counter Control Register

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CCAPMn Address	CCAPM0	0DAH						Reset Value = X000 0000B
	CCAPM1	0DBH						
	CCAPM2	0DCH						
	CCAPM3	0DDH						
	CCAPM4	0DEH						
Not Bit Addressable								
	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Bit:	7	6	5	4	3	2	1	0
Symbol	Function							
-	Not implemented, reserved for future use*.							
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.							
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.							
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.							
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.							
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.							
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.							
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.							
NOTE:								
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.								

SU00037

Figure 6. CCAPMn: PCA Modules Compare/Capture Registers

-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	MODULE FUNCTION
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	X	0	X	Watchdog Timer

Figure 7. PCA Module Modes (CCAPMn Register)

High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (see Figure 10).

Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 11 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn then allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

Enhanced UART

The UART operates in all of the usual modes that are described in the first section of this book for the 80C51. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The 87C51FA/FB UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 13). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 14.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal

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of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 15.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "IGiven" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111 1101</u>
	Given =	1100 00X0
Slave 1	SADDR =	1100 0000
	SADEN =	<u>1111 1110</u>
	Given =	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111 1001</u>
	Given =	1100 0XX0
Slave 1	SADDR =	1110 0000
	SADEN =	<u>1111 1010</u>
	Given =	1110 0X0X
Slave 2	SADDR =	1110 0000
	SADEN =	<u>1111 1100</u>
	Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

87C51FA/FB Reduced EMI Mode

AUXR (0X8E)

—	—	—	—	—	—	—	—	AO
---	---	---	---	---	---	---	---	----

AO: Turns off ALE output.

Interrupt Enable (IE) Register

EA	IE.7	enable all interrupts
EC	IE.6	enable PCA interrupt
ET2	IE.5	enable Timer 2 interrupt
ES	IE.4	enable Serial I/O interrupt
ET1	IE.3	enable Timer 1 interrupt
EX1	IE.2	enable External interrupt 1
ET0	IE.1	enable Timer 0 interrupt
EX0	IE.0	enable External interrupt 0

Interrupt Priority (IP) Register

IP.7	reserved
PPC	IP.6 PCA interrupt priority
PT2	IP.5 Timer 2 interrupt priority
PS	IP.4 Serial I/O interrupt priority
PT1	IP.3 Timer 1 interrupt priority
PX1	IP.2 External interrupt 1 priority
PT0	IP.1 Timer 0 interrupt priority
PX0	IP.0 External interrupt 0 priority

Priority	Source	Flag	Vector
1	INT0	IE0	03H highest priority
2	Timer 0	TF0	0BH
3	INT1	IE1	13H
4	Timer 1	TF1	1BH
5	PCA	CF,CCFn	33H
6	Serial I/O	RI,TI	23H
7	Timer 2	TF2/EXF2	2BH lowest priority

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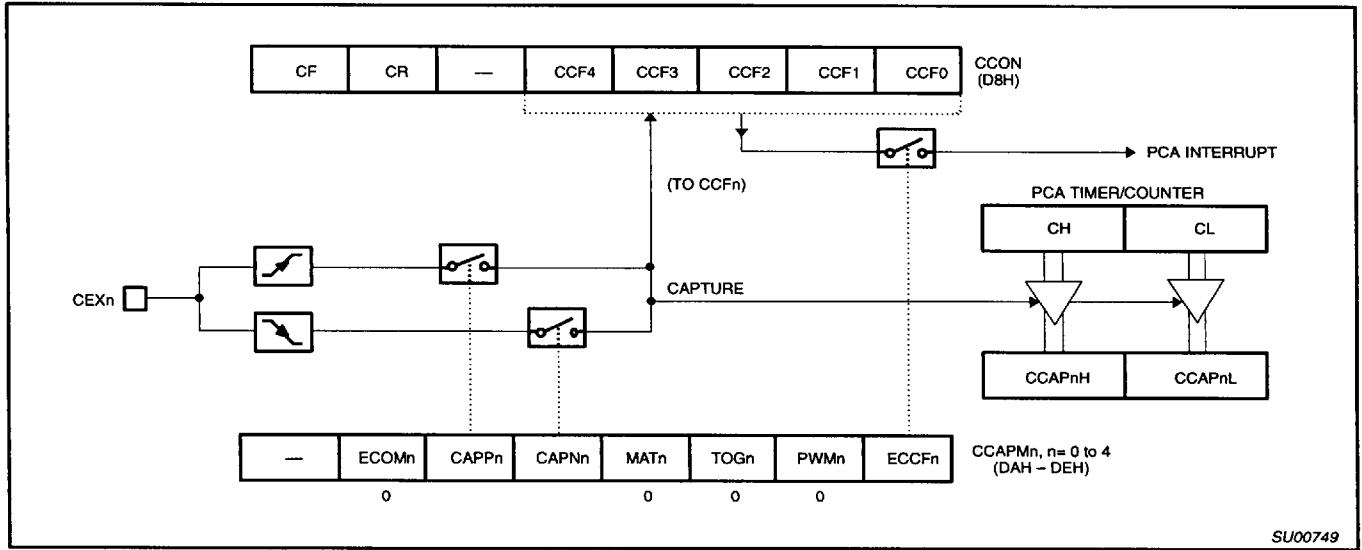


Figure 8. PCA Capture Mode

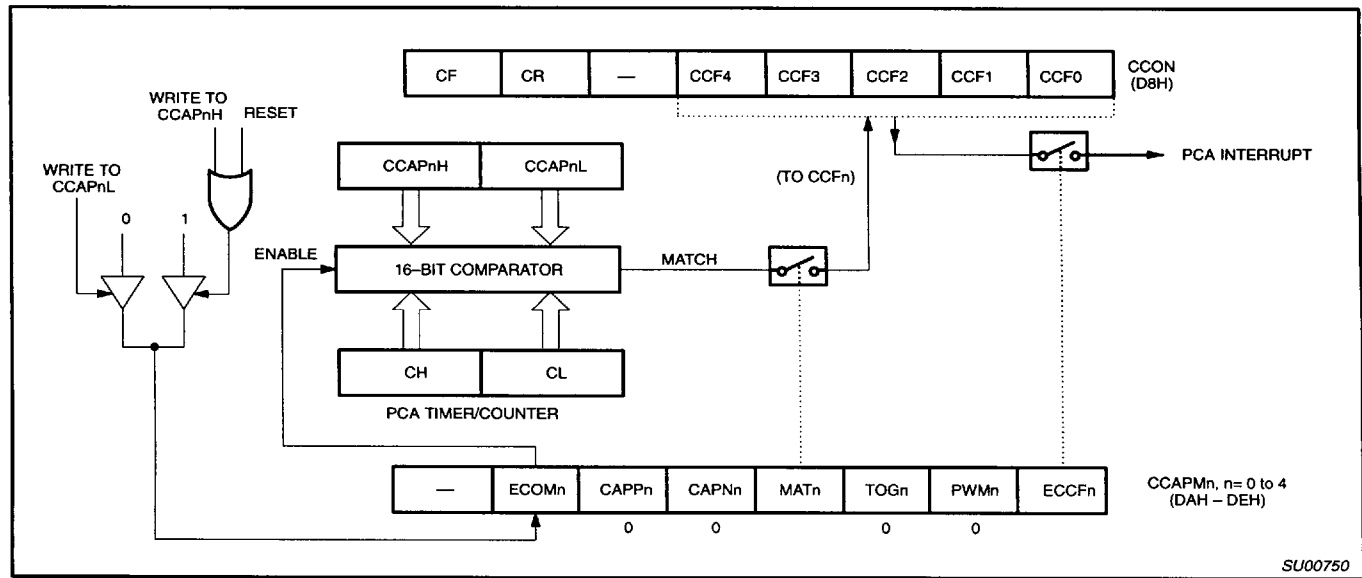


Figure 9. PCA Compare Mode

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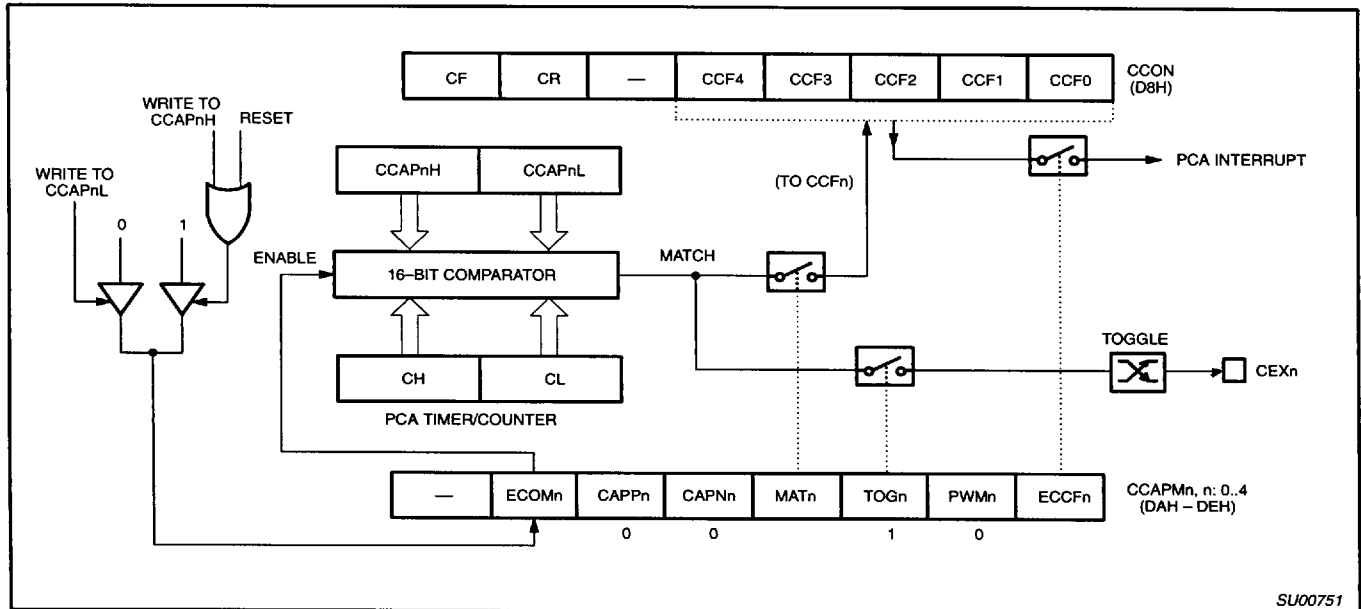


Figure 10. PCA High Speed Output Mode

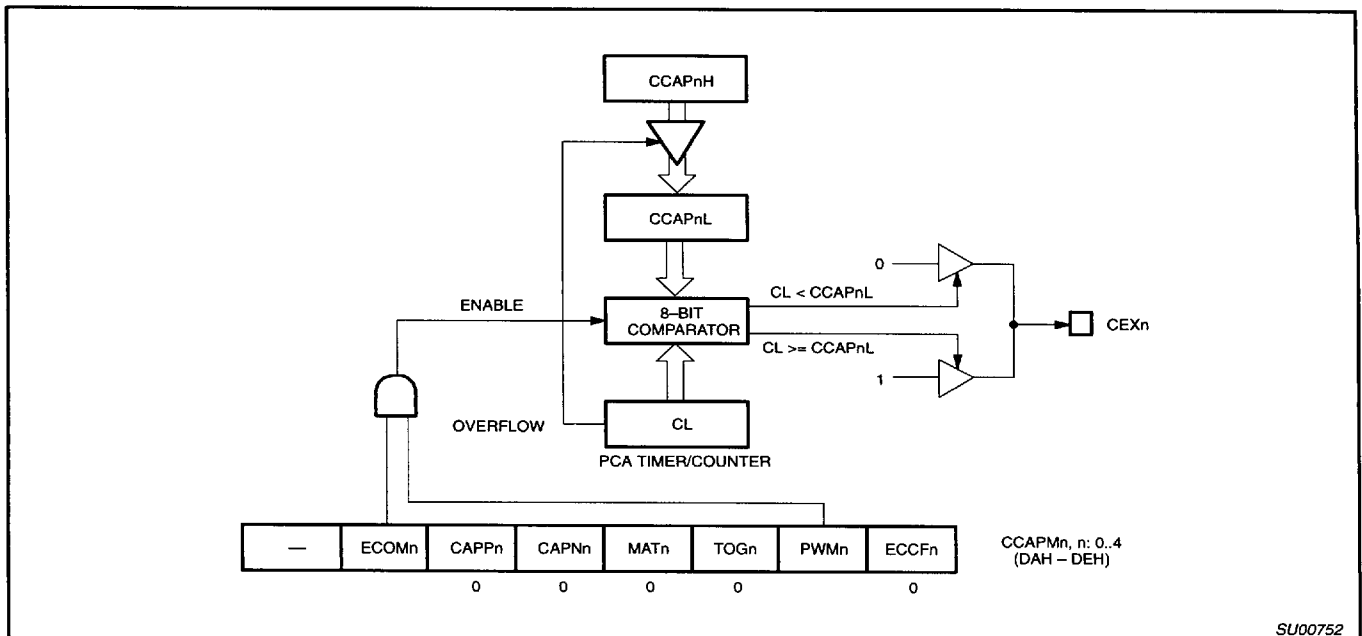


Figure 11. PCA PWM Mode

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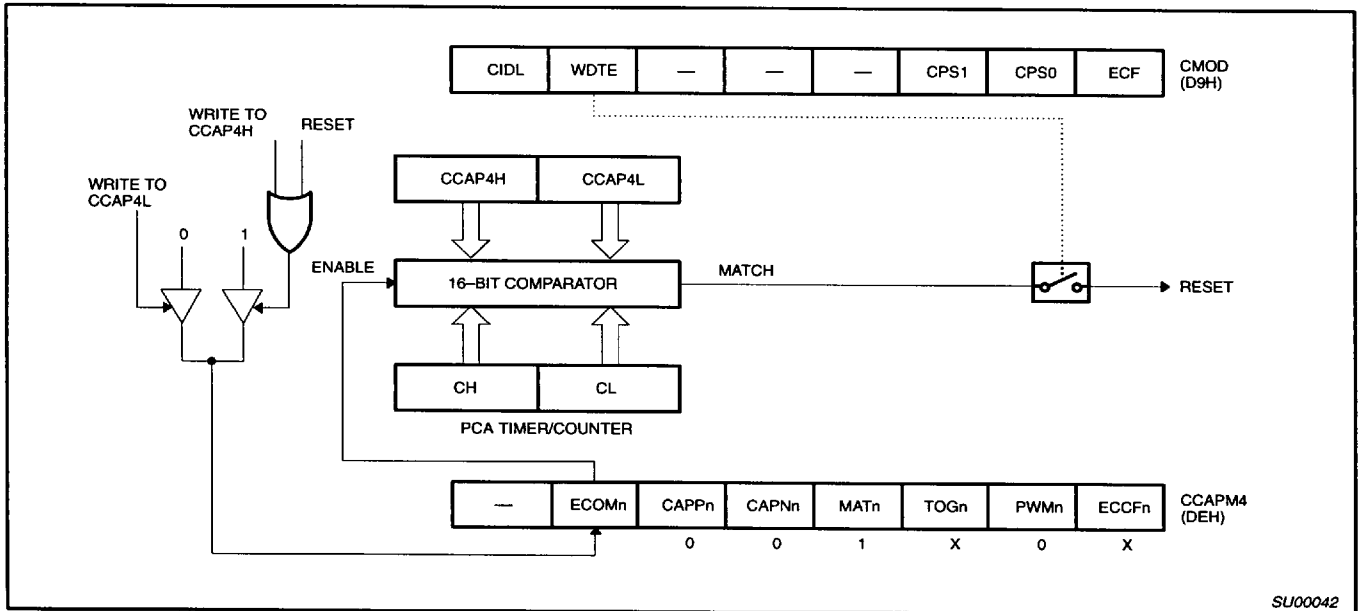


Figure 12. PCA Watchdog Timer

SCON Address = 98H Reset Value = 0000 0000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
Bit:	7	6	5	4	3	2	1	0

(SMOD0 = 0/1)*

Symbol	Function																									
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.																									
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)																									
SM1	Serial Port Mode Bit 1																									
	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>SM0</th> <th>SM1</th> <th>Mode</th> <th>Description</th> <th>Baud Rate**</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>shift register</td> <td>$f_{osc}/12$</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>8-bit UART</td> <td>variable</td> </tr> <tr> <td>1</td> <td>0</td> <td>2</td> <td>9-bit UART</td> <td>$f_{osc}/64$ or $f_{osc}/32$</td> </tr> <tr> <td>1</td> <td>1</td> <td>3</td> <td>9-bit UART</td> <td>variable</td> </tr> </tbody> </table>	SM0	SM1	Mode	Description	Baud Rate**	0	0	0	shift register	$f_{osc}/12$	0	1	1	8-bit UART	variable	1	0	2	9-bit UART	$f_{osc}/64$ or $f_{osc}/32$	1	1	3	9-bit UART	variable
SM0	SM1	Mode	Description	Baud Rate**																						
0	0	0	shift register	$f_{osc}/12$																						
0	1	1	8-bit UART	variable																						
1	0	2	9-bit UART	$f_{osc}/64$ or $f_{osc}/32$																						
1	1	3	9-bit UART	variable																						
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.																									
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.																									
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.																									
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.																									
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.																									
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.																									

NOTE:
 *SMOD0 is located at PCON6.
 **f_{osc} = oscillator frequency

Figure 13. SCON: Serial Port Control Register



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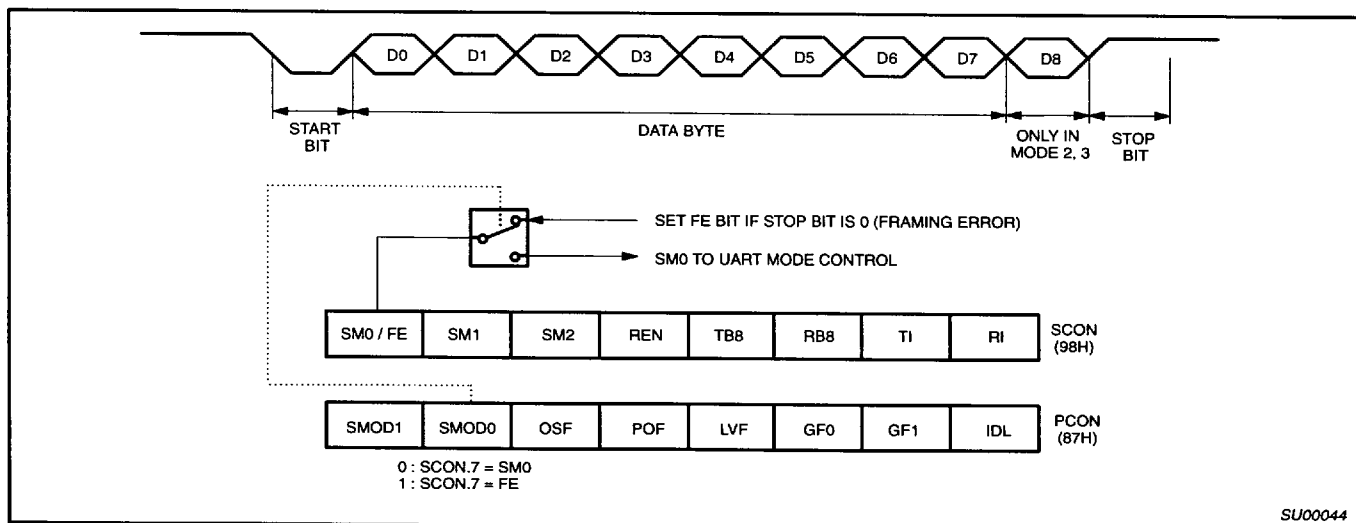


Figure 14. UART Framing Error Detection

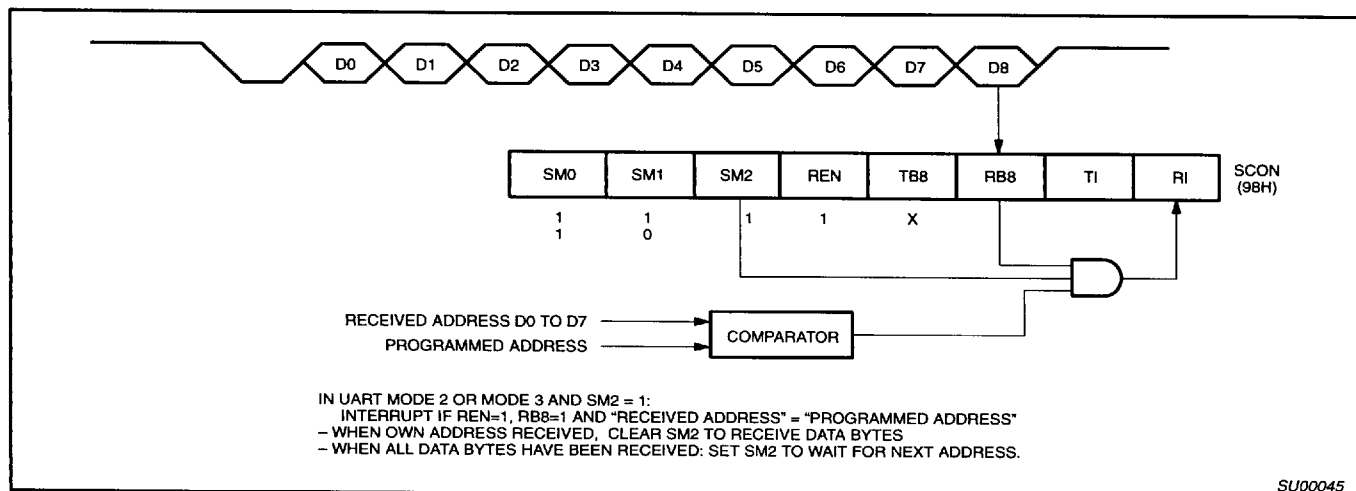


Figure 15. UART Multiprocessor Communication, Automatic Address Recognition

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ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or -40 to +85	°C
Storage temperature range	-65 to +150	°C
Voltage on \overline{EA}/V_{PP} pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	-0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Electrical Deviations from Commercial Specifications for Extended Temperature Range

DC and AC parameters not included here are the same as in the commercial temperature range table.

DC ELECTRICAL CHARACTERISTICS $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{IL}	Input low voltage, except \overline{EA}		-0.5	$0.2V_{CC}-0.15$	V
V_{IL1}	Input low voltage to \overline{EA}		0	$0.2V_{CC}-0.35$	V
V_{IH}	Input high voltage, except XTAL1, RST		$0.2V_{CC}+1$	$V_{CC}+0.5$	V
V_{IH1}	Input high voltage to XTAL1, RST		$0.7V_{CC}+0.1$	$V_{CC}+0.5$	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.45\text{V}$		-75	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3	$V_{IN} = 2.0\text{V}$		-750	μA

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DC ELECTRICAL CHARACTERISTICS

 $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage, except EA ⁷		-0.5		$0.2V_{CC}-0.1$	V
V_{IL1}	Input low voltage to EA ⁷		0		$0.2V_{CC}-0.3$	V
V_{IH}	Input high voltage, except XTAL1, RST ⁷		$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST ⁷		$0.7V_{CC}$		$V_{CC}+0.5$	V
V_{OL}	Output low voltage, ports 1, 2, 3 ⁹	$I_{OL} = 1.6\text{mA}^2$			0.45	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN ⁹	$I_{OL} = 3.2\text{mA}^2$			0.45	V
V_{OH}	Output high voltage, ports 1, 2, 3, ALE, PSEN ³	$I_{OH} = -30\mu\text{A}$	$V_{CC} - 0.7$			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ¹⁰ , PSEN ³	$I_{OH} = -3.2\text{mA}$	$V_{CC} - 0.7$			V
I_{IL}	Logical 0 input current, ports 1, 2, 3 ⁷	$V_{IN} = 0.45\text{V}$			-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁷	See note 4			-650	μA
I_{LI}	Input leakage current, port 0	$0.45 V_{IN} < V_{CC} - 0.3$			± 10	μA
I_{CC}	Power supply current: Active mode @ 16MHz ⁵ Idle mode @ 16MHz Power-down mode $T_{amb} = 0$ to $+70^{\circ}\text{C}$ $T_{amb} = -40$ to $+85^{\circ}\text{C}$	See note 6		15 3 10	32 5 50 75	 mA mA μA μA
R_{RST}	Internal reset pull-down resistor		50		225	k Ω
C_{IO}	Pin capacitance ¹¹ (except EA)				15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- I_{CCMAX} at other frequencies is given by: Active mode: $I_{CCMAX} = 1.50 \times \text{FREQ} + 8$; Idle mode: $I_{CCMAX} = 0.14 \times \text{FREQ} + 2.31$, where FREQ is the external oscillator frequency in MHz. I_{CCMAX} is given in mA. See Figure 23.
- See Figures 24 through 27 for I_{CC} test conditions.
- These values apply only to $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$. For $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, see table on previous page.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15mA (*NOTE: This is 85°C specification.)
Maximum I_{OL} per 8-bit port: 26mA
Maximum total I_{OL} for all outputs: 71mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except EA, it is 25pF).

CMOS single-chip 8-bit microcontrollers

87C51FA/87C51FB

AC ELECTRICAL CHARACTERISTICS $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}^{1, 2, 3}$

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	16	Oscillator frequency	-4, -5		3.5	16	MHz
			-A, -B			3.5	24
t_{LHLL}	16	ALE pulse width	85		$2t_{CLCL}-40$		ns
t_{AVLL}	16	Address valid to ALE low	22		$t_{CLCL}-40$		ns
t_{LLAX}	16	Address hold after ALE low	32		$t_{CLCL}-30$		ns
t_{LLIV}	16	ALE low to valid instruction in		150		$4t_{CLCL}-100$	ns
t_{LLPL}	16	ALE low to PSEN low	32		$t_{CLCL}-30$		ns
t_{PLPH}	16	PSEN pulse width	142		$3t_{CLCL}-45$		ns
t_{PLIV}^4	16	PSEN low to valid instruction in		82		$3t_{CLCL}-105$	ns
t_{PXIX}	16	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	16	Input instruction float after PSEN		37		$t_{CLCL}-25$	ns
t_{AVIV}	16	Address to valid instruction in		207		$5t_{CLCL}-105$	ns
t_{PLAZ}	16	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	17, 18	RD pulse width	275		$6t_{CLCL}-100$		ns
t_{WLWH}	17, 18	WR pulse width	275		$6t_{CLCL}-100$		ns
t_{RLDV}	17, 18	RD low to valid data in		147		$5t_{CLCL}-165$	ns
t_{RHDX}	17, 18	Data hold after RD	0		0		ns
t_{RHDZ}	17, 18	Data float after RD		65		$2t_{CLCL}-60$	ns
t_{LLDV}	17, 18	ALE low to valid data in		350		$8t_{CLCL}-150$	ns
t_{AVDV}	17, 18	Address to valid data in		397		$9t_{CLCL}-165$	ns
t_{LLWL}	17, 18	ALE low to RD or WR low	137	237	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	17, 18	Address valid to WR low or RD low	122		$4t_{CLCL}-130$		ns
t_{QVWX}	17, 18	Data valid to WR transition	13		$t_{CLCL}-50$		ns
t_{WHQX}	17, 18	Data hold after WR	13		$t_{CLCL}-50$		ns
t_{QVWH}	18	Data valid to WR high	287		$7t_{CLCL}-150$		ns
t_{RLAZ}	17, 18	RD low to address float		0		0	ns
t_{WHLH}	17, 18	RD or WR high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
External Clock							
t_{CHCX}	20	High time	20		20		ns
t_{CLCX}	20	Low time	20		20		ns
t_{CLCH}	20	Rise time		20		20	ns
t_{CHCL}	20	Fall time		20		20	ns
Shift Register							
t_{XLXL}	19	Serial port clock cycle time	750		$12t_{CLCL}$		ns
t_{QVXH}	19	Output data setup to clock rising edge	492		$10t_{CLCL}-133$		ns
t_{XHQX}	19	Output data hold after clock rising edge	8		$2t_{CLCL}-117$		ns
t_{XHDX}	19	Input data hold after clock rising edge	0		0		ns
t_{XHDX}	19	Clock rising edge to input data valid		492		$10t_{CLCL}-133$	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Interfacing the 87C51FA/FB to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
- See Application Note AN457.

CMOS single-chip 8-bit microcontrollers

87C51FA/87C51FB

AC ELECTRICAL CHARACTERISTICS
 $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C or } -40^{\circ}\text{C to } +85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}^{1,2,3}$

SYMBOL	FIGURE	PARAMETER	24MHz CLOCK		VARIABLE CLOCK ⁴		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	16	Oscillator frequency Speed versions : A, B (24MHz)	3.5	24	3.5	24	MHz
t_{LHLL}	16	ALE pulse width	43		$2t_{CLCL}-40$		ns
t_{AVLL}	16	Address valid to ALE low	17		$t_{CLCL}-25$		ns
t_{LLAX}	16	Address hold after ALE low	17		$t_{CLCL}-25$		ns
t_{LLIV}	16	ALE low to valid instruction in		102		$4t_{CLCL}-65$	ns
t_{LLPL}	16	ALE low to $\overline{\text{PSEN}}$ low	17		$t_{CLCL}-25$		ns
t_{PLPH}	16	$\overline{\text{PSEN}}$ pulse width	80		$3t_{CLCL}-45$		ns
t_{PLIV}	16	$\overline{\text{PSEN}}$ low to valid instruction in		65		$3t_{CLCL}-60$	ns
t_{PXIX}	16	Input instruction hold after $\overline{\text{PSEN}}$	0		0		ns
t_{PXIZ}	16	Input instruction float after $\overline{\text{PSEN}}$		17		$t_{CLCL}-25$	ns
t_{AVIV}	16	Address to valid instruction in		128		$5t_{CLCL}-80$	ns
t_{PLAZ}	16	$\overline{\text{PSEN}}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	17, 18	$\overline{\text{RD}}$ pulse width	150		$6t_{CLCL}-100$		ns
t_{WLWH}	17, 18	$\overline{\text{WR}}$ pulse width	150		$6t_{CLCL}-100$		ns
t_{RLDV}	17, 18	$\overline{\text{RD}}$ low to valid data in		118		$5t_{CLCL}-90$	ns
t_{RHDX}	17, 18	Data hold after $\overline{\text{RD}}$	0		0		ns
t_{RHDZ}	17, 18	Data float after $\overline{\text{RD}}$		55		$2t_{CLCL}-28$	ns
t_{LLDV}	17, 18	ALE low to valid data in		183		$8t_{CLCL}-150$	ns
t_{AVDV}	17, 18	Address to valid data in		210		$9t_{CLCL}-165$	ns
t_{LLWL}	17, 18	ALE low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low	75	175	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	17, 18	Address valid to $\overline{\text{WR}}$ low or $\overline{\text{RD}}$ low	92		$4t_{CLCL}-75$		ns
t_{QVWX}	17, 18	Data valid to $\overline{\text{WR}}$ transition	12		$t_{CLCL}-30$		ns
t_{WHQX}	17, 18	Data hold after $\overline{\text{WR}}$	17		$t_{CLCL}-25$		ns
t_{QVWH}	18	Data valid to $\overline{\text{WR}}$ high	162		$7t_{CLCL}-130$		ns
t_{RLAZ}	17, 18	$\overline{\text{RD}}$ low to address float		0		0	ns
t_{WHLH}	17, 18	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ high to ALE high	17	67	$t_{CLCL}-25$	$t_{CLCL}+25$	ns
External Clock							
t_{CHCX}	20	High time	17		17	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	20	Low time	17		17	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	20	Rise time		5		5	ns
t_{CHCL}	20	Fall time		5		5	ns
Shift Register							
t_{XLXL}	19	Serial port clock cycle time	505		$12t_{CLCL}$		ns
t_{QVXH}	19	Output data setup to clock rising edge	283		$10t_{CLCL}-133$		ns
t_{XHQX}	19	Output data hold after clock rising edge	3		$2t_{CLCL}-80$		ns
t_{XHDX}	19	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	19	Clock rising edge to input data valid		283		$10t_{CLCL}-133$	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and $\overline{\text{PSEN}} = 100\text{pF}$, load capacitance for all other outputs = 80pF .
- Interfacing the 87C51FA/FB to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
- Variable clock is specified for oscillator frequencies greater than 16MHz to 33MHz. For frequencies equal or less than 16MHz, see 16MHz "AC Electrical Characteristics", page 21.

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87C51FA/87C51FB

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

- A – Address
- C – Clock
- D – Input data
- H – Logic level high
- I – Instruction (program memory contents)
- L – Logic level low, or ALE

- P – PSEN
- Q – Output data
- R – RD signal
- t – Time
- V – Valid
- W – WR signal
- X – No longer a valid logic level
- Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to PSEN low.

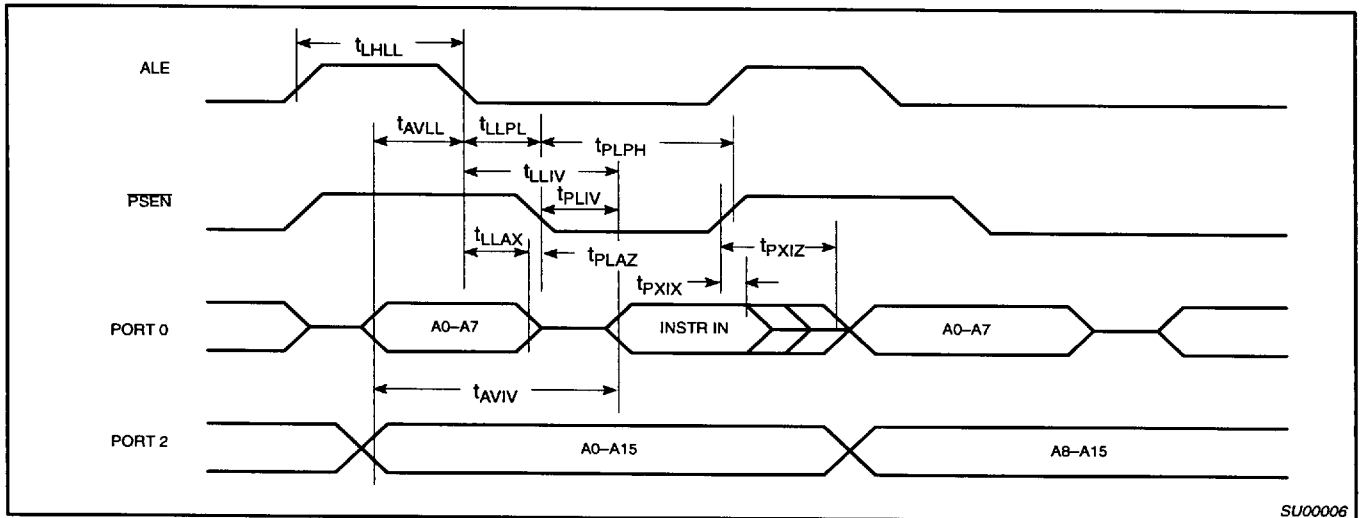


Figure 16. External Program Memory Read Cycle

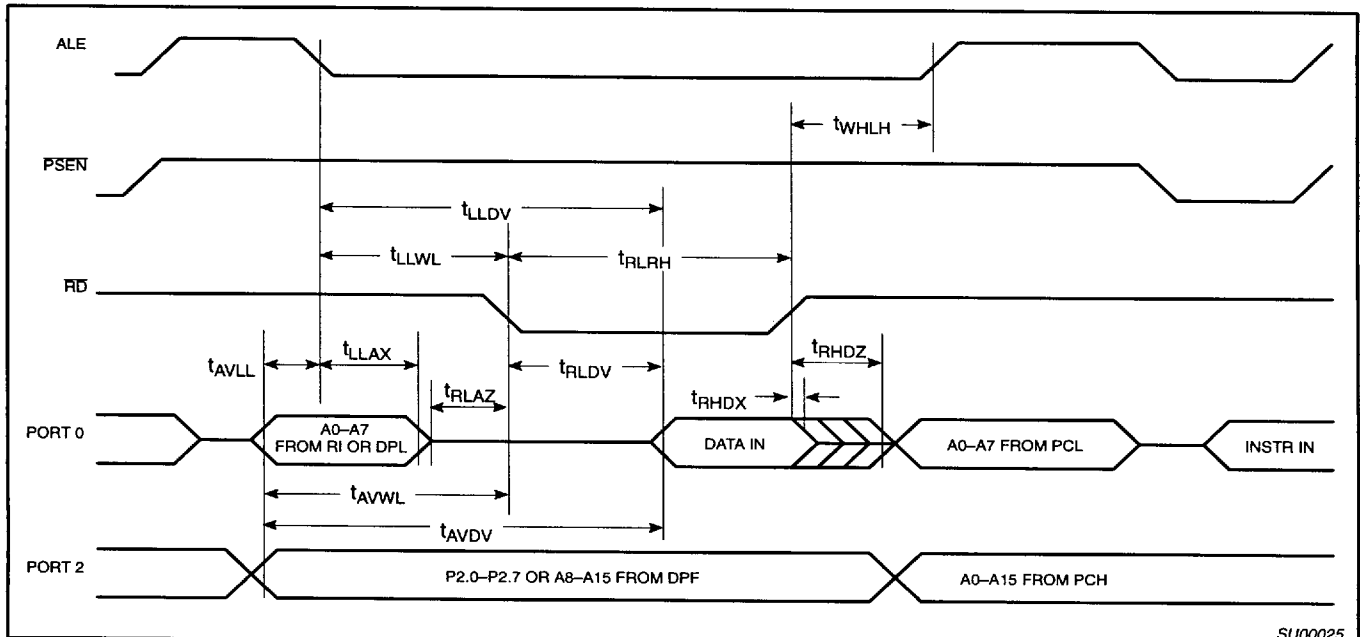


Figure 17. External Data Memory Read Cycle

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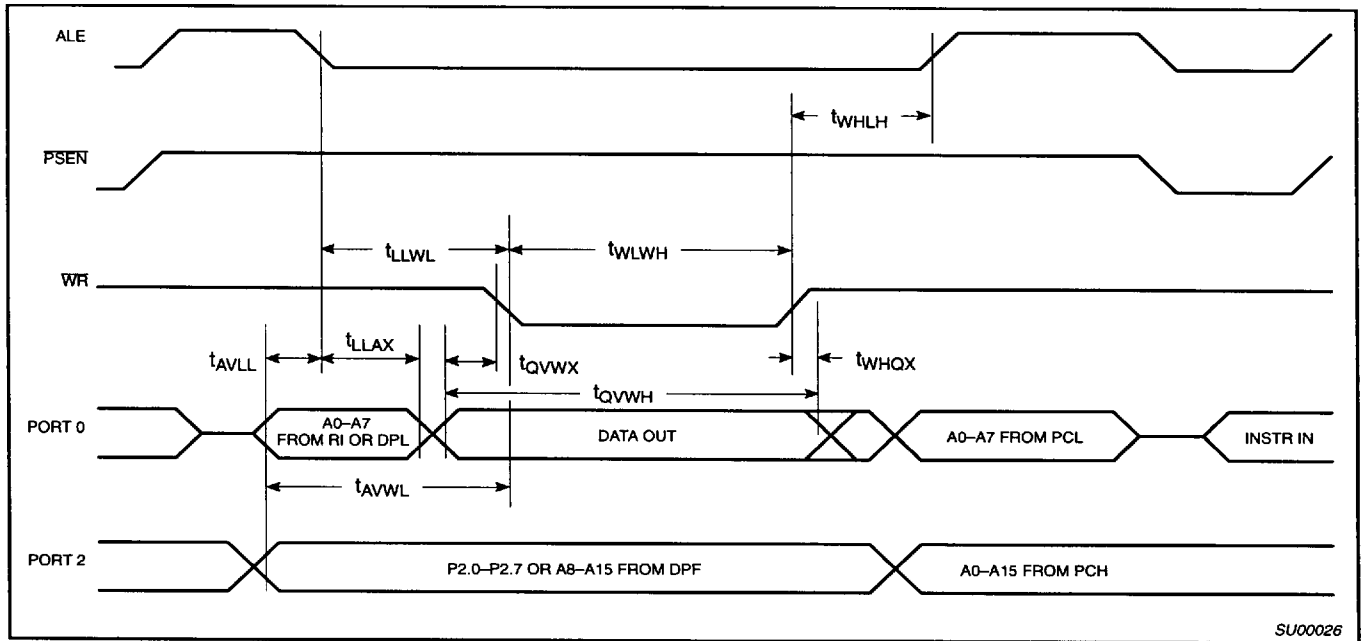


Figure 18. External Data Memory Write Cycle

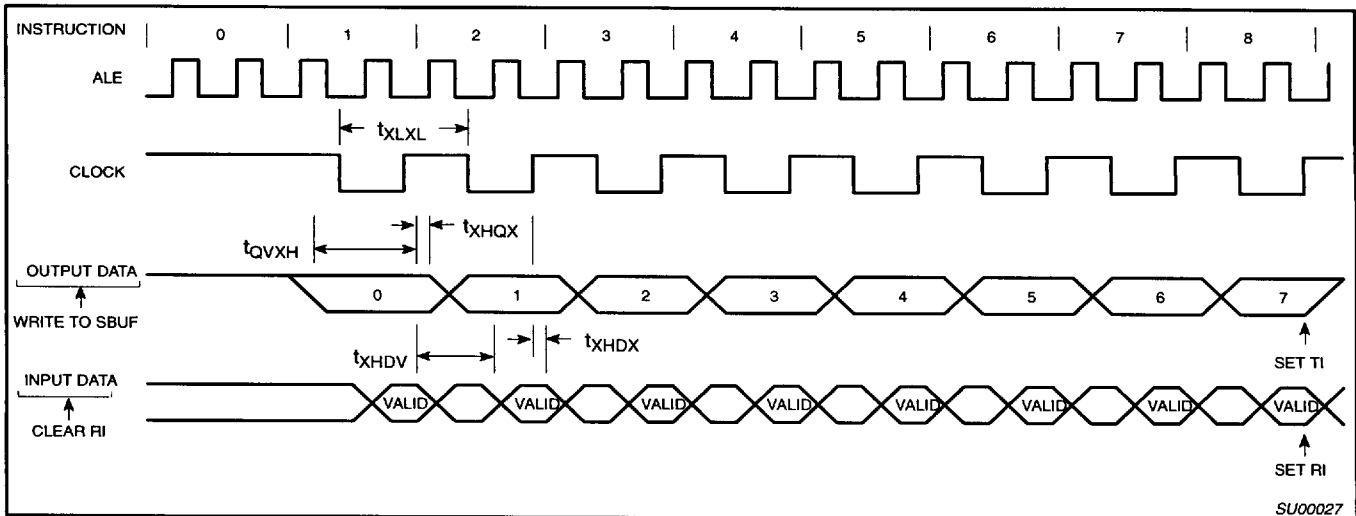


Figure 19. Shift Register Mode Timing

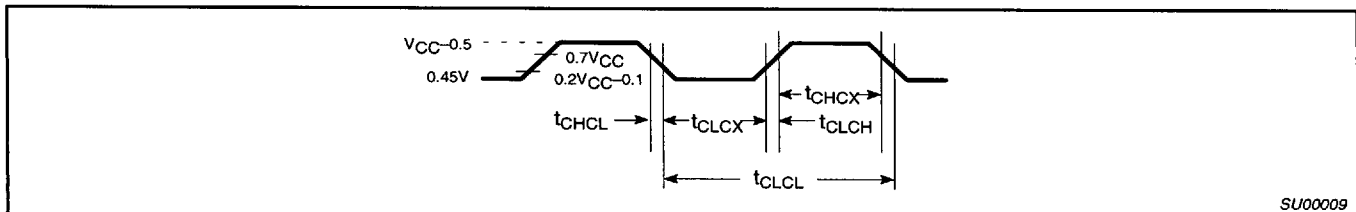
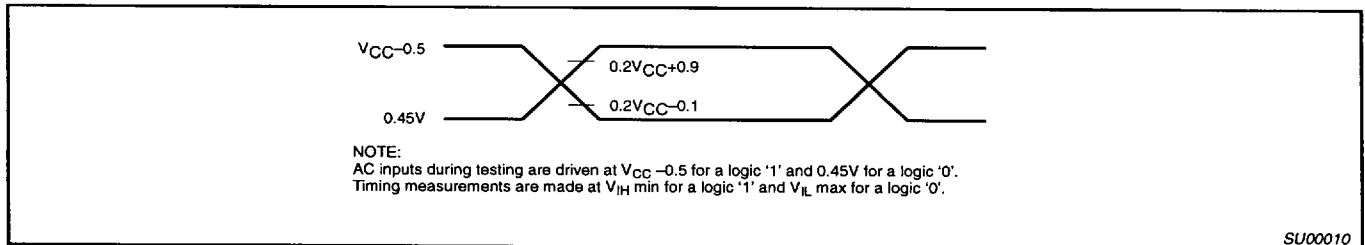


Figure 20. External Clock Drive

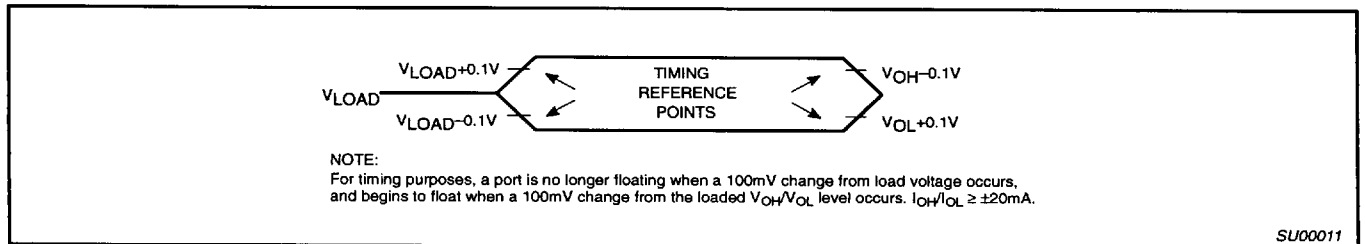
CMOS single-chip 8-bit microcontrollers

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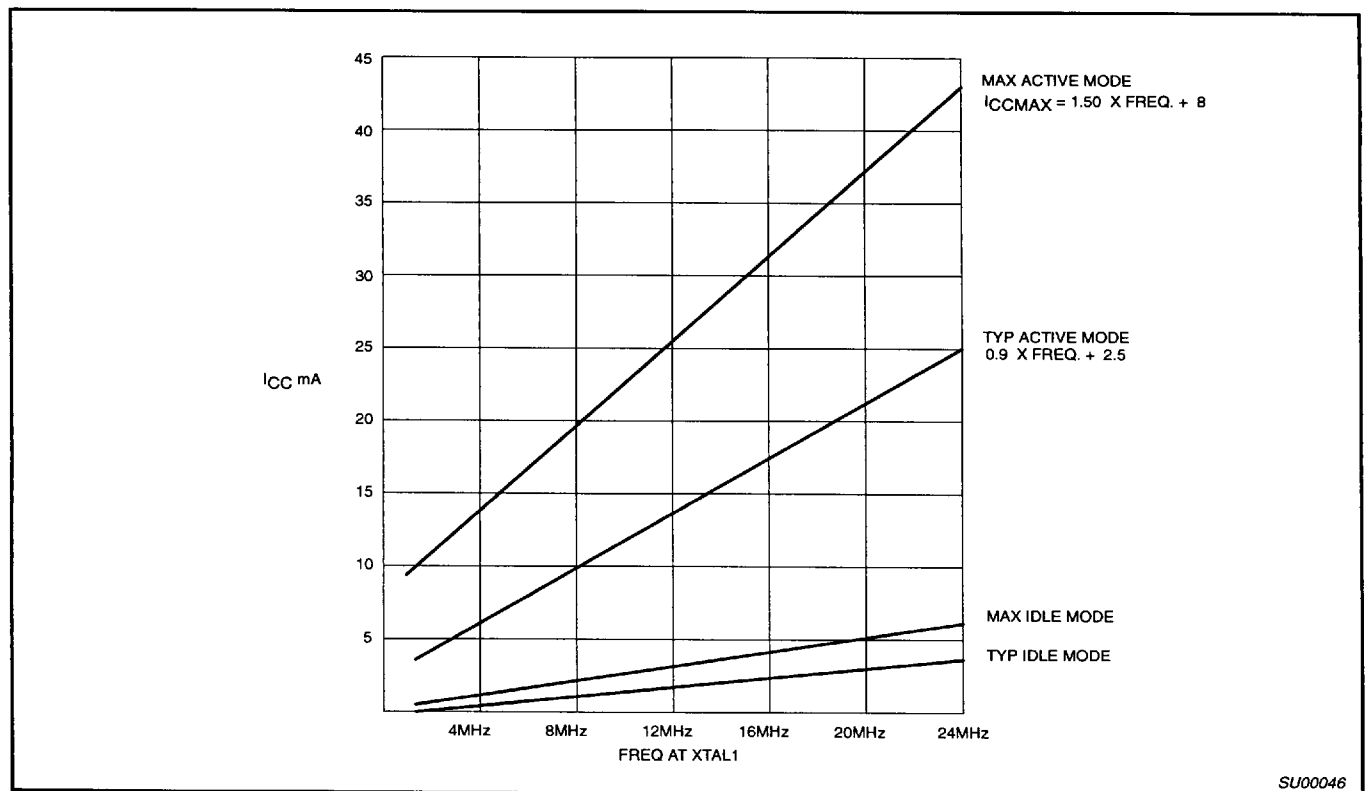
SU00010

Figure 21. AC Testing Input/Output



SU00011

Figure 22. Float Waveform



SU00046

Figure 23. I_{CC} vs. FREQ
 Valid only within frequency specifications of the device under test

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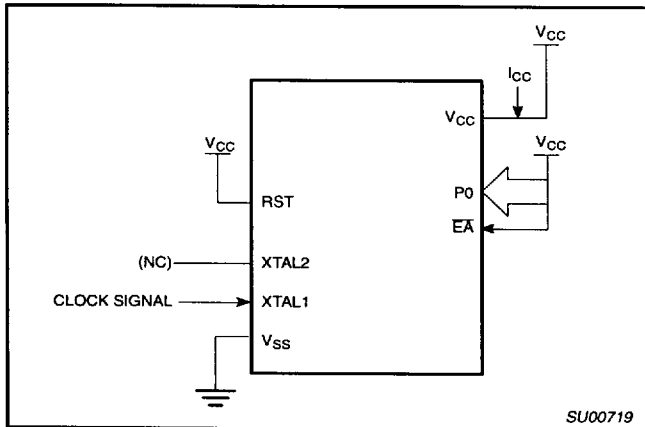


Figure 24. I_{CC} Test Condition, Active Mode
All other pins are disconnected

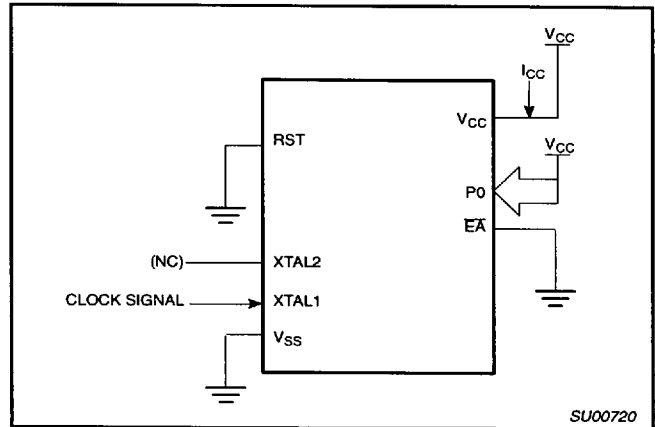


Figure 25. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

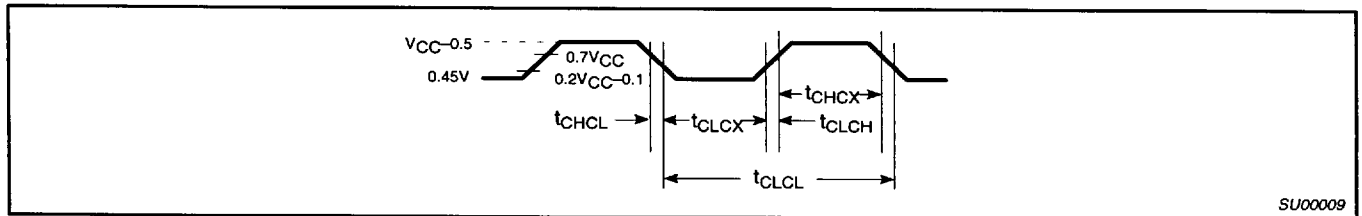


Figure 26. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
 $t_{CLCH} = t_{CHCL} = 5ns$

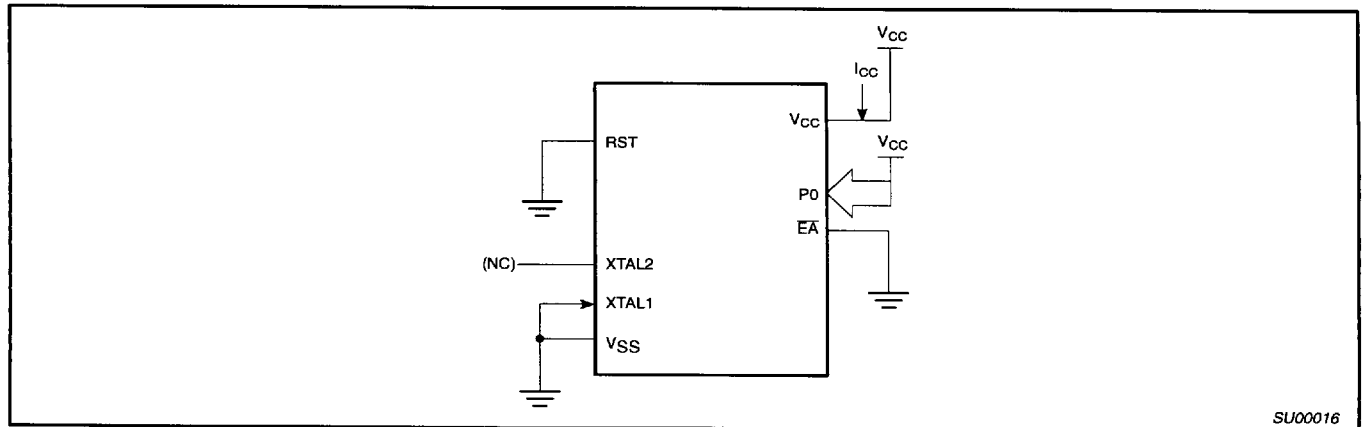


Figure 27. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected. $V_{CC} = 2V$ to $5.5V$

CMOS single-chip 8-bit microcontrollers

87C51FA/87C51FB

EPROM CHARACTERISTICS

The 87C51FA/FB is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C51FA/FB contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C51FA/FB manufactured by Philips.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 28 and 29. Figure 30 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 28. Note that the 87C51FA/FB is running with a 3.5MHz to 12MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 28. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 2 and 3 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3. The ALE/PROG is pulsed low 15 to 25 times as shown in Figure 29.

To program the encryption table, repeat the 15 to 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 15 to 25 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the \overline{EA}/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Table 3. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	\overline{EA}/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm security bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm security bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:

1. '0' = Valid low for that pin, '1' = valid high for that pin.

2. $V_{PP} = 12.75V \pm 0.25V$.

3. $V_{CC} = 5V \pm 10\%$ during programming and verification.

* ALE/PROG receives 15 to 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 50µs to 100µs and high for a minimum of 10µs.

™Trademark phrase of Intel Corporation.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 30. The other pins are held at the 'Verify Code Data' levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = B1H indicates 87C51FA

B2H indicates 87C51FB

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm². Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm² rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

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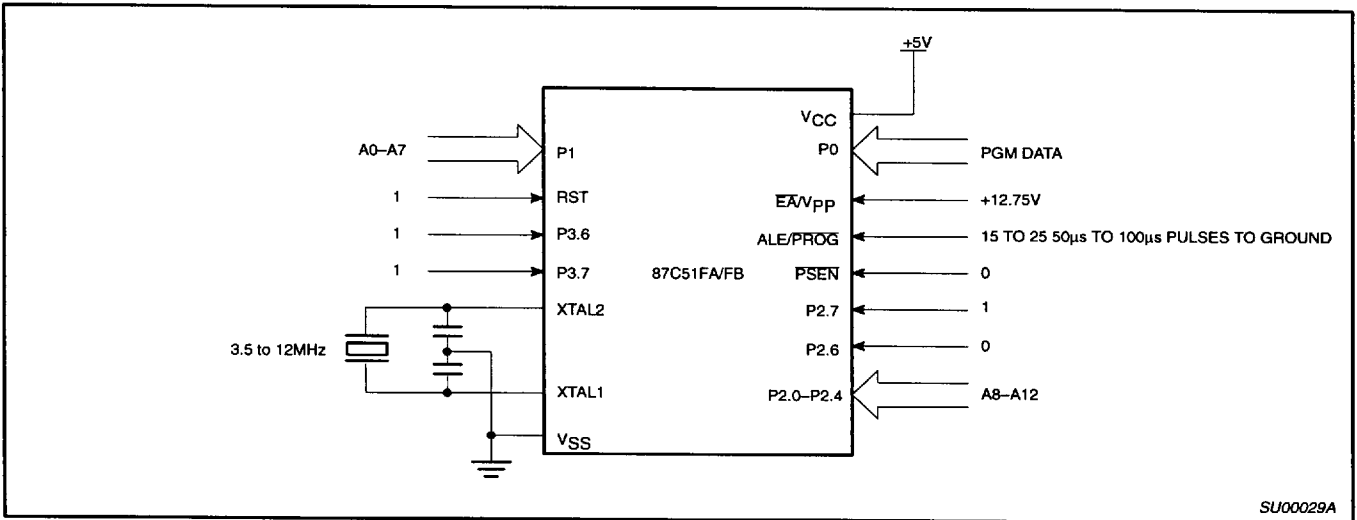


Figure 28. Programming Configuration

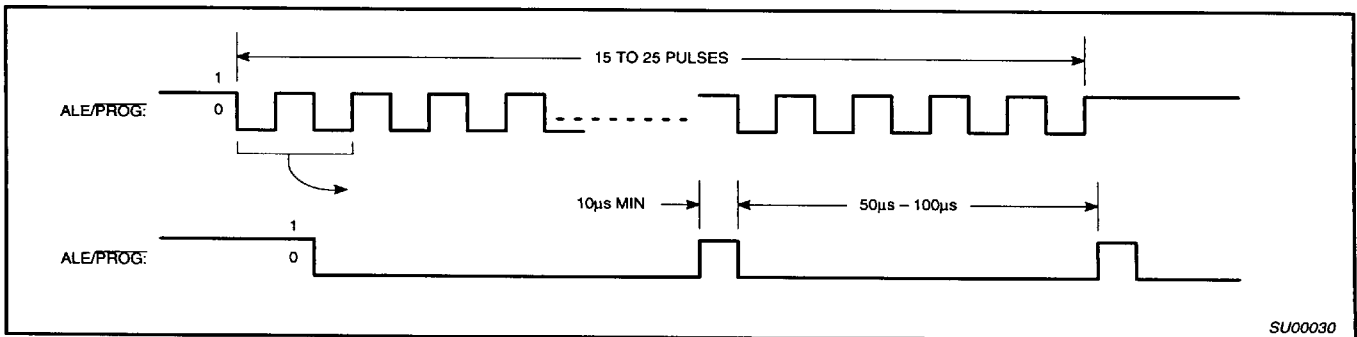


Figure 29. PROG Waveform

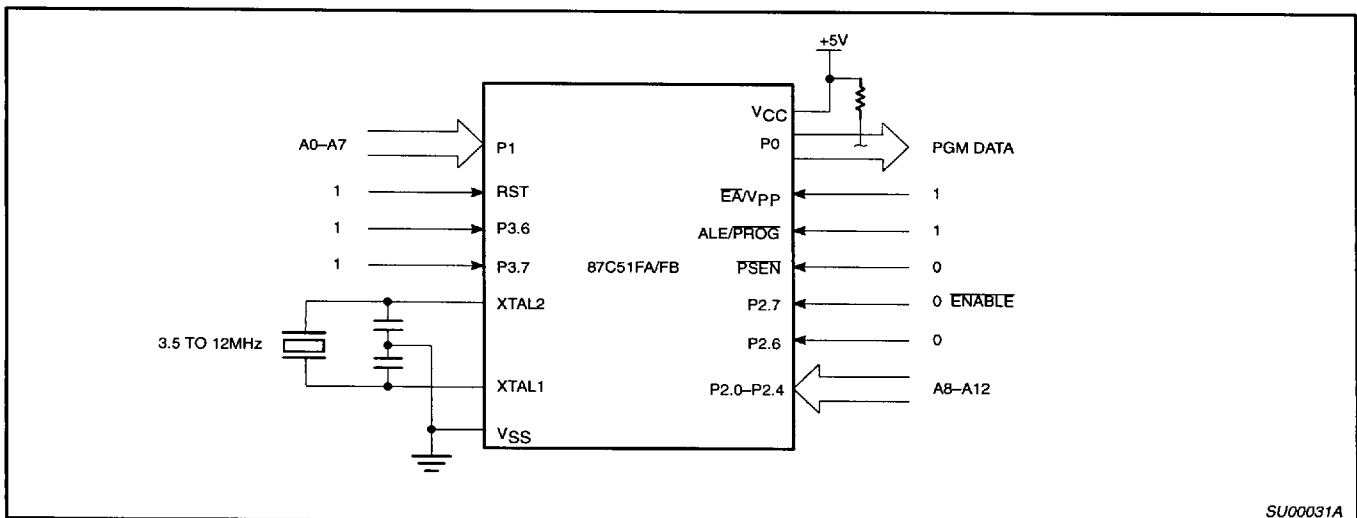


Figure 30. Program Verification

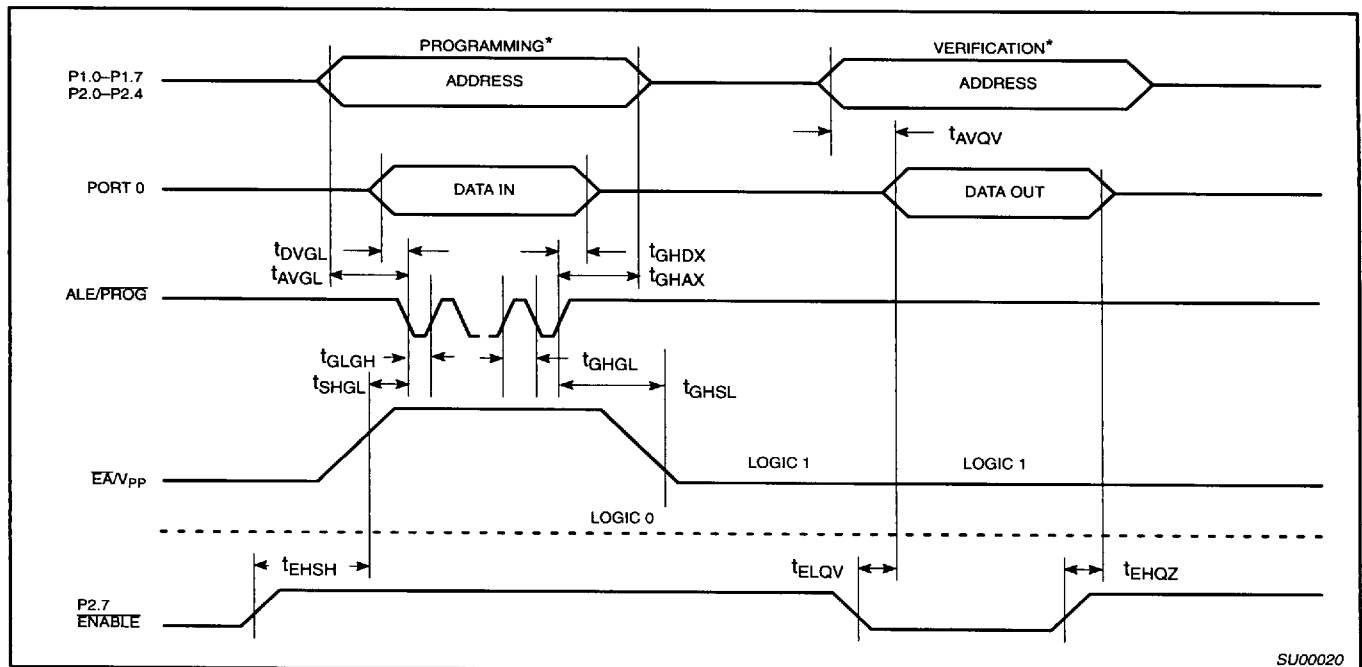
CMOS single-chip 8-bit microcontrollers

87C51FA/87C51FB

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_{amb} = 21^{\circ}\text{C}$ to $+27^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$ (See Figure 31)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{\text{PROG}}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{\text{PROG}}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{EHS}	P2.7 (ENABLE) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{\text{PROG}}$ low	10		μs
t_{GHSL}	V_{PP} hold after $\overline{\text{PROG}}$	10		μs
t_{GLGH}	$\overline{\text{PROG}}$ width	50	100	μs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	ENABLE low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after ENABLE	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{\text{PROG}}$ high to $\overline{\text{PROG}}$ low	10		μs



NOTE:

* FOR PROGRAMMING VERIFICATION SEE FIGURE 28.
 FOR VERIFICATION CONDITIONS SEE FIGURE 30.

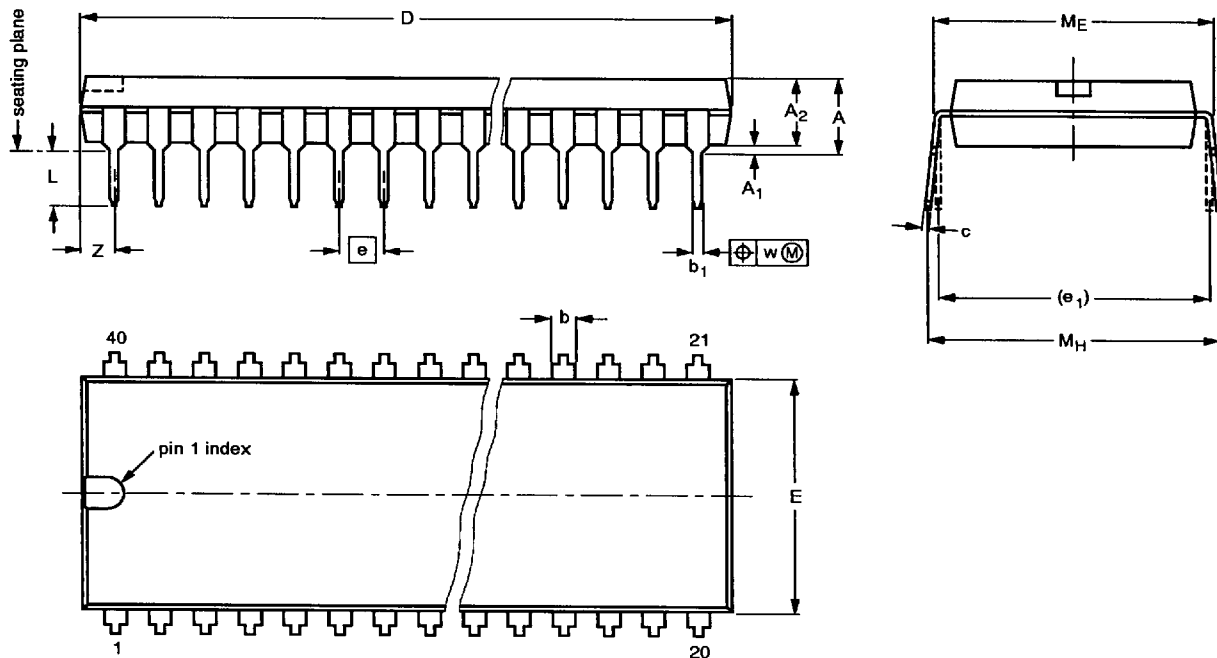
Figure 31. EPROM Programming and Verification

CMOS single-chip 8-bit microcontrollers

87C51FA/87C51FB

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				92-11-17 95-01-14

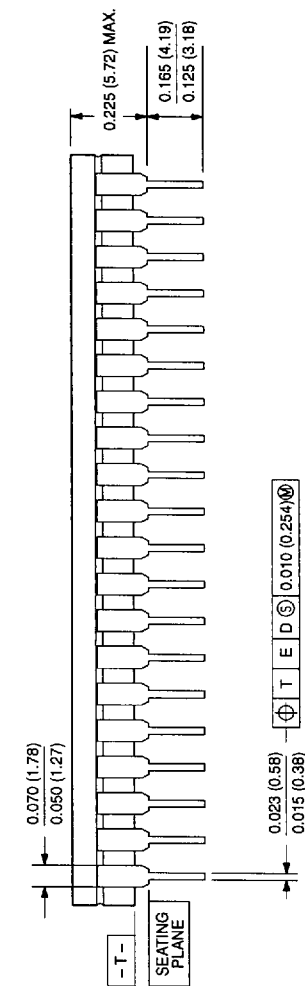
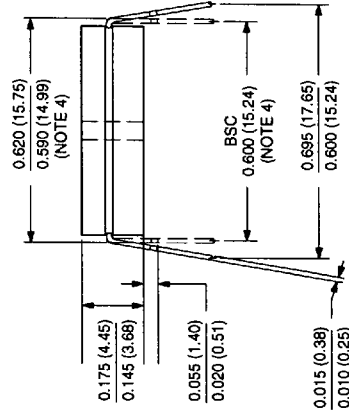
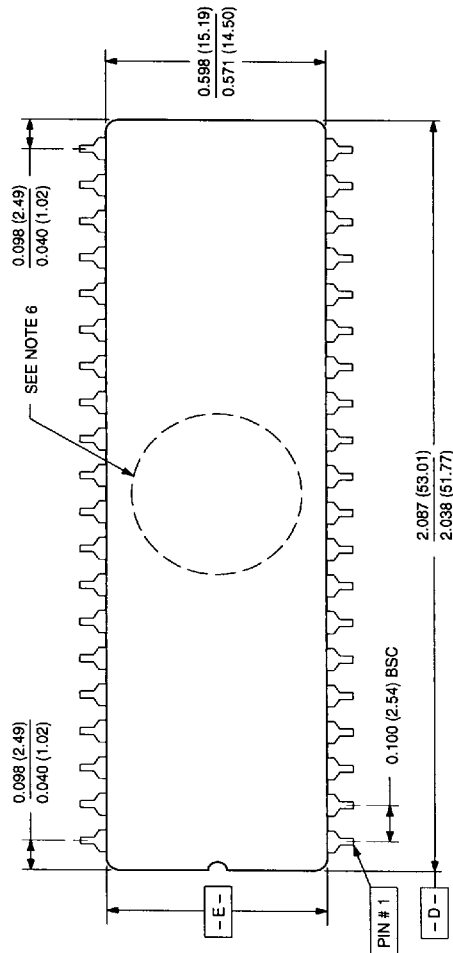
CMOS single-chip 8-bit microcontrollers

87C51FA/87C51FB

0590B 40-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE (WITH WINDOW (FA) PACKAGE)

NOTES:

1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14.5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #40 when viewed from the top.
6. Denotes window location for EPROM products.



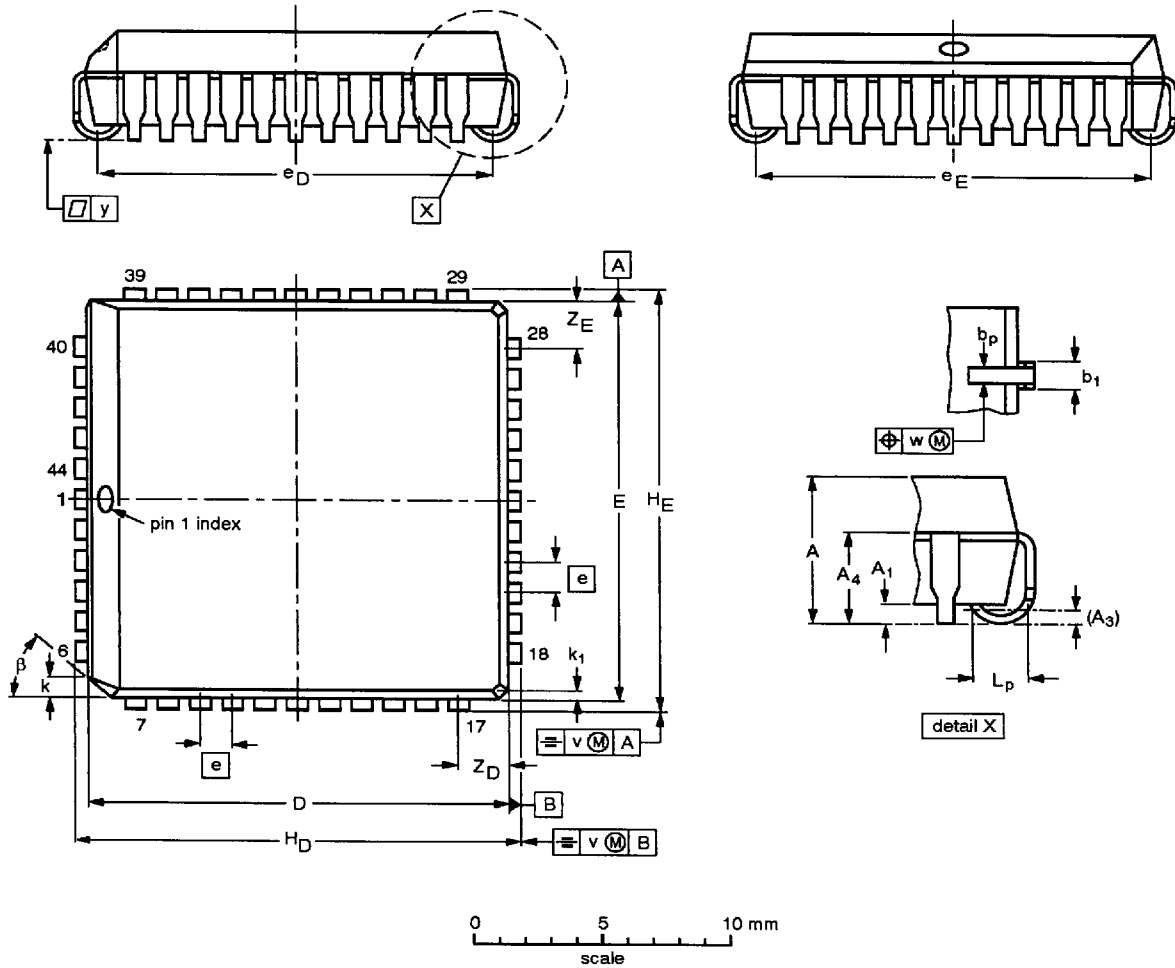
853-0590B 06688

CMOS single-chip 8-bit microcontrollers

87C51FA/87C51FB

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	k ₁ max.	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT187-2	112E10	MO-047AC			92-11-17 95-02-25

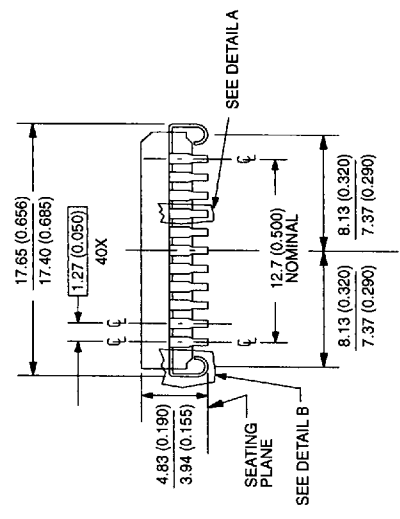
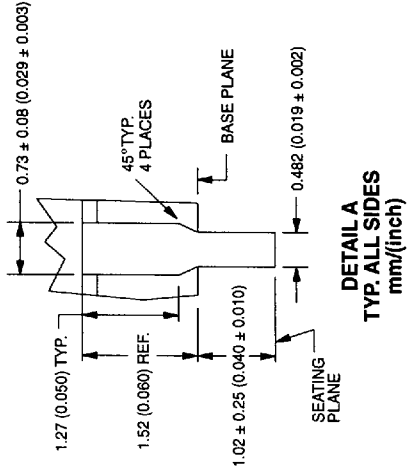
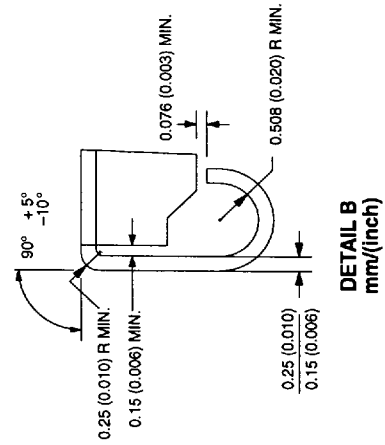
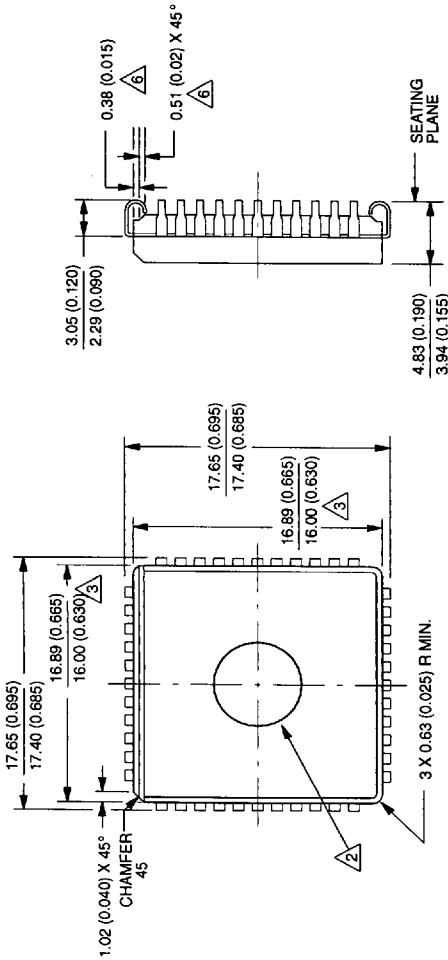
CMOS single-chip 8-bit microcontrollers

87C51FA/87C51FB

1472A 44-PIN CERQUAD J-BEND (K) PACKAGE

NOTES:

1. All dimensions and tolerances to conform to ANSI Y14.5-1982.
2. UV window is optional.
3. Dimensions do not include glass protrusion. Glass protrusion to be 0.005 inches maximum on each side.
4. Controlling dimension millimeters.
5. All dimensions and tolerances include lead trim offset and lead plating finish.
6. Backside solder relief is optional and dimensions are for reference only.

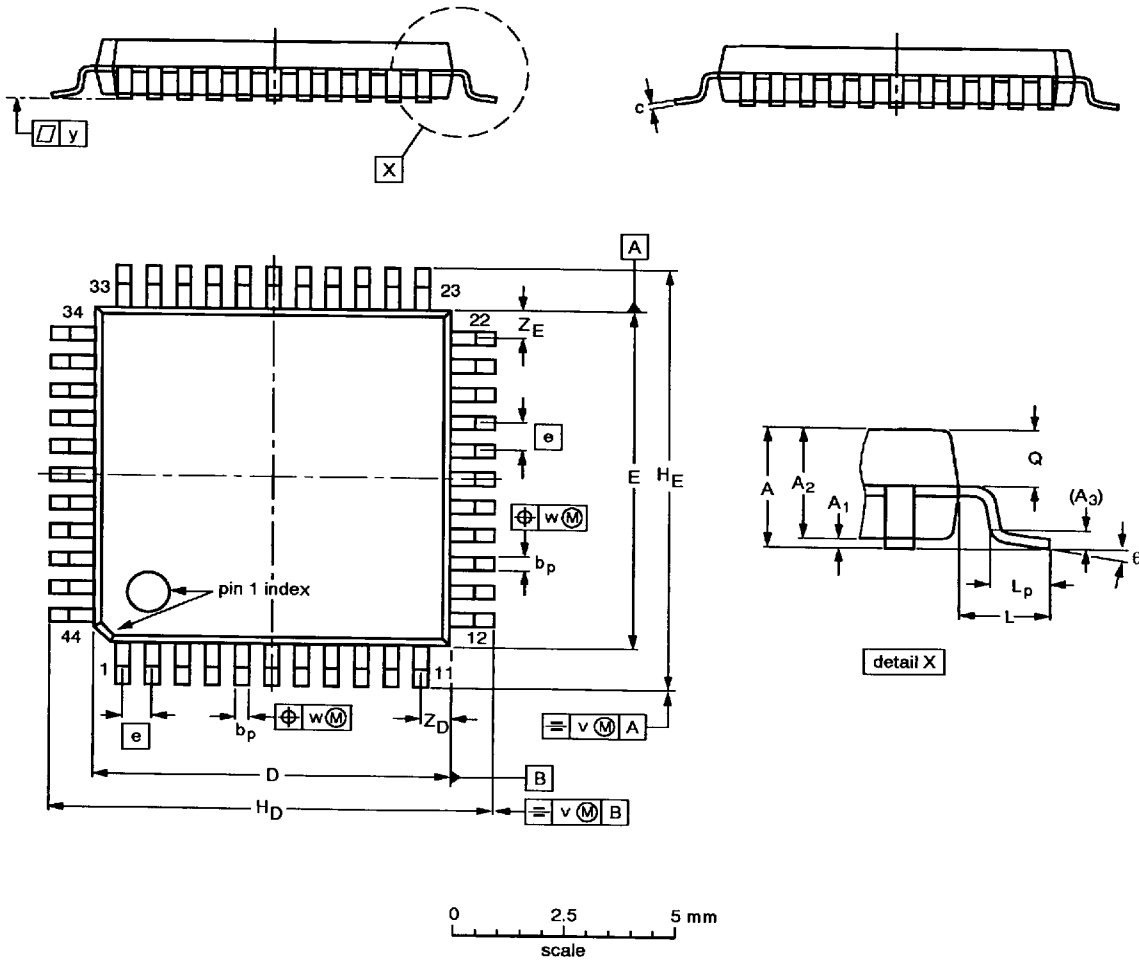


853-1472A 05854

CMOS single-chip 8-bit microcontrollers

87C51FA/87C51FB

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	Q	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						92-11-17 95-02-04