DATA SHEET

TDA8030; TDA8031
USB smart card reader (OTP or ROM)

Product specification

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Philips Semiconductors

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CONTENTS

USB smart card reader (OTP or ROM) TDA8030; TDA8031

1 FEATURES

- 83C51 core with 16 kbytes EPROM (ROM); 256 bytes RAM; 512 bytes AUXRAM; Timer 0,1, 2 and enhanced UART
- Full speed USB interface device which complies with USB 1.1 specification; accessible with MOVX instructions
- Control input and output; 1 generic input and output and 2 generic input end-points
- Compatible with bus powered and suspend mode supply current requirements
- Specific ISO7816 UART; accessible with MOVX instructions for automatic convention processing; variable baud rate through frequency or division ratio programming; error management at character level for T = 0 protocol; extra guard time register
- V_{CC} generation (5 or 3 V maximum current 55 mA or 1.8 V maximum current 35 mA) with controlled rise and fall times; current limitation and overload detection at 100 mA
- Cards clock generation with three times synchronous frequency doubling (12, 6, 3 and 1.5 MHz)
- Cards clock STOP HIGH or LOW or 1.25 MHz (from an integrated oscillator) for cards power reduction mode
- Automatic activation and deactivation sequences through an independent sequencer
- Supports the asynchronous protocols T = 0 and T = 1 in accordance with ISO7816 and EMV
- Versatile 24-bit time-out counter for Answer To Reset (ATR) and waiting times processing
- Supports synchronous cards
- Specific Elementary Time Unit (ETU) counter for Block Guard Time (BGT)
- Current limitations on cards contacts and emergency deactivation in case of over consumption or overheating
- Special circuitry for killing spikes during power-on or power-off
- Supply supervisor for power-on or power-off reset
- High efficiency inductive DC-to-DC converter for V_{CC} generation
- Soft switch on for avoiding current inrush at plug in
- Enhanced ESD protections on cards contacts (6 kV minimum)
- Software library for easy integration within the application.

2 APPLICATIONS

- Smart card readers for PC's or Set Top Boxes.

3 GENERAL DESCRIPTION

The TDA8030; TDA8031 is a bus powered full-speed USB device. All analog and digital functions for an EMV compliant Smart Card Reader are built-in. The embedded 83C51 microcontroller has 16 kbytes EPROM (ROM for TDA8031), 256 bytes RAM and 512 bytes of AUXRAM.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8030HL	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
TDA8031HL			

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDU}	bus supply voltage		4.2	–	5.5	V
I_{DDU}	bus supply current	V_{CC} = 5 V; I_{CC} = 40 mA; f_{clk} = 6 MHz	–	–	100	mA
I_{sus}	suspend current	card inactive; microcontroller in Power-down mode	–	–	500	μA
V_{CC}	card supply voltage	including static load; 5 V card	4.75	5	5.25	V
		with dynamic loads on 200 nF	4.60	–	5.40	V
		including static loads; 3 V card	2.85	3	3.15	V
		with dynamic loads on 200 nF	2.75	–	3.25	V
		including static loads; 1.8 V card	1.64	1.8	1.96	V
		with dynamic loads on 200 nF	1.62	–	1.98	V
I_{CC}	card supply current	5 V card	–	–	–55	mA
		3 V card	–	–	–55	mA
		1.8 V card	–	–	–35	mA
I_{lim}	current limit on V_{CC}		–	–	100	mA
I_{od}	overload detection on V_{CC}		–	–	100	mA
T_{amb}	ambient temperature		–25	–	+85	°C

6 BLOCK DIAGRAM

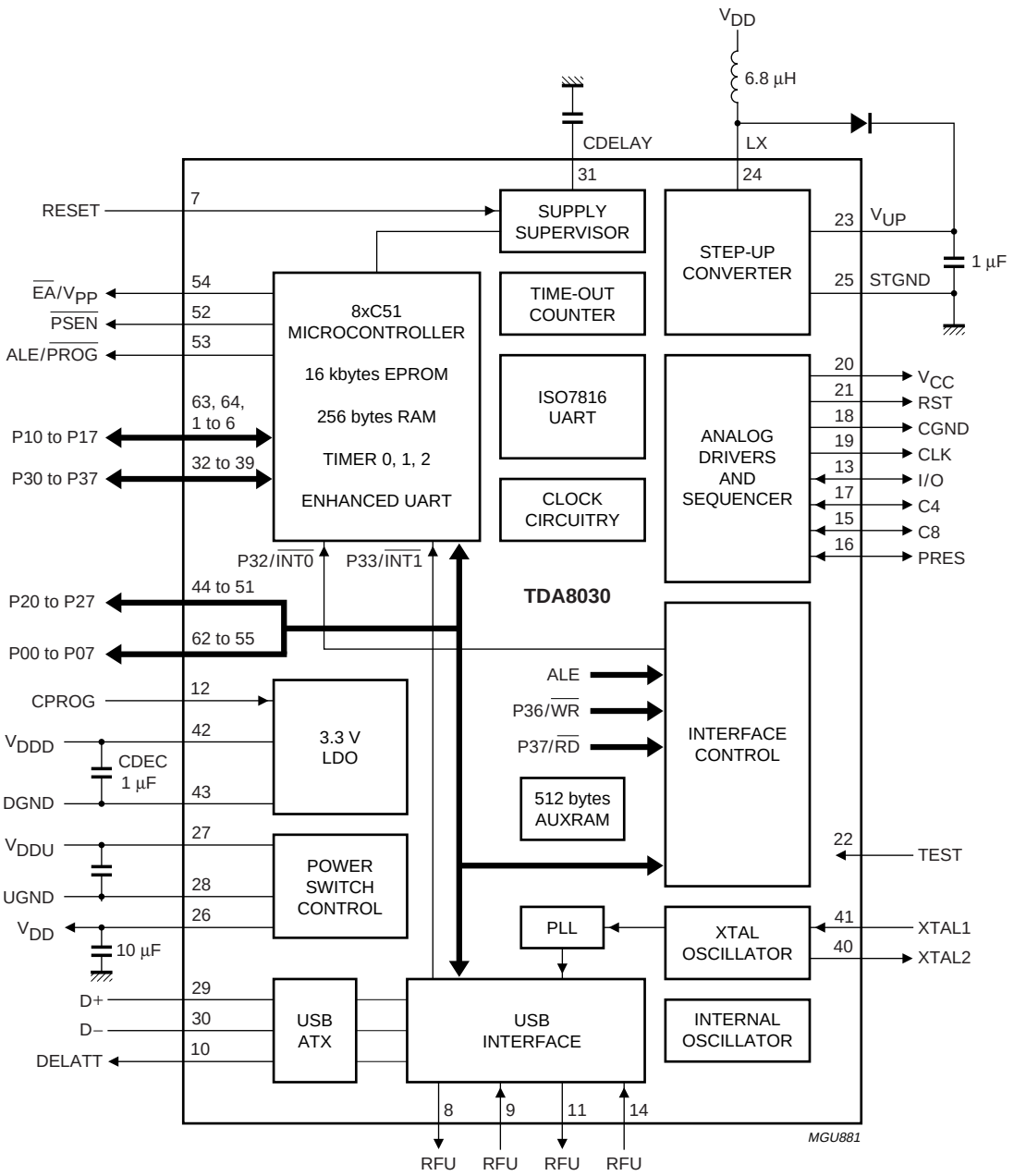

Fig.1 Block diagram (TDA8030).

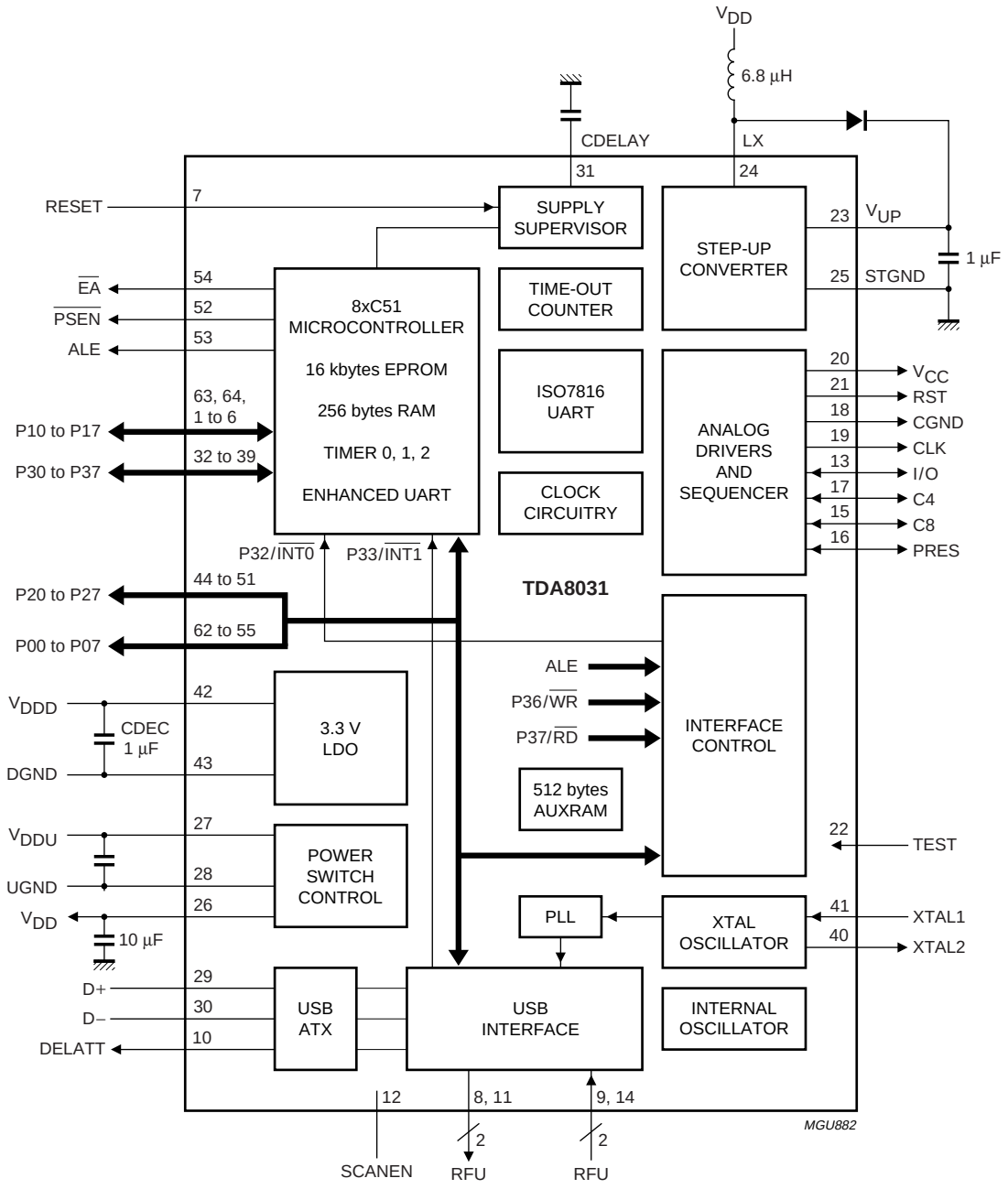

Fig.2 Block diagram (TDA8031).

7 PINNING

7.1 TDA8030

SYMBOL	PIN	DESCRIPTION
P12	1	8xC51 general purpose I/O port (USB_MC_READY)
P13	2	8xC51 general purpose I/O port (USB_CLK_EN_N)
P14	3	8xC51 general purpose I/O port (USB_RESET_N)
P15	4	8xC51 general purpose I/O port (USB_SOFTCONNECT_EXT)
P16	5	8xC51 general purpose I/O port (available for the application)
P17	6	8xC51 general purpose I/O port (available for the application)
RESET	7	reset input (active HIGH, integrated pull-down resistor to ground)
RFU	8	test pin; leave open-circuit in the application
RFU	9	test pin; leave open-circuit in the application
DELATT	10	delayed attachment reference signal output for external pull-up resistor on pin D+ (an internal 1.5 kΩ pull-up resistor is already embedded on-chip)
RFU	11	test pin; leave open-circuit in the application
CPROG	12	connect to GND within the application; for programming the EPROM connect to V_{DD} as well as pin TEST (pin 22); also used for test purposes
I/O	13	data input/output from the card (C7); 14 kΩ integrated pull-up resistor connected to V_{CC}
RFU	14	test pin; leave open-circuit in the application
C8	15	auxiliary I/O for C8 contact; 14 kΩ integrated pull-up resistor connected to V_{CC}
PRES	16	card presence detection input (active HIGH; no need for external pull-up)
C4	17	auxiliary I/O for C4 contact; 14 kΩ integrated pull-up resistor connected to V_{CC}
CGND	18	cards ground (C5) Must be connected to GND
CLK	19	clock output (C30)
V_{CC}	20	card supply output voltage (ISO C1 contact); must be decoupled with two 100 nF low ESR ceramic capacitors to CGND
RST	21	cards reset output (C2)
TEST	22	test pin input
V_{UP}	23	output of the DC-to-DC converter (decouple with a 1 μF capacitor to STGND)
LX	24	DC-to-DC converter inductor connection (a Schottky diode should be tied to V_{UP})
STGND	25	DC-to-DC converter ground connection
V_{DD}	26	soft switched positive supply voltage (decouple with 10 μF capacitor to GND)
V_{DDU}	27	positive supply voltage for the bus (4.2 to 5.5 V)
UGND	28	bus ground
D+	29	USB D+ data line
D–	30	USB D– data line
CDELAY	31	connection for an external capacitor to ground determining the Power-on reset pulse width (typ 1 ms per 2 nF)
P30/RxD	32	8xC51 general purpose I/O port/serial input port (available for the application)
P31/TxD	33	8xC51 general purpose I/O port/serial output port (available for the application)
P32/$\overline{\text{INT0}}$	34	8xC51 general purpose I/O port/external interrupt 0 (used by the ISO UART))
P33/$\overline{\text{INT1}}$	35	8xC51 general purpose I/O port/external interrupt 1 (used by the USB interface)

SYMBOL	PIN	DESCRIPTION
P34	36	8xC51 general purpose I/O port (USB_SUSPEND in TDA8030)
P35	37	8xC51 general purpose I/O port (USB_WAKEUP_N in TDA8031)
P36/$\overline{WR}$	38	external data memory write strobe
P37/$\overline{RD}$	39	external data memory read strobe
XTAL2	40	12 MHz crystal output; leave open-circuit if an external clock is used
XTAL1	41	external 12 MHz crystal connection or input for an external clock signal
V_{DDD}	42	3.3 V regulated digital supply voltage output (decouple with 1 μF ceramic capacitor)
DGND	43	Digital ground
P20/A8	44	8xC51 general purpose I/O port/address 8 (available for the application)
P21/A9	45	8xC51 general purpose I/O port/address 9 (available for the application)
P22/A10	46	8xC51 general purpose I/O port/address 10 (available for the application)
P23/A11	47	8xC51 general purpose I/O port/address 11 (available for the application)
P24/A12	48	8xC51 general purpose I/O port/address 12 (available for the application)
P25/A13	49	8xC51 general purpose I/O port/address 13 (USB_MP_C)
P26/A14	50	8xC51 general purpose I/O port/address 14 (USB_MP_SEL)
P27/A15	51	8xC51 general purpose I/O port/address 15 (ISO_UART_CS)
$\overline{PSEN}$	52	Program Store Enable: read strobe to external program memory when executing code from the external program memory; $\overline{PSEN}$ is activated twice each machine cycle except when two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
ALE/PROG	53	Address Latch Enable/Program Pulse: output pulse for latching the low byte of the address during an access to external memory. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency and can be used for external timing or clocking. It should be noted that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR Auxiliary0. With this bit set ALE will be active only during a MOVX instruction.
$\overline{EA}/V_{PP}$	54	External Access Enable/Programming Supply Voltage: $\overline{EA}$ must be externally held LOW to enable the device to fetch code from external program memory locations starting with 0000H. If $\overline{EA}$ is held HIGH the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (16 kbytes boundary). This pin also receives the 12.75 V programming supply voltage (V_{PP}) during EPROM programming. If security bit 1 is programmed $\overline{EA}$ will be internally latched on reset.
P07/AD7	55	8xC51 general purpose I/O port/address/data 7
P06/AD6	56	8xC51 general purpose I/O port/address/data 6
P05/AD5	57	8xC51 general purpose I/O port/address/data 5
P04/AD4	58	8xC51 general purpose I/O port/address/data 4
P03/AD3	59	8xC51 general purpose I/O port/address/data 3
P02/AD2	60	8xC51 general purpose I/O port/address/data 2
P01/AD1	61	8xC51 general purpose I/O port/address/data 1
P00/AD0	62	8xC51 general purpose I/O port/address/data 0
P10	63	8xC51 general purpose I/O port (USB_INT_MASK)
P11	64	8xC51 general purpose I/O port (USB_SOFTCONNECT_INT)

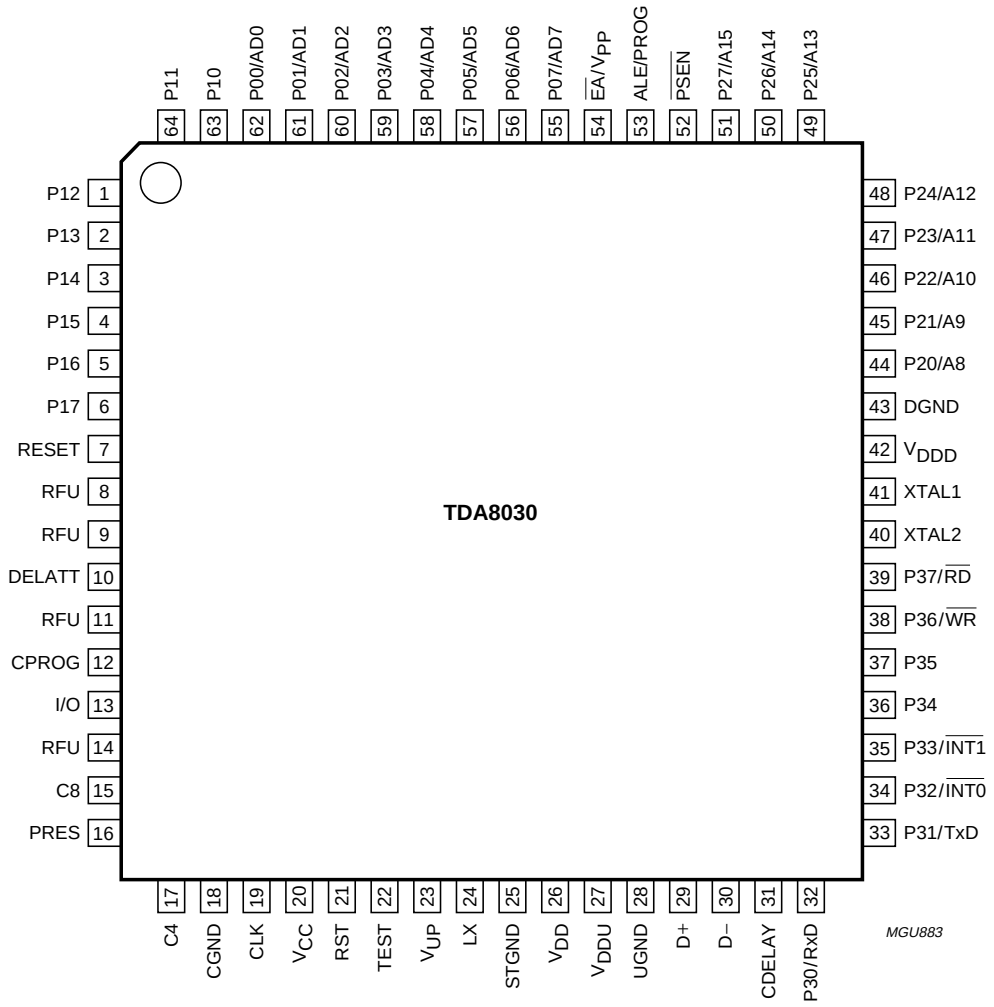

Fig.3 Pin configuration (top view).

7.2 TDA8031

SYMBOL	PIN	DESCRIPTION
P12	1	8xC51 general purpose I/O port (USB_MC_READY)
P13	2	8xC51 general purpose I/O port (USB_CLK_EN_N)
P14	3	8xC51 general purpose I/O port (USB_RESET_N)
P15	4	8xC51 general purpose I/O port (USB_SOFTCONNECT_EXT)
P16	5	8xC51 general purpose I/O port (available for the application)
P17	6	8xC51 general purpose I/O port (available for the application)
RESET	7	reset input (active HIGH, integrated pull-down resistor to ground)
RFU	8	test pin; leave open-circuit in the application
RFU	9	test pin; leave open-circuit in the application
DELATT	10	delayed attachment reference signal output for external pull-up resistor on pin D+ (an internal 1.5 kΩ pull-up resistor is already embedded in the chip)
RFU	11	test pin; leave open-circuit in the application
SCANEN	12	connect to GND within the application; for programming the EPROM connect to V_{DD} as well as pin TEST (pin 22); also used for test purposes
I/O	13	data input/output from the card (C7); 14 kΩ integrated pull-up resistor connected to V_{CC}
RFU	14	test pin; leave open-circuit in the application
C8	15	auxiliary I/O for C8 contact; 14 kΩ integrated pull-up resistor connected to V_{CC}
PRES	16	card presence detection input (active HIGH; no need for external pull-up)
C4	17	auxiliary I/O for C4 contact; 14 kΩ integrated pull-up resistor connected to V_{CC}
CGND	18	cards ground (C5) Must be connected to GND
CLK	19	clock output (C30)
V_{CC}	20	card supply output voltage (ISO C1 contact); must be decoupled with two 100 nF low ESR ceramic capacitors to CGND
RST	21	cards reset output (C2)
TEST	22	test pin input
V_{UP}	23	output of the DC-to-DC converter (decouple with a 1 μF capacitor to STGND)
LX	24	DC-to-DC converter inductor connection (a Schottky diode should be tied to V_{UP})
STGND	25	DC-to-DC converter ground connection
V_{DD}	26	soft switched positive supply voltage (decouple with 10 μF capacitor to GND)
V_{DDU}	27	positive supply voltage for the bus (4.2 to 5.5 V)
UGND	28	bus ground
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P33/$\overline{INT1}$	35	8xC51 general purpose I/O port/external interrupt 1 (used by the USB interface)
P34	36	8xC51 general purpose I/O port (USB_SUSPEND in TDA8030)

SYMBOL	PIN	DESCRIPTION
P35	37	8xC51 general purpose I/O port (USB_WAKEUP_N in TDA8030)
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P37/$\overline{RD}$	39	external data memory read strobe
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DGND	43	Digital ground
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P24/A12	48	8xC51 general purpose I/O port/address 12 (available for the application)
P25/A13	49	8xC51 general purpose I/O port/address 13 (USB_MP_C)
P26/A14	50	8xC51 general purpose I/O port/address 14 (USB_MP_SEL)
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$\overline{EA}$	54	External Access Enable/Programming Supply Voltage: $\overline{EA}$ must be externally held LOW to enable the device to fetch code from external program memory locations starting with 0000H. If $\overline{EA}$ is held HIGH the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (16 kbytes boundary). This pin also receives the 12.75 V programming supply voltage (V_{PP}) during EPROM programming. If security bit 1 is programmed $\overline{EA}$ will be internally latched on reset.
P07/AD7	55	8xC51 general purpose I/O port/address/data 7
P06/AD6	56	8xC51 general purpose I/O port/address/data 6
P05/AD5	57	8xC51 general purpose I/O port/address/data 5
P04/AD4	58	8xC51 general purpose I/O port/address/data 4
P03/AD3	59	8xC51 general purpose I/O port/address/data 3
P02/AD2	60	8xC51 general purpose I/O port/address/data 2
P01/AD1	61	8xC51 general purpose I/O port/address/data 1
P00/AD0	62	8xC51 general purpose I/O port/address/data 0
P10	63	8xC51 general purpose I/O port (USB_INT_MASK)
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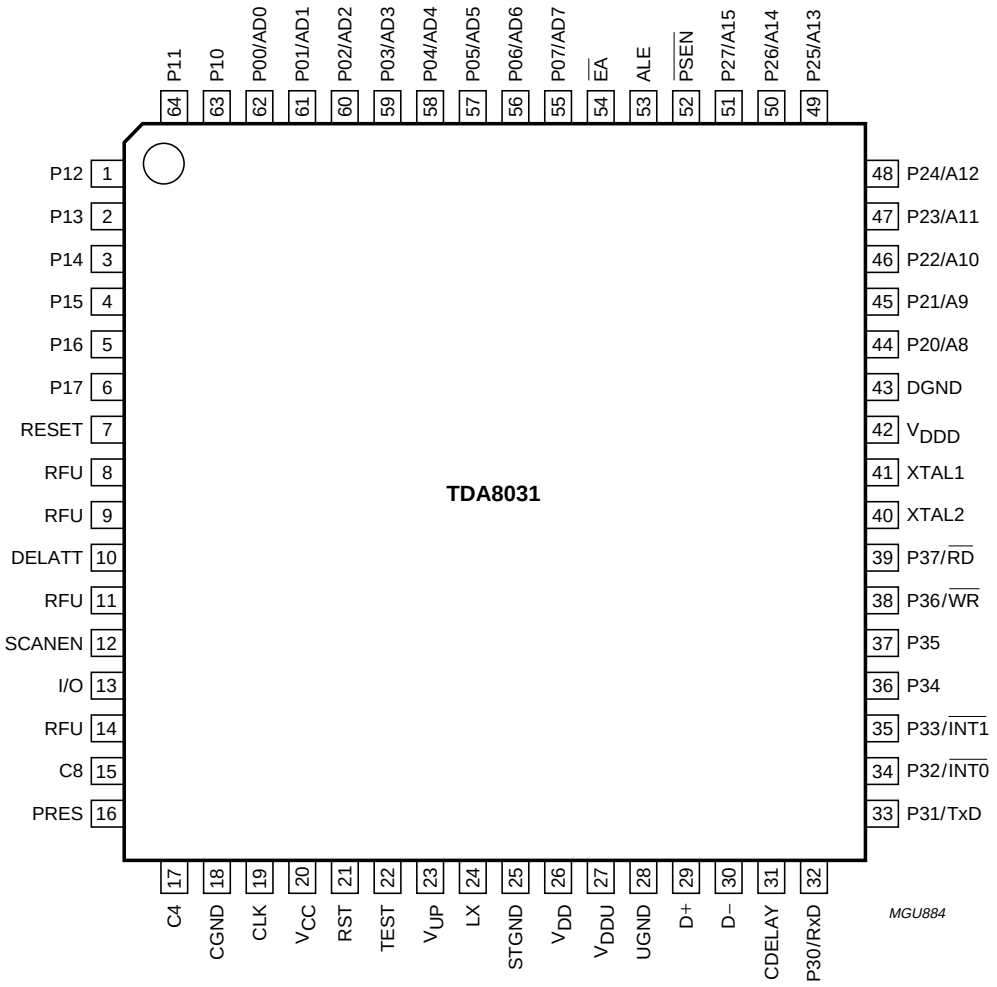


Fig.4 Pin configuration (top view).

8 FUNCTIONAL DESCRIPTION

Throughout this specification, it is assumed that the reader is aware of ISO7816 and USB norms terminology.

8.1 ISO7816 UART AND ASSOCIATED LOGIC

This section describes how the integrated ISO7816 UART operates, how it can be programmed by means of its control registers and how it is internally interfaced to the embedded microcontroller.

8.1.1 INTERFACE CONTROL

The ISO7816 UART can be controlled via an 8-bit parallel bus. This bus is directly (internally) connected to Port 0 (P07 to P00) of the embedded 83C51 microcontroller.

The registers within the ISO7816 UART may be written to or read from by using the standard 83C51 MOVX instructions. It should be noted, that only if pin P27/A15 is HIGH, can the UART be accessed.

When pin P27/A15 is HIGH, the demultiplexing of address and data is done internally by means of the ALE signal. A LOW pulse on pin P37/$\overline{RD}$ enables the selected register to be read, a LOW pulse on pin P36/$\overline{WR}$ enables the selected register to be written to.

The ISO UART interrupt line is directly connected to the microcontrollers External Interrupt 0 input, pin P32/$\overline{INT0}$. For that reason, the External Interrupt 0 of the 83C51 microcontroller must be enabled to ensure a proper function.

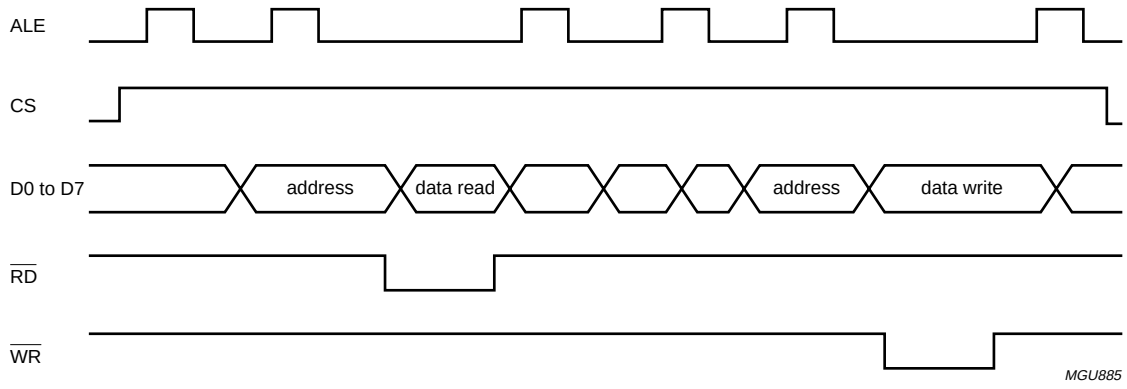


Fig.5 Control via MOVX instructions.

8.1.2 CONTROL REGISTERS

The TDA8030; TDA8031 has 1 analog interface for 7 contacts cards. The data to and from the cards is fed into an ISO UART.

The Card Select Register (CSR) contains one bit for resetting the ISO UART ($\overline{RIU}$, active LOW). This bit is reset after power-on and must be set HIGH before starting any operation. It may be reset by software when necessary.

The following dedicated registers enable the parameters of the ISO UART and the ETU counters to be set:

- Programmable Divider Register (PDR)
- Guard Time Register (GTR)
- Two UART Control Registers (UCR1 and UCR2)
- Clock Configuration Register (CCR)
- Time-Out Configuration Register (TOCR)
- Three Time-Out Registers (TOR1, TOR2 and TOR3).

There is also a dedicated Power Control Register (PCR) for controlling the power to the card.

When the specific parameters of the card have been programmed, the UART may be used with the following registers:

- UART Receive Register (URR)
- UART Transmit Register (UTR)
- UART Status Register (USR)
- Mixed Status Register (MSR).

In the reception mode, a FIFO of 1 to 8 characters may be used and is configured with the FIFO Control Register (FCR). This register may also be used for programming an automatic repetition of NAKed characters in the transmission mode.

The Hardware Status Register (HSR) gives the status of the supply voltage, of the hardware protections and of the card movements.

The USR and HSR give interrupts on pins INT when some of their bits have been changed.

The MSR does not give interrupts and may be used in the polling mode for some operations; when this is the case, the bit Transmit Buffer Empty/Receive Buffer Full (TBE/RBF) within the USR may be masked.

A 24-bit time-out counter may be started to provide an interrupt after a number of ETUs programmed in time-out registers TOR1, TOR2 and TOR3. This will help the microcontroller when processing different real-time tasks (ATR, WWT and BWT etc.), mainly if the microcontrollers and cards clock are asynchronous.

This counter is configured with a Time-Out Counter Configuration register (TOCC) and may be used as a 24-bit or as a 16 + 8-bit counter. Each counter may be set to start counting once data has been written, or on detection of a start bit on the I/O or as autoreload.

8.1.3 GENERAL REGISTERS

8.1.3.1 Card select register

The Card Select Register (CSR) is used for resetting the ISO UART.

The bit Reset ISO UART ($\overline{RIU}$) must be set to logic 1 by software before any action on the UART. When set to logic 0, this bit resets a large part of the UART registers to their default value; see Table 1. A minimum pulse of 10 ns is needed on $\overline{RIU}$. This bit must be reset before any new activation.

Table 1 Card select register (address 00H; write and read); note 1

7	6	5	4	3	2	1	0
–	–	–	–	$\overline{RIU}$	–	–	–

Note

1. All bits are cleared after reset.

8.1.3.2 Hardware status register

The Hardware Status Register (HSR) gives the status of the chip after a hardware problem has been detected.

Table 2 Hardware Status Register (address 0FH; read only); note 1

7	6	5	4	3	2	1	0
–	–	PRTL	SUPL	–	PRL	–	PTL

Note

1. All bits are cleared after reset.

Table 3 Description of the HSR bits

BIT	SYMBOL	DESCRIPTION
7 and 6	–	not used
5	PRTL	Protection 1: Bit PRTL = 1 when a default has been detected on card reader. Bit PRTL is the OR function of the protection on pins V_{CC} and RST.
4	SUPL	Supervisor Latch: Bit SUPL = 1 when the supervisor has been activated.
3	–	not used
2	PRL	Presence Latch: Bit PRL = 1 when a change has occurred on pin PRES.
1	–	not used
0	PTL	Overheating: Bit PTL = 1 if overheating has occurred.

When either bits PRTL, PRL or PTL is logic 1, then pin $\overline{INT0}$ is LOW. The bits having caused the interrupt are cleared when the HSR has been readout ($2 \times f_{int}$ cycles after the rising edge of $\overline{RD}$).

At power-on, or after a supply voltage drop-out, SUPL is set and $\overline{INT0}$ is LOW. $\overline{INT0}$ will return HIGH at the end of the internal Power-on reset pulse defined by the value of the capacitor connected to pin CDELAY. SUPL will be reset only after a status register readout outside the Power-on reset pulse; see Fig.8.

In the event of emergency deactivation (by PRTL, SUPL, PRL and PTL), bit START will be automatically reset by hardware.

8.1.3.3 Time-out registers

The three Time-Out Registers TOR1, TOR2 and TOR3 form a programmable 24-bit ETU counter, or two independant counters (one 16-bit and one 8-bit).

The value to load in TOR1, TOR2 and TOR3 is the number of ETUs to count.

Table 4 Time-out register 1 (address 09H; write only); note 1

7	6	5	4	3	2	1	0
TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0

Note

1. All bits are cleared after reset.

Table 5 Time-out register 2 (address 0AH; write only); note 1

7	6	5	4	3	2	1	0
TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8

Note

1. All bits are cleared after reset.

Table 6 Time-out register 3 (address 0BH; write only); note 1

7	6	5	4	3	2	1	0
TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16

Note

1. All bits are cleared after reset.

8.1.3.4 Time-out configuration register

The Time-Out Configuration register (TOCR) is used for setting different configurations of the time-out counter according to Table 8; all other configurations are undefined.

The timers can operate in 3 modes:

1. Software triggered
2. Start bit triggered
3. Autoreload.

Table 7 Time-out configuration register (address 08H; read and write); note 1

7	6	5	4	3	2	1	0
TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0

Note

1. All bits are cleared after reset.

Table 8 Time-out counter configuration

TOC VALUE	OPERATING MODE
00H	All counters are stopped.
05H	Counters 2 and 3 are stopped; counter 1 continues to operate in autoreload mode.
61H	Counter 1 is stopped and counters 3 and 2 form a 16-bit counter. Counting the value stored in TOR3 and TOR2 is started after 6H is written in the TOCR. An interrupt is given and bit TO3 is set within the USR when the terminal count is reached. The counter is stopped by writing 00H in the TOCR and will be stopped before reloading a new value in TOR2 and TOR3.
65H	Counter 1 is an 8-bit autoreload counter and counters 3 and 2 form a 16-bit counter. Counter 1 starts counting the content of TOR1 on the first START bit (reception or transmission) detected on I/O after 65H is written in the TOCR. When Counter 1 reaches its terminal count, an interrupt is given, bit TO1 in the USR is set and the counter automatically restarts the same count until it is stopped. It is not allowed to change the content of TOR1 during a count. Counters 3 and 2 are wired as a single 16-bit counter and starts counting the value TOR3 and TOR2 when 65H is written in the TOCR. When the counter reaches its terminal count, an interrupt is given and bit TO3 is set within the USR. Both counters are stopped when 00H is written in the TOCR. Counters 3 and 2 will be stopped by writing 05H in the TOCR before reloading a new value in TOR2 and TOR3.
68H	Counters 3, 2 and 1 are wired as a single 24-bit counter. Counting the value stored in TOR3, TOR2 and TOR1 is started after 68H is written in the TOCR. The counter is stopped by writing 00H in the TOCR. It is not allowed to change the content of TOR3, TOR2 and TOR1 within a count.
7CH	Counters 3, 2 and 1 are wired as a single 24-bit counter. Counting the value stored in TOR3, TOR2 and TOR1 on the first start bit detected on I/O (reception or transmission) after the value has been written. It is possible to change the content of TOR3, TOR2 and TOR1 during a count; the current count will not be affected and the new count value will be taken into account at the next start bit. The counter is stopped by writing 00H in the TOCR. In this configuration TOR3, TOR2 and TOR1 must not be all zero.
85H	Same as 05H, except that all the counters will be stopped at the end of the 12th ETU following the first received start bit detected after 85H has been written in the TOCR.
E5H	Same configuration as TOCR = 65H, except that Counter 1 will be stopped at the end of the 12th ETU following the first start bit detected after E5H has been written in the TOCR.

The time-out counter is very useful for processing the clock counting during ATR, the Work Waiting Time (WWT) or the waiting times defined in T = 1 protocol. The 200 and 384 clock counter used during ATR is done by hardware when Start Session is set, a specific hardware takes care of BGT in T = 1 protocol and a specific register is present for processing the extra guard time.

It is not allowed to change the content of the TOR registers whilst a counter is in software triggered mode, or in autoreload mode. In these modes, it is mandatory to stop the counters (TOCR = 00H or 05H) before updating the count value in the TOR registers. In start bit triggered mode, the value may be changed at any time; the new count value will be taken into account on the next start bit.

The minimum time interval between 2 successive write operations in TOCR is $^{2}/_{31}$ or $^{2}/_{32}$ ETU.

It is obvious that the counters may only be used once the card has been activated.

Detailed examples of how to use these specific timers can be found in Application Note *“AN01012”*.

8.1.4 ISO UART REGISTERS

8.1.4.1 UART transmit register

When the microcontroller wants to transmit a character to the card, it writes the data in direct convention in this register.

The transmission:

- Starts at the end of this writing (2 clock cycles after the rising edge of $\overline{WR}$) if the previous character has been transmitted and if the extra guard time has expired
- Starts at the end of the extra guard time if this one has not expired
- Starts at 13.5 ETU in manual mode and 15 ETU in automatic mode if the previous character has been NAKed by the card; see Section 8.1.4.4
- Does not start if the transmission of the previous character is not completed.

When the transmission is completed:

- In T = 0, bit TBE is set at 11.5 ETU, and bit PE in the event of parity error
- In T = 1, bit TBE is set at 10.5 ETU.

In the event of synchronous cards (bit SAN set within UCR2), UT0 is only relevant and is copied on the I/O of the card. It is possible to write within the UTR before setting the transmission mode, which may be useful in some cases.

Table 9 UART transmit register (address 0DH; write only); note 1

7	6	5	4	3	2	1	0
UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0

Note

1. All bits are cleared after reset.

8.1.4.2 UART receive register

When the microcontroller wants to read data from the card, it reads it from this register in direct convention.

In the event of synchronous cards, only UR0 is relevant and is a copy of the state of the card I/O.

In the event of parity error:

- The bit PE in the status register USR is set at 10.5 ETU and $\overline{INT0}$ falls LOW
- In protocol T = 0, the received byte is not stored in URR; In protocol T = 1, the received byte is stored.

In both protocols, when a character has been stored, then the bit RBF in the status register USR is set at 10.5 ETU. This bit is reset when the character has been read from the URR.

When the URR is empty, then bit FE (in the MSR) is set as long as no character has been received.

Table 10 UART receive register (address 0DH; read only); note 1

7	6	5	4	3	2	1	0
UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0

Note

1. All bits are cleared after reset.

8.1.4.3 Mixed status register

The Mixed Status Register (MSR) relates the status of the cards presence contact PRES, the BGT counter, the FIFO empty indication, the transmit/receive ready indicator TBE/RBF and the completion of clock switching to or from $\frac{1}{2}f_{int}$.

Table 11 Mixed status register (address 0CH; read only); note 1

7	6	5	4	3	2	1	0
CLKSW	FE	BGT	–	–	PR	–	TBE/RBF

Note

1. Bits TBE/RBF are cleared after reset; bit FE is set after reset.

Table 12 Description of the MSR bits; note 1

BIT	SYMBOL	DESCRIPTION
7	CLKSW	Clock switch: Bit CLKSW = 1 when the TDA8030; TDA8031 has performed a required clock switch from $\frac{1}{n}f_{xtal}$ to $\frac{1}{2}f_{int}$ and is reset when the TDA8030; TDA8031 has performed a required clock switch from $\frac{1}{2}f_{int}$ to $\frac{1}{n}f_{xtal}$; the application will wait until this bit has been set or reset before setting the microcontroller in power-down mode or restarting sending commands after leaving power-down mode (only needed when the clock is not stopped). This bit is also reset by $\overline{RIU}$ and at power-on.
6	FE	FIFO Empty: Bit FE = 1 when the reception FIFO is empty; it is reset when at least one character has been loaded in the FIFO.
5	BGT	Block Guard Time: In T = 1 protocol, the bit BGT is linked with a 22 ETU counter, which is started at every start bit on the I/O. If the count is finished before the next start bit, then bit BGT is set. This helps to ensure that the card has not answered before 22 ETU after the last transmitted character, or that the reader is not transmitting a character before 22 ETU after the last received character. In T = 0 protocol, the bit BGT is linked to a 16 ETU counter, which is started at every start bit on the I/O. If the count is finished before the next start bit, then the bit BGT is set. This helps to ensure that the reader is not transmitting too early after the last received character.
4 and 3		not used
2	PR	Presence: Bit PR = 1 when the card is present.
1	–	not used
0	TBE/RBF	Transmit Buffer Empty/Receive Buffer Full: Bit TBE/RBF = 1 when: • Changing from reception mode to transmission mode • A character has been transmitted by the UART (except when a character has been transmitted free of parity error while LCT = 1) • The reception buffer is full. Bit TBE/RBF = 0 after power-on, or after one of the following: • When the bit $\overline{RIU}$ is reset • When a character has been written into register UTR • When the character has been read in register URR • When changing from transmission mode to reception mode.

Note

1. No bits within the MSR have an effect on $\overline{INT0}$.

8.1.4.4 FIFO control register

The FIFO Control Register (FCR) relates the parity error count and the FIFO length.

Table 13 FIFO control register (address 0CH; write only); note 1

7	6	5	4	3	2	1	0
–	PEC2	PEC1	PEC0	–	FL2	FL1	FL0

Note

1. All bits are cleared after reset.

Table 14 Description of the FCR bits

BIT	SYMBOL	DESCRIPTION
7	–	not used
6 to 4	PEC2 to PEC0	Parity Error Count: PEC2, PEC1 and PEC0 determine the number of parity errors before setting the bit PE within the USR and pulling $\overline{INT0}$ LOW; 000 means that only one parity error has occurred and bit PE is set. The value 000 indicates that if only one parity error has occurred bit PE is set; the value 111 indicates that PE will be set after 8 parity errors. In protocol T = 0: • If a correct character is received before the programmed error number is reached the error counter will be reset • If the programmed number of allowed parity errors is reached, bit PE in the USR will be set as long as the USR has not been read • If a transmitted character has NAKed by the card, then the TDA8030; TDA8031 will automatically re-transmit it a number of times equal to the value programmed in PEC2, PEC1 and PEC0. The character will be resent at 15 ETU • In transmission mode, if bits PEC2, PEC1 and PEC0 are at logic 0, then the automatic re-transmission is invalidated; the character manually rewritten in the UTR will start at 13.5 ETU. In protocol T = 1: • The error counter has no action; bit PE is set at the first incorrectly received character.
3	–	not used
2 to 0	FL2 to FL0	FIFO Length: Bits FL2, FL1 and FL0 determine the depth of the FIFO: • 000 = length 1 • 111 = length 8

8.1.4.5 UART status register

The UART Status Register (USR) is used by the microcontroller to monitor the activity of the ISO UART and of the time-out counter.

Table 15 UART status register (address 0EH; read only); note 1

7	6	5	4	3	2	1	0
TO3	–	TO1	EA	PE	OVR	FER	TBE/RBF

Note

1. All bits are cleared after reset.

Table 16 Description of the USR bits

BIT	SYMBOL	DESCRIPTION
7	TO3	Time-Out counter 3: Bit TO3 = 1 when counter 3, or counters 3 + 2 or counters 3 + 2 + 1 have reached their terminal count.
6	–	not used
5	TO1	Time-Out counter 1: Bit TO1 = 1 when counter 1 has reached its terminal count.
4	EA	Early Answer: When bit RST is LOW, EA is HIGH if the first start bit on the I/O during ATR has been detected between 200 and 384 clock pulses (all activities on the I/O during the first 200 clock pulses with RST LOW are not taken into account). When RST is HIGH, EA is HIGH if a start bit has been detected before the 384th clock pulse. These two features are reinitialized at each toggling of RST.
3	PE	Parity Error: In T = 0 protocol, PE = 1 if the UART has detected a number of received characters with parity error equal to the number written in PEC2, PEC1 and PEC0 or if a transmitted character has been NAKed by the card a number of times equal to the value programmed in PEC2, 1 and 0. It is set at 10.5 ETU in reception mode and at 11.5 ETU in transmission mode. In T = 0 protocol, a character received with a parity error is not stored in the FIFO, the card is supposed to repeat this character. In T = 1 protocol, a character with a parity error is stored in the FIFO and the parity error counter is not operating.
2	OVR	Overrun: Bit OVR = 1 if the UART has received a new character while the URR was full. In this case, at least one character has been lost. OVR is set at 10.5 ETU.
1	FER	Framing Error: Bit FER = 1 when the I/O was not in high-impedance state at 10.25 ETU after a start bit. It is reset when the USR has been read-out.
0	TBE/RBF	Transmission Buffer Empty/Reception Buffer Full: Bits TBE and RBF share the same bit within the USR. When in transmission mode the relevant bit is TBE; when in reception mode it is RBF. Bit TBE = 1 when the UART is in transmission mode and when the microcontroller may write the next character to transmit in the UTR. It is reset when the microcontroller has written data in the Transmit Register, or when the bit T/R within UCR1 has been reset either automatically or by software. TBE is set at 11.5 ETU in T = 0 protocol and at 10.5 ETU in T = 1 protocol. Bit RBF = 1 when the FIFO is full. The microcontroller may read some of the characters in the URR, which clears the bit RBF. Bit RBF is also reset when entering the reception mode and is set at 10.5 ETU.

If any of the status bits FER, OVR, PE, EA, TO1 or TO3 are set, then $\overline{INT0}$ is LOW. The bit having caused the interrupt is reset $2 \times f_{int}$ cycles after the rising edge of $\overline{RD}$ during a read operation of the USR. If TBE/RBF is set and if the mask bit DISTBE/RBF within UCR2 is not set, then $\overline{INT0}$ is also LOW. TBE/RBF is reset 2 clock cycles after data has been written into the UTR, or 2 clock cycles after data has been read from the URR, or when changing from transmission mode to reception mode if the FIFO had not been left full when going to transmission mode. If the Last Character to Transmit (LCT) is used for transmitting the last character, then TBE will not be set at the end of the transmission.

8.1.5 CARDS REGISTERS

When working with a card, the following registers may be used for programming some specific parameters:

8.1.5.1 Programmable divider register

The Programmable Divider Register (PDR) is used for counting the cards clock cycles which form the ETU. It is an autoreload 8-bit counter decounting from the programmed value down to 0.

Table 17 Programmable divider register (address 02H; read and write); note 1

7	6	5	4	3	2	1	0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Note

1. All bits are cleared after reset.

8.1.5.2 UART configuration register 2

Table 18 UART configuration register 2 (address 03H; read and write); note 1

27	26	25	24	23	22	21	20
ENINT1	DISTBE/ RBF	–	–	SAN	$\overline{AUTOCONV}$	CKU	PSC

Note

1. All bits are cleared after reset.

Table 19 Description of the UCR2 bits

BIT	SYMBOL	DESCRIPTION
27	ENINT1	Enable Interrupt 1: If bit ENINT1 = 1, then a HIGH-to-LOW transition on $\overline{INT1}$ will wake-up the microcontroller from power-down mode. When not in power-down mode, bit ENINT1 has no effect.
26	DISTBE/ RBF	Disable TBE/RBF interrupts: If bit DISTBE/RBF = 1, then reception or transmission of a character will not generate an interrupt. This feature is useful for increasing communication speed with the card; in this case, the copy of TBE/RBF bit within the MSR must be polled and not the original, in order not to loose priority interrupts which can occur in the USR.
25	–	not used
24	–	not used
23	SAN	Synchronous/$\overline{\text{Asynchronous}}$: Bit SAN is set by software if a synchronous card is expected. Then, the UART is bypassed and only bit 0 in the URR and UTR is connected to the I/O. In this case, the clock is controlled by bit SC in the CCR.
22	$\overline{\text{AUTOCONV}}$	Auto convention: If bit $\overline{\text{AUTOCONV}}$ = 1, then the convention is set by software with bit CONV in the UART Configuration Register. If it is reset, then the configuration is automatically detected on the first received character while the bit SS (Start Session) is set.
21	CKU	Clock UART: Bit CKU is used to clock the UART at twice the clock frequency of the card. An ETU will last 31 × PDR clock pulses if CKU = 0 and half if CKU = 1. It should be noted that when CKU = 1 it has no effect if $f_{CLK} = f_{XTAL1}$. This means, for example, that a baud rate of 76800 is not possible when the card is clocked with the frequency on XTAL1.
20	PSC	Prescaler: If bit PSC = 1, then the prescaler value is 32. If PSC = 0, then the prescaler value is 31. One ETU will last a number of cards clock cycles equal to PSC × PDR. All baud rates specified in *"ISO7816"* norm are achievable with this configuration.

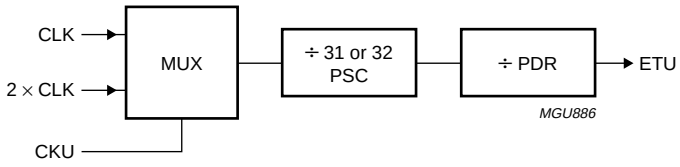


Fig.6 ETU generation.

8.1.5.3 Baud rate selection using F and D; card clock frequency f_{CLK} = 3.58 MHz for PSC = 31 and 4.92 MHz for PSC = 32 (31;12 means prescaler set to 31 and PDR set to 12)

D	F											
	0	1	2	3	4	5	6	9	10	11	12	13
1	31;12 9600	31;12 9600	31;18 6400	31;24 4800	31;36 3200	31;48 2400	31;60 1920	32;16 9600	32;24 6400	32;32 4800	32;48 3200	32;64 2400
2	31;6 19200	31;6 19200	31;9 12800	31;12 9600	31;18 6400	31;24 4800	31;30 3840	32;8 19200	32;12 12800	32;16 9600	32;24 6400	32;32 4800
3	31;3 38400	31;3 38400		31;6 19200	31;9 12800	31;12 9600	31;15 7680	32;4 38400	32;6 25600	32;8 19200	32;12 12800	32;16 9600
4				31;3 38400		31;6 19200		32;2 76800	32;3 51300	32;4 38400	32;6 25600	32;8 19200
5						31;3 38400		32;1 153600		32;2 76800	32;3 51300	32;4 38400
6										32;1 153600		32;2 76800
8	31;1 115200	31;1 115200		31;2 57600	31;3 38400	31;4 28800	31;5 23040		32;2 76800		32;4 38400	
9							31;3 38400					

8.1.5.4 Guard time register

The Guard Time Register (GTR) is used for storing the number of guard ETUs given by the card during ATR. In transmission mode, the UART will wait this number of ETU + 0.5 before transmitting the character stored in UTR. In T = 1 protocol, GTR = FFH means operation at 11.5 ETU. In T = 0 protocol and GTR = FFH means operation at 12.5 ETU.

Table 20 Guard time register (address 05H; read and write); note 1

7	6	5	4	3	2	1	0
GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0

Note

1. All bits are cleared after reset.

8.1.5.5 UART configuration register 1

The UART Configuration Register 1 (UCR1) is used for setting the parameters of the ISO UART.

Table 21 UART configuration register 1 (address 06H; read and write); note 1

7	6	5	4	3	2	1	0
–	FIP	FC	PROT	T/R	LCT	SS	CONV

Note

1. All bits are cleared after reset.

Table 22 Description of the UCR1 bits

BIT	SYMBOL	DESCRIPTION
7	–	not used
6	FIP	Force Inverse Parity: If FIP = 1, then the UART will NAK a correct received character and will transmit characters with wrong parity bit.
5	FC	Bit FC is a test bit and must be left at logic 0.
4	PROT	Protocol: Bit PROT = 1 if the protocol type is asynchronous T = 1. If PROT = 0, the protocol is T = 0.
3	T/R	Transmit/Receive: Bit T/R is set by software for transmission mode. A change from 0 to 1 will set bit TBE in the USR. T/R is automatically reset by hardware if LCT has been used before transmitting the last character.
2	LCT	Last Character to Transmit: Bit LCT is set by software before writing the last character to transmit into the UTR. It allows automatic change to reception mode when reset by hardware at the end of a successful transmission (11 + $^{28}/_{31}$ or $^{28}/_{32}$ ETU in T = 0 and 10 + $^{28}/_{31}$ or $^{28}/_{32}$ ETU in T = 1). When LCT is being reset, the bit T/R is also reset and the UART is then ready for receiving a character.
1	SS	Start Session: Bit SS is set by software before ATR for automatic convention detection and early answer detection. It is automatically reset by hardware at 10.5 ETU after reception of the initial character.
0	CONV	Convention: Bit CONV = 1 if the convention is direct. CONV is either automatically written to by hardware, according to the convention detected during ATR, or by software if bit $\overline{\text{AUTOCONV}}$ is set.

8.1.5.6 Clock configuration register

The Clock Configuration Register (CCR) defines the clock to the card and the clock to the ISO UART. If bit CKU in the Prescaler Register (UCR2) of the card is set, then the ISO UART is clocked at twice the frequency to the card, this allows higher baud rates to be reached than foreseen in the ISO7816 norm.

Table 23 Clock configuration register (address 01H; read and write); note 1

7	6	5	4	3	2	1	0
–	–	SHL	CST	SC	AC2	AC1	AC0

Note

1. All bits are cleared after reset.

Table 24 Description of the CCR bits

BIT	SYMBOL	DESCRIPTION
7	–	not used
6	–	not used
5	SHL	Stop HIGH or LOW: If bit CST = 1, then the clock is stopped at LOW level if SHL = 0 and at HIGH level if SHL = 1. In these modes, the bias current in the card drivers is reduced; the current drawn by the card (I_{CC}) should be less than 10 mA at all V_{CC} voltages.
4	CST	Clock stop: In case of asynchronous cards, bit CST defines whether the clock to the card is stopped or not. If bit CST is reset, then the clock is determined by bits AC0, AC1 and AC2; see Table 25. All frequency changes are synchronous, thus ensuring that no spike or unwanted pulse widths occurs during changes.
3	SC	Synchronous Clock: In the event of synchronous cards, the clock contact is a copy of the value written in SC. In reception mode, the data from the card is available in bit UR0 after a read operation of the URR register. In transmission mode, bit UT0 is written on the I/O line of the card when UTR register has been written.
2 to 0	AC2 to AC0	When switching from $1/n f_{xtal}$ to $1/2 f_{int}$ or vice versa, only bit AC2 must be changed; AC1 and AC0 must remain the same. When switching from $1/n f_{xtal}$ or $1/2 f_{int}$ to CLK STOP or vice versa, only bits CST and SHL must be changed. When switching from $1/n f_{xtal}$ to $1/2 f_{int}$ or vice versa, a maximum delay of 200 µs can occur between the command and the effective frequency change on pin CLK. The fastest switch is from $1/2 f_{xtal}$ to $1/2 f_{int}$ or vice versa, the best duty cycle is from $1/8 f_{xtal}$ to $1/2 f_{int}$ or vice versa. The status bit CLKSW within the MSR gives the effective switch moment.

Table 25 CLK value for an asynchronous card

AC2	AC1	AC0	CLK(1)
0	0	0	f_{xtal}
0	0	1	$1/2 f_{xtal}$
0	1	0	$1/4 f_{xtal}$
0	1	1	$1/8 f_{xtal}$
1	0	0	$1/2 f_{int}$
1	0	1	$1/2 f_{int}$
1	1	0	$1/2 f_{int}$
1	1	1	$1/2 f_{int}$

Note

1. If $f_{CLK} = f_{XTAL}$, the duty cycle must be ensured by the incoming clock signal on XTAL1.

8.1.5.7 Power control register

The Power Control Register (PCR) performs two tasks:

1. Starts or stops card sessions
2. Reads from or writes to auxiliary card contacts C4 and C8.

Table 26 Power control register (address 07H; read and write); note 1

7	6	5	4	3	2	1	0
–	–	C8	C4	1.8V	RSTIN	3/5V	START

Note

1. All bits are cleared after reset.

Table 27 Description of the PCR bits

BIT	SYMBOL	DESCRIPTION
7	–	not used
6	–	not used
5	C8	Contact 8: When writing to the PCR bit C8 will output the value of bit C8. When reading from the PCR, bit C8 will store the value on pin C8.
4	C4	Contact 4: When writing to the PCR bit C4 will output the value written of bit C4. When reading from the PCR bit C4 will store the value on pin C4.
3	1.8V	1.8 V cards: if bit 1.8V is set, then V_{CC} = 1.8 V.
2	RSTIN	Reset bit: When the card is activated, pin RST is the copy of the value written in RSTIN.
1	3/5V	3 or 5 V cards: If bit 3/5V is set to logic 1, then V_{CC} is 3 V; If bit 3/5V is set to logic 0, then V_{CC} is 5 V.
0	START	Start: If the microcontroller sets bit START to logic 1, then the selected card is activated; see Section 8.3.3. If the microcontroller resets START to logic 0, then the card is deactivated; see Section 8.3.4. START is automatically reset in the event of emergency deactivation. For deactivating the card, only bit START should be reset.

–

8.1.6 REGISTERS SUMMARY

NAME	ADDR	R/W	7	6	5	4	3	2	1	0	VALUE AT RESET	VALUE WHEN RIU = 0
CSR	00H	R/W	–	–	–	–	$\overline{\text{RIU}}$	–	–	–	XXXX0XXX	XXXX0XXX
CCR	01H	R/W	–	–	SHL	CST	SC	AC2	AC1	AC0	XX000000	XX000000
PDR	02H	R/W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	00000000	00000000
UCR2	03H	R/W	ENINT1	DISTBE/ $\overline{\text{RBF}}$	–	–	SAN	$\overline{\text{AUTOCONV}}$	CKU	PSC	00XX0000	00XX0000
GTR	05H	R/W	GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0	00000000	00000000
UCR1	06H	R/W	–	FIP	FC	PROT	T/R	LCT	SS	CONV	X0000000	X0000000
PCR	07H	R/W	–	–	C8	C4	1.8 V	RSTIN	3/5 V	START	XX110000	XX110000
TOC	08H	R/W	TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0	00000000	00000000
TOR1	09H	W	TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0	00000000	00000000
TOR2	0AH	W	TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8	00000000	00000000
TOR3	0BH	W	TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16	00000000	00000000
MSR	0CH	R	CLKSW	FE	BGT	–	–	PR	–	TBE/RBF	010XXXX0	010XXXX0
FCR	0CH	W	–	PEC2	PEC1	PEC0	–	FL2	FL1	FL0	X000X000	X000X000
UTR	0DH	W	UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0	00000000	00000000
URR	0DH	R	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0	00000000	00000000
USR	0EH	R	TO3	–	TO1	EA	PE	OVR	FER	TBE/RBF	0X000000	00000000
HSR	0FH	R	–	–	PRTL	SUPL	–	PRL	–	PTL	XX01X0X0	XX01X0X0

8.2 SUPPLY

The supply to the chip is delivered by the USB-bus (pins V_{DDU} and UGND).

8.2.1 POWER SWITCH CONTROL

A power switch control is used in order to limit the inrush current when plugging the reader into the bus. The main decoupling capacitor is connected to the output of this power switch control (pin V_{DD}).

8.2.2 3.3 V REGULATOR

The output voltage of the 3.3 V linear regulator is used for:

- Powering-up the microcontroller and the ISO7816 UART
- It is the reference voltage for the signalling pull-up resistor connected to pin D+.

If this voltage is used within the application, the current should not exceed 10 mA.

For stability reasons, a 1 μF low ESR decoupling capacitor is needed between the output of the regulator (V_{DDD}) and the specific regulator ground (DGND).

For programming the EPROM of the TDA8030; TDA8031, by applying a logic 1 to pin CPROG it will disable the regulator, so that the microcontroller will be powered-up at 5 V.

8.2.3 DC-TO-DC CONVERTER

In case of a 5 V card, the card buffers are supplied by an inductive DC-to-DC converter.

In case of a 3 or 1.8 V card, the DC-to-DC converter is transparent and the card buffers are then supplied directly by V_{DD}.

The external components for the DC-to-DC converter should be an inductance of 6.8 μH, a low ESR capacitor of 1 μF and a Schottky diode (type BAT54).

The power efficiency is approximately 85% up to I_{CC} = 55 mA. The current is limited at 100 mA during the start-up phase to avoid spurious supply drop-outs.

The DC-to-DC converter is transparent for a 3 V card.

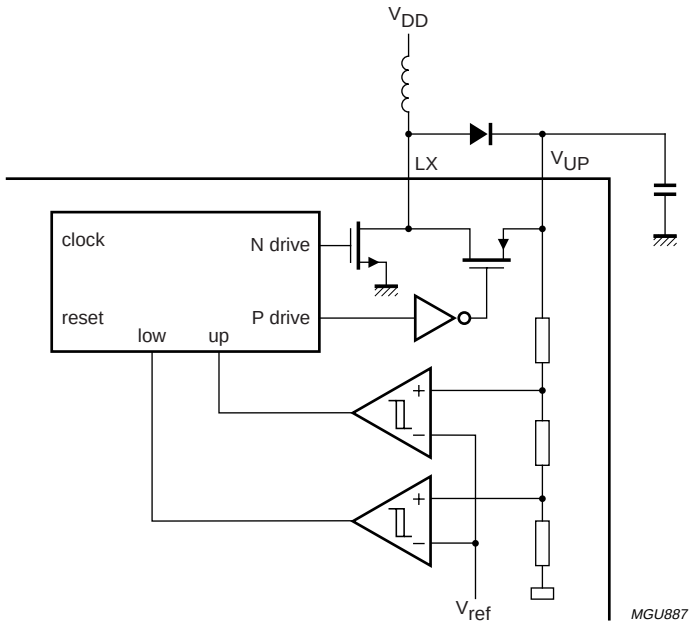


Fig.7 DC-to-DC converter.

8.2.4 SUPPLY SUPERVISOR

The switched supply voltage (V_{DD}) is surveyed by a voltage supervisor, to ensure proper Power-on reset when the reader is plugged into the USB-bus, to maintain all cards contacts inactive during power-on and also to enforce an emergency deactivation sequence in case of V_{DD} drop-out or when the reader is unplugged from the USB-bus.

The voltage supervisor generates an alarm pulse, whose length is defined by an external capacitor tied to the CDELAY pin, when V_{DD} is too low to ensure proper operation (1 ms per 2 nF typical).

This pulse is used as a Power-on reset pulse and also to either block any spurious spikes on card contacts during microcontrollers reset, or to force an automatic deactivation of the contacts in the event of supply drop-out; see Sections 8.3.3 and 8.3.4.

After power-on, or after a voltage drop, bit SUPL is set within the Hardware Status Register (HSR) and remains set until HSR is readout outside the alarm pulse. As long as the Power-on reset is active, $\overline{INT0}$ is LOW.

The same events occurs when the RESET pin has been set active; the RESET pin should be set HIGH for a minimum of 100 µs for a proper reset.

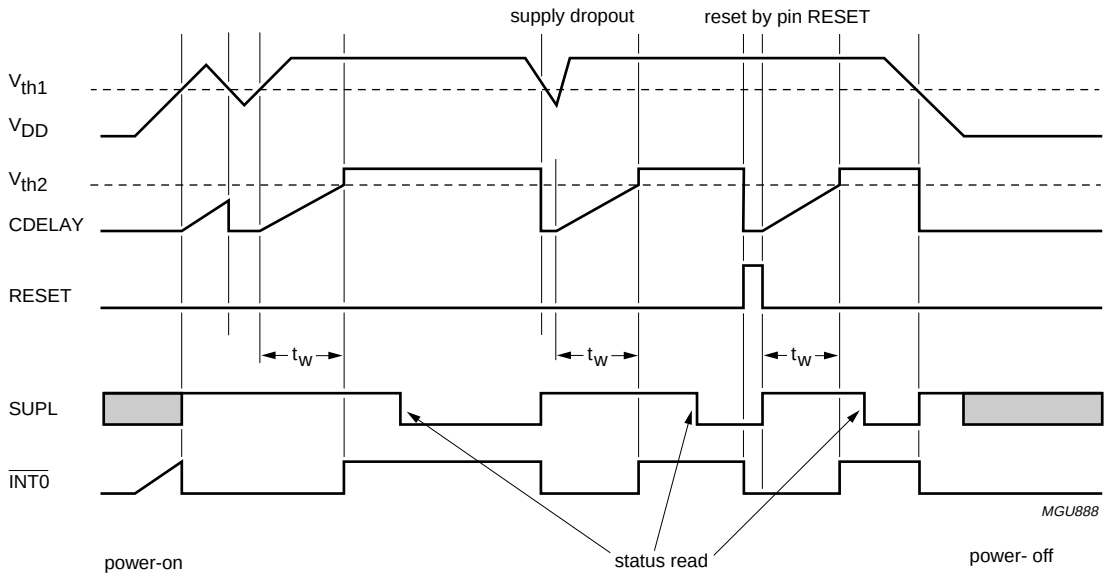


Fig.8 Voltage supervisor.

8.3 ISO7816 SECURITY

8.3.1 INTRODUCTION

The correct sequence during activation and deactivation of the cards is ensured through a specific sequencer, clocked by a division ratio of the internal oscillator.

Activation (START bit HIGH in the Power Control Register) is only possible if the card is present (PRES active HIGH) and if the supply voltage is correct (supervisor not active).

The presence of the card is signalled to the microcontroller by the Hardware Status Register (HSR).

Bit PRL in the HSR is set if the card is present. Bit PRL in the HSR is set if bit PRL has toggled.

During a session, the sequencer performs an automatic emergency deactivation on the card in the event of card take off, a short-circuit, a supply drop-out or overheating. When the HSR register is updated and the $\overline{INT0}$ line goes LOW, the microcontroller will also be updated.

8.3.2 PROTECTIONS AND LIMITATIONS

The TDA8030; TDA8031 features the following protections and limitations:

1. I_{CC} limited to 100 mA, deactivated when this limit is reached
2. Current to and from RST is limited to 20 mA, deactivated when this limit is reached
3. Deactivation when the temperature of the die exceeds 150 °C
4. Current to and from the I/O is limited to 10 mA
5. Current to and from pin CLK is limited to 70 mA (not in current reduction modes, when clock is stopped)
6. ESD protection on all cards contacts + PRES at 6 kV (min.), thus no need of extra components for protection against ESD flash caused by a charged card being introduced in the slot
7. Short-circuit between any cards contacts can last any duration without any damage.

8.3.3 ACTIVATION SEQUENCE

When the card is inactive, V_{CC}, CLK, RST, I/O, C4 and C8 are LOW, with low-impedance with referenced to CGND. The DC-to-DC converter is stopped.

When everything is in normal conditions (no error flag set), the microcontroller will initiate an activation sequence of the card.

After leaving the UART reset mode and then configuring the necessary parameters for the UART, the START bit in the PCR (t_0) will be activated. The following sequence then occurs:

1. The DC-to-DC converter is started (t_1)
2. V_{CC} starts rising from 0 to 5 V or 3 or 1.8 V with a controlled rise time of 0.17 V/µs typically (t_2)
3. I/O, C4 and C8 rise to V_{CC} (t_3); integrated 10 kΩ pull-up resistors connected to V_{CC}
4. Clock pulses are sent to the card and RST is enabled (t_4).

After a number of clock pulses that can be counted with the Time-Out Counter, the bit RSTIN may be set by software and RST will rise to V_{CC}.

The sequencer is clocked by $\frac{1}{64}f_{int}$ which leads to a time interval of t = 25 µs typical.

Thus t_1 = 0 to $\frac{3}{64}t$, $t_2 = t_1 + \frac{5}{2}t$, $t_3 = t_1 + \frac{9}{2}t$ and $t_4 = t_1 + 5t$.

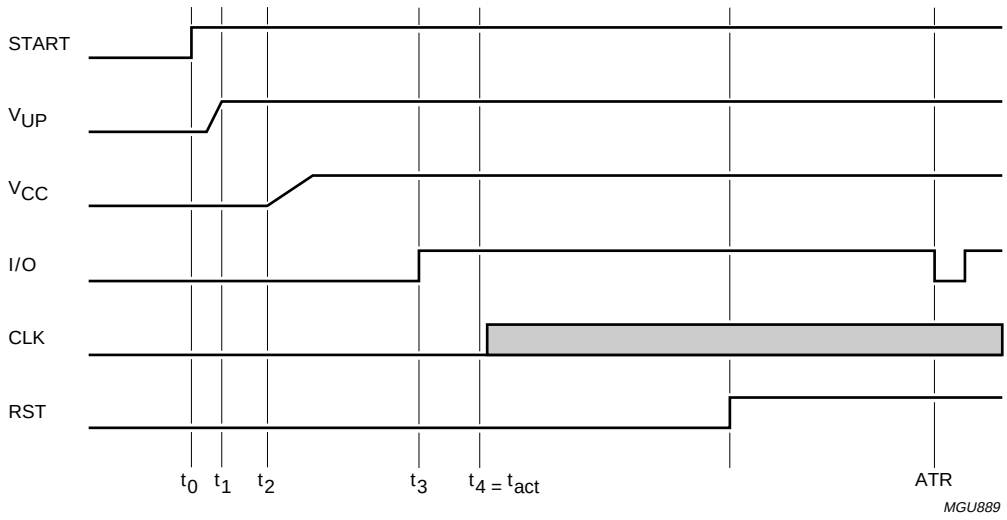


Fig.9 Activation sequence.

8.3.4 Deactivation sequence

When the session is completed, the microcontroller resets START (t_{10}). The circuit then executes an automatic deactivation sequence as follows:

1. Card reset (RST falls LOW; t_{11})
2. Clock (CLK) is stopped LOW (t_{12})
3. I/O, C4 and C8 fall to 0 V (t_{13})
4. V_{CC} falls to 0 V with typical 0.17 V/µs slew rate (t_{14})
5. The DC-to-DC converter is stopped and CLK, RST, V_{CC}, I/O, C4 and C8 become low-impedance to CGND (t_{15}).

Thus:

$t_{11} = t_{10} + 1/64t$

$t_{12} = t_{11} + 1/2t$

$t_{13} = t_{11} + t$

$t_{14} = t_{11} + 3/2t$

$t_{15} = t_{11} + 7/2t$

t_{de} = time that V_{CC} needs to decrease to less than 0.3 V.

Automatic emergency deactivation is performed in the following cases:

1. Withdrawal of the card (PRES LOW)
2. Overcurrent detection on V_{CC} (bit PRTL set)
3. Overcurrent detection on RST (bit PRTL set)
4. Overheating (bit PTL set)
5. Supply too low (bit SUPL set)
6. RESET pin active HIGH.

In all of these cases, the deactivation sequence as described above occurs.

If the reason for the deactivation is a card take-off, an overcurrent or overheating, then $\overline{INT0}$ will be LOW and the corresponding bit in the Hardware Status Register will be set. The START bit is automatically reset.

If the reason is a supply drop-out, then the deactivation sequence occurs and a complete reset of the chip is performed. When the supply recovers, then the SUPL bit will be set in the HSR.

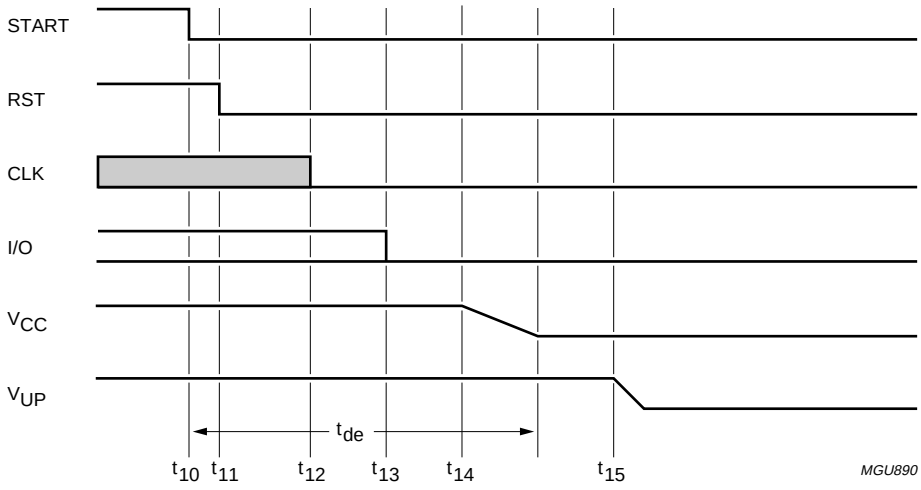


Fig.10 Deactivation sequence.

8.4 MICROCONTROLLER

The embedded microcontroller is an 80C51RB+ with an internal 16 kbyte EPROM (80C51FB with 16 kbyte ROM for the TDA8031), 256 RAM and 512 AUXRAM. It has the same instruction set as the 80C51.

The embedded microcontroller is clocked by the frequency present on pin XTAL1.

The embedded microcontroller may be reset by an active HIGH signal on pin RESET, but it is also reset by the Power-on reset signal generated by the voltage supervisor.

The external interrupt $\overline{INT0}$ is used by the ISO UART, by the analog drivers and by the ETU counters. It must be left open-circuit in the application.

The external interrupt $\overline{INT1}$ is used by the USB interface. It must be left open-circuit in the application.

A general description, together with the added features, is described below.

The added features to the 80C51 microcontroller are similar to the 8XC51FB/RB+ microcontrollers, except for the wake-up from power-down mode, which is enabled by a falling edge on pin $\overline{INT0}$ (card reader event) or on pin $\overline{INT1}$ due to the addition of an extra delay counter and enable configuration bits within the UCR2 register; see Section 8.4.1. For further information please refer to the published specification of the 8xC51RB + /FB in *"Data Handbook IC20; 80C51-Based 8-bit Microcontrollers"*.

The 80C51 microcontroller has four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, 4-level priority nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra memory capability up to 64 kbytes, it can be expanded by using standard TTL compatible memories and logic.

1. 80C51 Central Processing Unit (CPU)
2. Full static operation
3. Security bits: ROM 2 bits
4. Encryption array of 64 bits
5. 4-level priority structure
6. 6 interrupt sources
7. Full duplex enhanced UART with framing error detection and automatic address recognition
8. Power control modes (the clock can be stopped and resumed in IDLE mode and power-down mode)
9. Wake-up from power-down by a falling edge on pins $\overline{INT0}$ and $\overline{INT1}$; with an embedded delay counter
10. Programmable clock output
11. Second DPTR register
12. Asynchronous port reset
13. Low EMI (inhibit ALE).

Table 28 gives a list of main features to get a better understanding of the differences between a standard 80C51, an 8XC51RB+ and the embedded microcontroller in the TDA8030; TDA8031.

Table 28 Principal blocks in the 80C51, 8XC51RB+ and the TDA8030; TDA8031

FEATURE	80C51	8XC51RB+	TDA8030; TDA8031
ROM/EPROM	4 kbytes	16 kbytes	16 kbytes
RAM	128 bytes	256 bytes	256 bytes
ERAM (MOVX)	no	256 bytes	512 bytes
PCA	no	yes	no
WDT	no	yes	no
T0	yes	yes	yes
T1	yes	yes	yes
T2	no	yes	yes
		lowest interrupt priority vector at 002BH	
4 level priority interrupt	no	yes	yes
enhanced UART	no	yes	yes
delay counter	no	no	yes

8.4.1 LOW POWER MODES

Stop Clock Mode: The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers (SFRs) retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. The power-down mode is suggested for the lowest power consumption.

IDLE Mode: In the Idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the Idle mode is the last instruction executed in the normal operating mode before the Idle mode is activated. The CPU contents, the on-chip RAM and all of the special function registers remain intact during this mode. The Idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a Power-on reset.

Power-down Mode: To save even more power, a power-down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked the power-down is the last instruction executed.

Either a hardware reset or external interrupt can be used to exit from the power-down mode. Applying a reset redefines all of the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

The bits in the Interface Engine (IE) must be enabled with $\overline{INT0}$ and $\overline{INT1}$. Within the $\overline{INT0}$ interrupt service routine, the microcontroller has to read out the Hardware Status Register (HSR at 0FH) and/or the UART Status register (USR at 0EH) by means of MOVX instructions in order to establish the exact interrupt reason and to reset the interrupt source.

For enabling a wake-up by $\overline{INT1}$, the bit ENINT1 within UCR2 must be set.

An integrated delay counter maintains $\overline{INT0}$ and $\overline{INT1}$ LOW long enough to allow the oscillator to restart properly. A falling edge on pins $\overline{INT0}$ and $\overline{INT1}$ is enough to awaken the whole circuit.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into power-down.

8.5 USB INTERFACE

8.5.1 END-POINTS

The TDA8030; TDA8031 has 4 logic end-points which are listed in Table 29.

Each physical end-point, except for the control ones, can be enabled or disabled. All enabled end-points generate interrupts to the microcontroller via $\overline{INT1}$ when the end-point needs to be serviced.

The implementation of the function makes use of an SRAM for buffering the data.

Logic end-points can be accessed by the microcontroller interface.

Table 29 Mapping of logic to physical end-point numbers for used end-points

END-POINT NAME	LOGIC END-POINT	BUFFER SIZE	PHYSICAL END-POINT	
			OUT	IN
Control end-point	0	16	0	1
Generic end-point (may be used as bulk	1	32	2	3
Generic end-point (may be used as interrupt)	2	8	–	4
Generic end-point	3	8	–	5

8.5.2 PHASE-LOCKED LOOP

A 12 to 48 MHz clock multiplier PLL is integrated on-chip. No external components are needed for the operation of the PLL.

8.5.3 BIT CLOCK RECOVERY

The bit clock recovery circuit recovers the clock from the incoming USB data stream using 4× oversampling principle. It is able to track jitter and frequency drift as specified by the USB specification.

8.5.4 INTERFACE SIGNALS WITH THE MICROCONTROLLER

Table 30 The following I/O ports of the 83C51 are used for controlling the USB bus:

PORT	FUNCTION	DESCRIPTION
P10	USB_INT_MASK	should be set to logic 1 before entering power-down mode during suspend and reset to logic 0 when leaving power-down mode
P11	USB_SOFTCONNECT_INT	when set to logic 1, the internal 1.5 kΩ resistor is connected to pin D+
P12	USB_MC_READY	the device is ready to accept a new transaction
P13	USB_CLK_EN_N	when LOW, this signal indicates that the bus is no longer suspended
P14	USB_RESET_N	a LOW-level will reset the USB interface
P15	USB_SOFTCONNECT_EXT	when set to logic 1, V_{DDD} is applied on the optional external 1.5 kΩ resistor which has been placed between pins D+ and DELATT
P33	USB_INT_N	interrupt to the microcontroller
P34	USB_SUSPEND	the device is in suspended state (TDA8030 only)
P35	USB_WAKEUP_N	remote wake-up (TDA8030 only)
P25	USB_MP_C	if set to logic 1, the data to the bus is a command; if set to logic 0 it is data
P26	USB_MP_SEL	if set to logic 1, the USB interface is selected

8.5.5 BLOCK DIAGRAM

The digital interface consists of 3 major blocks:

- The Philips Serial Interface Engine (SIE) handles the USB protocol (i.e. synchronization pattern, recognition, parallel/serial conversion, bit stuffing/de-stuffing, CRC checking/generating, PID verification/generation, address recognition and handshake evaluation/generation)
- A Memory Management Unit (MMU), controlling the buffering of data to and from the bus
- An interface to the embedded 83C51 microcontroller.

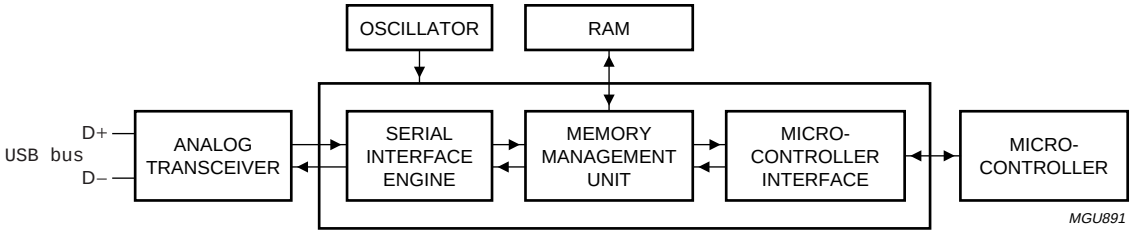


Fig.11 USB block diagram.

8.5.6 USB REGISTERS

A first MOVX@DPTR instruction enables the module to be selected (via DPH) and send the command. A second one communicates the data (read or write).

8.5.7 INSTRUCTION SET

8.5.7.1 Overview

Table 31 summarizes all commands that can be used by the embedded microcontroller.

Table 31 Instruction set

COMMAND NAME	RECIPIENT	CODING	FUNCTION	DATA PHASE
Device commands; see Table 32				
Set address	device	0XD0H	set address	write 1 byte
Set end-points enable	device	0XD8H	set EP enable	write 1 byte
Set mode	device	0XF3H	set mode	write 1 byte
Read interrupt register	device	0XF4H		read 1 byte
Read current frame number	device	0XF5H		read 1 or 2 bytes
Read chip ID	device	0XFDH		read 2 bytes
Get device status	device	0XFEH		read 1 byte
Set device status	device	0XFEH		write 1 byte
Debug command: get error code	device	0XFFH		read 1 byte
End-point commands; see Table 41				
Select end-point	control output	0X00H	select EP0 output	read 1 byte (optional)
	control input	0X01H	select EP0 input	read 1 byte (optional)
	end-point 1 output	0X02H		read 1 byte (optional)
	end-point 1 input	0X03H		read 1 byte (optional)
	end-point 2 input	0X04H		read 1 byte (optional)
	end-point 3 input	0X05H		read 1 byte (optional)
Select end-point/clear interrupt	control output	0X40H		read 1 byte
	control input	0X41H		read 1 byte
	end-point 1 output	0X42H		read 1 byte
	end-point 1 input	0X43H		read 1 byte
	end-point 2 input	0X44H		read 1 byte
	end-point 3 input	0X45H		read 1 byte
Set end-point status	control output	0X40H		write 1 byte
	control input	0X41H		write 1 byte
	end-point 1 output	0X42H		write 1 byte
	end-point 1 input	0X43H		write 1 byte
	end-point 2 input	0X44H		write 1 byte
	end-point 3 input	0X45H		write 1 byte
Read buffer	selected end-point	0XF0H		read n + 2 bytes
Write buffer	selected end-point	0XF0H		write n + 2 bytes
Clear buffer	selected end-point	0XF2H		read 1 byte (optional)
Validate buffer	selected end-point	0XFAH		none

Table 32 Device commands

COMMAND	DESCRIPTION
Set address	The set address command is used to set the USB assigned address and to enable the function. In the event that the status phase of the set address transaction is not successful, the device address will not be updated. The power-on value is given in Table 33.
Set end-points enable	A value of 1 written to the register indicates that the non-control end-points are enabled. The power-on value is given in Table 34.
Set Mode	The default value is logic 0; if logic 1 is written in this register, then NAKing is reported and will generate an interrupt. When set to logic 0, only successful transactions are reported.
Read interrupt register	This command indicates the origin of an interrupt. The end-point interrupt bits are cleared by the Select end-point/Clear Interrupt command. The power-on value is given in Table 35.
Read Current Frame Number	The Read Current Frame Number returns the frame number of the last received Start Of Frame (SOF). The frame number is eleven bits wide. The frame number is returned LSB first, so, if the user is only interested in the lower 8 bits of the frame number, only the first byte needs to be read; see Table 36. The frame number returned by this commend can be invalid in the event of one of the following conditions: • If no SOF was received by the device at the beginning of a frame, the frame number returned is that of the last successfully received SOF • If the SOF frame number contained a CRC error, the frame number received will be the corrupted frame number as received by the device.
Read chip ID	The chip Identification is 16 bits wide. The command divides the ID into bytes and returns the least significant byte first: For the TDA8030; TDA8031, the ID is fixed at 2B00H.
Get Device Status	The Get Device Status command returns the Device Status Register; refer to the Set Device Status command
Set Device Status	The Set Device Status command sets bits in the Device Status Register. In Table 37, the Type column indicates if the bit can be written and if the bit is cleared after reading the register. The Interrupt column indicates if the bit generates an interrupt when it is set.
Debug command: Get Error Code	The Get Error Code command returns the error code of the last generated error; this command is for debugging purpose. The 4 least significant bits form the error code. Bit 4 (Error Occurred) can be cleared by each new transfer. The power-on value is given in Table 39. This command is only useful during debugging. Table 40 gives an overview of the Error Codes.

Table 33 Power-on value for Set address

FUNCTION	7	6	5	4	3	2	1	0
Device address[1]	–	0	0	0	0	0	0	0
Enable[2]	0	–	–	–	–	–	–	–

Notes

1. The value written becomes the address.
2. A logic 1 enables the function.

After a bus reset, the address is reset to 000 0000. The enable bit is set. The device will respond on packets for function address 000 0000, end-point 0 (default end-point).

Table 34 Power-on value for Set end-points enable

FUNCTION	7	6	5	4	3	2	1	0
Enable all end-points	–	–	–	–	–	–	–	0
Reserved	–	–	–	–	–	–	–	–

Table 35 Power-on value for Read interrupt register

FUNCTION	7	6	5	4	3	2	1	0
Physical EP0 (control output end-point)	–	–	–	–	–	–	–	0
Physical EP1 (control input end-point)	–	–	–	–	–	–	0	–
Physical EP2 (generic output end-point)	–	–	–	–	–	0	–	–
Physical EP3 (generic input end-point)	–	–	–	–	0	–	–	–
Physical EP4 (generic input end-point)	–	–	–	0	–	–	–	–
Physical EP5 (generic input end-point)	–	–	0	–	–	–	–	–
Reserved	–	0	–	–	–	–	–	–
Device event[1]	0	–	–	–	–	–	–	–

Note

1. The Device event bit is cleared by issuing the Get Device Status command.

Table 36 Read current frame number

BYTE	7	6	5	4	3	2	1	0
Byte 0	F	F	F	F	F	F	F	F
Byte 1	0	0	0	0	0	F	F	F

Table 37 Set device status command functions

FUNCTION	TYPE	INTERRUPT	7	6	5	4	3	2	1	0
Reserved	–	–	–	–	–	–	–	–	0	0
Suspend	read/write	no	–	–	–	–	–	0	–	–
Suspend change	read only; cleared on read	yes	–	–	–	–	0	–	–	–
Bus reset	read only; cleared on read	yes	–	–	–	0	–	–	–	–
Reserved	–	–	–	–	–	–	–	–	–	–

Table 38 Set device status command function bits

FUNCTION	DESCRIPTION
Suspend	The Suspend bit represents the current Suspend state. It is logic 1 when the device has not seen any activity on its upstream port for more than 3 ms. It is reset to logic 0 on any activity. When the device is suspended, (Suspend bit = 1) and the microcontroller writes logic 0 into it, the device will generate a remote wake-up. When the device is not suspended, writing a logic 0 has no effect. Writing a logic 1 in this register has no an effect.
Suspend Change	The Suspend Change bit is set to logic 1 when the Suspend bit toggles. The Suspend bit can toggle because: • The device goes into the suspended state • The device receives resume signalling on its upstream port • The Suspend Change bit is reset after the register has been read.
Bus reset	The Bus reset bit is set when the device receives a bus reset. It is cleared when read. On a bus reset, the device will automatically go to the default state (unconfigured and responding to address 0).

Table 39 Power-on value for Get Error Code

FUNCTION	7	6	5	4	3	2	1	0
Error code	–	–	–	–	0	0	0	0
Error occurred	–	–	–	0	–	–	–	–
Reserved	–	–	–	–	–	–	–	–

Table 40 Error codes

ERROR CODE[3:0]	DESCRIPTION
0000	no error
0001	PID encoding error
0010	unknown PID
0011	unexpected packet
0100	error in token CRC
0101	error in data CRC
0110	time-out error
0111	babble
1000	error in end of packet
1001	sent NAK
1010	sent Stall
1011	buffer overrun error
1100	reserved
1101	bitstuff error
1110	error in sync
1111	wrong toggle bit in data PID; ignored data

Table 41 End-point commands

COMMAND	DESCRIPTION
Select end-point	The select end-point command initializes an internal pointer to the start of the selected buffer. Optionally, this command can be followed by a data read, which returns some additional information on the packet in the buffer. The command code of the select end-point is equal to the physical end-point number. The power-on value is given in Tables 42 and 43.
Select End-point/ Clear Interrupt	These commands are identical to Select End-point commands, but with the following differences: • They clear the associated interrupt • In the event of a control output end-point; they clear the set-up and overwritten bits • The read one byte is mandatory.
Set end-point status	The Set end-point status command sets status bits 7 to 5 and 0 of the end-point. The command code is equal to the sum of 40H and the physical end-point number. Not all bits can be set for all types of end-points. The power-on value is given in Tables 44 and 45.
Read buffer	The Read buffer command is followed by a number of data reads, which return the contents of the selected end-point data buffer. After each read, the internal buffer pointer is incremented. The buffer pointer is not reset to the beginning of the buffer by the Read buffer command. This means that reading a buffer can be interrupted by any other command (except for the Select end-point). The data buffer organization is given in Table 46.
Write buffer	The Write buffer command is followed by a number of data writes, which load the data buffer of the selected end-point. After each write, the internal buffer pointer is incremented The buffer pointer is not reset to the beginning of the buffer by the Write buffer command. This means that writing to a buffer can be interrupted by any other command (except for the Select end-point and Select end-point/Clear Interrupt). The data buffer organization is given in Table 47.
Clear buffer	When a packet sent by the host has been received successfully, an internal end-point buffer full flag is set. All subsequent packets will be refused by returning a NAK. When the microcontroller has read the data, it should free the buffer by the Clear buffer command. When the buffer is cleared, new packets will be accepted. When bit 0 of the optional data byte is set to logic 1, the previously received packet was overwritten by a set-up packet. A buffer cannot be cleared when its Packet overwritten bit is set. The power-on value is given in Table 48.
Validate buffer	When the microcontroller has written data into an input buffer, it should set the buffer full flag by the Validate buffer command. This indicates that the data in the buffer is valid and can be sent to the host when the next input token is received. A control input buffer cannot be validated when the Packet overwritten bit of its corresponding output buffer is set.

Table 42 Power-on value for Select end-point

FUNCTION	7	6	5	4	3	2	1	0
Full or empty	–	–	–	–	–	–	–	0
Stall	–	–	–	–	–	–	0	–
Set-up	–	–	–	–	–	0	–	–
Packet overwritten	–	–	–	–	0	–	–	–
Sent NAK	–	–	–	0	–	–	–	–
Reserved	–	–	–	–	–	–	–	–

Table 43 Description of the Power-on value for Select end-point bits

FUNCTION	DESCRIPTION
Full or empty	If set to logic 1, the buffer of the selected end-point is full. In the event of an output end-point, this bit is cleared by executing the Clear Buffer command, if the buffer was not overwritten. In the event of an input end-point, this bit is set by the Validate Buffer command.
Stall	If set to logic 1, the selected end-point is stalled.
Set-up	If set to logic 1, the last received packet for the selected end-point was a set-up packet. The value of this bit is updated after each successfully received packet (i.e. an ACKED package on that particular end-point).
Packet overwritten	If set to logic 1, the previously received packet was overwritten by a set-up packet. The value of this bit is cleared by the Select End-point command.
Sent NAK	If set to logic 1, the device has sent a NAK. If the host sends an output packet to a filled output buffer, the device returns a NAK. If the host sends an input token to an empty input buffer, the device returns a NAK. This bit is set when a NAK is sent and the Interrupt On Nak feature is enabled. This bit is reset after the device has sent an ACK after an output packet or when the device has seen an ACK after sending an input packet. It is only defined for the 2 physical control end-points.

Table 44 Power-on value for Set end-point status; notes 1 and 2

FUNCTION	7	6	5	4	3	2	1	0	CTRL EP	GEN IN/OUT	GEN IN
Stall	–	–	–	–	–	–	–	0	def	def	def
Disable	–	–	0	–	–	–	–	–	X	def	def
Rate feedback mode	–	0	–	–	–	–	–	–	X	def	def
Interrupt unmasked	0	–	–	–	–	–	–	–	X	X	X
Conditional stall	0	–	–	–	–	–	–	–	def	X	X

Notes

1. X = dont care.
2. def means that the bit can be set if the end-point is of the specified type.

Table 45 Description of the Power-on value for Set end-point status bits

FUNCTION	DESCRIPTION
Stall	If set to logic 1, the end-point is stalled.
Disable	If set to logic 1, the end-point is disabled. After a bus reset; each end-point is enabled, i.e. this bit is set to logic 0.
Rate feedback mode	If set to logic 0, the interrupt end-point is in toggle mode. If set to logic 1, the interrupt end-point is in rate feedback mode.
Interrupt unmasked	If set to logic 1, an event on the end-point causes an interrupt to the microcontroller.
Conditional stall	If set to logic 1, both end-points zero are stalled; unless the set-up packet bit is set. A stalled control end-point is automatically unstalled when it receives a SET-UP token, regardless of the content of the packet. If the end-point stays in the stalled state, the microcontroller should re-install it. When a stalled end-point is unstalled (either by the Set end-point status command or by receiving a Set-up token) it is also re-initialized. This flushes the buffer: in case of an output buffer, it waits for a DATA 0 PID; in case of an input buffer, it writes a DATA 0 PID. Even when unstalled, setting the stalled bit to logic 0 initializes the end-point. When an end-point is stalled by the Set end-point status command, it is also re-initialized.

Table 46 Data buffer organization (read)

BYTE	7[1]	6[2]	5	4	3	2	1	0
Byte 0	0/1	0/1	–	–	–	–	–	0
Byte 1	–	number of data bytes in buffer						
Byte 2	data byte 0							
....								
Byte n + 1	data byte n – 1							

Notes

1. Bit 7 of Byte 0 indicates whether the packet in the buffer was received successfully over the USB-bus. When this bit is set to logic 1, the packet was received successfully.
2. Bit 6 of Byte 0 indicates whether the packet in the buffer is a set-up packet.

Table 47 Data buffer organization (write)

BYTE	7	6	5	4	3	2	1	0
Byte 0	–	–	–	–	–	–	–	0
Byte 1	–	number of data bytes in buffer						
Byte 2	data byte 0							
....								
Byte n + 1	data byte n – 1							

Table 48 Power-on value for Clear buffer

FUNCTION	7	6	5	4	3	2	1	0
Packet overwritten	–	–	–	–	–	–	–	0
Reserved	–	–	–	–	–	–	–	–

8.5.8 ANALOG INTERFACE

The transceiver interfaces directly to the USB cables through termination resistors. They are able to transmit and receive serial data at full speed (12 Mbits/s).

A 1.5 kΩ pull-up resistor is integrated between pins D+ and V_{DDD} and is connected by software by the microcontroller; in case a ±5% resistor is preferred, it can be externally connected between pins DELATT and D+ (DELATT is also controlled by software and is floating when OFF, or connected to V_{DDD} when ON).

8.5.9 SUSPEND MODE

When the USB interface enters Suspend mode, the software should set the microcontroller in power-down mode in order to respect the suspend current condition. The following sequence should be executed:

1. When the device enters the Suspend mode, it generates an interrupt on pin $\overline{INT1}$
2. The software should set USB_INT_MASK to logic 1
3. Then it should wait until CLK_EN_N is HIGH before entering power-down mode.

When the device detects an activity on the bus, it resets CLK_EN_N to logic 0 and generates an interrupt on pin $\overline{INT1}$. When leaving the Suspend mode, the following sequence should be executed:

1. The software should read the DEVICE_STATUS to enable the interrupt to be cleared
2. Reset USB_INT_MASK to logic 0.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDU}	bus supply voltage		–0.5	+6.5	V
V_n	input voltage on all pins		–0.5	+6.5	V
P_{tot}	total power dissipation		–	tbf	mW
T_{stg}	IC storage temperature		–55	+150	°C
T_j	junction temperature		–	125	°C
V_{esd}	electrostatic discharge voltage	TDA8030; HBM JEDEC			
	pins I/O, V_{CC}, RST, C4, C8, CLK and PRES		–5	+5	kV
	all other pins		–1	+1	kV
		MM JEDEC	–50	+50	V
		MM JEDEC	–100	+100	V
V_{esd}	electrostatic discharge voltage				
	pins I/O, V_{CC}, RST, C4, C8, CLK and PRES	TDA8031; HBM JEDEC	–6	+6	kV
	all other pins		–1.5	+1.5	kV
I_{lu}	latch-up free current on all pins	JEDEC; maximum voltage is 1.5/–0.5 supply voltage of the block	–100	+100	mA

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	63	K/W

11 CHARACTERISTICS

V_{DDU} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDU}	supply voltage for the bus		4.2	–	5.5	V
V_{DD}	supply voltage after inrush current suppression switch		4.2	–	5.5	V
I_{DDU}	supply current for the bus	5 V card; I_{CC} = 40 mA; f_{clk} = 6 MHz	–	–	100	mA
I_{sus}	suspend current	card inactive; microcontroller in power-down mode	–	–	500	μA
$V_{th(VDD)}$	threshold voltage on V_{DD}	falling	3.6	–	3.8	V
V_{hys}	hysteresis voltage on $V_{th(VDD)}$		150	–	350	mV
$V_{th(CDELAY)}$	threshold voltage on pin CDELAY		–	1.25	–	V
V_{CDELAY}	voltage on pin CDELAY		–	–	V_{DD} + 0.3	V
$I_{o(CDELAY)}$	output current on pin CDELAY	pin ground; charge current	–	–2	–	μA
		$V_{CDELAY} = V_{DD}$; discharge current	–	9	–	mA
C_{CDELAY}	capacitor on pin CDELAY		–	22	–	nF
Crystal oscillator (XTAL1 and XTAL2)						
f_{XTAL}	crystal frequency		–	12	–	MHz
V_{IL}	LOW-level input voltage on pin XTAL1		–0.3	–	$+0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage on pin XTAL1		$0.7V_{DDD}$	–	V_{DDD} + 0.3	V
DC-to-DC converter						
f_{clk}	clock frequency		–	12	–	MHz
V_{UP}	output voltage	V_{CC} = 5 V	–	5.5	–	V
		V_{CC} = 3 or 1.8 V	–	5	–	V
P_E	power efficiency	L = 6.8 μH; C = 1 μF	–	85	–	%
V_{DDD} voltage regulator						
V_{DDD}	output voltage	PROG = 0	3	–	3.6	V
		PROG = 1 (TDA8030 only)	4.5	–	5.5	V
I_{DDD}	output current		0	–	25	mA
C_{dec}	decoupling capacitor		1000	–	–	nF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset output to the card (RST)						
V_{inact}	output voltage in inactive mode	no load	0	–	0.1	V
		I_{inact} = 1 mA	0	–	0.3	V
I_{inact}	current from RST when inactive and pin grounded		0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
		I_{OL} = 20 mA	V_{CC} – 0.4	–	V_{CC}	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	$0.9V_{CC}$	–	V_{CC}	V
		I_{OH} = –20 mA	0	–	0.4	V
t_r	rise time	C_L = 100 pF; V_{CC} = 5 or 3 V	–	–	0.1	µs
t_f	fall time	C_L = 100 pF; V_{CC} = 5 or 3 V	–	–	0.1	µs
Clock output to the card (CLK)						
V_{inact}	output voltage in inactive mode	no load	0	–	0.1	V
		I_{inact} = 1 mA	0	–	0.3	V
I_{inact}	current from CLK when inactive and pin grounded		0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
		I_{OL} = 70 mA	V_{CC} – 0.4	–	V_{CC}	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	$0.9V_{CC}$	–	V_{CC}	V
		I_{OH} = –70 mA	0	–	0.4	V
t_r	rise time	C_L = 35 pF	–	–	16	ns
t_f	fall time	C_L = 35 pF	–	–	16	ns
f_{clk}	clock frequency	1 MHz Idle configuration	1	–	1.5	MHz
		operational	0	–	12	MHz
δ	duty factor (except for XTAL)	C_L = 35 pF	45	–	55	%
SR	slew rate (rise and fall)	C_L = 30 pF	0.2	–	–	V/ns
Card supply voltage (V_{CC}) (2 ceramic multilayer capacitors with low ESR of minimum 100 nF should be used in order to meet these specifications)						
V_{inact}	output voltage inactive	no load	0	–	0.1	V
		I_{inact} = 1 mA	0	–	0.3	V
I_{inact}	current from V_{CC} when inactive and pin grounded		–	–	–1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	output voltage	active mode; I_{CC} < 55 mA; 5 V card	4.75	5	5.25	V
		active mode; I_{CC} < 55 mA; 3 V card	2.78	3	3.22	V
		active mode; current pulses of 40 nAs with I < 200 mA; t < 400 ns; f < 20 MHz; 5 V card	4.6	–	5.4	V
		active mode; current pulses of 24 nAs with I < 200 mA; t < 400 ns; f < 20 MHz; 3 V card	2.75	–	3.25	V
		active mode; I_{CC} < 35 mA; 1.8 V card	1.64	1.8	1.96	V
		active mode; current pulses of 12 nAs with I < 200 mA; t < 400 ns; f < 20 MHz; 1.8 V card	1.62	–	1.98	V
I_{CC}	output current	5 V card; from 0 to 5 V	–	–	–55	mA
		3 V card; from 0 to 3 V	–	–	–55	mA
		1.8 V card; from 0 to 1.8 V	–	–	–35	mA
		when clock is stopped; at all V_{CC} values	–	–	–10	mA
		V_{CC} shorted to ground	–	–	–120	mA
SR	slew rate	up or down (maximum capacitance = 300 nF)	0.05	0.16	0.22	V/µs
$V_{ripple(p-p)}$	ripple voltage on V_{CC} (peak-to-peak value)	20 kHz < f < 200 MHz				
		5 V card	–	–	350	mV
		3 V card	–	–	200	mV
		1.8 V card	–	–	100	mV
Data line (I/O); I/O has an integrated 14 kΩ pull-up resistor at V_{CC}						
V_{inact}	output voltage inactive	no load	0	–	0.1	V
		I_{inact} = 1 mA	–	–	0.3	V
I_{inact}	current from I/O when inactive and pin grounded		–	–	–1	mA
V_{OL}	LOW-level output voltage	the I/O is configured as an output				
		I_{OL} = 1 mA	0	–	0.3	V
		I_{OL} = 10 mA	V_{CC} – 0.4	–	V_{CC}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH-level output voltage	the I/O is configured as an output				
		$I_{OH} < -20$ µA	$0.8V_{CC}$	–	$V_{CC} + 0.25$	V
		$I_{OH} < -40$ µA; 5 and 3 V card	$0.75V_{CC}$		$V_{CC} + 0.25$	V
		$I_{OH} = -10$ mA	0	–	0.4	V
V_{IL}	LOW-level input voltage	the I/O is configured as an input	–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage	the I/O is configured as an input	1.5	–	V_{CC}	V
I_{IL}	LOW-level input current on I/O	$V_{IL} = 0$	–	–	500	µA
I_{LIH}	HIGH-level input leakage current on I/O	$V_{IH} = V_{CC}$	–	–	10	µA
$t_{i(tr)}$	input transition times	$C_L \leq 60$ pF; 5 or 3 V card	–	–	1.2	µs
$t_{o(tr)}$	output transition times	$C_L \leq 60$ pF 5 or 3 V card	–	–	0.1	µs
R_{pu}	internal pull-up resistance between I/O and V_{CC}		11	14	17	kΩ
$t_{W(pu)}$	width of active pull-up pulse	the I/O is configured as an $2/f_{XTAL1}$ output; LOW-to-HIGH transition	$2/f_{XTAL1}$	–	$3/f_{XTAL1}$	ns
I_{pu}	current from I/O when active pull-up pulse	$V_{OH} = 0.9V_{CC}$; $C_L = 60$ pF	–1	–	–	mA
Auxiliary contacts C4/C8; integrated 10 kΩ pull-up resistor to V_{CC}						
V_{inact}	output voltage inactive	no load	0	–	0.1	V
		$I_{inact} = 1$ mA	–	–	0.3	V
I_{inact}	current from I/O when inactive and pin grounded		–	–	–1	mA
V_{OL}	LOW-level output voltage	C4 and C8 configured as an output; $I_{OL} = 1$ mA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	C4 and C8 configured as an output; $I_{OH} < -40$ µA; 5 and 3 V card	$0.8V_{CC}$	–	$V_{CC} + 0.25$	V
V_{IL}	LOW-level input voltage	C4 and C8 configured as an input	–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage	C4 and C8 configured as an input	1.5	–	V_{CC}	V
I_{IL}	LOW-level input current	$V_{IL} = 0$	–	–	500	µA
I_{LIH}	HIGH-level input leakage current	$V_{IH} = V_{CC}$	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{i(tr)}$	input transition times	$C_L \leq 60$ pF	–	–	1.2	µs
$t_{o(tr)}$	output transition times	$C_L \leq 60$ pF	–	–	0.1	µs
R_{pu}	internal pull-up resistance between C4/C8 and V_{CC}		8	10	12	kΩ
$t_{W(pu)}$	width of active pull-up pulse	the I/O is configured as an output; LOW-to-HIGH transition	–	200	–	ns
I_{pu}	current from C4 and C8 when active pull-up	$V_{OH} = 0.9V_{CC}$; C_L = 60 pF	–1	–	–	mA
Timing						
t_{act}	activation sequence duration		–	–	160	µs
t_{de}	deactivation sequence duration		–	–	100	µs
Protections and limitations						
$I_{CC(sd)}$	shutdown and limitation current at V_{CC}		–	–100	–	mA
$I_{I/O(lim)}$	limitation current on I/O		–10	–	+10	mA
$I_{CLK(lim)}$	limitation current on pin CLK		–70	–	+70	mA
$I_{RST(lim)}$	limitation current on pin RST		–20	–	+20	mA
$I_{RST(sd)}$	shutdown current on pin RST		–	–20	–	mA
T_{sd}	shutdown temperature		–	150	–	°C
Card presence input; pin PRES						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
I_{IL}	input leakage current low	$V_{IN} = 0$	–	–	±20	µA
I_{IH}	input leakage current high	$V_{IN} = V_{DD}$	–	–	±20	µA
General purpose I/Os; pins P0X, P1X, P2X and P3X						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.2V_{DDD} + 0.9$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –30 µA	$V_{DDD} - 0.7$	–	–	V
I_{IL}	LOW-level input current	V_I = 0.4 V	–1	–	–50	µA
I_{TL}	HIGH-to-LOW transition current	V_I = 2 V	–	–	–650	µA
Pins ALE and $\overline{\text{PSEN}}$						
V_{OL}	LOW-level output voltage	I_{OL} = 3.2 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –3.2 mA	$V_{DDD} - 0.7$	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin $\overline{EA}/V_{PP}$						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.2V_{DDD}$ + 0.9	–	–	V
V_{prog}	programming voltage	TDA8030	12.5	12.75	13	V
Reset input; pin RESET (active HIGH)						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
DELATT output pin; optional connection for an external 1.5 kΩ resistor on pin D+						
V_{OH}	HIGH-level output voltage	when switched on; I_{OH} = 2 mA	3.0	–	3.6	V
I_L	leakage current	when switched off	–	–	10	μA
Programming input; pin PROG (active HIGH) and Test input; pin TEST (active HIGH)						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
ATX Transceiver						
DRIVER CHARACTERISTICS IN FULL-SPEED MODE; PINS D+ AND D–						
$V_{OL(stat)}$	LOW-level static output voltage	R_L = 1.5 kΩ	–	–	0.3	V
$V_{OH(stat)}$	HIGH-level static output voltage		2.8	–	3.6	V
$R_{o(drive)}$	driver output resistance	excluding outside resistors	10	–	30	Ω
t_{tr}	transition times	C_L = 50 pF	4	–	20	ns
t_{RFM}	rise and fall time matching	C_L = 50 pF	90	–	110	%
V_{cross}	output signal crossover voltage		1.3	–	2	V
$R_{int(DP)}$	integrated resistor on DP	when connected USB_SOFTCONNECT active	1.1	–	1.9	kΩ
RECEIVER CHARACTERISTICS IN FULL-SPEED MODE; PINS ATXDP AND ATXDM						
$V_{i(dif)}$	differential input sensitivity		0.2	–	–	V
$V_{dif(CM)}$	differential common mode range in which $V_{i(dif)}$ applies		0.8	–	2.5	V
$V_{th(SE)}$	single-ended receiver threshold		0.8	–	2.0	V

12 APPLICATION INFORMATION

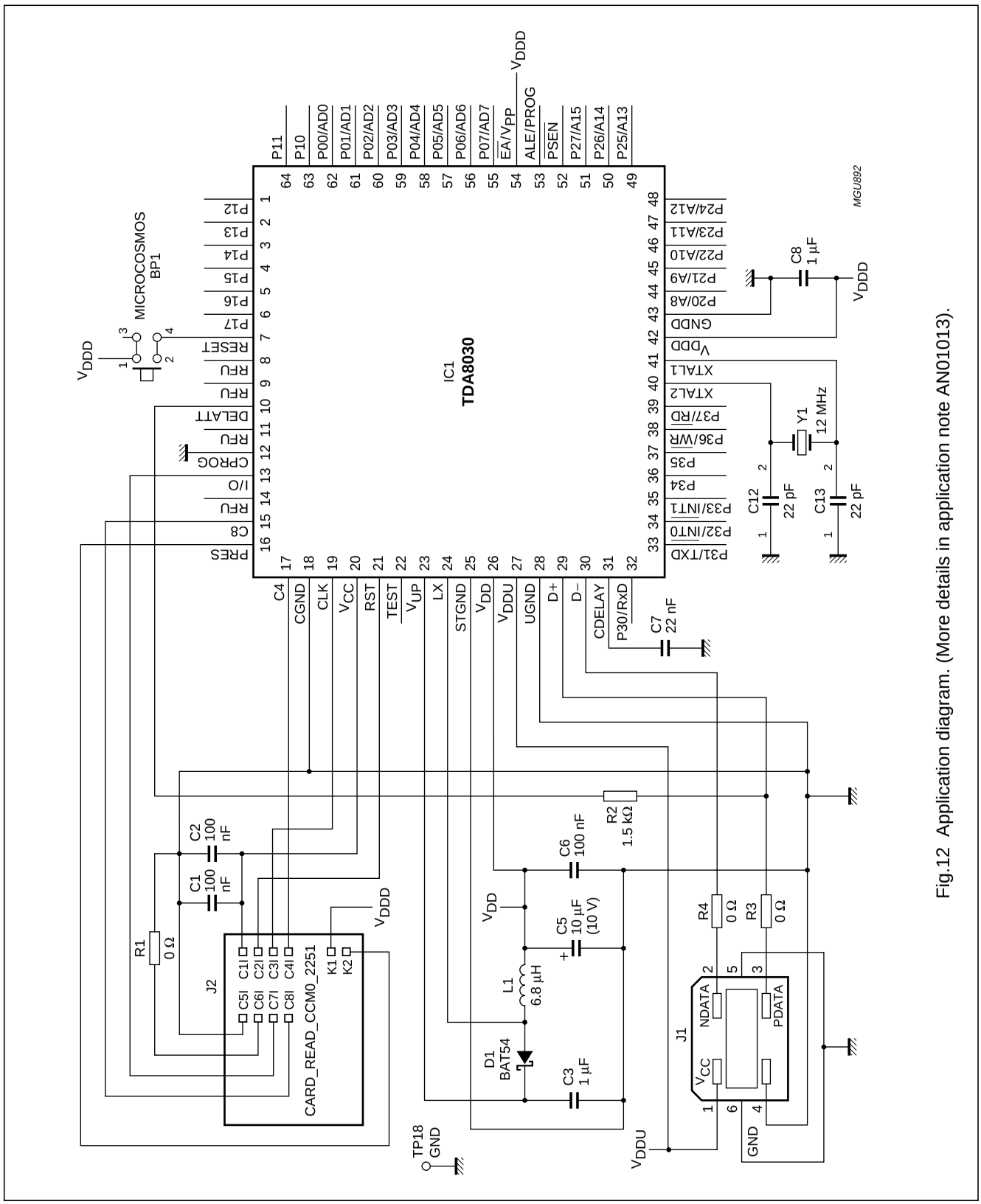
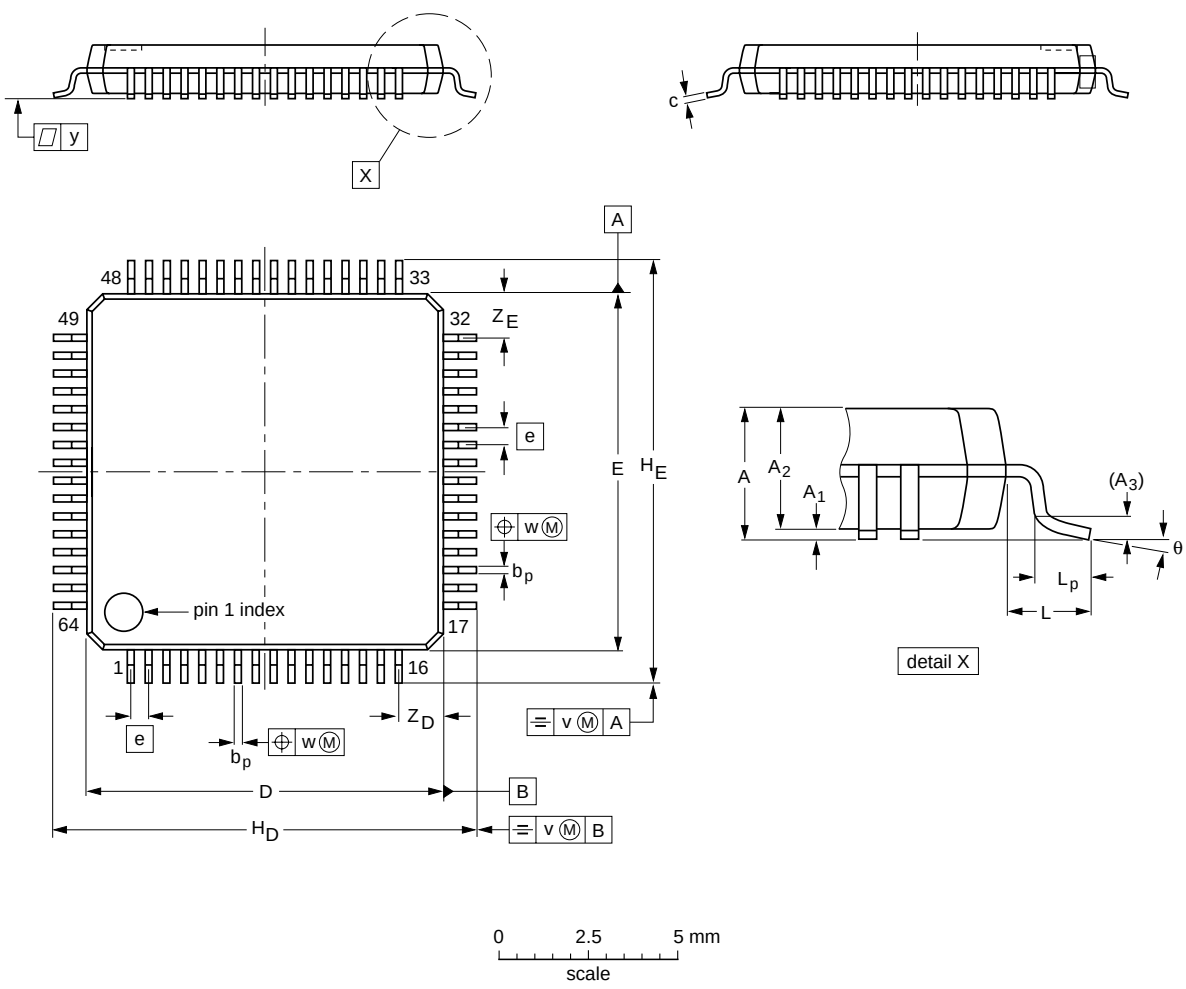


Fig.12 Application diagram. (More details in application note AN01013).

13 PACKAGE OUTLINE

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

14 SOLDERING

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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