Preliminary *64K X 16 CMOS DYNAMIC RAM WITH FAST PAGE MODE*

Document Title

64K X 16 CMOS DYNAMIC RAM WITH FAST PAGE MODE

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	November 15, 2000	Preliminary

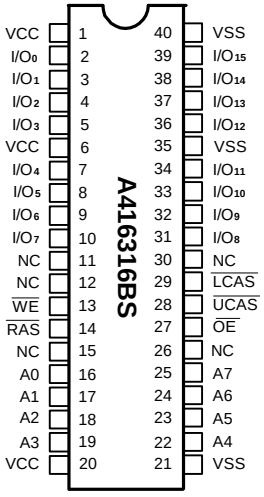
Preliminary 64K X 16 CMOS DYNAMIC RAM WITH FAST PAGE MODE

Features

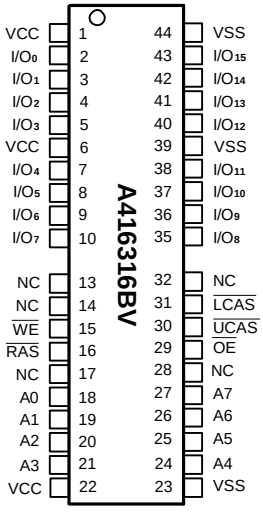
- Organization: 65,536 words X 16 bits
- Part Identification:
  - A416316B
  - A416316B-L (with self-refresh mode)
- High speed
  - 30/35/40 ns $\overline{RAS}$ access time
  - 16/18/20 ns column address access time
  - 10/11/12 ns $\overline{CAS}$ access time
- Low power consumption
  - Operating: 75mA (-30 max)
  - Standby: 3 mA (TTL)
- Separate $\overline{CAS}$ ($\overline{UCAS}$, $\overline{LCAS}$) for byte selection
- Self refresh mode
- 256 refresh cycles, 4 ms refresh interval
- Read-modify-write, $\overline{RAS}$ -only, $\overline{CAS}$ -before- $\overline{RAS}$, Hidden refresh capability
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400mil, 40-pin SOJ
  - 400mil, 40/44 TSOP type II package
- Single 5V power supply/built-in VBB generator

Pin Configuration

■ **SOJ**



■ **TSOP**



Pin Descriptions

Symbol	Description
A0 – A7	Address Inputs
I/O0 - I/O15	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	+5V Power Supply
VSS	Ground
NC	No Connection

Selection Guide

Symbol	Description	-30	-35	-40	Unit
t_{RAC}	Maximum $\overline{RAS}$ Access Time	30	35	40	ns
t_{AA}	Maximum Column Address Access Time	16	18	20	ns
t_{CAC}	Maximum $\overline{CAS}$ Access Time	10	11	12	ns
t_{OEA}	Maximum Output Enable ($\overline{OE}$) Access Time	10	11	12	ns
t_{RC}	Minimum Read or Write Cycle Time	65	70	75	ns
t_{PC}	Minimum Fast Page Mode Cycle Time	19	21	23	ns
I_{CC1}	Maximum Operating Current	95	85	75	mA
I_{CC6}	Maximum CMOS Standby Current	2	2	2	mA

Functional Description

The A416316B is a high performance CMOS Dynamic Random Access Memory organized as 65,536 words X 16 bits. The A416316B is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels.

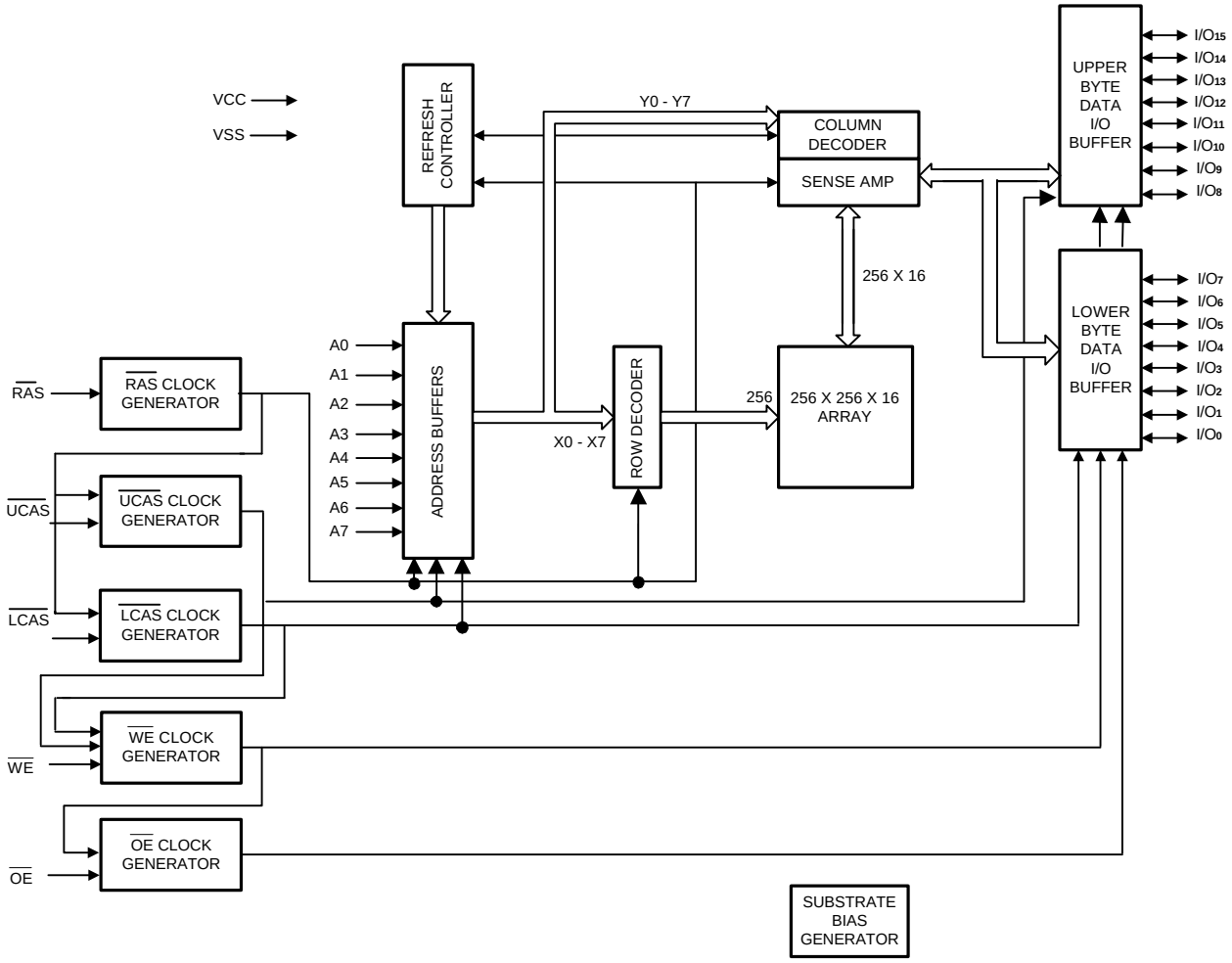
The A416316B features a high speed page mode operation in which high speed read, write and read-write are performed on any of the bits defined by the column address. The asynchronous column address uses an extremely short row address capture time to ease the system level timing constraints associated with multiplexed addressing. Output is tri-stated by a column address strobe ($\overline{UCAS}$ and $\overline{LCAS}$) which acts as an output enable independent of $\overline{RAS}$. Very fast $\overline{UCAS}$ and $\overline{LCAS}$ to output access time eases system design.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 256 X 16 bits within a page, with cycle time as short as 19/21/23 ns.

The A416316B is best suited for graphics, digital signal processing and high performance peripherals.

The A416316B is available in JEDEC standard 40-pin plastic SOJ package and 40/44 TSOP type II package.

Block Diagram



Recommended Operating Conditions (Ta = 0°C to +70°C)

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
VSS		0.0	0.0	0.0	V
V_{IH}	Input Voltage	2.4	-	VCC + 1	V
V_{IL}		-1.0	-	0.8	V

Truth Table

Function	$\overline{RAS}$	$\overline{UCAS}$	$\overline{LCAS}$	$\overline{WE}$	$\overline{OE}$	Address	I/Os	Notes
Standby	H	H	H	L	L	L	L	
Read: Word	L	L	L	H	L	Row/Col.	Data Out	
Read: Lower Byte	L	H	L	H	L	Row/Col.	I/O_{0-7} = Data Out I/O_{8-15} = High-Z	
Read: Upper Byte	L	L	H	H	L	Row/Col.	I/O_{0-7} = High-Z I/O_{8-15} = Data Out	
Write: Word(Early)	L	L	L	L	X	Row/Col.	Data In	
Write: Lower Byte(Early)	L	H	L	L	X	Row/Col.	I/O_{0-7} = Data In I/O_{8-15} = X	
Write: Upper Byte(Early)	L	L	H	L	X	Row/Col.	I/O_{0-7} = X I/O_{8-15} = Data In	
Read-Write	L	L	L	H→L	L→H	Row/Col.	Data Out → Data In	1.2
Fast-Page-Mode Read: Hi-Z								
-First cycle	L	H→L	H→L	H	H→L	Row/Col.	Data Out	2
-Subsequent Cycles	L	H→L	H→L	H	H→L	Col.	Data Out	2
Fast-Page-Mode Write(Early)								
-First cycle	L	H→L	H→L	L	X	Row/Col.	Data In	1
-Subsequent Cycles	L	H→L	H→L	L	X	Col.	Data In	1
Fast-Page-Mode Read-Write								
-First cycle	L	H→L	H→L	H→L	L→H	Row/Col.	Data In	1, 2
-Subsequent Cycles	L	H→L	H→L	H→L	L→H	Col.	Data In	1, 2
Hidden Refresh Read	L→H→L	L	L	H	L	Row/Col.	Data Out	2
Hidden Refresh Write	L→H→L	L	L	L	X	Row/Col.	Data In → High-Z	1
$\overline{RAS}$-Only Refresh	L	H	H	X	X	Row	High-Z	
CBR Refresh	H→L	L	L	X	X	X	High-Z	3
Self Refresh (L-ver only)	H→L	L	L	X	X	X	High-Z	

Note: 1. Byte Write may be executed with either $\overline{UCAS}$ or $\overline{LCAS}$ active.
2. Byte Read may be executed with either $\overline{UCAS}$ or $\overline{LCAS}$ active.
3. Only one $\overline{CAS}$ signal ($\overline{UCAS}$ or $\overline{LCAS}$) must be active.

Absolute Maximum Ratings*

Input Voltage (Vin) . . . . . -1.0V to +7.0V
Output Voltage (Vout) . . . . . -1.0V to +7.0V
Power Supply Voltage (VCC) . . . . . -1.0V to +7.0V
Operating Temperature (T_{OPR}) . . . . . 0°C to +70°C
Storage Temperature (T_{STG}) . . . . . -55°C to +150°C
Soldering Temperature X Time (T_{SLODER}) . . . . . 260°C X 10sec
Power Dissipation (P_D) 1W
Short Circuit Output Current (Iout) 50mA
Latch-up Current 200mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

Symbol	Parameter	-30		-35		-40		Unit	Test Conditions	Notes
		Min.	Max.	Min.	Max.	Min.	Max.			
I_{IL}	Input Leakage Current	-10	+10	-10	+10	-10	+10	µA	0V ≤ Vin ≤ +5.5V Pins not under test = 0V	
I_{OL}	Output Leakage Current	-10	+10	-10	+10	-10	+10	µA	DOUT disabled, 0V ≤ Vout ≤ +5.5V	
I_{CC1}	Operating Current	-	95	-	85	-	75	mA	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ Address cycling t_{RC} = min.	1, 2
I_{CC2}	TTL Standby Power Supply Current	-	3	-	3	-	3	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} All other inputs ≥ VSS	
I_{CC3}	Refresh Current ($\overline{RAS}$ only Refresh)	-	95	-	85	-	75	mA	$\overline{RAS}$ cycling, $\overline{UCAS}$=$\overline{LCAS}$ = V_{IH}, t_{RC} = min.	1
I_{CC4}	Fast Page Mode Current	-	95	-	85	-	75	mA	$\overline{RAS}$ = V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$ Address cycling t_{PC} = min.	1, 2
I_{CC5}	Refresh Current ($\overline{CAS}$ -before-$\overline{RAS}$ Refresh)	-	95	-	85	-	75	mA	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ cycling t_{RC} = min.	1
I_{CC6}	CMOS Standby Power Supply Current	-	2	-	2	-	2	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ VCC - 0.2V All other inputs ≥ VSS	
I_{CC7}	Self Refresh Mode Current	-	3	-	3	-	3	mA	$\overline{RAS}$ = $\overline{CAS}$ ≤ VSS + 0.2V All other inputs ≥ VSS	
V_{OH}	Output High Voltage	2.4	-	2.4	-	2.4	-	V	I_{OUT} = -5.0mA	
V_{OL}	Output Low Voltage	-	0.4	-	0.4	-	0.4	V	I_{OUT} = 4.2mA	

AC Characteristics

(VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

#	Std Symbol	Parameter	-30		-35		-40		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RC}	Random Read or Write Cycle Time	65	-	70	-	75	-	ns	
2	t_{RP}	$\overline{RAS}$ Precharge Time	25	-	25	-	25	-	ns	
3	t_{RAS}	$\overline{RAS}$ Pulse Width	30	75K	35	75K	40	75K	ns	
4	t_{CAS}	$\overline{CAS}$ Pulse Width	12	-	12	-	12	-	ns	
5	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	20	16	24	17	28	ns	6
6	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	14	11	17	12	20	ns	7
7	t_{RSH}	$\overline{CAS}$ to $\overline{RAS}$ Hold Time	10	-	10	-	10	-	ns	
8	t_{CSH}	$\overline{CAS}$ Hold Time	30	-	35	-	40	-	ns	
9	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
10	t_{ASR}	Row Address Setup Time	0	-	0	-	0	-	ns	
11	t_{RAH}	Row Address Hold Time	5	-	6	-	7	-	ns	
	t_T	Transition Time (Rise and Fall)	2	50	2	50	2	52	ns	4, 5
	t_{REF}	Refresh Period	-	4	-	4	-	4	ms	3
12	t_{CLZ}	$\overline{CAS}$ to Output in Low Z	0	-	0	-	0	-	ns	8
13	t_{RAC}	Access Time from $\overline{RAS}$	-	30	-	35	-	40	ns	6,7
14	t_{CAC}	Access Time from $\overline{CAS}$	-	10	-	11	-	12	ns	6, 13
15	t_{AA}	Access Time from Column Address	-	16	-	18	-	20	ns	7, 13
16	t_{AR}	Column Address Hold Time from $\overline{RAS}$	26	-	28	-	30	-	ns	
17	t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	

AC Characteristics (continued)

(VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

#	Std Symbol	Parameter	-30		-35		-40		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
18	t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	9
19	t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	0	-	0	-	0	-	ns	9
20	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	16	-	18	-	20	-	ns	
21	t_{COH}	Output Hold After $\overline{CAS}$ Low	5	-	5	-	5	-	ns	
22	t_{ODS}	Output Disable Setup Time	0	-	0	-	0	-	ns	
23	t_{OFF}	Output Buffer Turn-Off Delay Time	0	6	0	6	0	6	ns	8, 10
24	t_{ASC}	Column Address Setup Time	0	-	0	-	0	-	ns	
25	t_{CAH}	Column Address Hold Time	5	-	5	-	5	-	ns	
26	t_{RPS}	$\overline{RAS}$ Precharge Setup Time	50	-	60	-	70	-	ns	
27	t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	11
28	t_{WCH}	Write Command Hold Time	5	-	5	-	5	-	ns	11
29	t_{WCR}	Write Command Hold Time to $\overline{RAS}$	26	-	28	-	30	-	ns	
30	t_{WP}	Write Command Pulse Width	5	-	5	-	5	-	ns	
31	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	-	11	-	12	-	ns	
32	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	-	11	-	12	-	ns	
33	t_{DS}	Data-in setup Time	0	-	0	-	0	-	ns	12
34	t_{DH}	Data-in Hold Time	5	-	5	-	5	-	ns	12
35	t_{DHR}	Data-in Hold Time to $\overline{RAS}$	26	-	28	-	30	-	ns	
36	t_{RMW}	Read-Modify-Write Cycle Time	100	-	105	-	100	-	ns	
37	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time (Read-Modify-Write)	50	-	54	-	58	-	ns	11

AC Characteristics (continued)

(VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

#	Std Symbol	Parameter	-30		-35		-40		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
38	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time (Read-Modify-Write)	26	-	28	-	30	-	ns	11
39	t_{AWD}	Column Address to $\overline{WE}$ Delay Time (Read-Modify-Write)	32	-	35	-	35	-	ns	11
40	t_{RASS}	$\overline{RAS}$ Pulse Width (Self Refresh Mode)	300	-	300	-	300	-	µs	
41	t_{CPN}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	10	100K	10	100K	10	100K	ns	
42	t_{PC}	Read or Write Cycle Time (Fast Page)	19	-	21	-	23	-	ns	14
43	t_{CPA}	Access Time from $\overline{CAS}$ Precharge (Fast Page)	-	19	-	21	-	23	ns	13
44	t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page)	3	-	4	-	5	-	ns	
45	t_{PRM}	Fast Page Mode RMW Cycle Time	56	-	58	-	60	-	ns	
46	t_{CRW}	Fast Page Mode $\overline{CAS}$ Pulse Width (RMW)	-	44	-	46	-	48	ns	
47	t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page)	30	75K	35	75K	40	75K	ns	
48	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$)	0	-	0	-	0	-	ns	3
49	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$)	7	-	8	-	8	-	ns	3
50	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$)	0	-	0	-	0	-	ns	
51	t_{ROH}	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	6	-	7	-	8	-	ns	
52	t_{OEA}	$\overline{OE}$ Access Time	-	10	-	11	-	12	ns	
53	t_{OED}	$\overline{OE}$ to Data Delay	5	-	5	-	5	-	ns	
54	t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	5	0	6	0	6	ns	8

AC Characteristics (continued)

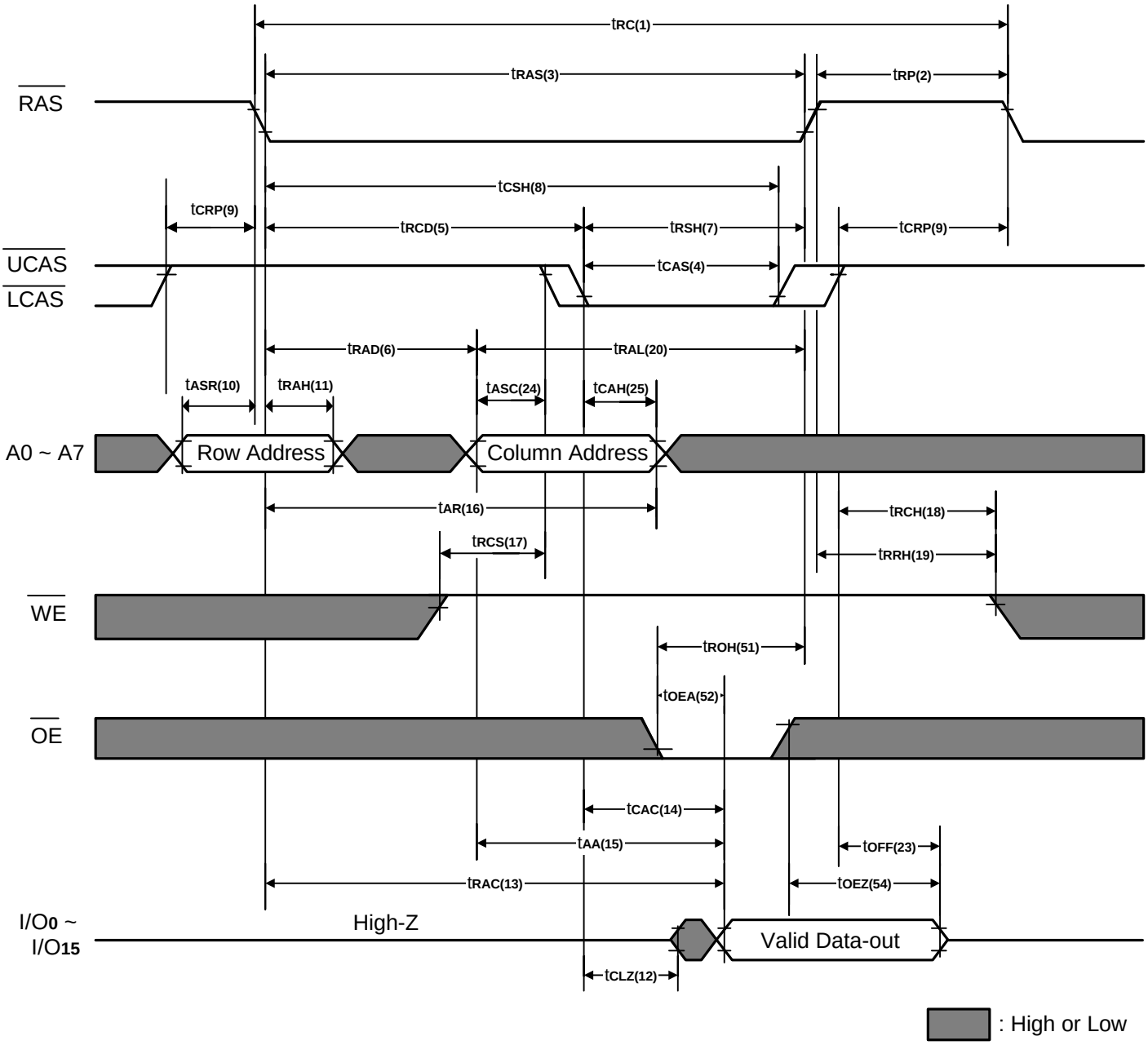
(VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

#	Std Symbol	Parameter	-30		-35		-40		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
55	t_{OEH}	$\overline{OE}$ Command Hold Time	0	-	0	-	0	-	ns	
56	t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Counter Test)	20	-	20	-	20	-	ns	

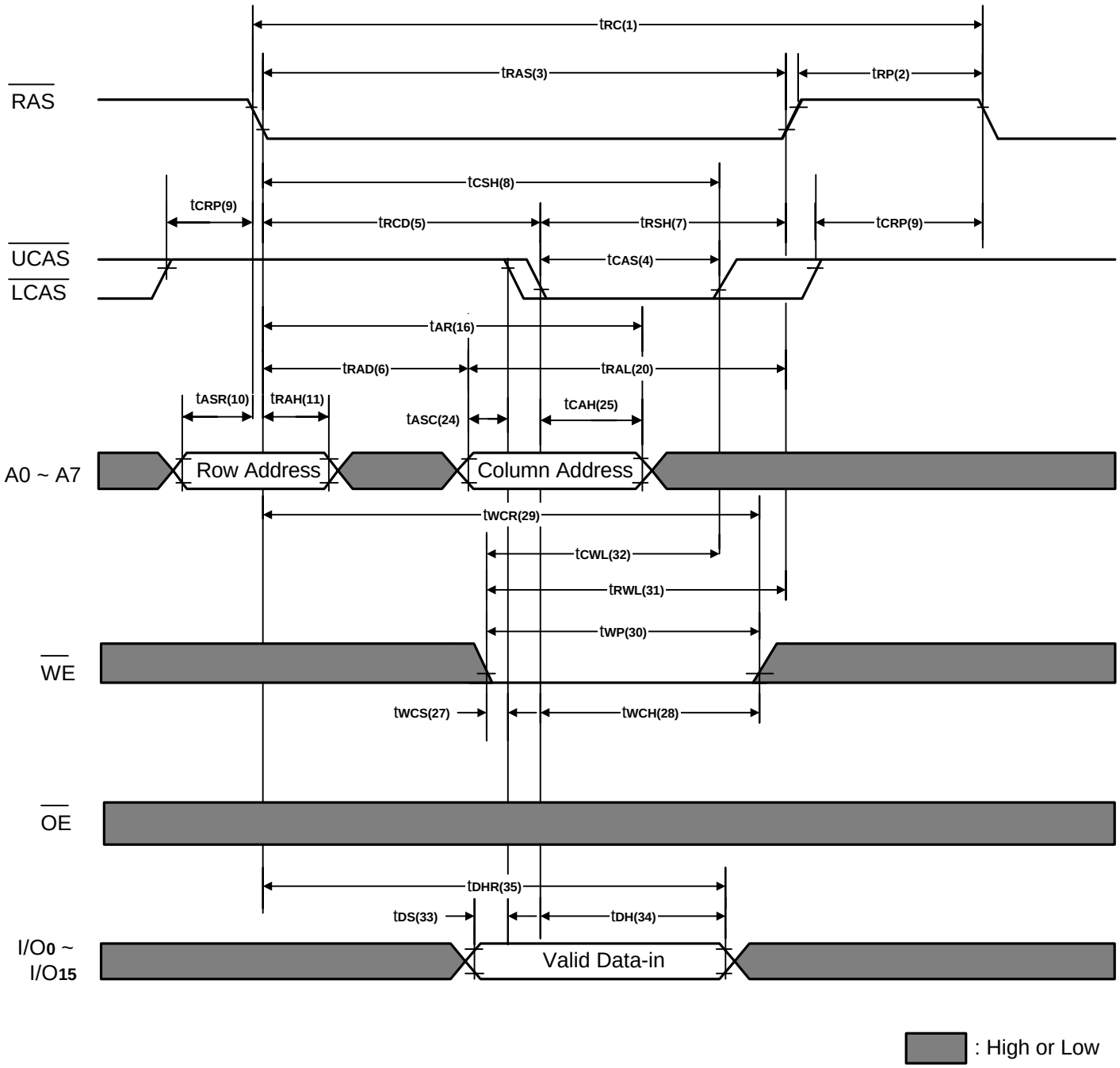
Notes:

1. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
3. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8ms).
4. AC Characteristics assume t_T = 3ns. All AC parameters are measured with a load equivalent to one TTL loads and 50pF, V_{IL} (min.) ≥ GND and V_{IH} (max.) ≤ VCC.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
7. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
8. Assumes three state test load (5pF and a 380Ω Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.
11. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS} (min.) and t_{WCH} ≥ t_{WCH} (min.), the cycle is an early write cycle and data-out pins will remain open circuit, high impedance, throughout the entire cycle. If t_{RWD} ≥ t_{RWD} (min.) , t_{CWD} ≥ t_{CWD} (min.) and t_{AWD} ≥ t_{AWD} (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
12. These parameters are referenced to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
14. t_{ASC} ≥ t_{CP} to achieve t_{PC} (min.) and t_{CPA} (max.) values.
15. These parameters are sampled and not 100% tested.

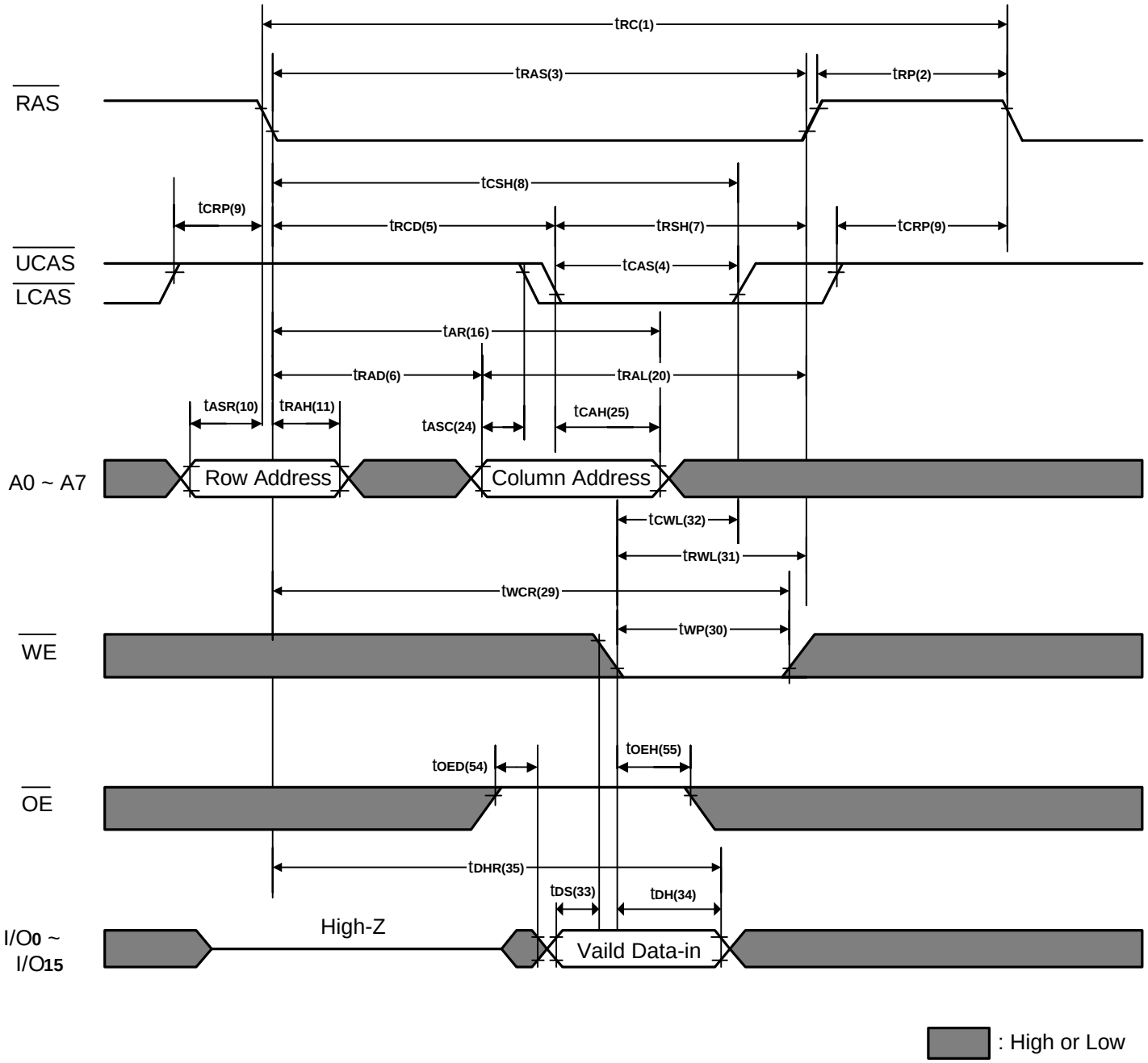
Word Read Cycle



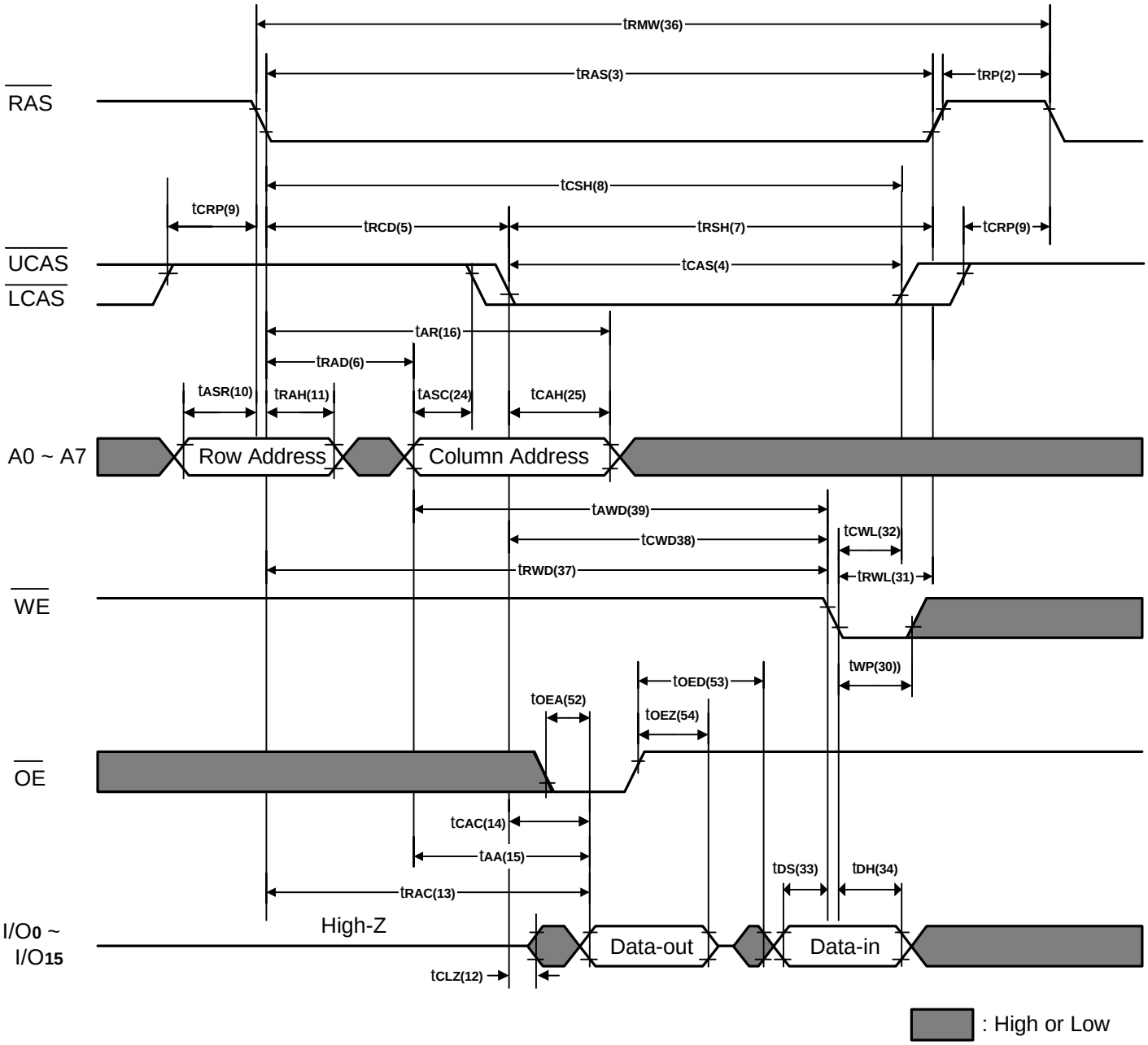
Word Write Cycle (Early Write)



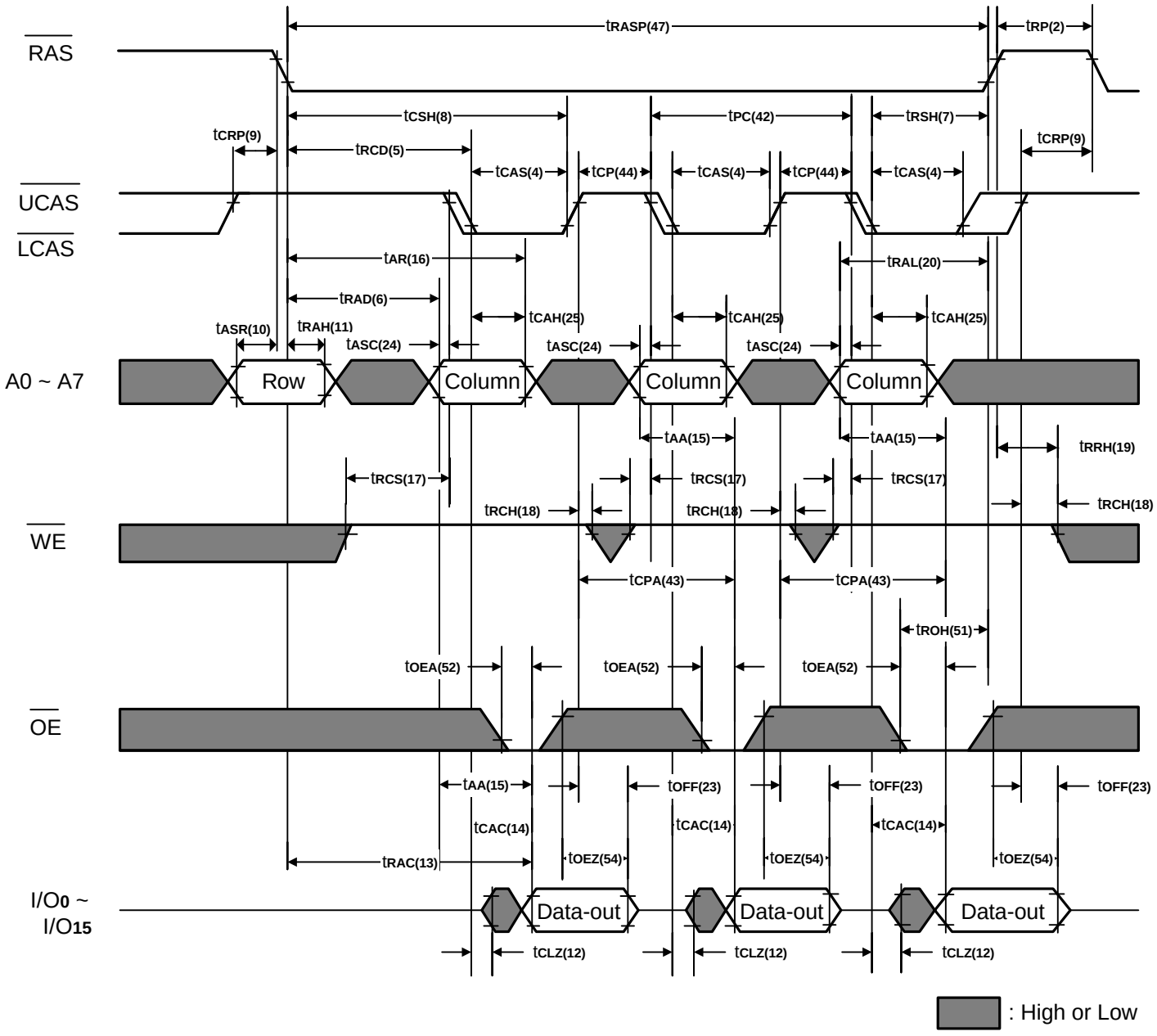
Word Write Cycle (Late Write)



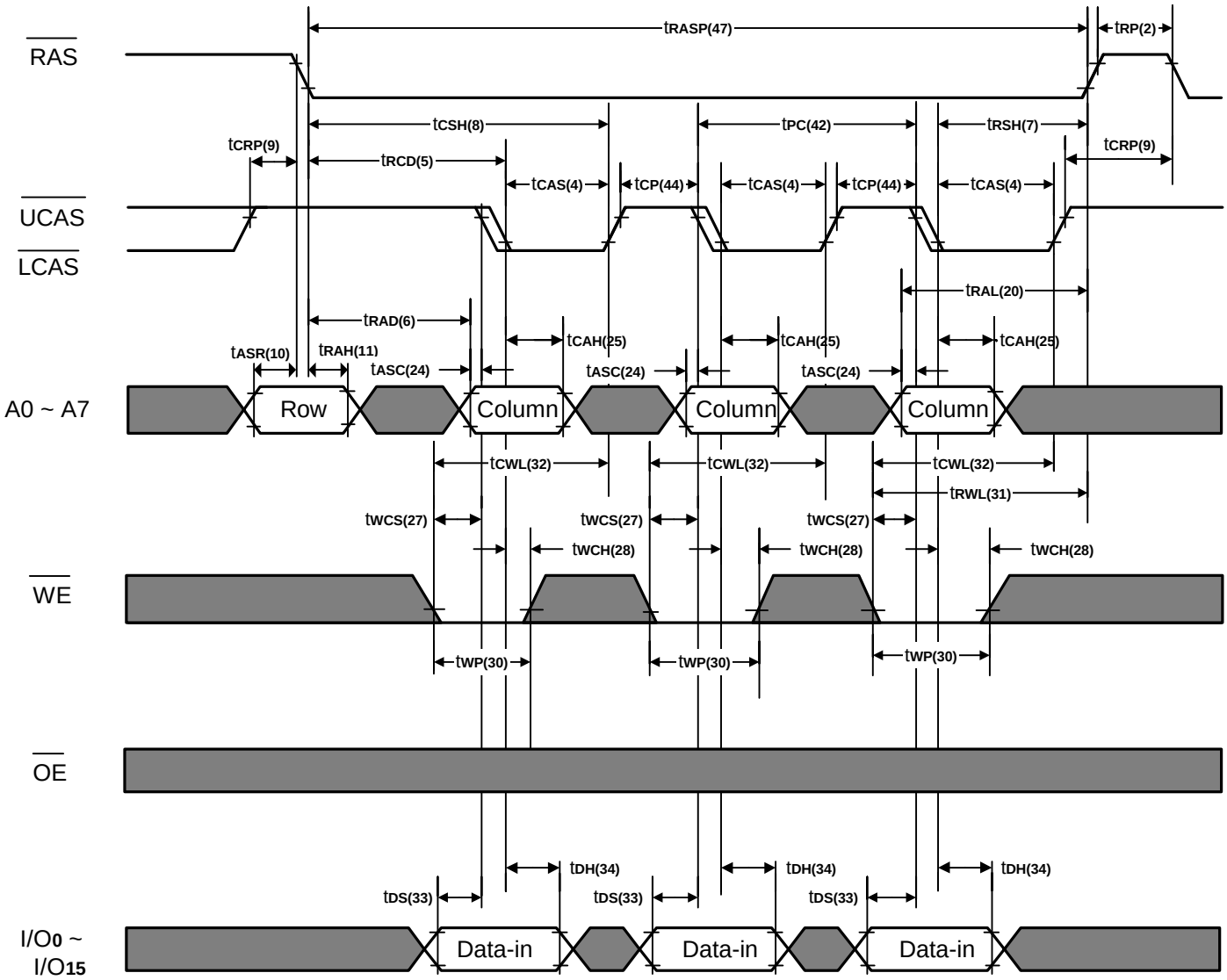
Word Read-Modify-Write Cycle



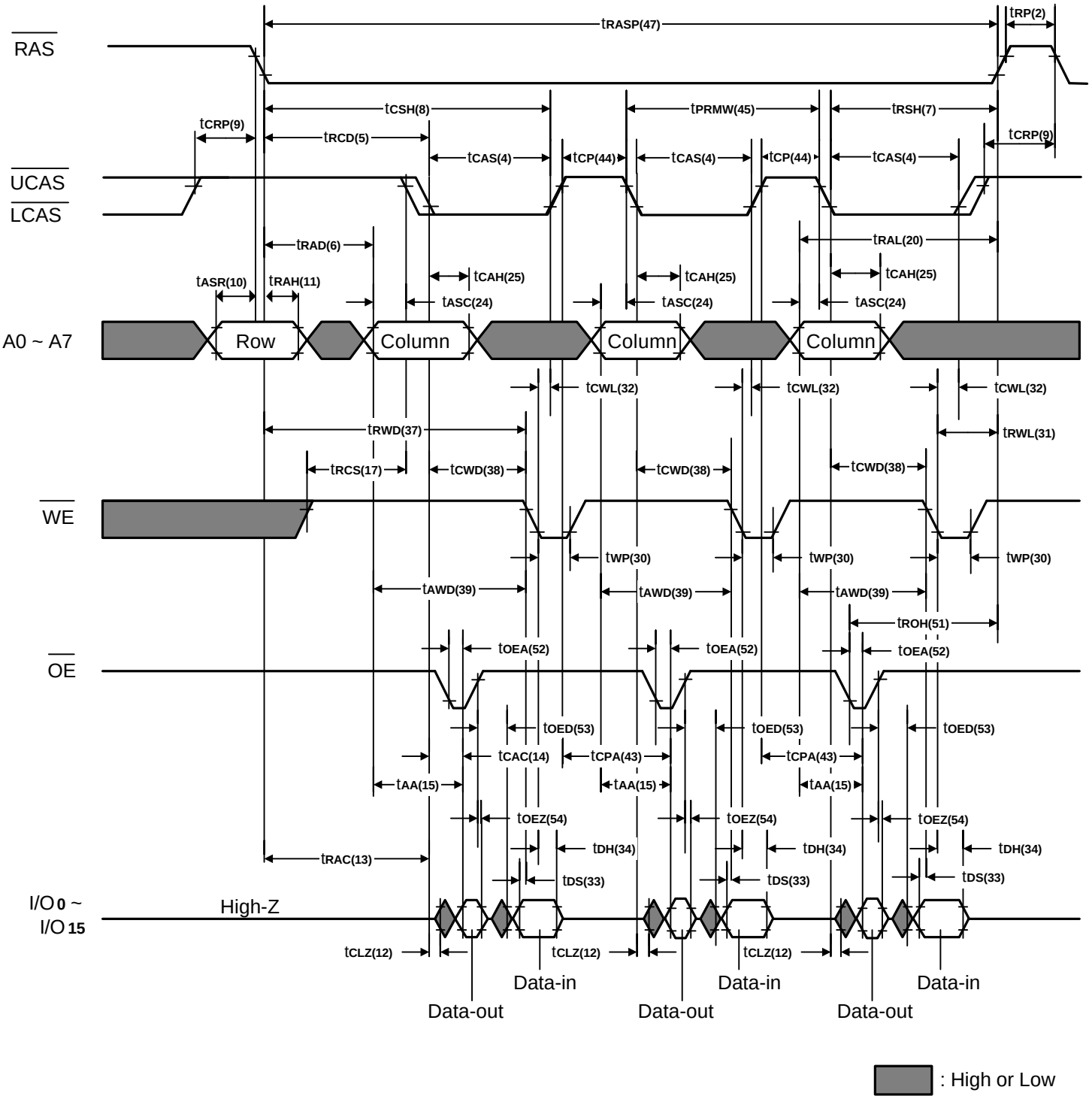
Fast Page Mode Word Read Cycle



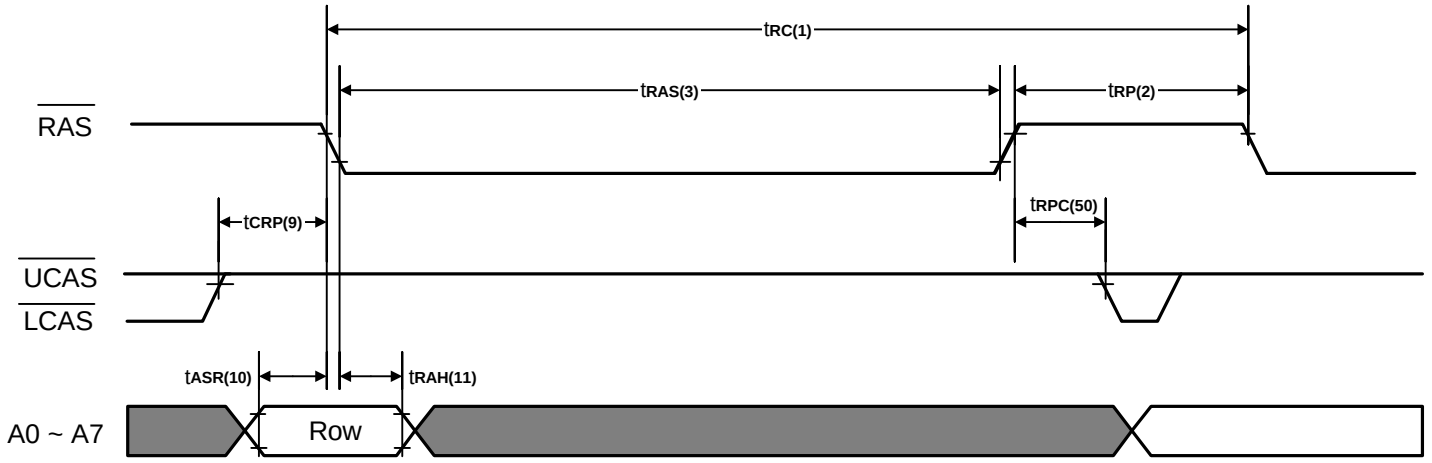
Fast Page Mode Early Word Write Cycle



Fast Page Mode Word Read-Modify-Write Cycle



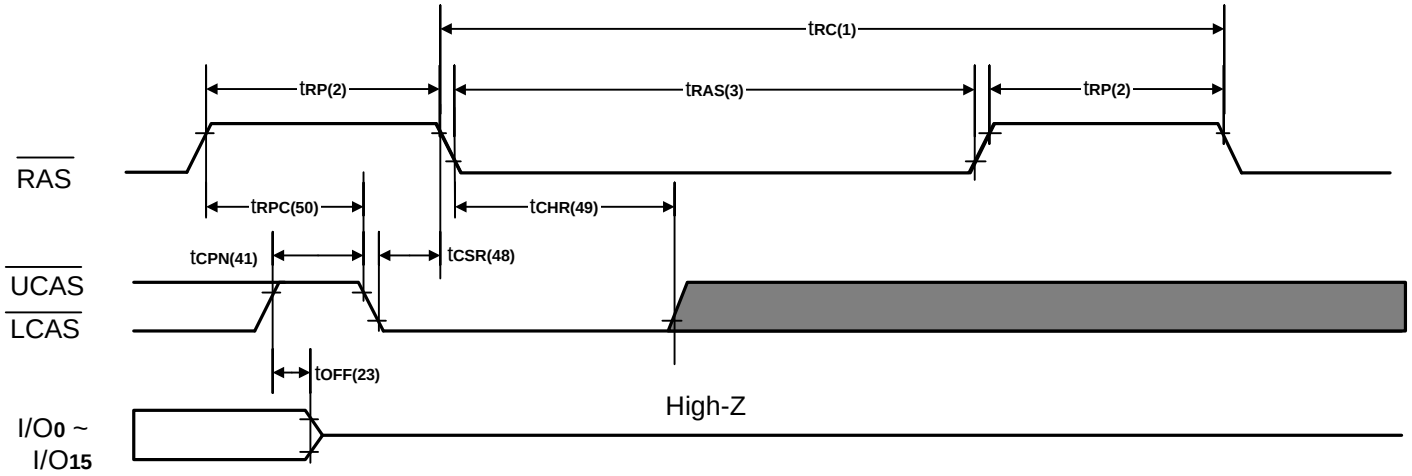
$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

: High or Low

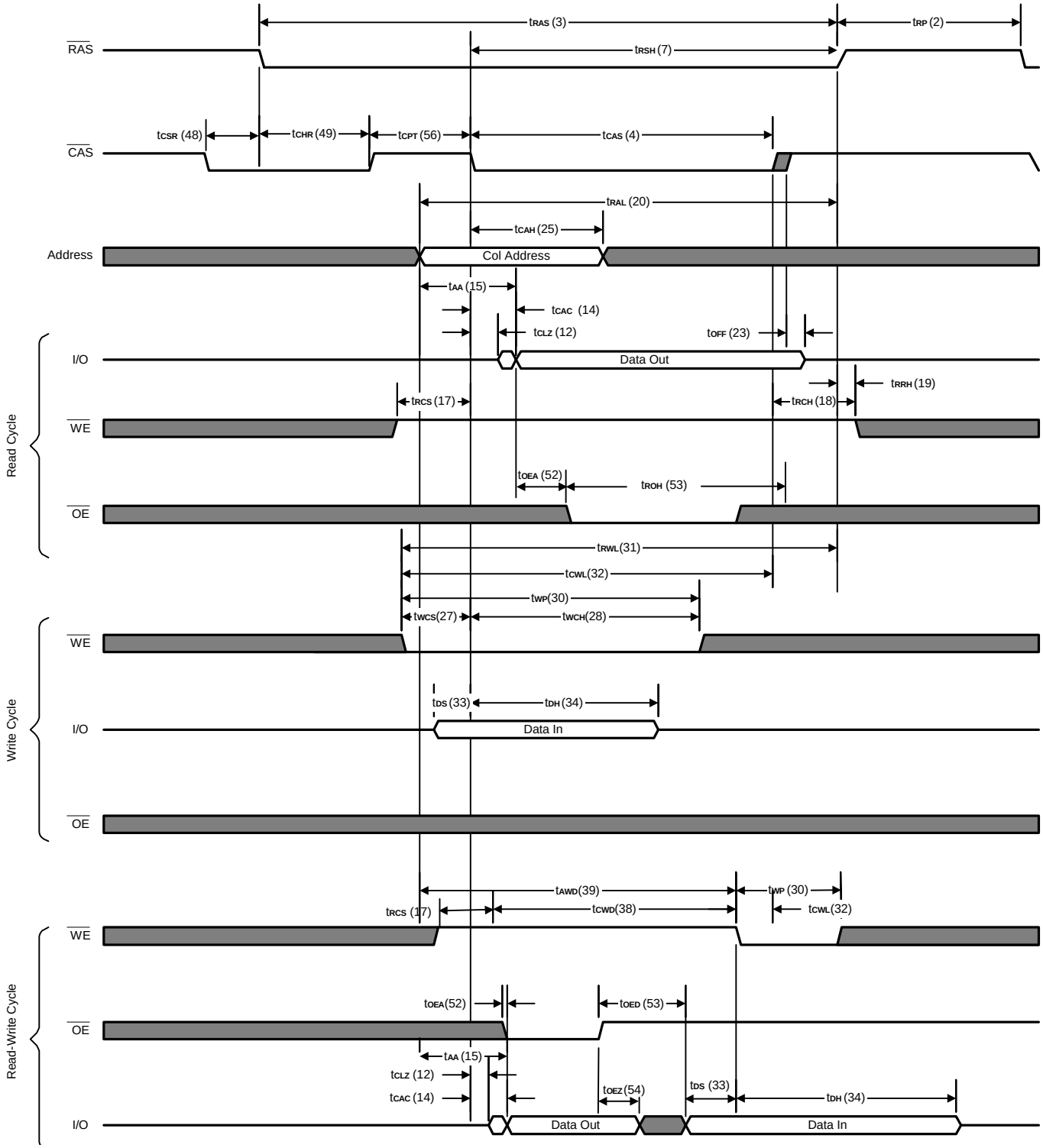
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



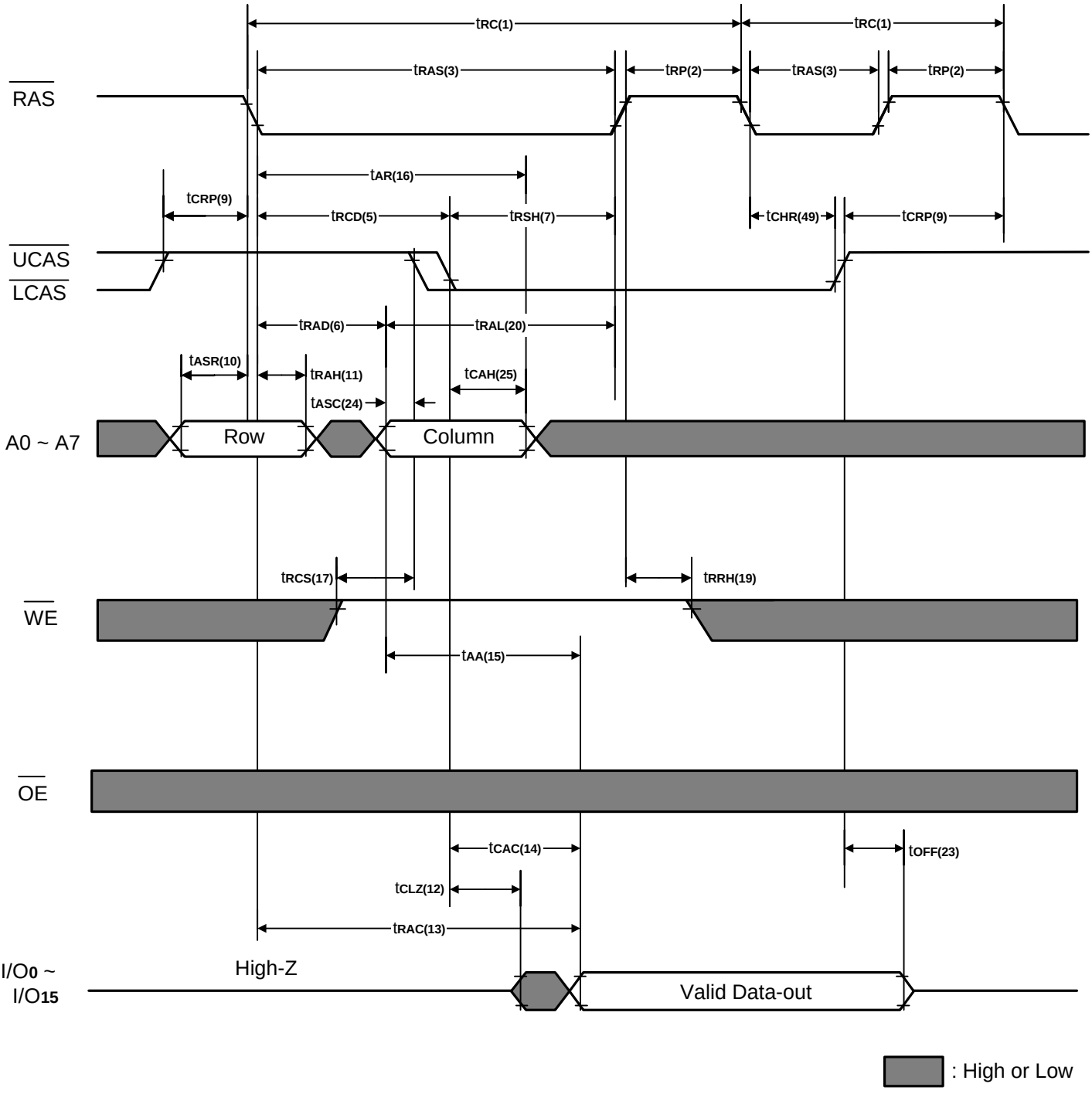
Note: $\overline{WE}$, $\overline{OE}$, A0 ~ A7 = Don't care.

: High or Low

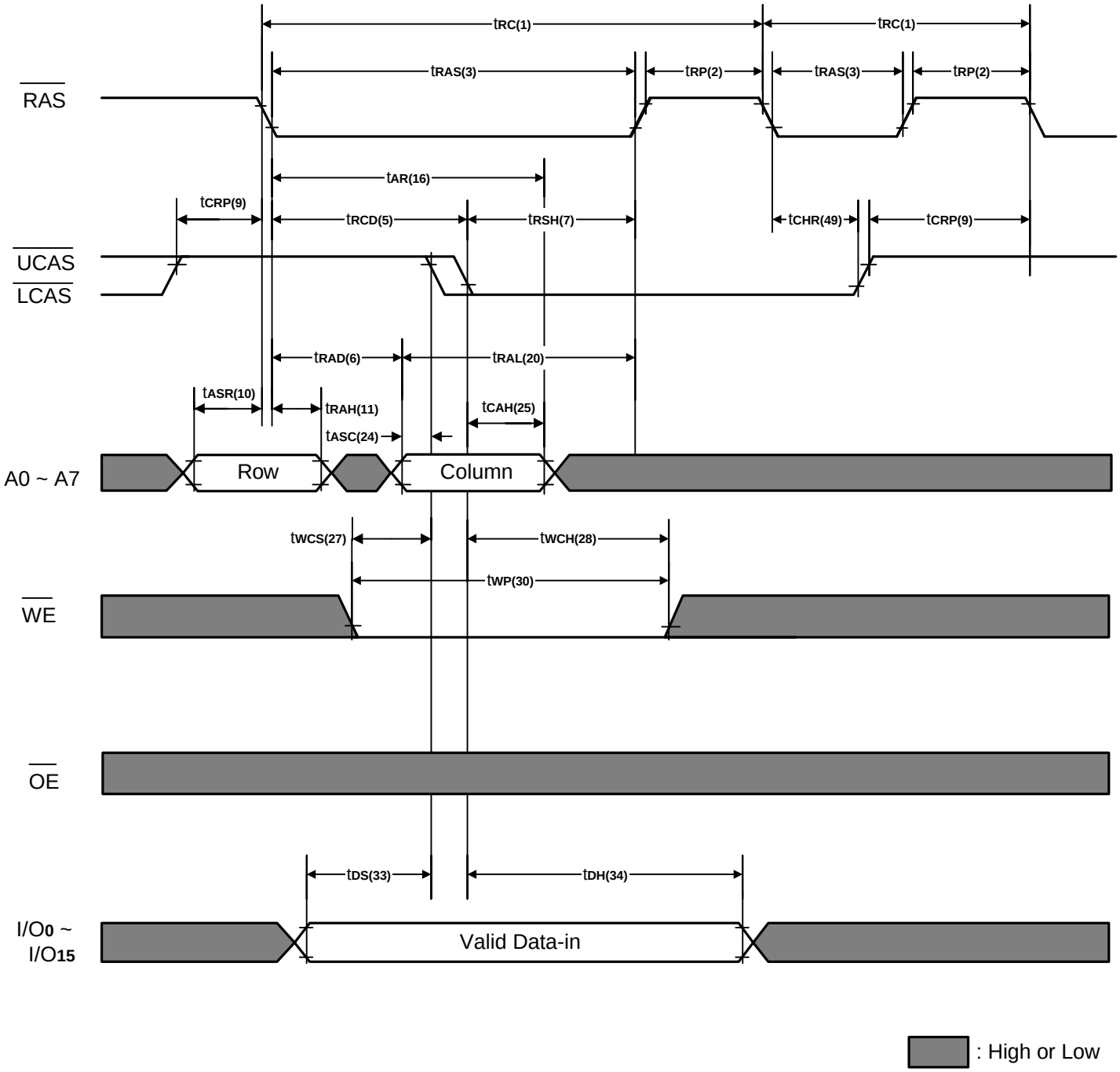
Timing Waveform of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



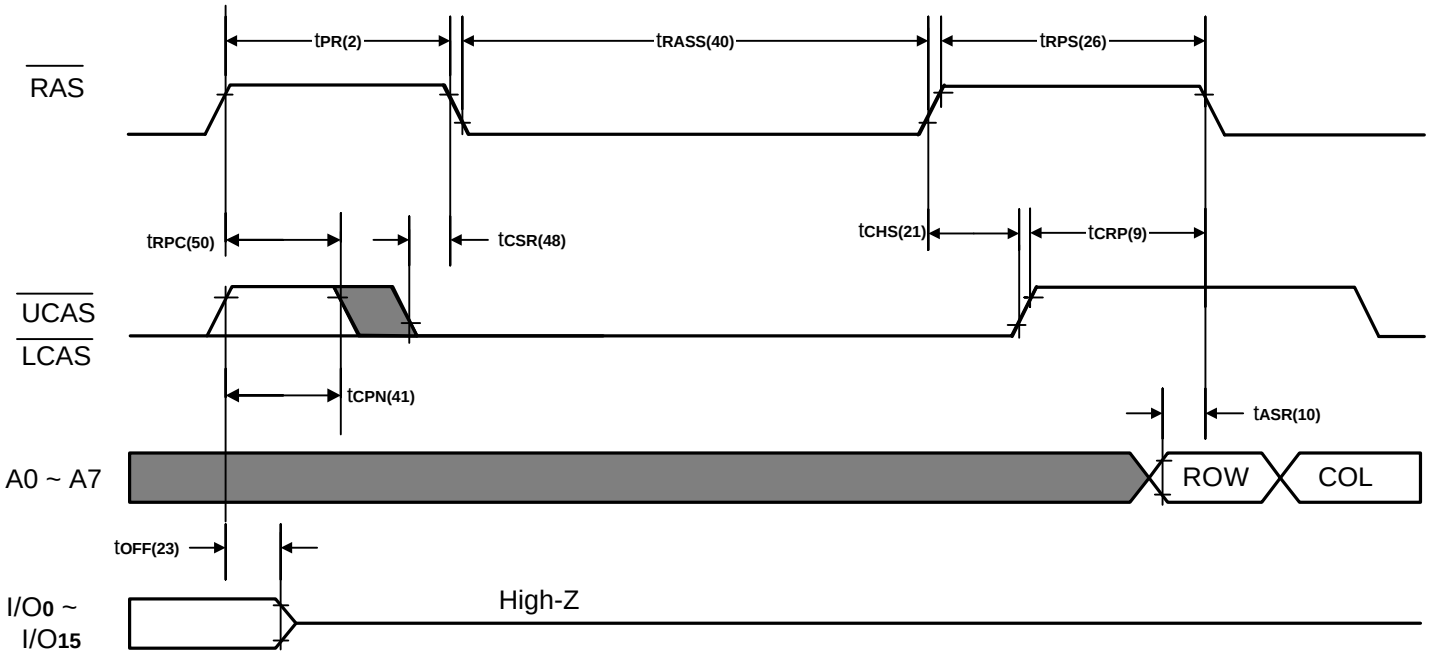
Hidden Refresh Cycle (Word Read)



Hidden Refresh Cycle (Early Word Write)



Self Refresh Mode (A416316B-L Only)



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

: High or Low

■ Self Refresh Mode.

a. Entering the Self Refresh Mode:

The A416316B-L Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle and holding $\overline{RAS}$ and $\overline{CAS}$ signal "low" longer than 300μs.

b. Continuing the Self Refresh Mode:

The Self Refresh Mode is continued by holding $\overline{RAS}$ "low" after entering the Self Refresh Mode.

It does not depend on $\overline{CAS}$ being "high" or "low" after entering the Self Refresh Mode continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:

The A416316B exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought "high".

Capacitance[15] (f = 1MHz, Ta = Room Temperature, VCC = 5V ± 10%)

Symbol	Signals	Parameter	Max.	Unit	Test Conditions
C_{IN1}	A0 – A7	Input Capacitance	5	pF	Vin = 0V
C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$		7	pF	Vin = 0V
$C_{I/O}$	I/O_0 - I/O_{15}	I/O Capacitance	7	pF	Vin = Vout = 0V

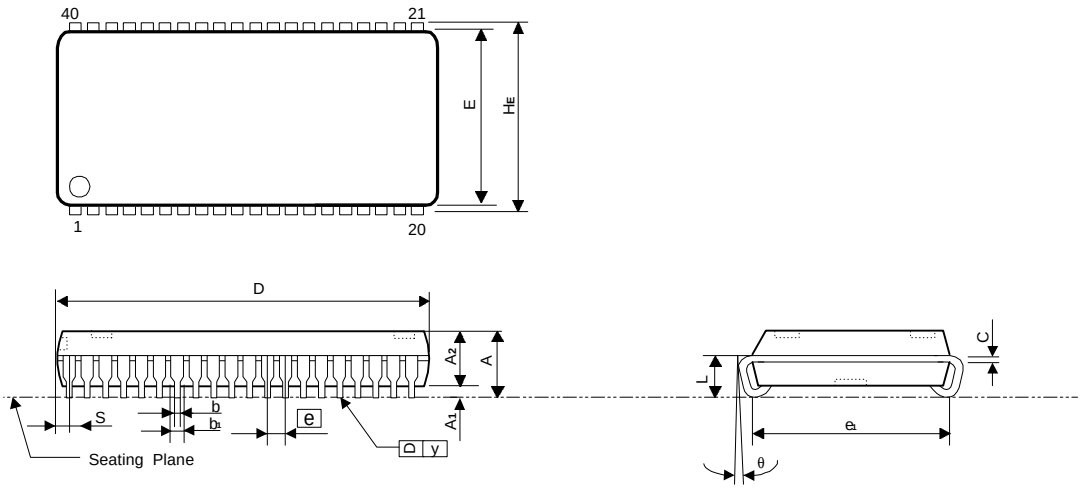
Ordering Codes

Package\ $\overline{RAS}$ Access Time	30ns	35ns	40ns	Self-Refresh
40L SOJ (400 mil)	A416316BS-30	A416316BS-35	A416316BS-40	No
40/44L TSOP type II (400mil)	A416316BV-30	A416316BV-35	A416316BV-40	No
40L SOJ (400mil)	A416316BS-30L	A416316BS-35L	A416316BS-40L	Yes
40/44L TSOP II (400mil)	A416316BV-30L	A416316BV-35L	A416316BV-40L	Yes

Package Information

SOJ 40L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.144	-	-	3.66
A_1	0.025	-	-	0.64	-	-
A_2	0.105	0.110	0.115	2.67	2.79	2.92
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
C	0.008	0.010	0.014	0.20	0.25	0.36
D	1.020	1.025	1.030	25.91	26.04	26.16
E	0.395	0.400	0.405	10.03	10.16	10.29
e	0.044	0.050	0.056	1.12	1.27	1.42
e_1	0.355	0.366	0.376	9.114	9.383	9.652
H_E	0.430	0.440	0.450	10.92	11.18	11.43
L	0.081	0.093	0.105	2.083	2.39	2.70
S	-	-	0.050	-	-	1.27
y	-	-	0.004	-	-	0.10
θ	0°	-	10°	0°	-	10°

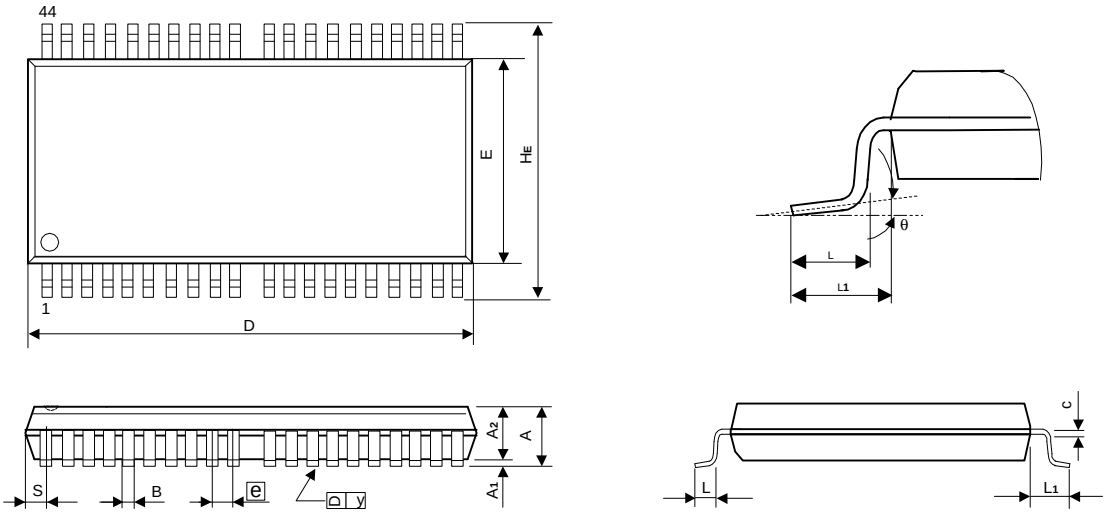
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

TSOP 40/44L (Type II) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.013	0.015	0.017	0.32	0.37	0.42
c	0.003	0.005	0.009	0.08	0.13	0.23
D	0.720	0.725	0.730	18.28	18.41	18.54
E	0.395	0.400	0.405	10.03	10.16	10.29
e	0.031 BSC			0.80 BSC		
H_E	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	-	0.031	-	-	0.80	-
S	-	-	0.035	-	-	0.90
y	-	-	0.004	-	-	0.10
θ	1°	3°	5°	1°	3°	5°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.