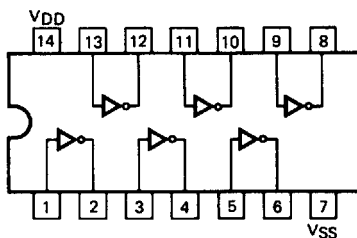


# GD4069UB

## HEX INVERTER

**DESCRIPTION** — The 4069UB is a general purpose Hex Inverter which has standard GS input and output characteristics. A single-stage design has been used since the output impedance of a single-input gate is not pattern sensitive. The 4069UB is a Direct Replacement for the 74C04/54C04.

**LOGIC AND CONNECTION DIAGRAM**  
DIP (TOP VIEW)



**NOTE:**  
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

**DC CHARACTERISTICS:**  $V_{DD}$  as shown,  $V_{SS} = 0\text{ V}$  (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DD} = 5\text{ V}$			$V_{DD} = 10\text{ V}$			$V_{DD} = 15\text{ V}$					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
$I_{DD}$	Quiescent Power	XC			1			2			4	$\mu\text{A}$	MIN, 25°C	All inputs at 0 V or $V_{DD}$
					7.5			15			30		MAX	
	Supply Current	XM			0.25			0.5			1	$\mu\text{A}$	MIN, 25°C	
					7.5			15			30		MAX	

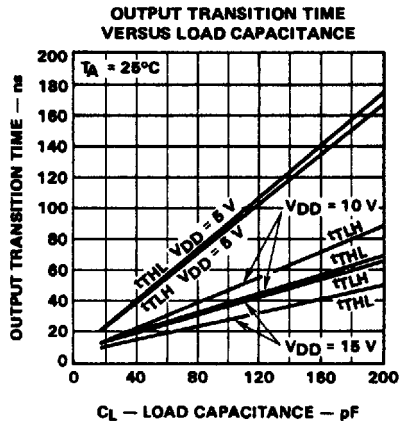
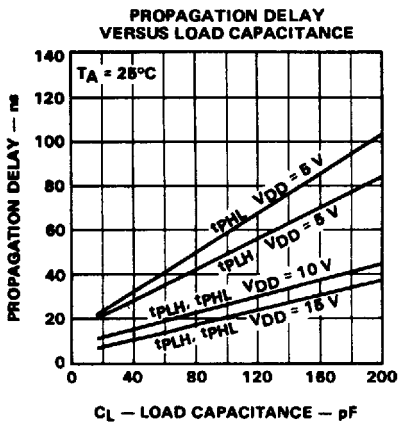
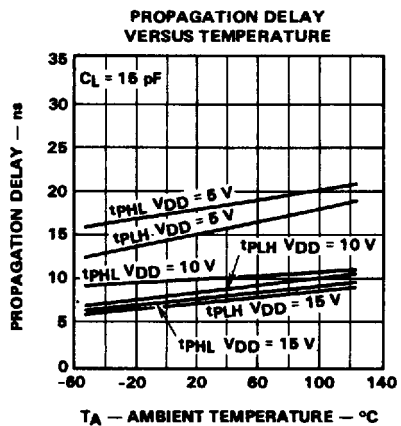
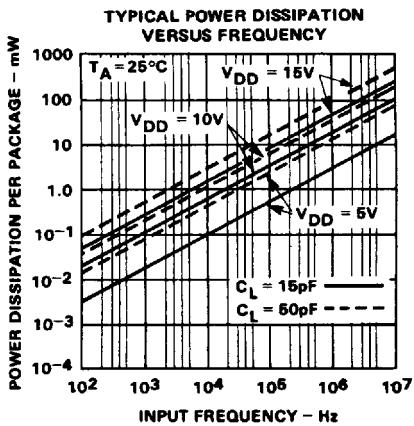
**AC CHARACTERISTICS AND SET-UP REQUIREMENTS:**  $V_{DD}$  as shown,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (See Note 2)

SYMBOL	PARAMETER		LIMITS									UNITS	TEST CONDITIONS
			$V_{DD} = 5\text{ V}$			$V_{DD} = 10\text{ V}$			$V_{DD} = 15\text{ V}$				
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay		32	64		16	32		13	26	ns	$C_L = 50\text{ pF}$ , $R_L = 200\text{ k}\Omega$	
$t_{PHL}$			32	64		16	32		13	26			
$t_{TLH}$	Output Transition Time		45	135		23	70		18	45	ns	Input Transition Times < 20 ns	
$t_{THL}$			45	135		23	70		18	45			

**NOTES:**

- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS



**TYPICAL VOLTAGE TRANSFER CHARACTERISTICS**

