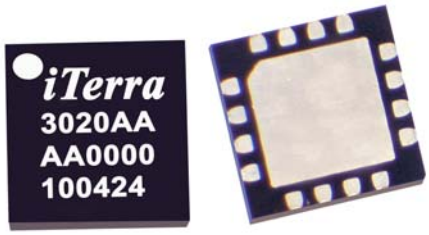
iT3020
10 GHz Variable Gain Amplifier

Description

The iT3020 is a highly linear low noise differential variable gain amplifier with a bandwidth of DC to 10 GHz. It is suitable for Automatic Gain Control (AGC) in high bandwidth applications such as a 10/12.5 Gb/s STM-64/OC-192 receiver front end. Offset correction and shutoff control are provided. Both AC and DC coupling are allowed at the input and output. High sensitivity allows the device to be used at the output of a transimpedance amplifier.

Features

- 3-dB bandwidth: 10 GHz
- Differential gain: 29 dB
- Bias supply: -5 V, 156 mA, and +5 V, 74 mA
- Power consumption: 1150 mW
- Gain control: 30 dB
- CMRR: Better than 25 dB
- DC offset correction
- Low RMS jitter
- Low-cost JEDEC QFP-N (MO-220) package



Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
Vee	Power supply voltage negative	-6	0	V
Vcc	Power supply voltage positive	0	6	V
Vd	Applied voltage at data input (differential)		3	V
Vm	Applied voltage at data input (single ended)		1.5	V
Ioffset(+),(-)	Offset control current		5	mA
Tch	Maximum channel temperature		150	°C
Tstg	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Tc	Operating temperature range (Tcase)	0		85	°C
Vee	Power supply voltage	-5.25	-5	-4.75	V
Vcc	Power supply voltage	4.75	5	5.25	V
Iee	Negative bias supply current	146	156	167	mA
Icc	Positive bias supply current	65	74	82	mA
BR	Bit rate			12.5	Gb/s
Vimn	Offset control voltage	-5		5	V
Vgc	Gain control voltage	-3.2		0	V
Vsh	Shut-off control voltage	-5		0	V
	Input/output interface	AC and DC coupled			
Vin_DC	Input DC voltage (DC coupling)		0		V
Vd_max	Maximum differential input signal for linear mode			40	mVpp
Vm_max	Maximum single-ended input signal for linear mode			40	mVpp

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Electrical Characteristics

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
P	Power consumption	1030	1150	1260	mW
G	Single-ended small signal gain	22	23		dB
	Gain control dynamic range		20		dB
B3dB	3 dB bandwidth	9	10		GHz
RLin	Input return loss (up to 10 GHz)	12	20		dB
RLout	Output return loss (up to 10 GHz)	10	15		dB
Voutdc	Output DC voltage (DC coupled to 50 ohm load)		0		mV
P1dB	Output power at 1-dB gain compression Frequency 2 GHz, maximum gain setting	4.5	5.5		dBm
Psat	Saturated output power Frequency 2 GHz, maximum gain setting	6	7		dBm
IP3O	3rd-order output intercept point Frequency 2 GHz, maximum gain setting	15	16		dBm
THD	Total harmonic distortion (up to 10 GHz, Pout = 0 dBm) Single-ended output Differential output			-34 -42	dBm dBm
Trse	Rise time (20% - 80%)		36	39	ps
Tfse	Fall time (20% - 80%)		37	39	ps
Jrms	Jitter degradation		0.7	1	ps
	Overshoot (Bit rate = 10 Gb/s, maximum gain setting)			6	%
CMRR	Common-mode rejection ratio (up to 10 GHz))	25			dB

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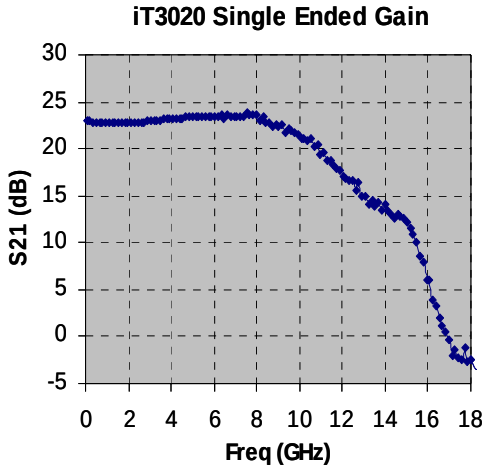
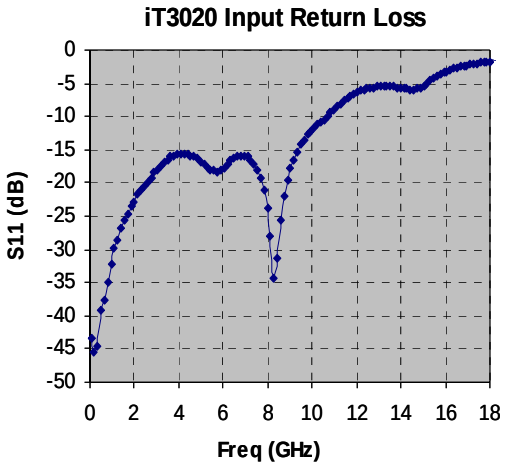
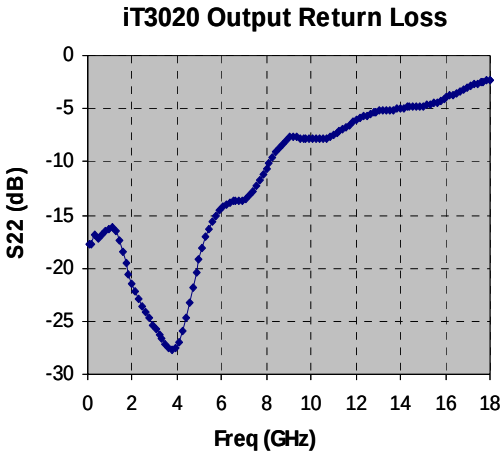
S-Parameter Data

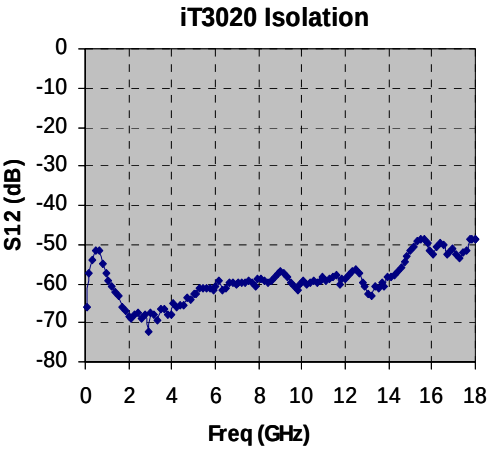
(Measured on connectorized evaluation board)

Vee = -5 V, Vcc = 5 V
Iee = 156 mA, Icc = 74 mA
Vgc = 0 V, 10.2 mA
Vsh = 0 V, 21.8 mA





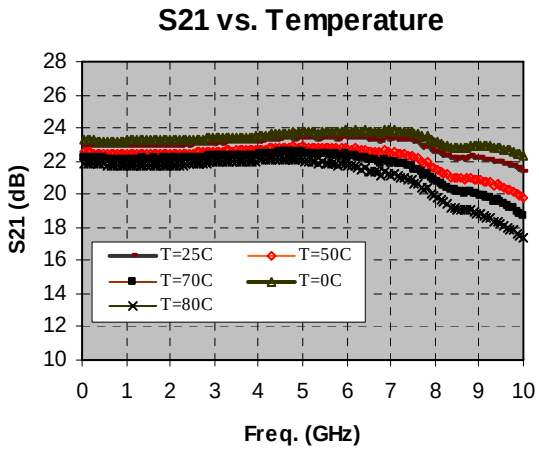




S21 Versus Temperature 0 to 80 °C

(Measured on connectorized evaluation board)

Vee = -5 V, Vcc = 5 V
Iee = 156 mA, Icc = 74 mA
Vgc = 0 V, 10.2 mA
Vsh = 0 V, 21.8 mA



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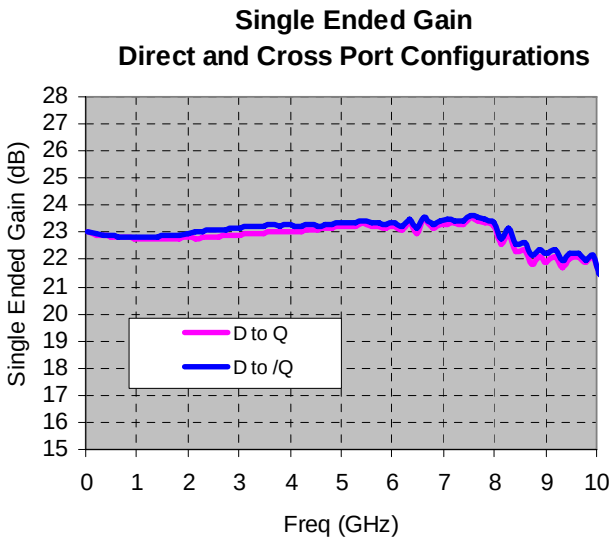
Single-Ended Gain in Direct and Cross Port Configurations

(Measured on connectorized Evaluation board)

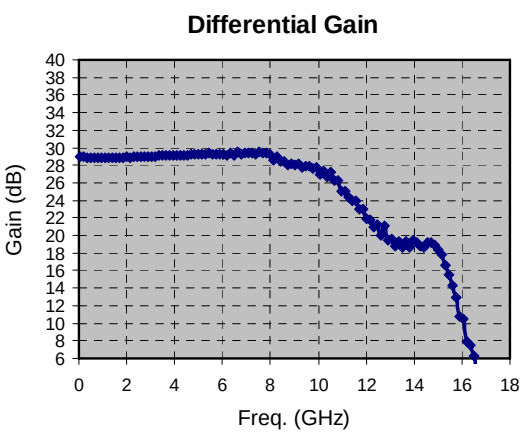
Vee =-5 V, Vcc = 5 V
Iee = 156 mA, Icc = 74 mA
Vgc = 0 V, 10.2 mA
Vsh = 0 V, 21.8 mA

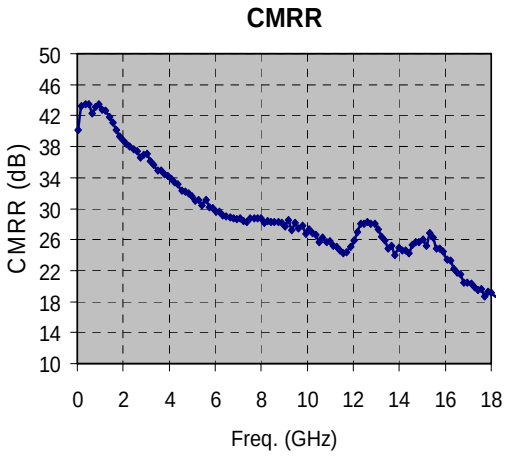


Differential Gain and CMRR

Measured on connectorized Evaluation board)

Vee = -5 V, Vcc = 5 V
Iee = 156 mA, Icc = 74 mA
Vgc = 0 V, 10.2 mA
Vsh = 0 V, 21.8 mA





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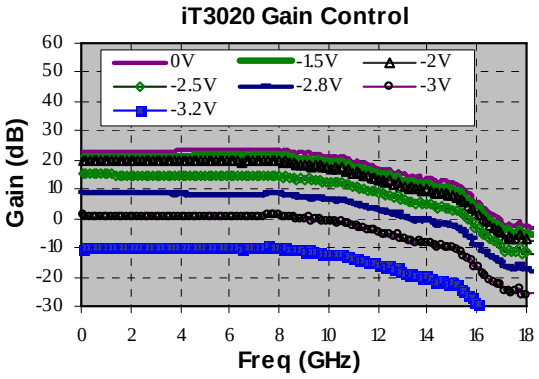
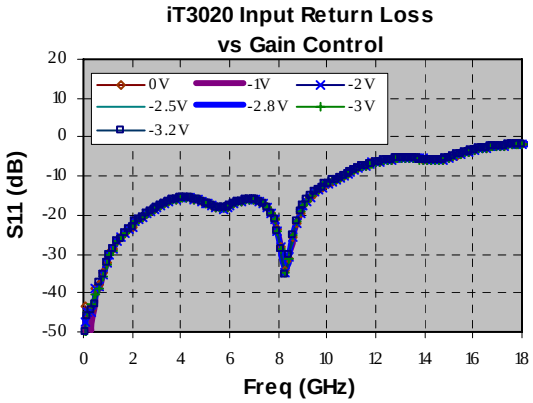
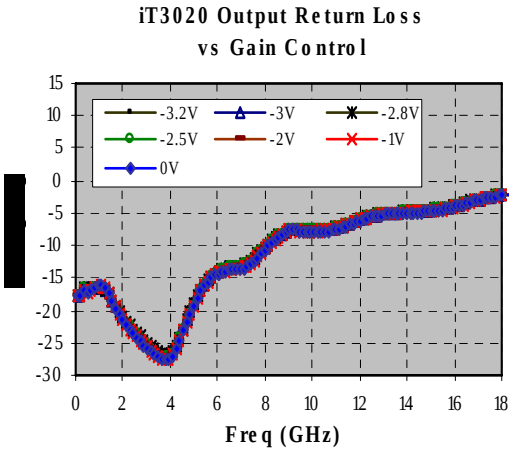
S-Parameter Data, Varying Vgc (Gain Control)

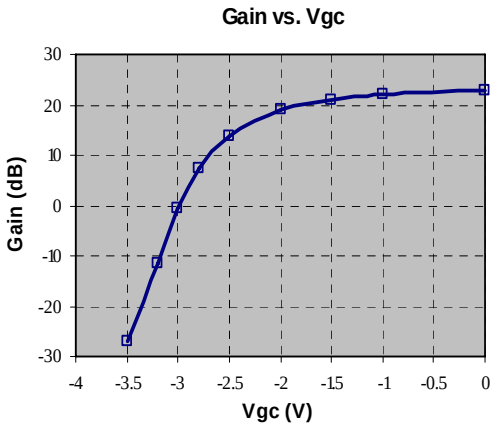
(Measured on connectorized Evaluation board)

Vee =-5 V, Vcc = 5 V
Iee = 156 mA, Icc = 74 mA









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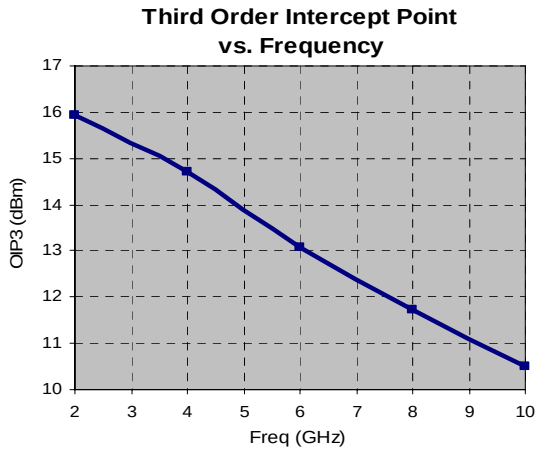
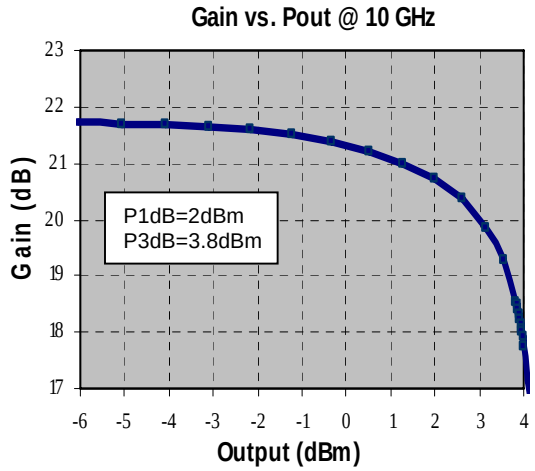
Third Order Intercept Point Versus Frequency

Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA



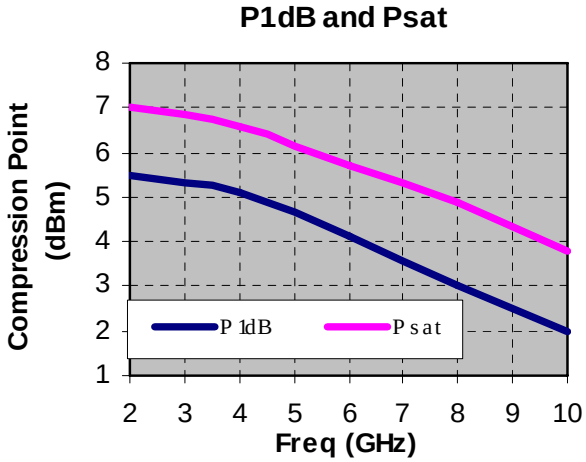
Gain Versus Output power At 10 GHz

Vee =-5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA



P1dB and Psat

Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA



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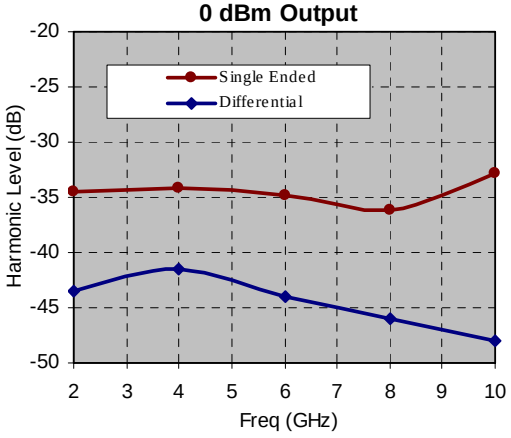
(a) Total Harmonic Distortion at 0 dBm Single-Ended/ Differential

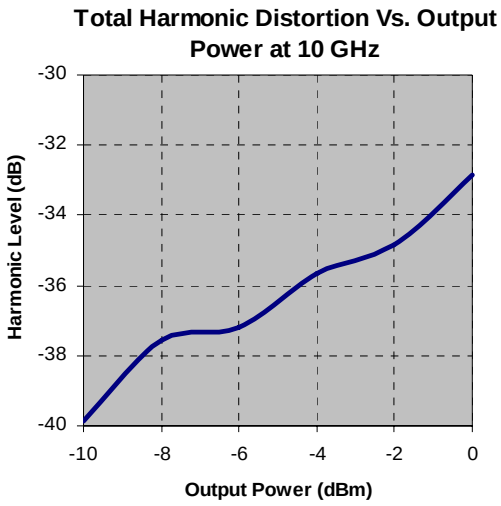
Vee =-5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA

(b) Total Harmonic Distortion Versus Output Power At 10 GHz

Vee =-5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA



(a)



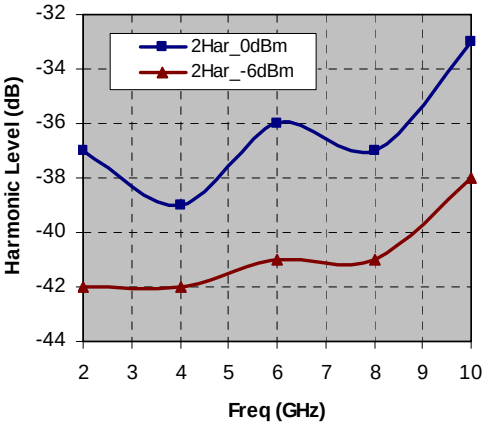
(b)

(a) Second Harmonic Versus Frequency At 0 and -6 dBm

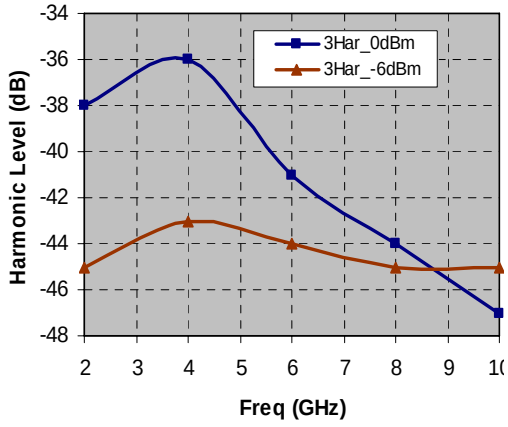
Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA

(b) Third Harmonic Versus Frequency At 0 and -6 dBm

Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA



(a)



(b)

*Differential THD is estimated from single-ended measurement. It is assumed to be equal to the third harmonic level at -3 dBm power output

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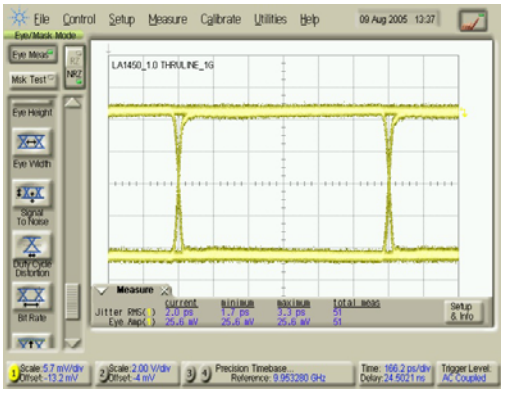
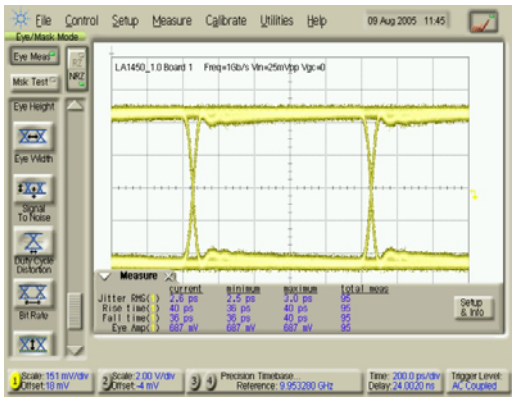
Eye Diagram Performance Versus Bit Rates

Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA
Vin = 25 mV pp, Vgc = 0 V

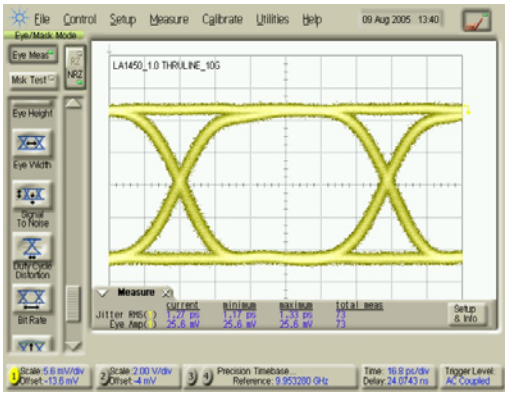
Differential input and DC coupled



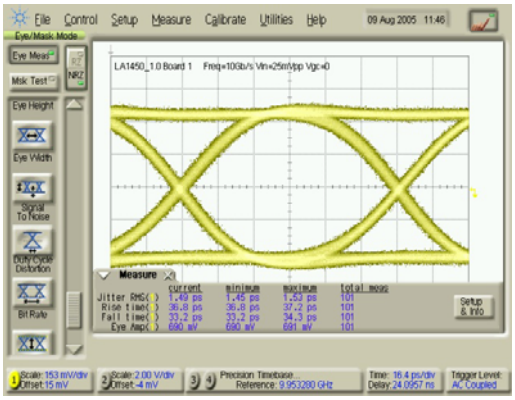
Bit rate: 1 Gb/s
Through Line



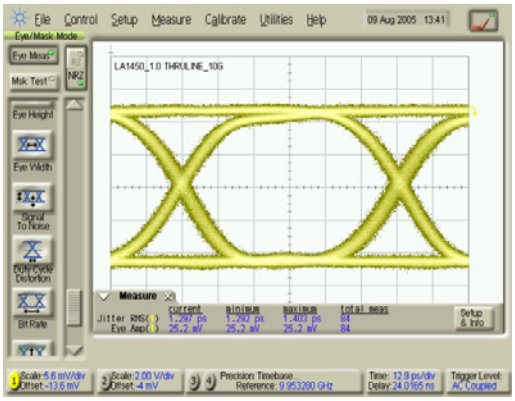
Bit rate: 1 Gb/s
Vout = 687 mVpp, tr = 40 ps, tf = 40 ps



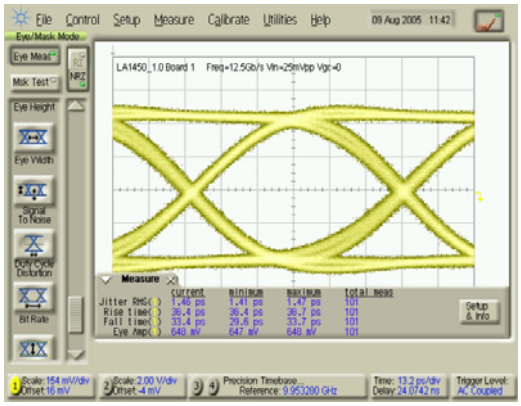
Bit rate: 10 Gb/s
Through Line



Bit rate: 10 Gb/s
Vout = 690 mVpp, tr = 37.2 ps, tf = 34.3 ps



Bit rate: 12.5 Gb/s
Through Line



Bit rate: 12.5 Gb/s
Vout = 648 mVpp, tr = 36.7 ps, tf = 33.7 ps

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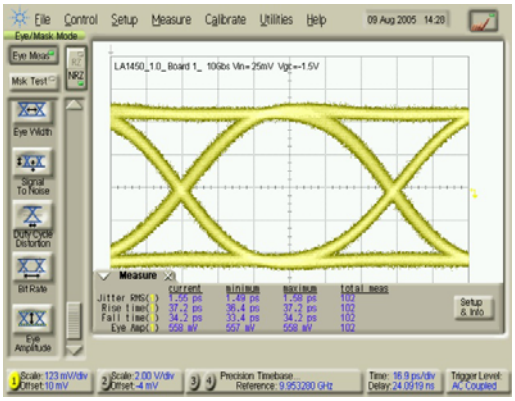
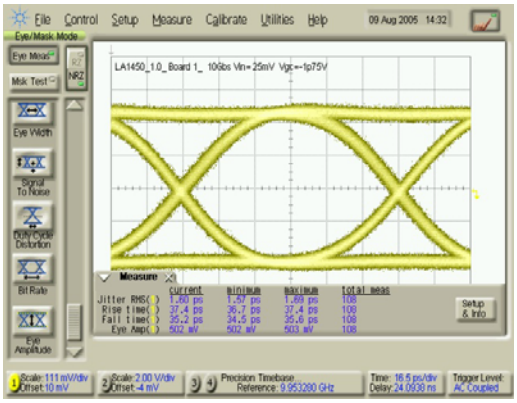
Eye Diagram Performance Versus Vgc

Vee = -5 V, Iee = 156 mA
Vcc =5 V, Icc = 74 mA
Vin = 25 mV pp,
BR = 10 Gb/s

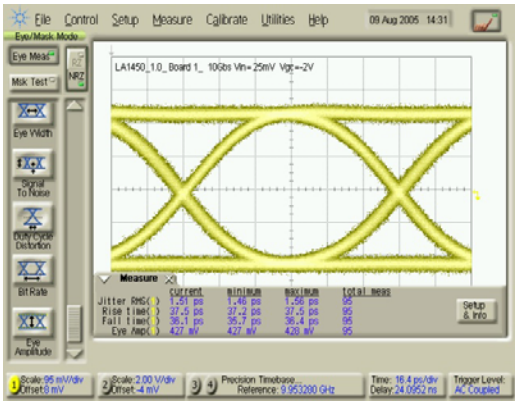
Differential input and
DC coupled



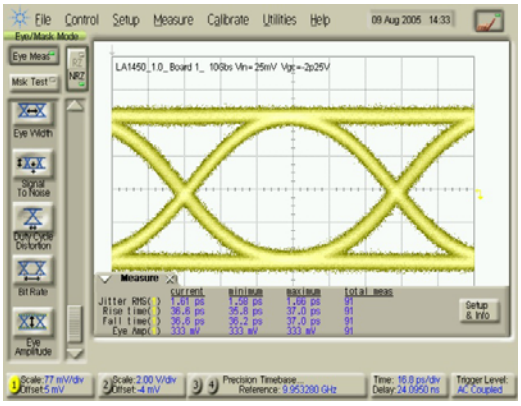
Vgc =-1.5 V
Vout = 558 mV pp, tr = 37.2 ps, tf = 34.2 ps



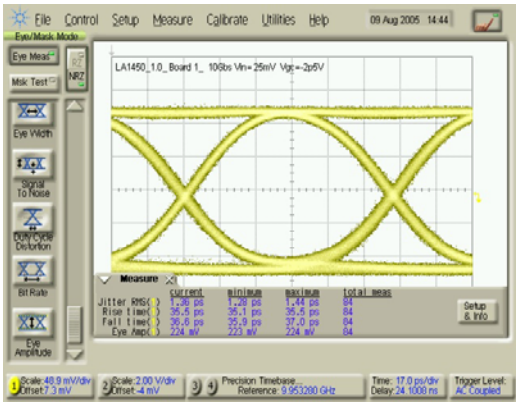
Vgc = -1.75 V
Vout = 503 mVpp, tr = 37.4 ps, tf = 35.6 ps



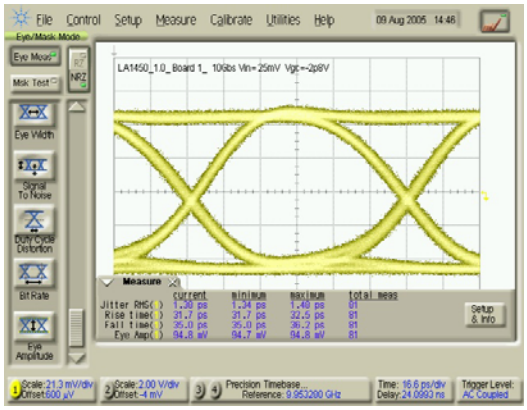
Vgc =-2 V
Vout = 428 mV pp, tr = 37.5 ps, tf = 36.4 ps



Vgc = -2.25 V
Vout = 333 mVpp, tr = 37 ps, tf = 37 ps



Vgc =-2.5 V
Vout = 224 mV pp, tr = 35.5 ps, tf = 37 ps



Vgc =-2.8 V
Vout = 94.8 mV pp, tr = 32.5 ps, 36.2 ps

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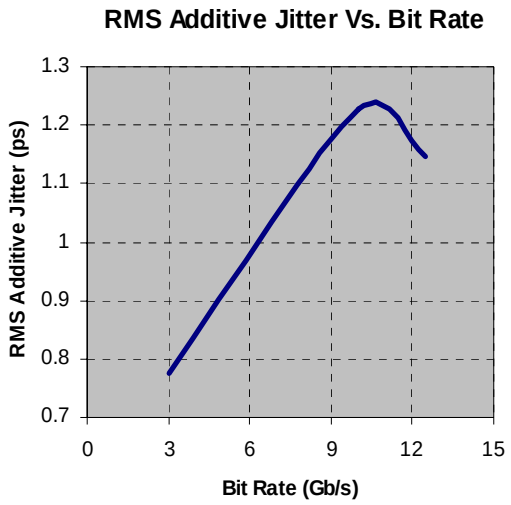
(a) RMS Additive Jitter Versus Bit Rate at Maximum Gain

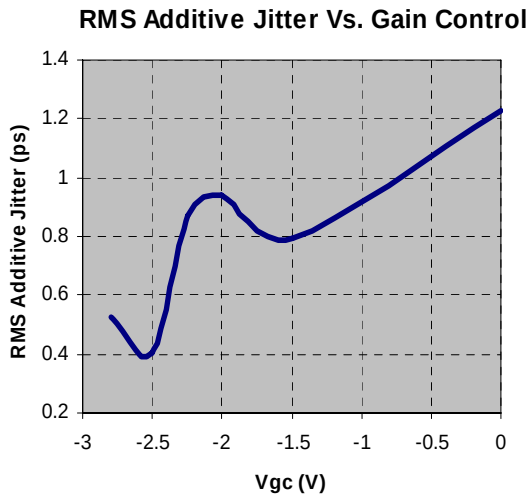
Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA
Vin = 25 mV pp, Vgc = 0 V

(b) RMS Additive Jitter Versus Gain Control At 10 Gb/s

Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA
Vin = 25 mV pp



(a)



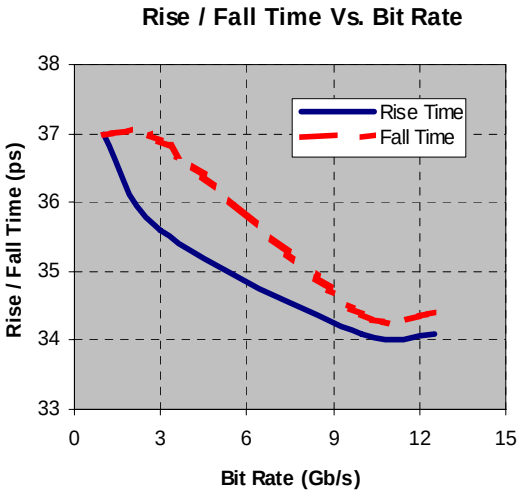
(b)

(a) Rise / Fall Time Versus Bit Rate at Maximum Gain

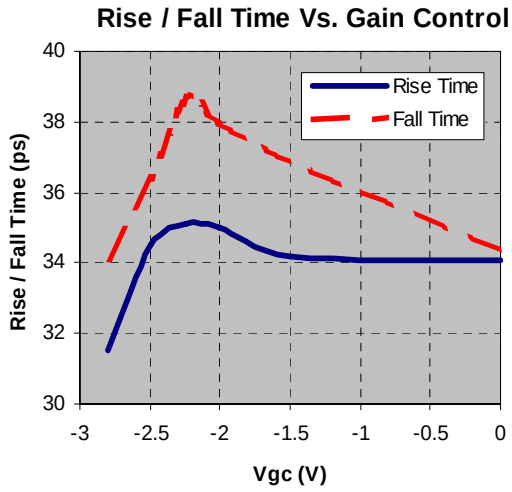
Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA
Vin = 25 mV pp, Vgc = 0 V

(b) Rise / Fall Time Versus Gain Control At 10 Gb/s

Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA
Vin = 25 mV pp



(a)



(b)

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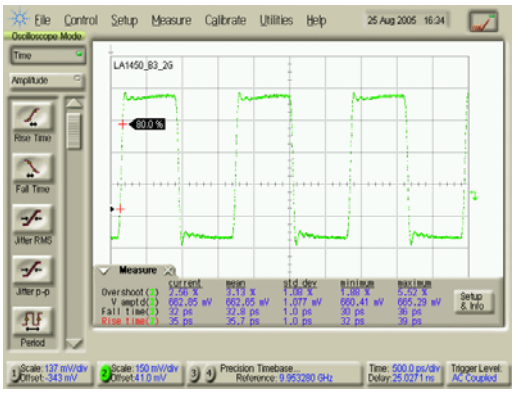
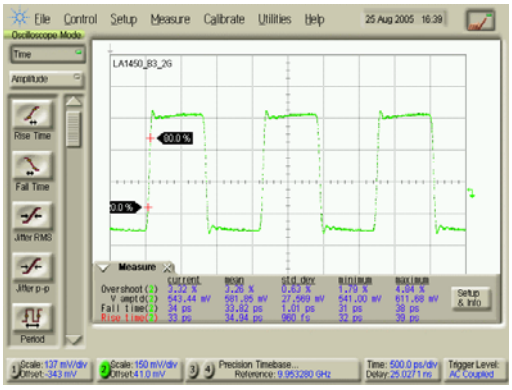
Square Wave Performance Varying Vgc At 5 Gb/s

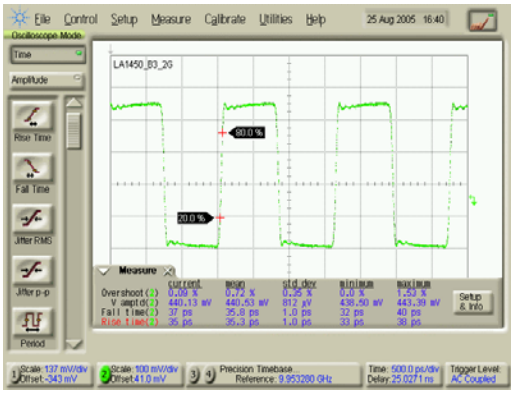
Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA
Vin = 25 mV pp



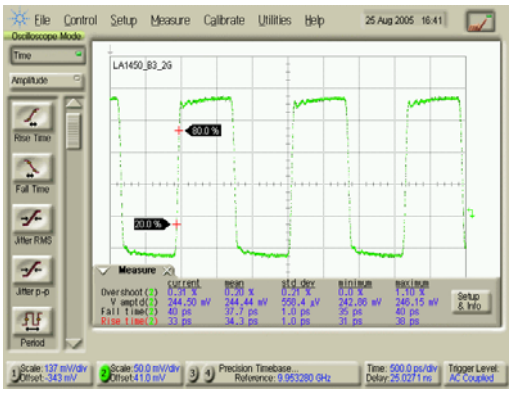
Vgc =0 V
Vout = 662.7 mV pp, Overshoot = 3.1 %



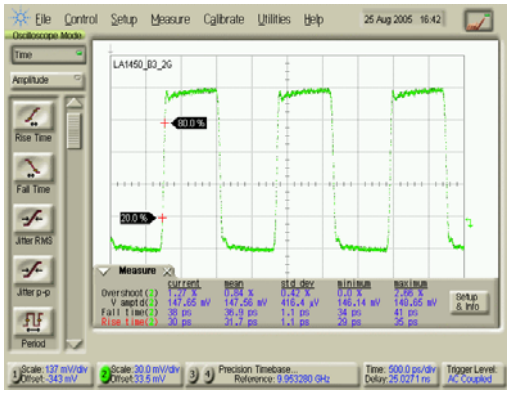
Vgc = -1.5 V
Vout = 581.9 mVpp, Overshoot = 3.26 %



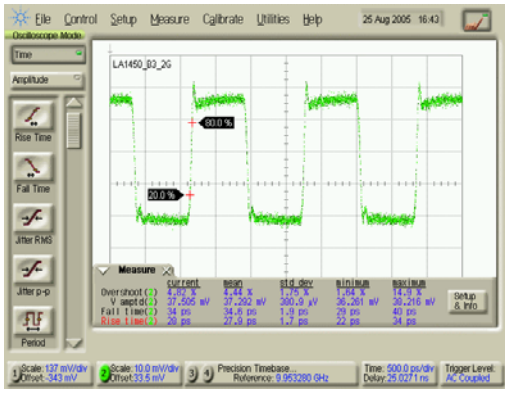
Vgc = -2 V
Vout = 440.5 mVpp, Overshoot = 0.72 %



Vgc = -2.5 V
Vout = 244.4 mVpp, Overshoot = 0.2 %



Vgc = -2.7 V
Vout = 147.6 mVpp, Overshoot = 0.84 %



Vgc = -3 V
Vout = 37.3 mVpp, Overshoot = 4.44 %

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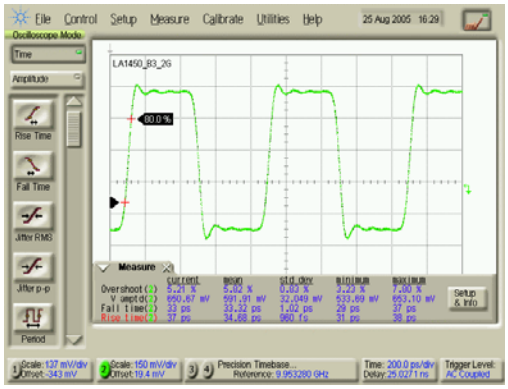
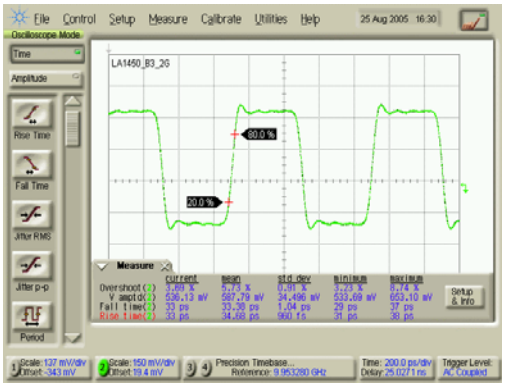
Square Wave Performance Varying Vgc At 10 Gb/s

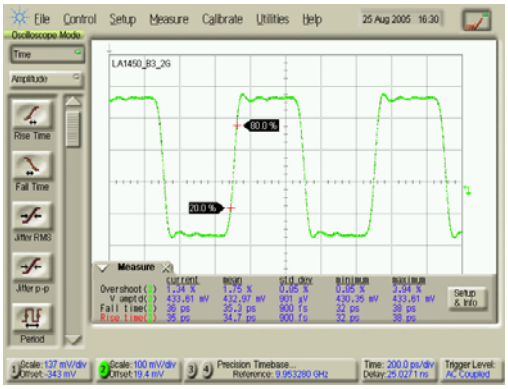
Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA
Vin = 25 mV pp



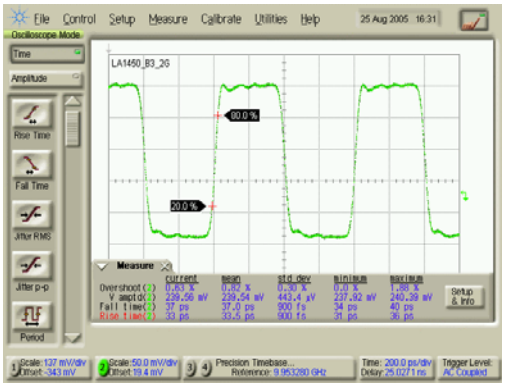
Vgc =0 V
Vout = 591.9 mV pp, Overshoot = 5.82 %



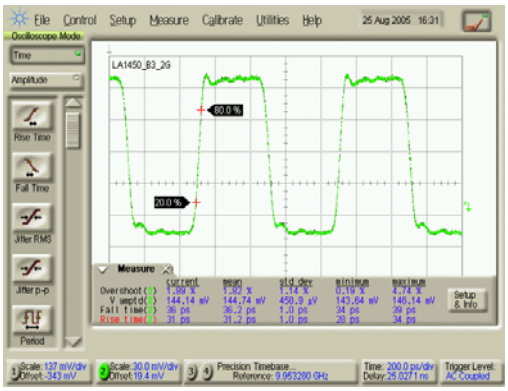
Vgc = -1.5 V
Vout = 587.8 mVpp, Overshoot = 5.73 %



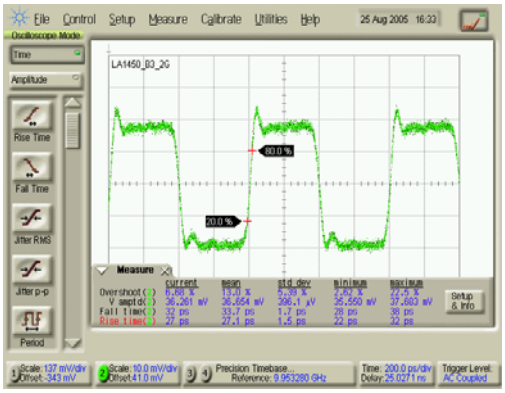
Vgc = -2 V
Vout = 433 mVpp, Overshoot = 1.75 %



Vgc = -2.5 V
Vout = 239.5 mVpp, Overshoot = 0. 82 %



Vgc = -2.7 V
Vout = 144.7 mVpp, Overshoot = 1.82 %



Vgc = -3 V
Vout = 36.7 mVpp, Overshoot = 13.0 %

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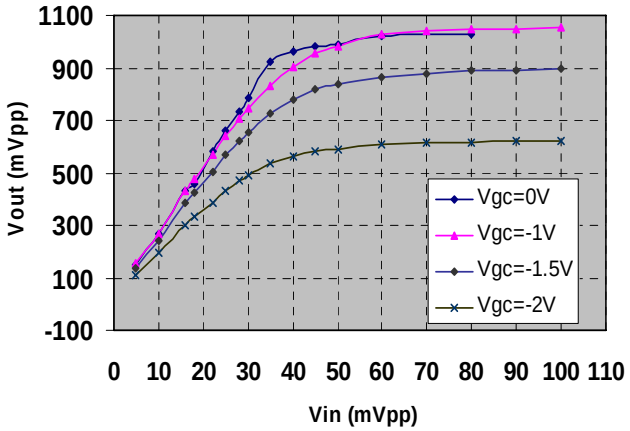
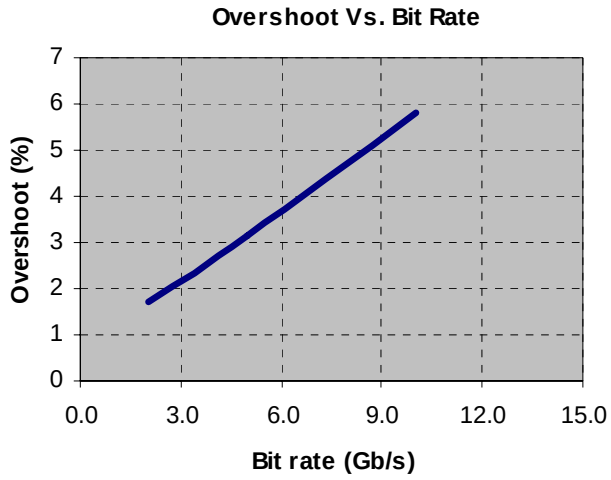
Performance as Function of Input Voltage

Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA



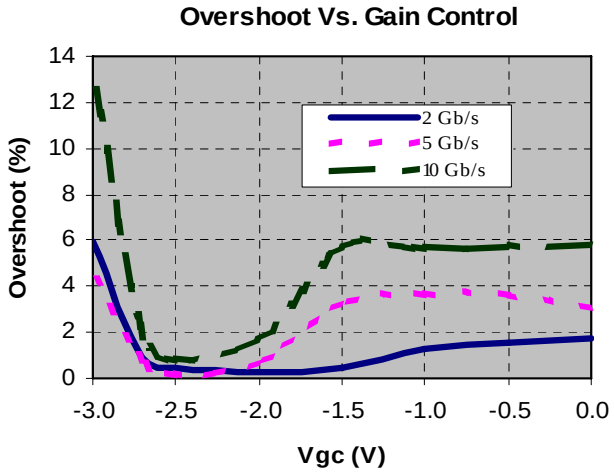
Overshoot Versus Bit Rate at Maximum Gain

Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA
Vin = 25 mV pp, Vgc = 0 V



Overshoot Versus Gain Control At 2, 5 and 10 Gb/s

Vee = -5 V, Iee = 156 mA
Vcc = 5 V, Icc = 74 mA
Vin = 25 mV pp



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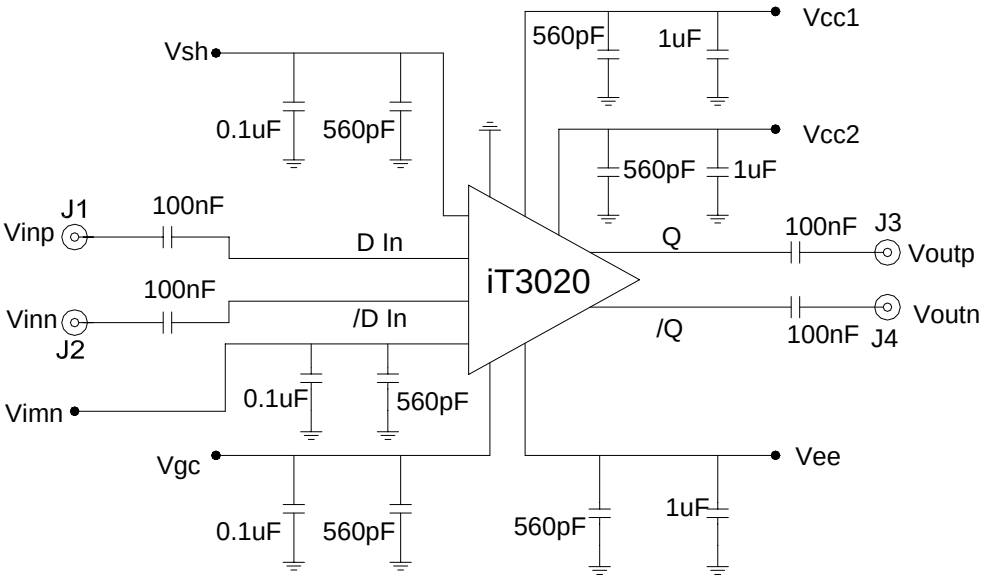
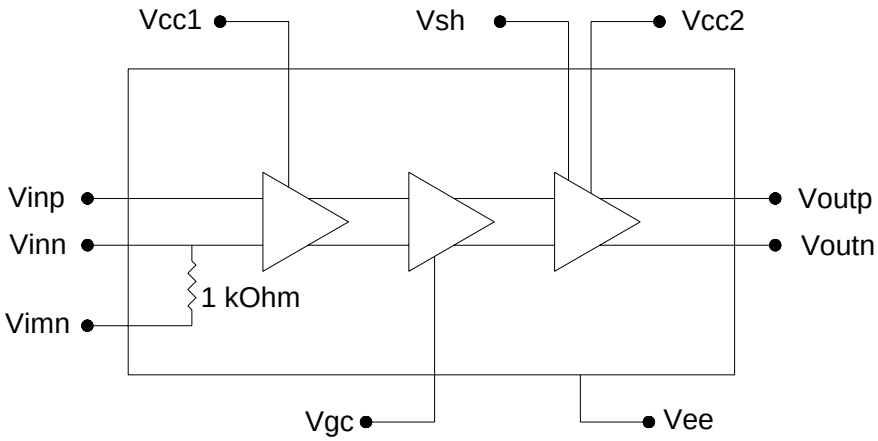
Recommended Operational Setup

Apply –5 V at Vee,
+5 V at Vcc
Apply 0 V at Vsh
and Vgc for
maximum output

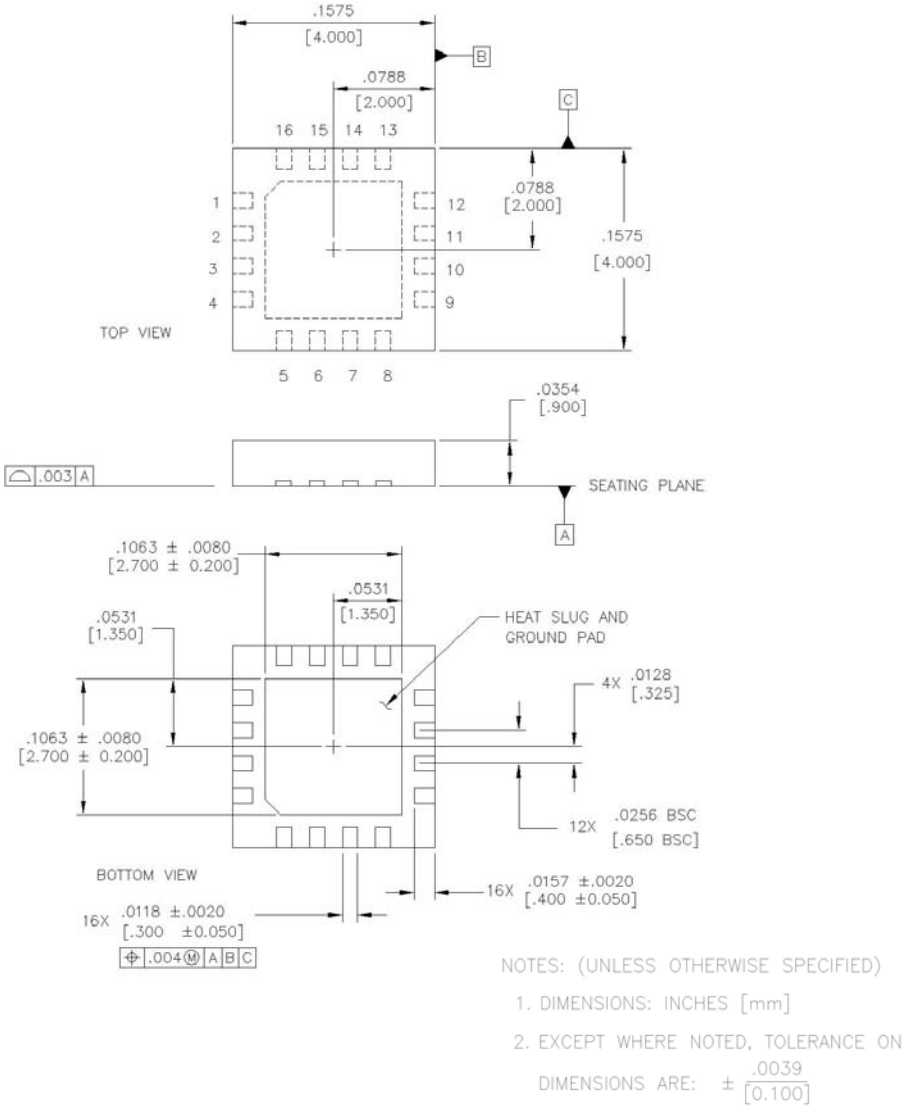
DC blocking
capacitors optional



Device System Diagram



Package Drawings, Pinouts



Pinouts:

P1: Gnd
P2: Vinp (RF input)
P3: Vinn (/RF input)
P4: Gnd
P5: Vgc (Gain control)
P6: Vee (Negative supply)
P7: N/C
P8: N/C
P9: Gnd
P10: Voutp (/RF out)
P11: Voutn (RF out)
P12: Gnd
P13: Vcc2 (positive supply)
P14: Vsh (shutoff control)
P15: Vcc1 (positive supply)
P16: Vimn (input offset control)

Biasing Procedures:

Apply power supply
in the following order:

1. Vgc
2. Vsh
3. Vcc-1&2
4. Vee

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