SG320240E (320 DOTS X 240 DOTS)

FEATURES

- NO BUIT-IN CONTROLLER
- +3.3V POWER SUPPLY
- 1/240 DUTY CYCLE
- BUIT-IN ELECTRIC VOLUME
- 4-BIT PARALLEL INTERFACE

MECHANICAL DATA

ITEM	DIMENSIONS	UNIT
Module Size (W x H x T)	109.0 x 70.25 x 7.9	mm
Viewing Area (W x H)	78.8 x 59.6	mm
Active Area (W x H)	76.79 x 57.59	mm
Dot Size (W x H)	0.23 x 0.23	mm
Dot Pitch (W x H)	0.24 x 0.24	mm

INTERFACE PIN CONNECTIONS

NO.	SYMBOL	LEVEL	FUNCTION
1	VDIN	H/L	Electric Volume data input pin.
2	VCLK	H/L	Electric Volume data input pin.
3	VSTRB	H/L	Electric Volume data input pin.
4	V_{DD}	3.3V	Power Supply Voltage
5	FLM	H/L	Frame start signal
6	V_{SS}	0V	Power Supply Ground
7	CL1	H/ L	Common Driver Data Shift Signal
8	V_{SS}	0V	Power Supply Ground
9	M	H/L	Control Signal For AC Driving
10	/D-OFF	H/L	Display OFF. Active LOW.
11	CL2	H→L	Common Driver Data Shift Signal
12～13	NC	-	No Connection.
14～17	DB3～DB0	H/L	Data Bus Line
18～22	FGND	-	Frame Ground
23	V_{DD}	3.3V	Logic supply voltage
24	/EL_ON	H	EL/LED Backlight Signal

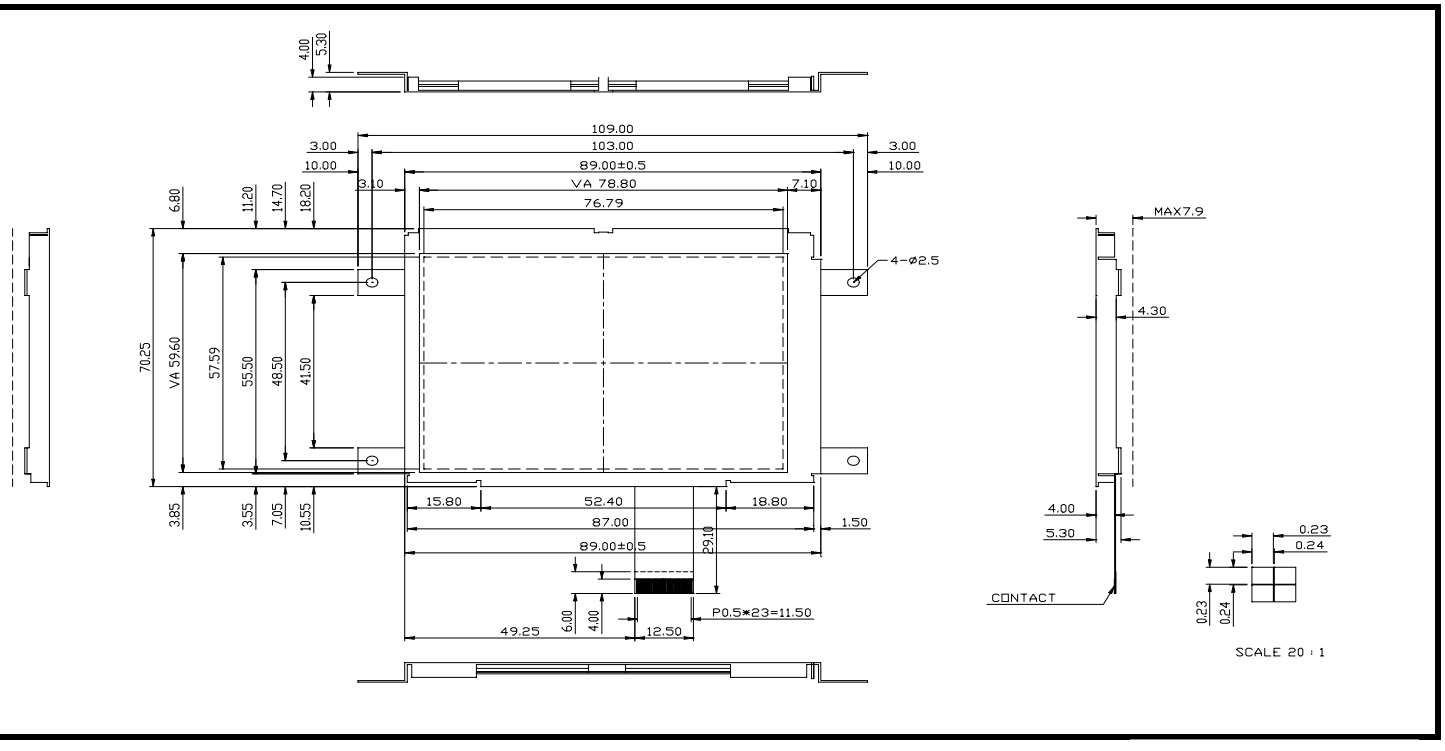
ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage For Logic	V_{DD}-V_{SS}	0	-	7	V
Supply Voltage For LCD Drive	V_{DD}-V_o	0	-	30	V
Input Voltage	V_I	Vss	-	V_{DD}	V

ELECTRICAL CHARACTERISTICS

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage For Logic		V_{DD}-V_{SS}	-	2.7	3.3	4.5	V
LCD Supply Voltage		V_{DD}-V_o	VDD=3.3V Ta=25℃	19.8	21.0	22.3	V
Supply Current		I_{DD}	V_{DD}=3.3V	-	4.5	6.5	mA
Input Voltage	"HIGH" Level	V_{IH}	-	2.2	-	VDD	V
	"LOW" Level	V_{IL}	-	-	-	0.6	V
Output Voltage	"HIGH" Level	V_{OH}	-	2.4	-	-	V
	"LOW" Level	V_{OL}	-	-	-	0.4	V

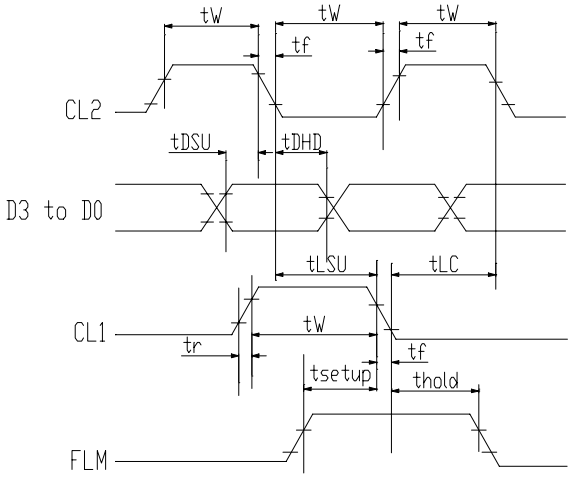
EXTERNAL DIMENSIONS

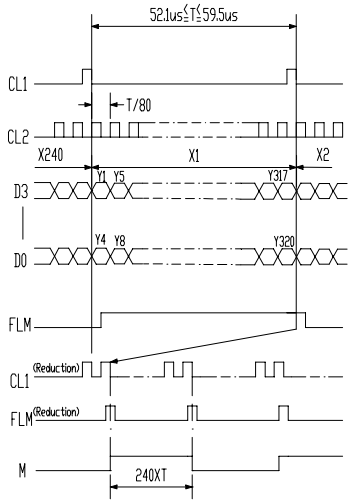


SG320240E (320 DOTS X 240 DOTS)

■ TIMING CHARACTERISTICS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT.
Frequency Of Maximum Clock	f_{CP}	-	-	8	MHZ
CL1 , CL2 , Pulse Width	t_W	45	-	-	ns
Rise , Fall Time	t_r , t_f	-	-	15	ns
Data Setup Time	t_{DSU}	20	-	-	ns
Data Hold Time	t_{DHD}	20	-	-	ns
CL1 Setup Time	t_{LSU}	80	-	-	ns
CL1→ CL2 Time	t_{LC}	80	-	-	ns
FLM Setup Time	t_{setup}	100	-	-	ns
FLM Hold Time	t_{hold}	100	-	-	ns
M Delay Time	t_{DF}	-	-	300	ns





■ BLOCK DIAGRAM