

VA2708

**DUAL HIGH-SPEED, FAST-SETTLING,
HIGH OUTPUT CURRENT
OPERATIONAL AMPLIFIER, $A_{CL} \geq 3$**

T-79-07-20

FEATURES

- Fast Settling Time: $\pm 0.1\%$ in 150ns
- High Slew Rate: 90V/ μ s
- Large Gain-Bandwidth: 100MHz
- Full Power Bandwidth: 4.8MHz at 6V p-p
- Ease Of Use: Internally Compensated for $A_{CL} \geq 3$ with 50° - 60° Phase Margin
- Large Output Current: ± 50 mA
- Low Supply Voltage Operation: ± 4 V
- Minimal Crosstalk: >90dB Separation
- Short Circuit Protection
- Available In Commercial and Military Versions

DESCRIPTION

The VA2708 offers the high-speed and fast-settling advantages of the VA708 in a dual package configuration. The high slew rate, output drive and open-loop gain allows the amplifier to fit analog amplification and high-speed processing applications capable of driving large capacitance loads at high speeds.

The VA2708 is offered in an 8-pin CERDIP, plastic or metal can package, as well as a 20-pin LCC.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages ± 6 V
 Differential Input Voltage ± 9 V
 Common Mode Input Voltage $|V_S| - 0.5$ V
 Power Dissipation (Note 1) 450mW
 Output Short Circuit Current Duration (Note 2) Indefinite
 Operating Temperature Range:

Commercial (2708 J, K) 0° to 70°C
 Military (2708 S) -55° to +125°C

Storage Temperature Range -65° to +150°C
 Lead Temp. Range (Soldering to 60 Sec.) 300°C

Note 1: Power derating above $T_A = 70^\circ\text{C}$ to be based on a maximum junction temperature of 150°C and the following thermal resistance factors:

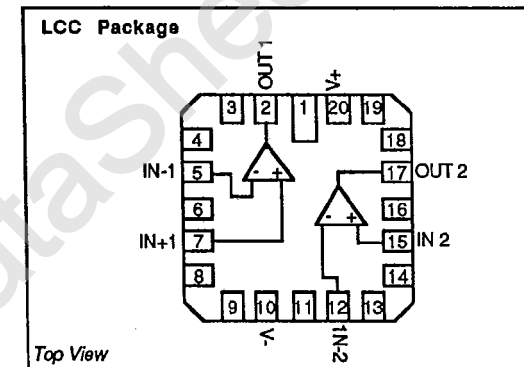
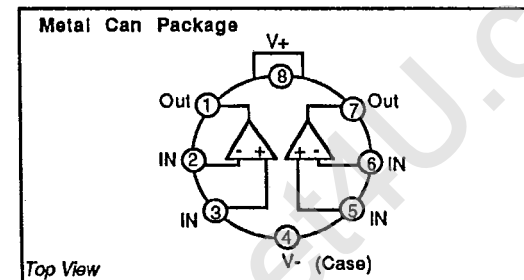
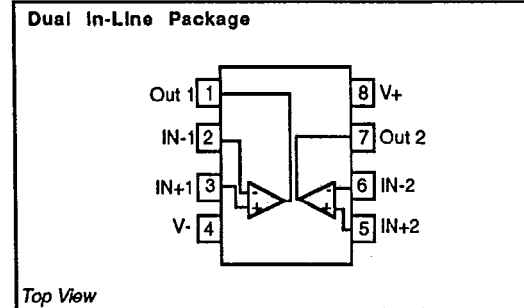
PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)
DIP	75	180
TO-99	115	250

Note 2: Continuous short circuit protection is allowed on one amplifier per time up to the following case and ambient temperatures:

PACKAGE	T_C (°C)	T_A (°C)
DIP	100	30
TO-99	75	(Note 3)

Note 3: Long duration shorts (>5 sec) will result in junction temperature exceeding 150°C which may result in part damage.

CONNECTION DIAGRAMS



PACKAGE TYPES AVAILABLE

- 8-Pin Plastic DIP
- 8-Pin CERDIP
- 8-Pin Metal Can, TO-99
- 20-Pin LCC

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ELECTRICAL CHARACTERISTICS ($V_S = \pm 5V$, $T_A = 25^\circ C$ unless otherwise stated) (each amplifier)

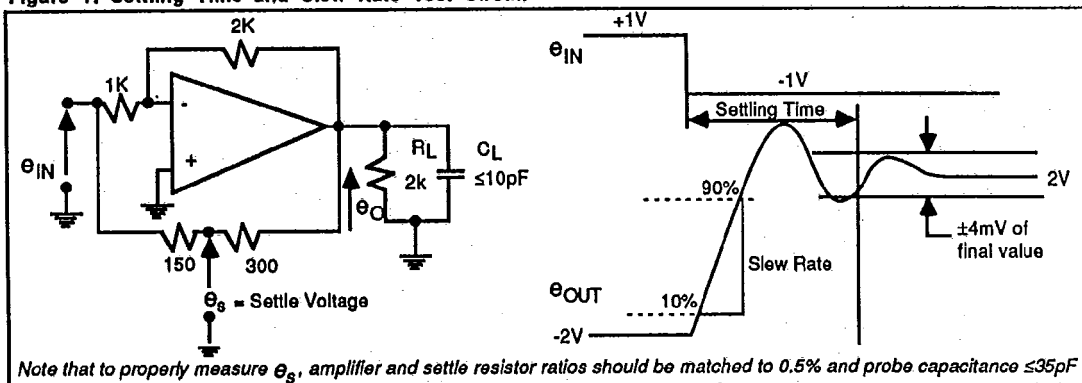
PARAMETER	SYMBOL	CONDITIONS	VA2708J			VA2708K			VA2708S			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage T_{Min} to T_{Max}	V_{OS}			5	12		3	6		3	6	mV
		$0^\circ \leq T_A \leq 70^\circ C$		8	16		5	10				
		$-55 \leq T_A \leq 125^\circ C$								6	12	
Average Offset Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	$0^\circ \leq T_A \leq 70^\circ C$		20			20					$\mu V/^\circ C$
		$-55 \leq T_A \leq 125^\circ C$								15		
Input Bias Current T_{Min} to T_{Max}	I_B			650	1100		650	1100		650	1100	nA
		$0^\circ \leq T_A \leq 70^\circ C$			1700			1700				
		$-55 \leq T_A \leq 125^\circ C$									2200	
Input Offset Current	I_{OS}			35	120		35	120		35	120	nA
Input Common Mode Range	V_{CM}		+3 -4	+3.5 -4.5		+3 -4	+3.5 -4.5		+3 -4	+3.5 -4.5		V
Differential Input Resistance	R_{IND}	(Note 1)	3	10		3	10		3	10		$M\Omega$
Common Mode Input Resistance	R_{INC}	(Note 1)	4	8		4	8		4	8		$M\Omega$
Differential Input Capacitance	C_{IND}	(Note 1)		2						2		pF
Common Mode Input Capacitance	C_{INC}	(Note 1)		3			3			3		pF
Input Voltage Noise	e_N	BW = 10Hz to 100KHz		12			12			12		$\mu VRMS$
Open Loop Voltage Gain	A_V	$V_{OUT} = \pm 3V$ $R_L = 2k\Omega$	2	5		5	10		5	10		V/mV
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	± 3.5			± 3.5			± 3.5			V
		$R_L = 51\Omega$	± 2.0	± 2.4		± 2.5	± 2.7		± 2.5	± 2.7		
Power Supply Current (Both Amplifiers)	I_S			15	20		15	20		15	20	mA
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2V$	60	70		60	70		60	70		dB
Power Supply Rejection Ratio	PSRR	$\Delta V_{PS} = \pm 0.5V$	60	66		60	66		60	66		dB
Slew Rate	SR	10-90% of Leading Edge (Figure 1)	60	90		60	90		60	90		V/ μs
Settling Time	t_S	To $\pm 0.1\%$ ($\pm 4mV$) of Final Value (Figure 1) (Note 1)		150	200		150	200		150	200	ns
Gain Bandwidth Product	GBW			100			100			100		MHz
Small Signal Rise/Fall Time	$t_r \Delta f$	$e_O = \pm 100mV$ 10-90% (Figure 1)		7			7			7		ns
Full Power Bandwidth	BW_{FP}	$R_L = 2k\Omega$ $C_L = 50pF$ $V_{OUT} = 6V_{pp}$		4.8			4.8			4.8		MHz
Amplifier to Amplifier Crosstalk		Input Referenced $f = 10KHz$ (Figure 2)		-96			-96			-96		dB

Notes: 1. Not tested, guaranteed by design.

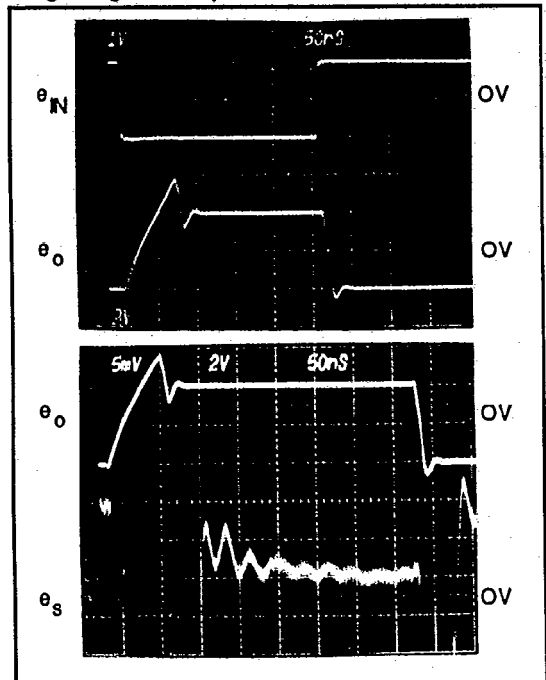
LSP FAMILY DATA SHEETS

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Figure 1: Settling Time and Slow Rate Test Circuit



Large Signal Response



Small Signal Response

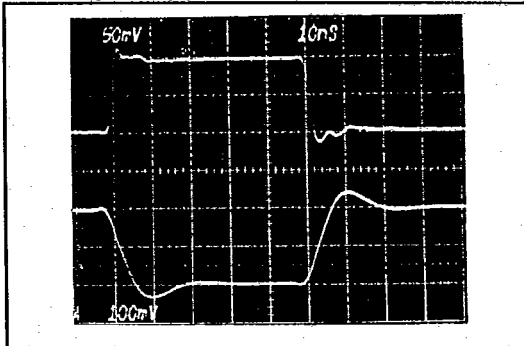
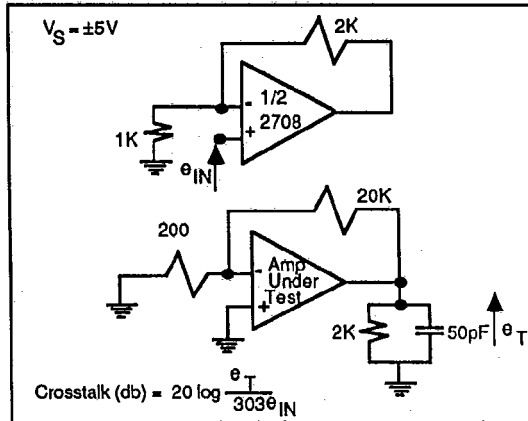


Figure 2: Crosstalk Test Circuit

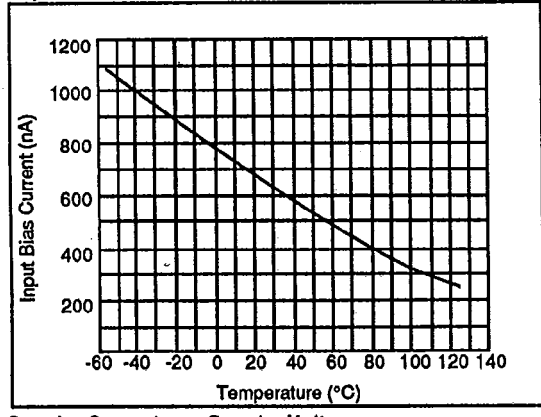


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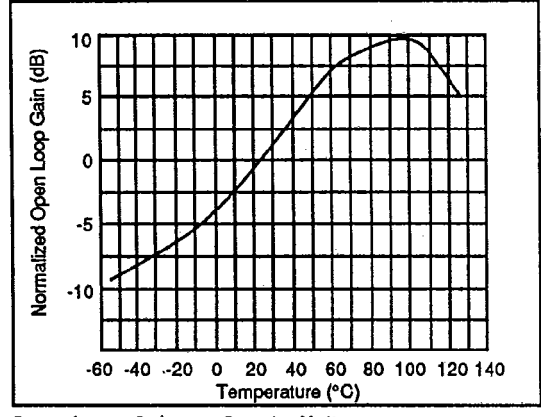
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TYPICAL PERFORMANCE CHARACTERISTICS (V_S= ±5V, T_A= 25°C unless otherwise stated)

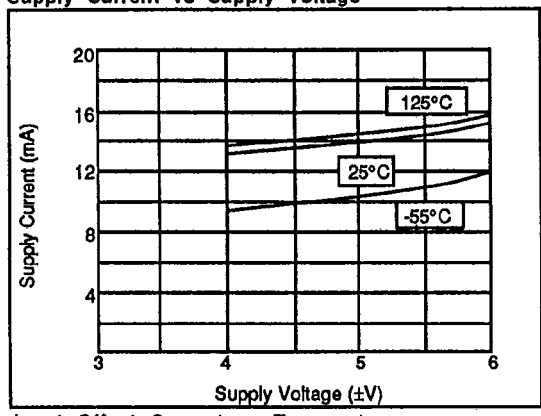
Input Bias Current vs Temperature



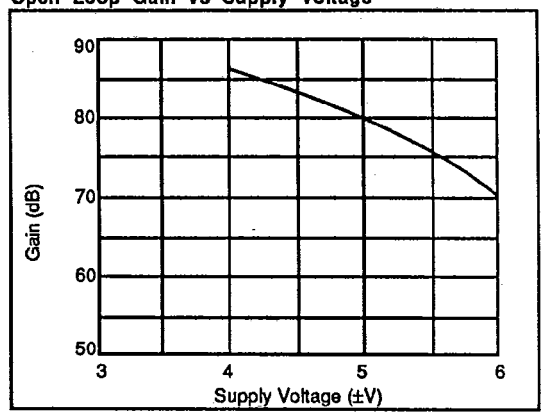
Normalized Open Loop Gain vs Temperature



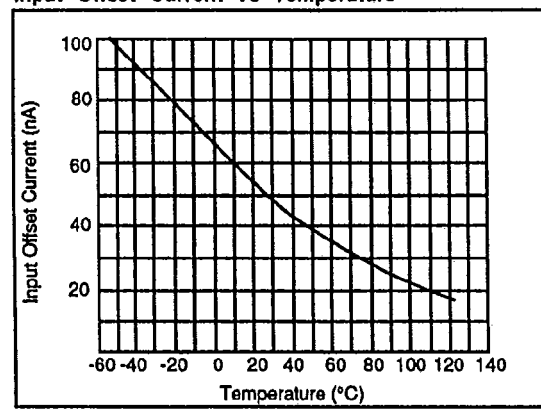
Supply Current vs Supply Voltage



Open Loop Gain vs Supply Voltage



Input Offset Current vs Temperature

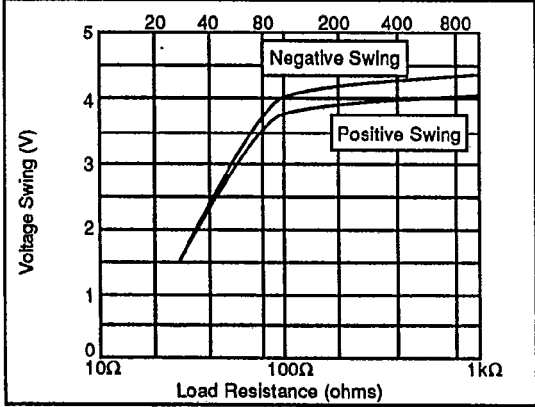


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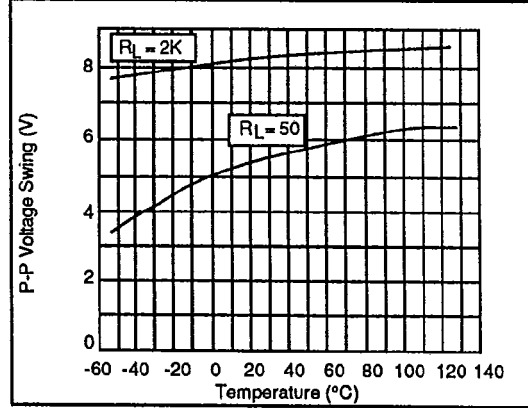
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TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 5V$, $T_A = 25^\circ C$ unless otherwise stated)

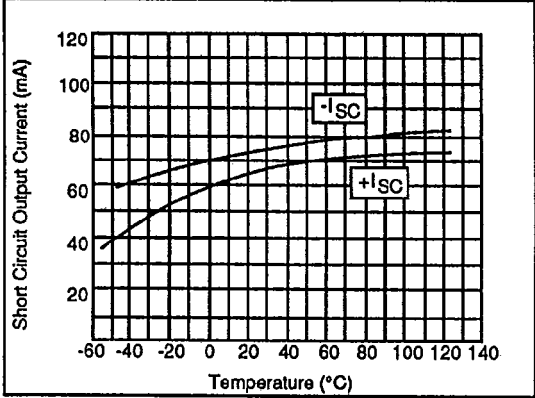
Maximum Output Voltage Swing vs Load Resistance



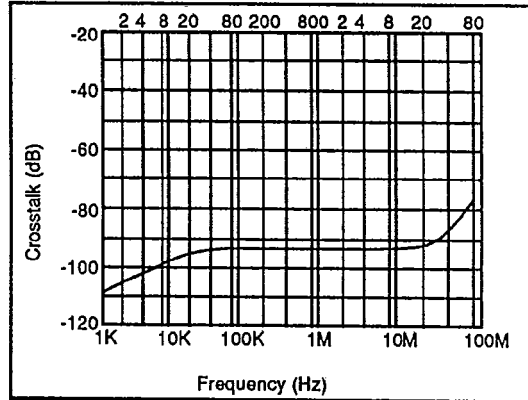
Maximum Output Voltage Swing vs Temperature



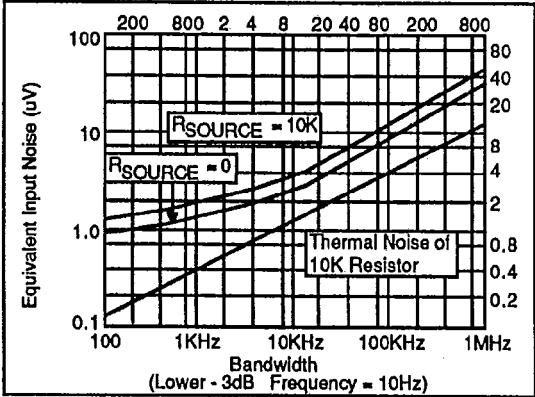
Short Circuit Output Current vs Temperature



Amplifier/Amplifier Crosstalk vs Frequency



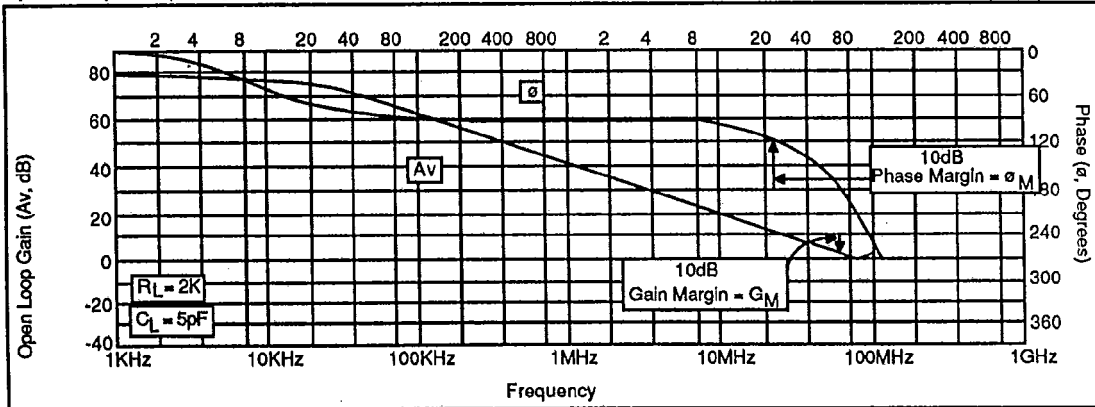
Equivalent Input Noise vs Bandwidth



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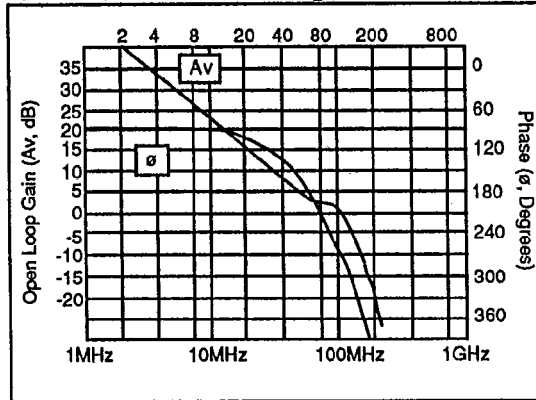
TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 5V$, $T_A = 25^\circ C$ unless otherwise stated)

Open Loop Frequency Response

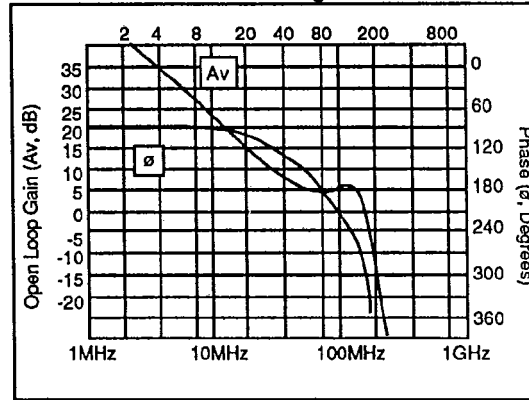


LSP FAMILY DATA SHEETS

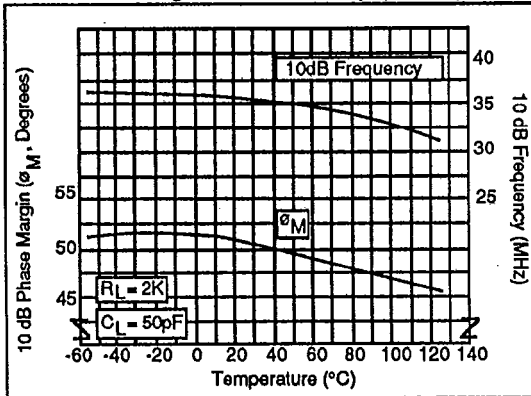
Open Loop Freq. Response, $R_L = 50\Omega$, $C_L = 50pF$



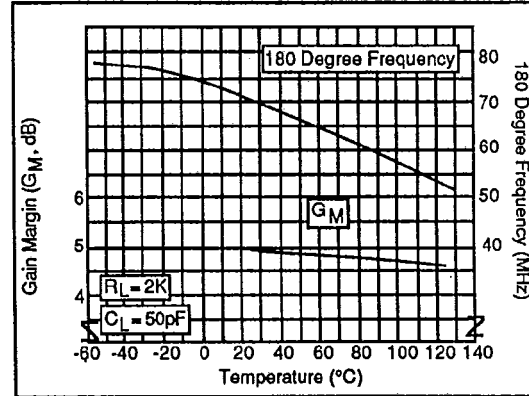
Open Loop Freq. Response, $R_L = 2K\Omega$, $C_L = 50pF$



10dB Phase Margin and 10dB Freq. vs Temp.



Gain Margin and 180 Degree Freq. vs Temp.



APPLICATION INFORMATION

AC Characteristics

The 35MHz 10dB crossover point of the VA2708 is achieved without feed forward compensation, a technique which can produce long tails in the recovery characteristics. The single pole rolloff follows the classic 20dB/decade slope to frequency approaching 50MHz. The 10dB (3.2 V/V) phase margin of 50°, even with a capacitive load of 50pF, gives stable and predictable performance down to non-inverting gain configurations of approximately 3 V/V (inverting gains of -2V/V). At frequencies beyond 50MHz, the 20dB/decade slope is disturbed by an output stage zero, the damping factor of which is dependent upon the R_L, C_L load combination. This results in loss of gain margin (gain at loop phase = 360°) at frequencies of 70 to 100MHz which at a gain margin of 5dB ($R_L = 2K, C_L = 50pF$) results in a peak in the gain of 3 amplifier configurations as shown in Figures 3 and 4.

Figure 3 shows a blow up of the open loop characteristics in the 10MHz to 200MHz frequency range, as well as the corresponding closed loop characteristics for a gain of 3 non-inverting amplifier at similar load conditions. It should be noted that the open loop characteristic does not show the additional phase shift covered by the input capacitance pole — this is why the closed loop peaking at 30 to 40MHz is greater than what would be expected from the 50 to 60 degrees of phase margin indicated by the open loop characteristics. Corresponding small signal step response characteristics show well behaved pulse waveforms with 16-33% overshoot.

The input capacitive pole can be neutralized by adding a feedback capacitor to R_2 . The value of capacitance is selected according to $R_1 C_{IN} = R_2 C_{FB}$, where C_{IN} is the sum of the common mode and differential input capacitance $\approx 5pF$. For $R_2 = 2R_1, C_{FB} = C_{IN}/2 \approx 2.5pF$.

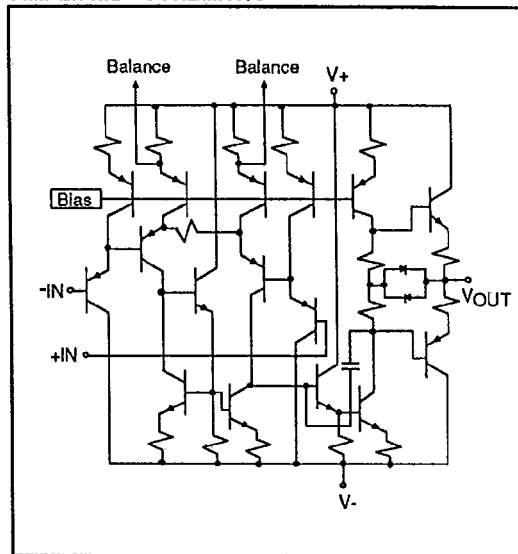
Figure 4 shows the results of this feedback capacitor addition. Neutralizing the input capacitance demonstrates the peaking that can result from the loss of gain margin at 70 to 100MHz. As the load time constant ($R_L C_L$) increases the peaking gets progressively worse $\approx 6dB$ at $R_L = 2K, C_L = 50pF$. The step response waveforms are as expected with a very strong 88MHz ring being exhibited at $R_L = 2K, C_L = 50pF$ and no overshoot at $R_L = 50\Omega, C_L = 5pF$.

Layout Considerations

As with any high-speed wideband amplifier, certain layout considerations are necessary to ensure stable operation. All connections to the amplifier should be kept as short as possible, and the power supplies bypassed with 0.1 μF capacitors to signal ground. It is suggested that a ground plane be considered as the best method for ensuring stability because it minimizes stray inductance and unwanted coupling in the ground signal paths.

To minimize capacitive effects, resistor values should be kept as small as possible, consistent with the application.

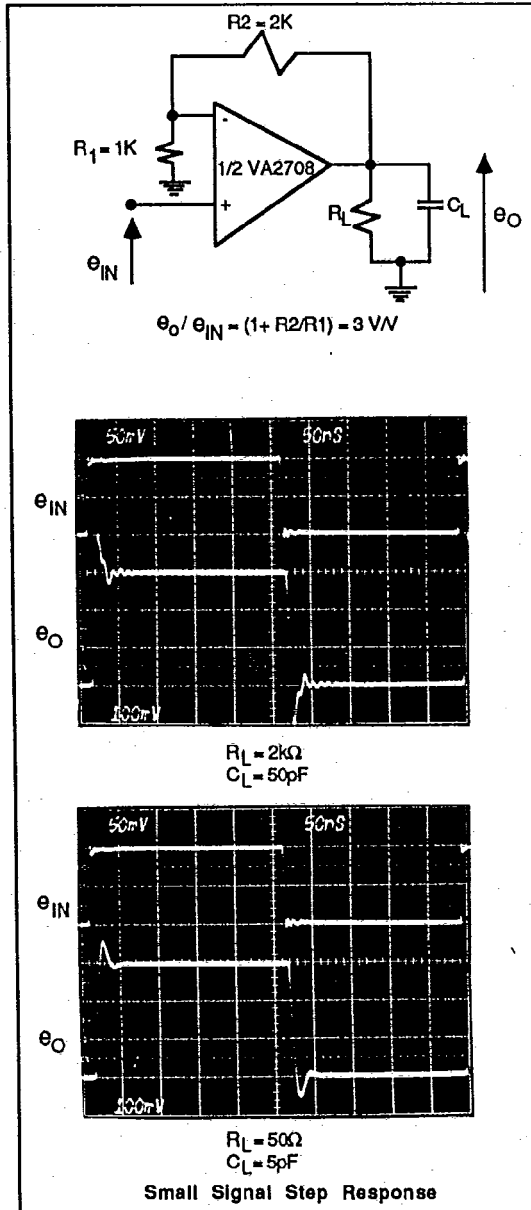
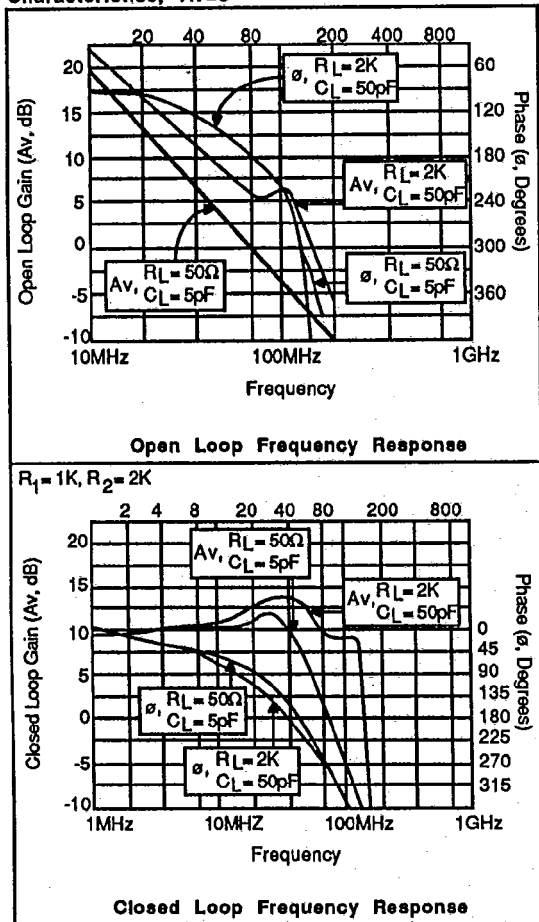
SIMPLIFIED SCHEMATIC



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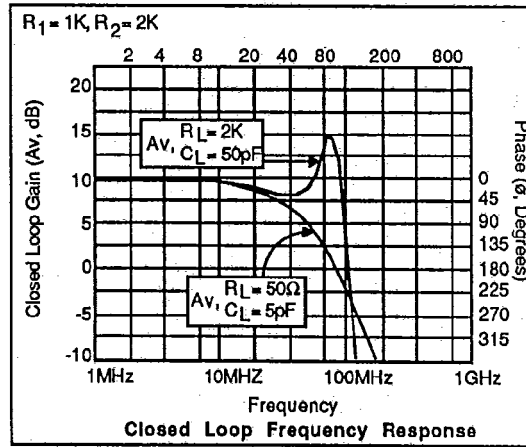
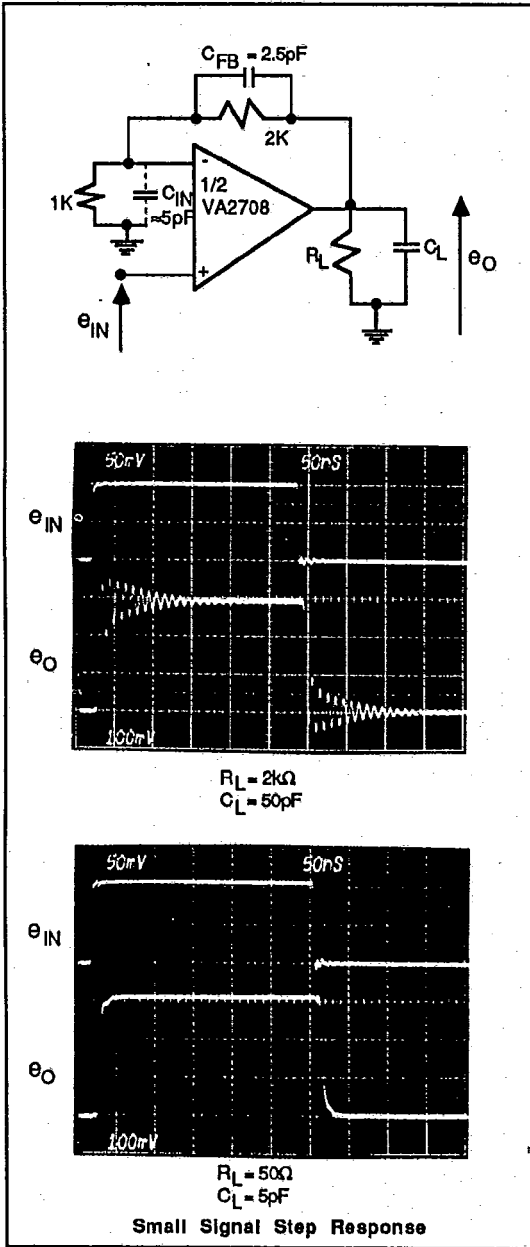
Figure 3: Frequency and Time Domain Response Characteristics, $A_v=3$



LSP FAMILY DATA SHEETS

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Figure 4: Response Characteristics with Input Pole Cancellation, $A_v=3$



LSP FAMILY DATA SHEETS

PACKAGE INFORMATION

8 PIN PLASTIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.148	0.152	3.76	3.86
B	0.016	0.020	0.41	0.51
C	0.008	0.012	0.20	0.30
D	0.370	0.390	9.40	9.91
E	0.245	0.265	6.22	6.73
F	0.290	0.310	7.37	7.87
G	0.050	0.070	1.27	1.78
H	0.090	0.110	2.29	2.79
J	0.128	0.132	3.25	3.35
K	0.020	0.040	0.51	1.02
L	0.030	0.050	0.76	1.27
	0°	15°	0°	15°

*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

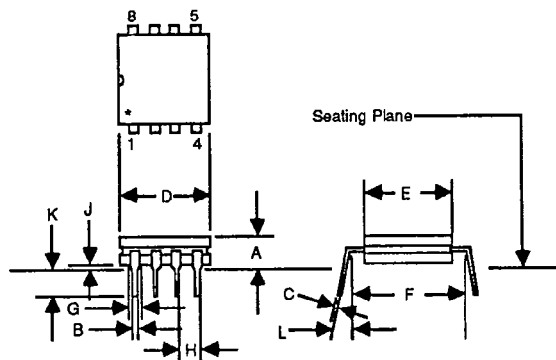
8 PIN METAL CAN				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.345	.365	8.76	9.27
B	.165	.185	4.19	4.70
C	.020	.040	0.51	1.02
D	.010	.045	0.25	1.14
E	.500	.550	12.70	13.97
F	.200	BSC	5.08	BSC
G	.016	.021	0.41	0.53
J	.027	.045	0.69	1.14
K	.027	.034	0.69	0.86

8-PIN SOIC, PLASTIC				
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.053	.069	1.35	1.75
B	.014	.018	0.35	0.45
C	.007	.009	0.19	0.22
D	.150	.158	3.8	4.0
E	.181	.205	4.6	5.2
F	.228	.244	5.8	6.2
G	.004	.008	0.10	0.20
H	.50	BSC	1.27	BSC
J	.025	.030	0.64	0.77
K	.024	.031	0.61	0.78
L	.188	.197	4.8	5.0
M	.015	BSC	0.37	BSC
N	—	45°	—	45°
P	3°	6°	3°	6°
Q	—	7°	—	7°
R	.019	.022	0.49	0.56

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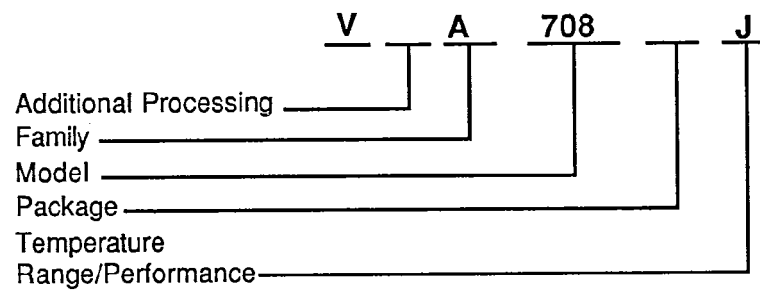
VA708

8 PIN CERAMIC DIP				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
B	0.014	0.023	0.36	0.58
C	0.008	0.015	0.20	0.38
D	—	1.060	—	26.92
E	0.220	0.310	5.59	7.87
F	0.290	0.320	7.37	8.13
G	0.030	0.070	0.76	1.78
H	0.090	0.110	2.29	2.79
J	0.015	0.060	0.38	1.52
K	0.125	0.200	3.18	5.08
L	0°	15°	0°	15°



*Note: Index area; a notch or a lead one identification mark is located adjacent to lead one.

ORDERING INFORMATION:



ADDITIONAL PROCESSING

Blank = No Burn-In B = Burn-In (168 Hours, T_j = 150°C or equivalent)

PACKAGE TYPE

D = Cerdip P = Plastic Dip T = Metal Can X = Die PO = SOIC

TEMPERATURE RANGE/PERFORMANCE

J thru K = Commercial (0° to 70°C)

T = Military (-55°C to +125°C)

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