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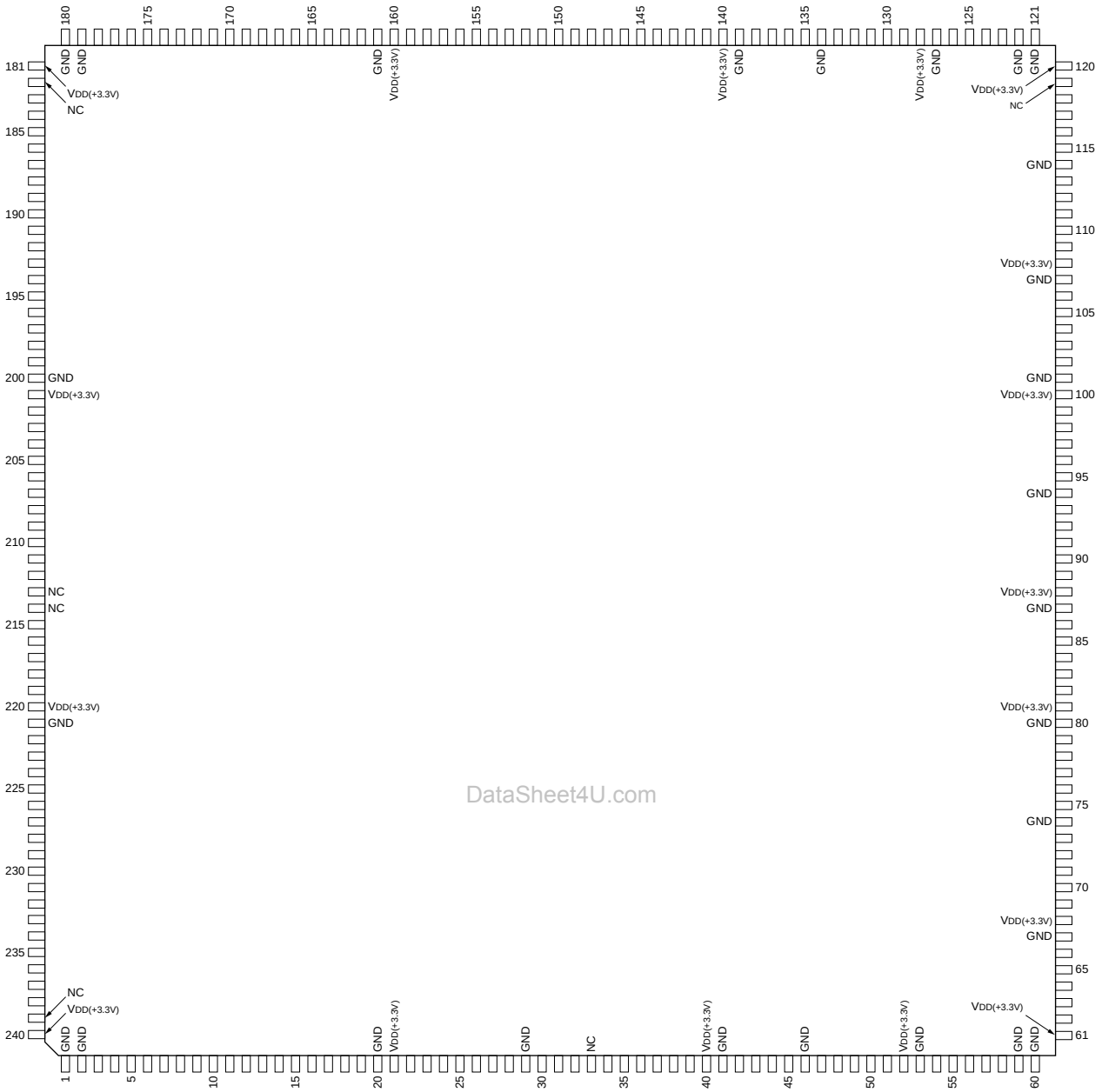
C-MOS SDDI-TO-DISK FORMAT CONVERTER

–TOP VIEW–



(V_{DD} = +3.3V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	61	—	V_{DD}	121	—	GND	181	—	V_{DD}
2	—	GND	62	I/O	DQA8	122	—	GND	182	—	NC
3	I	SCK	63	I/O	DQA7	123	O	CKEB	183	I	SPCRD7
4	I	AMC	64	O	LDQMA	124	O	RASB	184	I	SPCRD6
5	I	SMC	65	O	UDQMA	125	O	AB9	185	I	SPCRD5
6	I	SYSCS	66	O	WEA	126	O	AB11	186	I	SPCRD4
7	O	IINTD	67	—	GND	127	—	GND	187	I	SPCRD3
8	O	OINTD	68	—	V_{DD}	128	—	V_{DD}	188	I	SPCRD2
9	I	DIRR	69	O	CASA	129	O	AB8	189	I	SPCRD1
10	I	DIRW	70	O	CKEA	130	O	AB10	190	I	SPCRD0
11	I	SYSA7	71	O	RASA	131	O	AB7	191	I	SPCEMP
12	I	SYSA6	72	O	AA9	132	O	AB0	192	O	SPCHOE
13	I	SYSA5	73	O	AA11	133	O	AB6	193	O	SPCLOE
14	I	SYSA4	74	—	GND	134	—	GND	194	O	SPCHRE
15	I	SYSA3	75	O	AA8	135	O	AB1	195	O	SPCLRE
16	I	SYSA2	76	O	AA10	136	O	AB5	196	O	SPCWD7
17	I	SYSA1	77	O	AA7	137	O	AB2	197	O	SPCWD6
18	I	SYSA0	78	O	AA0	138	O	AB4	198	O	SPCWD5
19	I/O	SYSD7	79	O	AA6	139	—	GND	199	O	SPCWD4
20	—	GND	80	—	GND	140	—	V_{DD}	200	—	GND
21	—	V_{DD}	81	—	V_{DD}	141	O	AB3	201	—	V_{DD}
22	I/O	SYSD6	82	O	AA1	142	O	TSTD0	202	O	SPCWD3
23	I/O	SYSD5	83	O	AA5	143	O	TSTD1	203	O	SPCWD2
24	I/O	SYSD4	84	O	AA2	144	O	TSTD2	204	O	SPCWD1
25	I/O	SYSD3	85	O	AA4	145	O	TSTD3	205	O	SPCWD0
26	I/O	SYSD2	86	O	AA3	146	O	TSTD4	206	I	DMAREQ
27	I/O	SYSD1	87	—	GND	147	O	TSTD5	207	O	BHWEN
28	I/O	SYSD0	88	—	V_{DD}	148	O	TSTD6	208	O	BLWEN
29	—	GND	89	O	CS0	149	O	TSTD7	209	O	BWRST
30	I	RESET	90	O	CS1	150	O	TSTD8	210	O	AHWEN
31	I	CK27	91	O	CS2	151	O	TSTD9	211	O	ALWEN
32	I	CK54	92	O	CS3	152	O	TSTD10	212	O	AWRST
33	—	NC	93	I/O	DQB15	153	O	TSTD11	213	—	NC
34	I	TSTMD4	94	—	GND	154	O	TSTD12	214	—	NC
35	I	TSTMD3	95	I/O	DQB0	155	O	TSTD13	215	I	IND9
36	I	TSTMD2	96	I/O	DQB14	156	O	TSTD14	216	I	IND8
37	I	TSTMD1	97	I/O	DQB1	157	O	TSTD15	217	I	IND7
38	I	TSTMD0	98	I/O	DQB13	158	O	ORRST	218	I	IND6
39	I	RAMTES	99	I/O	DQB2	159	I	OAINT	219	I	IND5
40	—	V_{DD}	100	—	V_{DD}	160	—	V_{DD}	220	—	V_{DD}
41	—	GND	101	—	GND	161	—	GND	221	—	GND
42	I/O	DQA15	102	I/O	DQB12	162	I	OVINT	222	I	IND4
43	I/O	DQA0	103	I/O	DQB3	163	I	OCINT	223	I	IND3
44	I/O	DQA14	104	I/O	DQB11	164	O	DPEND	224	I	IND2
45	I/O	DQA1	105	I/O	DQB4	165	O	DPSYNC	225	I	IND1
46	—	GND	106	I/O	DQB10	166	O	OUTD7	226	I	IND0
47	I/O	DQA13	107	—	GND	167	O	OUTD6	227	O	INTCWE
48	I/O	DQA2	108	—	V_{DD}	168	O	OUTD5	228	O	INVRE
49	I/O	DQA12	109	I/O	DQB5	169	O	OUTD4	229	O	INARE
50	I/O	DQA3	110	I/O	DQB9	170	O	OUTD3	230	O	INRRST
51	I/O	DQA11	111	I/O	DQB6	171	O	OUTD2	231	O	INWRST
52	—	V_{DD}	112	I/O	DQB8	172	O	OUTD1	232	O	COREOE
53	—	GND	113	I/O	DQB7	173	O	OUTD0	233	O	DGREN
54	I/O	DQA4	114	—	GND	174	O	DPTCWE	234	O	DGRRST
55	I/O	DQA10	115	O	LDQMB	175	O	OVWE	235	O	DGOE
56	I/O	DQA5	116	O	UDQMB	176	O	OAWE	236	I	IAINT
57	I/O	DQA9	117	O	WEB	177	O	OWRST	237	I	IVINT
58	I/O	DQA6	118	O	CASB	178	I	FP	238	I	ICINT
59	—	GND	119	—	NC	179	—	GND	239	—	NC
60	—	GND	120	—	V_{DD}	180	—	GND	240	—	V_{DD}

INPUT

AMC	;	TEST
CK27	;	27 MHz CLOCK
CK54	;	54 MHz CLOCK
DIRR	;	CPU INTERFACE READ ENABLE
DIRW	;	CPU INTERFACE WRITE ENABLE
DMAREQ	;	DMA DATA REQUEST
FP	;	FRAME PULSE
IAINT	;	RX CORE IC-CHIP AUDIO INTERRUPT
ICINT	;	RX CORE IC-CHIP COMMAND INTERRUPT
IND0 - IND9	;	SDDI DATA
IVINT	;	RX CORE IC-CHIP VIDEO INTERRUPT
OAINT	;	TX CORE IC CHIP AUDIO INTERRUPT
OCINT	;	TX CORE IC CHIP COMMAND INTERRUPT
OVINT	;	TX CORE IC CHIP VIDEO INTERRUPT
RAMTES	;	SD RAM TEST MODE SETTING
RESET	;	SYSTEM RESET
SCK	;	TEST
SMC	;	TEST
SPCEMP	;	SPC READ FIFO EMPTY FLAG
SPCRD0 - SPCRD7	;	SPC READ DATA
SYSA0 - SYSA7	;	CPU INTERFACE ADDRESS BUS
SYSCS	;	CHIP SELECT
TSTMD0 - TSTMD4	;	TEST MODE SETTING

INPUT/OUTPUT

DQA0 - DQA15	;	SDRAM DATA PORT A
DQB0 - DQB15	;	SDRAM DATA PORT B
SYSD0 - SYSD7	;	CPU INTERFACE DATA BUS

OUTPUT

AA0 - AA11	;	SDRAM ADDRESS PORT A
AB0 - AB11	;	SDRAM ADDRESS PORT B
AHWEN	;	SPC WRITE A HIGHER FIFO WRITE ENABLE
ALWEN	;	SPC WRITE A LOWER FIFO WRITE ENABLE
AWRST	;	SPC WRITE A FIFO WRITE RESET
BHWEN	;	SPC WRITE B HIGHER FIFO WRITE ENABLE
BLWEN	;	SPC WRITE B LOWER FIFO WRITE ENABLE
BWRST	;	SPC WRITE B FIFO WRITE RESET
CASA	;	COLUMN ADDRESS STROBE FOR PORT A
CASB	;	COLUMN ADDRESS STROBE FOR PORT B
CKEA	;	SDRAM CLOCK ENABLE FOR PORT A
CKEB	;	SDRAM CLOCK ENABLE FOR PORT B
COREOE	;	RX CORE IC-CHIP OUTPUT ENABLE
CS0 - CS3	;	SDRAM CHIP SELECT
DGOE	;	DIAG-FIFO OUTPUT ENABLE
DGREN	;	DIAG FIFO READ ENABLE
DGRRST	;	DIAG FIFO READ RESET
DPEND	;	DEPACKED END PULSE
DPSYNC	;	DEPACKED SYNC
DPTCWE	;	TX TIME-CODE WRITE ENABLE
IINTD	;	RX SDDI RECEIVING STATUS
INARE	;	RX CORE AUDIO FIFO READ ENABLE
INRRST	;	RX CORE FIFO READ RESET
INTCWE	;	RX TIME-CODE WRITE ENABLE
INVRE	;	RX CORE VIDEO FIFO READ ENABLE
INWRST	;	RX CORE FIFO WRITE RESET
LDQMA	;	LOWER DQ MASK ENABLE FOR PORT A
LDQMB	;	LOWER DQ MASK ENABLE FOR PORT B
OAWE	;	TX CORE AUDIO FIFO WRITE ENABLE
OINTD	;	TX SDDI TRANSMITTING STATUS
ORRST	;	TX CORE FIFO READ RESET
OUTD0 - OUTD7	;	DEPACKED DATA
OVWE	;	TX CORE VIDEO FIFO WRITE ENABLE
OWRST	;	TX CORE FIFO WRITE RESET
RASA	;	ROW ADDRESS STROBE FOR PORT A
RASB	;	ROW ADDRESS STROBE FOR PORT B
SPCHOE	;	SPC READ HIGHER FIFO OUTPUT ENABLE
SPCHRE	;	SPC READ HIGHER FIFO READ ENABLE
SPCLOE	;	SPC READ LOWER FIFO OUTPUT ENABLE
SPCLRE	;	SPC READ LOWER FIFO READ ENABLE
SPCWD0 - SPCWD7	;	SPC WRITE DATA
TSTD0 - TSTD15	;	TEST DATA
UDQMA	;	HIGHER DQ MASK ENABLE FOR PORT A
UDQMB	;	HIGHER DQ MASK ENABLE FOR PORT B
WEA	;	SDRAM WRITE ENABLE FOR PORT A
WEB	;	SDRAM WRITE ENABLE FOR PORT B