

**MOS INTEGRATED CIRCUIT**  
 **$\mu$ PD75208****4-BIT SINGLE-CHIP MICROCOMPUTER****DESCRIPTION**

The  $\mu$ PD75208 is a microcomputer with a CPU capable of 1-, 4-, and 8-bit-wise data processing, a ROM, a RAM, I/O ports, a fluorescent display tube controller/driver, a watch timer, a timer/pulse generator capable of outputting 14-bit PWM, a serial interface and a vectored interrupt function integrated on a single-chip.

It uses the VCR, ECR and CD fluorescent display tubes as display devices and is most suitable for applications requiring the timer/watch function and high-speed interrupt servicing. It can help to provide the unit with many functions and to decrease performance costs.

With the  $\mu$ PD75208, the  $\mu$ PD75P216A, 75P218 one-time PROM products are available for system development evaluation or small production. ★

**The following manual provides detailed description of the functions of the  $\mu$ PD75208. Be sure to read this manual when you design an application system.**

**$\mu$ PD75216A User's Manual: IEM-988**

**FEATURES**

- Architecture equal to that of an 8-bit microcomputer
- High-speed operation : Minimum instruction execution time : 0.95  $\mu$ s (when operated at 4.19 MHz)
- Instruction execution time variable function realizing a wide range of operating voltages
- On-chip large-capacity program memory : 8K bytes
- Watch operation with an ultra low current consumption : 5 $\mu$ A TYP. (at the 3 V operation)
- On-chip programmable fluorescent display tube controller/driver
- Timer function : 4 ch
  - 14-bit PWM output capability with the voltage synthesizer type electronic tuner
  - Buzzer output capability
- Interrupt function with importance attached to applications
  - For power-off detection
  - For remote controlled reception
- Product with an on-chip PROM :  $\mu$ PD75P216A,  $\mu$ PD75P218 (on-chip EPROM : WQFN package) ★

**ORDERING INFORMATION** ★

Ordering Code	Package	Quality Grade
$\mu$ PD75208CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
$\mu$ PD75208GF-xxx-3BE	64-pin plastic QFP (14 × 20 mm)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

★ LIST OF FUNCTIONS

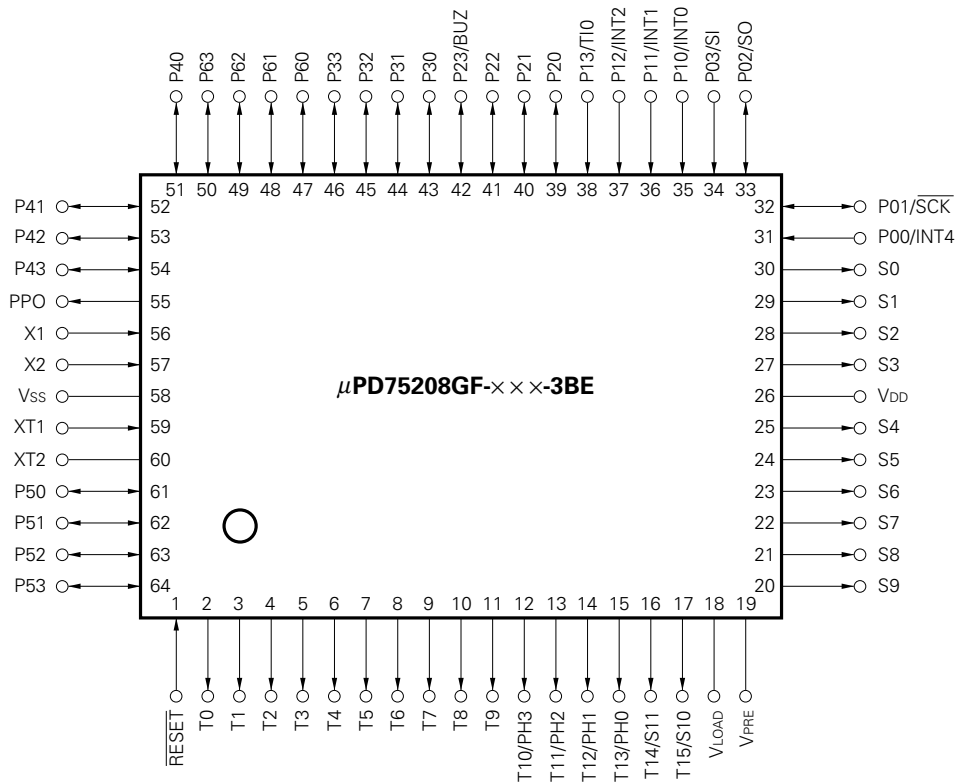
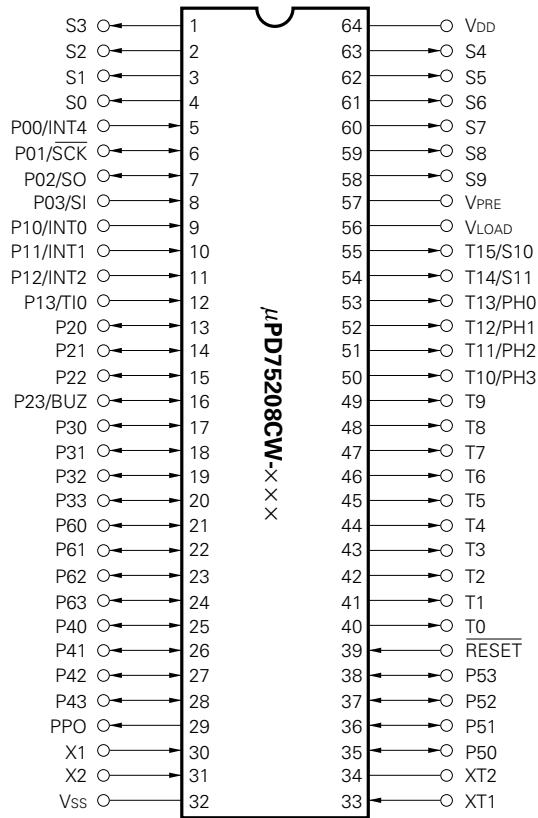
Item		Function		
Instruction execution time		<ul style="list-style-type: none"> <li>• 0.95, 1.91, 15.3 μs (Main system clock : 4.19 MHz operation)</li> <li>• 122 μs (Subsystem clock : 32.768 kHz operation)</li> </ul>		
On-chip memory	ROM	8064 × 8 bits		
	RAM	497 × 4 bits		
General register		<ul style="list-style-type: none"> <li>• 4-bit manipulation : 8 × 4 banks</li> <li>• 8-bit manipulation : 4 × 4 banks</li> </ul>		
Input/output port  <div style="border-left: 1px solid black; border-right: 1px solid black; padding: 2px; display: inline-block;">                     FIP<sup>®</sup> dual-function pin included                      FIP dedicated pin excluded                 </div>	33	8	CMOS input pin	
		20	CMOS input/output pins	<ul style="list-style-type: none"> <li>• Direct LED drive capability : 8</li> <li>• On-chip pull-down resistor by mask option capability : 4</li> </ul>
		5	CMOS output pin	<ul style="list-style-type: none"> <li>• Direct LED drive capability : 4</li> <li>• PWM/pulse output : 1</li> <li>• On-chip pull-down resistor by mask option capability : 4</li> </ul>
FIP controller/driver		<ul style="list-style-type: none"> <li>• No. of segments : 9 to 12 segments</li> <li>• No. of digits : 9 to 16 digits</li> <li>• Dimmer function : 8 levels</li> <li>• On-chip pull-down resistor by mask option capability</li> <li>• Key scan interrupt generation</li> </ul>		
Timer		4 channels	<ul style="list-style-type: none"> <li>• Timer/pulse generator : 14-bit PWM output enabled</li> <li>• Watch timer : Buzzer output enabled</li> <li>• Timer/event counter</li> <li>• Basic interval timer : Watchdog timer application capability</li> </ul>	
Serial interface		<ul style="list-style-type: none"> <li>• MSB start/LSB start switchable</li> <li>• Serial bus configuration capability</li> </ul>		
Vectored interrupt		External : 3, Internal : 5		
Test input		External : 1, Internal : 1		
System clock oscillator		<ul style="list-style-type: none"> <li>• Ceramic/crystal oscillator for main system clock oscillation : 4.194304 MHz standard</li> <li>• Crystal oscillator for subsystem clock oscillation : 32.768 kHz standard</li> </ul>		
Standby function		STOP/HALT mode		
Mask option		<ul style="list-style-type: none"> <li>• Power-on reset, power-on flag</li> <li>• High withstand voltage port : Pull-down resistor or open-drain output</li> <li>• Port 6 : Pull-down resistor</li> </ul>		
Operating temperature range		-40 to +85 °C		
Operating voltage		2.7 to 6.0 V (standby data hold : 2.0 to 6.0 V)		
Package		<ul style="list-style-type: none"> <li>• 64-pin plastic shrink DIP (750 mil)</li> <li>• 64-pin plastic QFP (14 × 20 mm)</li> </ul>		

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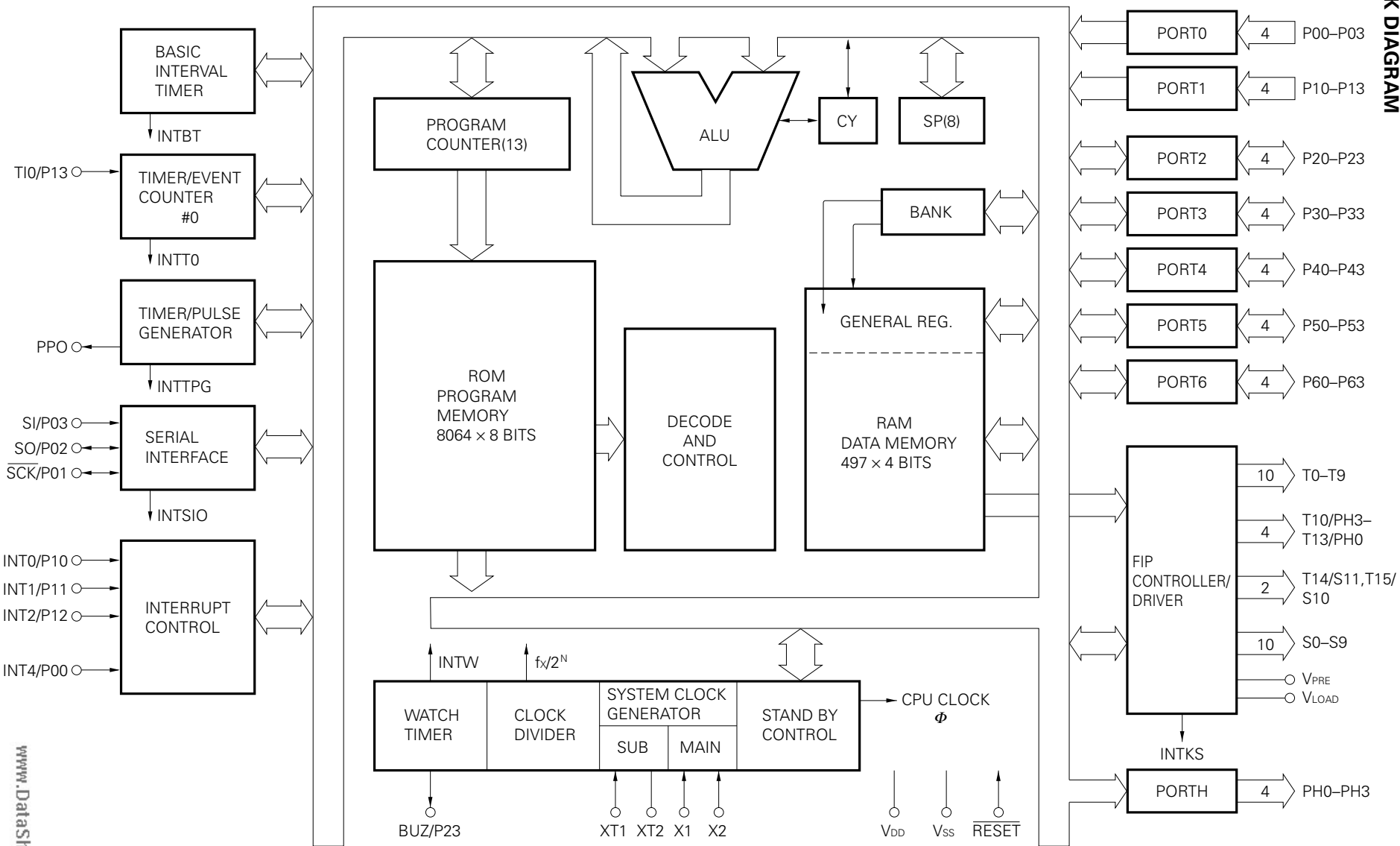
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1. PIN CONFIGURATION (TOP VIEW)



2. BLOCK DIAGRAM



### 3. PIN FUNCTIONS

#### 3.1 PORT PINS

Pin Name	I/O	Dual-Function Pin	Function	8-Bit I/O	After Reset	Input / Output Circuit Type *1	
P00	Input	INT4	4-bit input port (PORT0).	×	Input	Ⓑ	
P01	Input/output	SCK				Ⓕ	
P02	Input/output	SO				Ⓖ	
P03	Input	SI				Ⓑ	
P10	Input	INT0	4-bit input port (PORT1). Noise removing function available		Input	Ⓑ	
P11		INT1					Noise removing function available
P12		INT2					
P13		T10					
P20	Input/output	—	4-bit input/output port (PORT2).	×	Input	E	
P21		—					
P22		—					
P23		BUZ					
P30–P33	Input/output	—	Programmable 4-bit input/ output port (PORT3). Input/output specifiable in 1-bit units.		Input	E	
P40 to P43	Input/output	—	4-bit input/output port (PORT4). LED direct drive capability.	○	Input	E	
P50 to P53	Input/output	—	4-bit input/output port (PORT5). LED direct drive capability.		Input	E	
P60 to P63	Input/output	—	Programmable 4-bit input/output port (PORT6). Input/output specifiable in 1-bit units. On-chip pull-down resistor available (mask option). Suitable for key input.	×	Input	V	
PH0	Output	T13	4-bit P-ch open-drain, high-dielectric, high-current output port (PORTH). LED direct drive capability. On-chip pull-down resistor available (mask option).	×	Low level (with an on-chip pull-down resistor) or high impedance.	I	
PH1		T12					
PH2		T11					
PH3		T10					

\* Schmitt trigger inputs are circled.

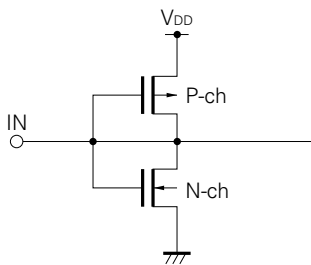
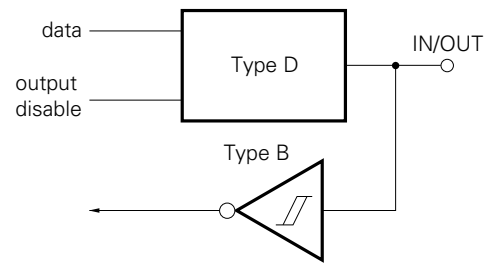
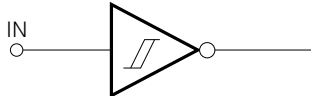
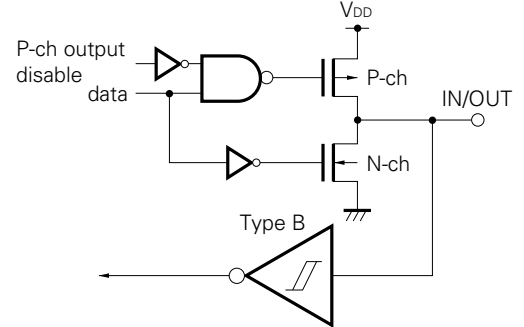
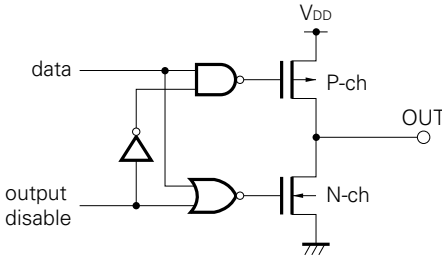
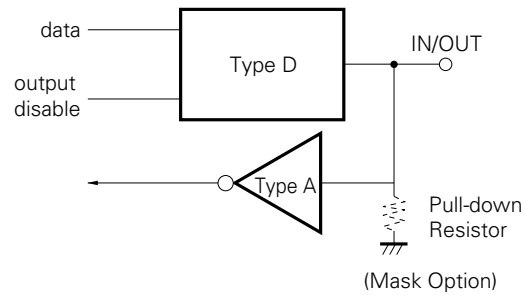
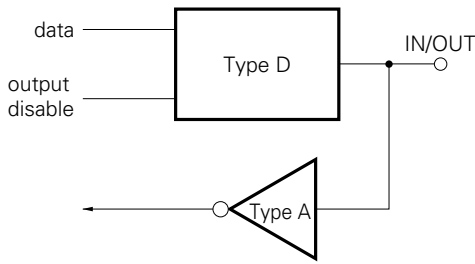
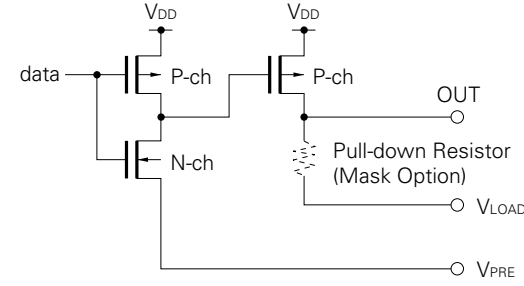
3.2 NON-PORT PINS

Pin Name	I/O	Dual-Function Pin	Function		After Reset	Input / Output Circuit Type *
T0 to T9	Output	—	FIP controller/driver output pins. Pull-down resistor can be incorporated in bit units (mask option).	Digit output high-voltage high-current output.	Low level (with an on-chip pull-down resistor ) or high impedance (without a pull-down resistor)	I
T10 to T13		PH3 to PH0		Digit/segment output dual-function high-voltage high-current output. Extra pins can be used as PORTH.		
T14/S11, T15/S10		—		Digit/segment output dual-function high-voltage high-current output. Static output also possible.		
S9		—		Segment output high voltage output. Static output also possible.		
S0 to S8		—		Segment high-voltage output.		
PPO	Output	—	Timer/pulse generator pulse output.		High impedance	D
TI0	Input	P13	External event pulse input for timer/event counter.			ⓑ
$\overline{\text{SCK}}$	Input/output	P01	Serial clock input/output.		Input	Ⓕ
SO	Input/output	P02	Serial data output pin or serial data input/output.		Input	Ⓖ
SI	Input	P03	Serial data input or normal input.		Input	ⓑ
INT4	Input	P00	Edge-detected vectored interrupt input (rising and falling edge detection).			ⓑ
INT0	Input	P10	Edge-detected vectored interrupt input with noise eliminate function (detection edge selection possible).			ⓑ
INT1		P11				
INT2	Input	P12	Edge-detected testable input (rising edge detection).			ⓑ
BUZ	Input/output	P23	Fixed frequency output (for buzzer or system clock trimming).		Input	E
X1, X2	Input	—	Crystal/ceramic connect pin for main system clock oscillation. External clock input to X1 and its inverted clock input to X2.			
XT1	Input	—	Crystal connect pin for subsystem clock oscillation. External clock input to XT1 and XT2 open.			
XT2	—					
$\overline{\text{RESET}}$	Input		System reset input (low level active).			ⓑ
V <sub>PRE</sub>		—	FIP controller/driver output buffer power supply.			I
V <sub>LOAD</sub>		—	FIP controller/driver pull-down resistor connect pin.			I
V <sub>DD</sub>		—	Positive power supply.			
V <sub>SS</sub>		—	GND potential.			

\* Schmitt trigger inputs are circled.



3.3 PIN INPUT/OUTPUT CIRCUIT LIST

<p>TYPE A</p>  <p>CMOS-Specified Input Buffer</p>	<p>TYPE F</p>  <p>Input/Output Circuit Consisting of Type D Push-Pull Output and Type B Schmitt Trigger Input</p>
<p>TYPE B</p>  <p>Schmitt Trigger Input Having Hysteresis Characteristics</p>	<p>TYPE G</p>  <p>Input/Output Circuit Capable of Switching between Push-Pull Output and N-ch Open-Drain Output (with P-ch OFF).</p>
<p>TYPE D</p>  <p>Push-Pull Output which can be Set to Output High Impedance (with Both P-ch and N-ch Set to OFF)</p>	<p>TYPE V</p>  <p>(Mask Option)</p>
<p>TYPE E</p>  <p>Input/Output Circuit Consisting of Type D Push-Pull Output and Type A Input Buffer</p>	<p>TYPE I</p>  <p>Pull-down Resistor (Mask Option)</p> <p>V<sub>LOAD</sub></p> <p>V<sub>PRE</sub></p>

## 3.4 UNUSED PINS TREATMENT

Pin	Recommended Connection	
P00/INT4	Connect to V <sub>SS</sub>	
P01/ $\overline{\text{SCK}}$	Connect to V <sub>SS</sub> or V <sub>DD</sub>	
P02/SO		
P03/SI		
P10/INT0 to P12/INT2		
P13/TI0	Connect to V <sub>SS</sub>	
P20 to P22	Input state : Connect to V <sub>SS</sub> or V <sub>DD</sub> Output state : Leave open	
P23/BUZ		
P30 to P33		
P40 to P43		
P50 to P53		
P60 to P63		
PPO		Leave open
S0 to S9		
T15/S10 to T14/S11		
T0 to T9		
T10/PH3 to T13/PH0		
XT1	Connect to V <sub>SS</sub> or V <sub>DD</sub>	
XT2	Leave open	
$\overline{\text{RESET}}$ when there is an on-chip power-on reset circuit	Connect to V <sub>DD</sub>	
V <sub>LOAD</sub> when there is no on-chip load resistor	Connect to V <sub>SS</sub> or V <sub>DD</sub>	

**3.5 P00/INT4 PIN AND RESET PIN OPERATING PRECAUTIONS**

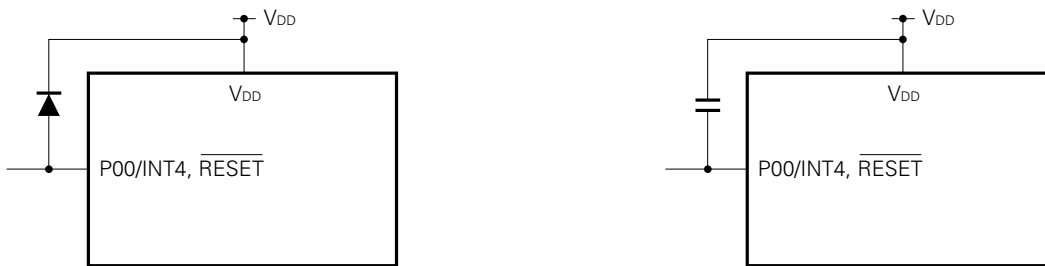
P00/INT4 and RESET pins have the function (especially for IC test) to test uPD75208 internal operations in addition to the functions described in sections 3.1 and 3.2.

The test mode is set when a voltage larger than V<sub>DD</sub> is applied to one of these pins. If noise larger than V<sub>DD</sub> is applied in normal operation, the test mode may be set thereby adversely affecting normal operation.

Since there is a display output pin having a high-voltage amplitude (35 V) next to the P00/INT4 and RESET pins, if cables for the related signals are routed in parallel, wiring noise larger than V<sub>DD</sub> may be applied to the P00/INT4 and RESET pins causing errors.

Thus, carry out wiring so that wiring noise can be minimized, If noise still cannot be suppressed, take the measure against noise using the following external components.

- Connect diode with small V<sub>F</sub> (0.3 V or less) between the pins and V<sub>DD</sub>
- Connect a capacitor between the pins and V<sub>DD</sub>.

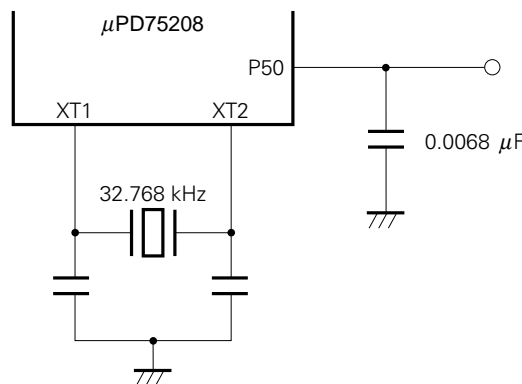


**3.6 XT1, XT2 AND P50 PIN OPERATING PRECAUTIONS**

When selecting the 32.768 kHz subsystem clock connected to the XT1 and XT2 pins as the watch timer source clock, the signal to be input or output to the P50 pin next to the XT2 pin must be a signal required to be switched between high and low the minimum number of times (once/second or less).

If the P50 pin signal is switched frequently between high and low, a spike is generated in the XT2 pin because of capacitance coupling of the P50 and XT2 pins and the correct watch functions cannot be achieved (the watch becomes fast).

If it is necessary to allow the P50 pin signal to switch between high and low, mount an external capacitor to the P50 pin as shown below.



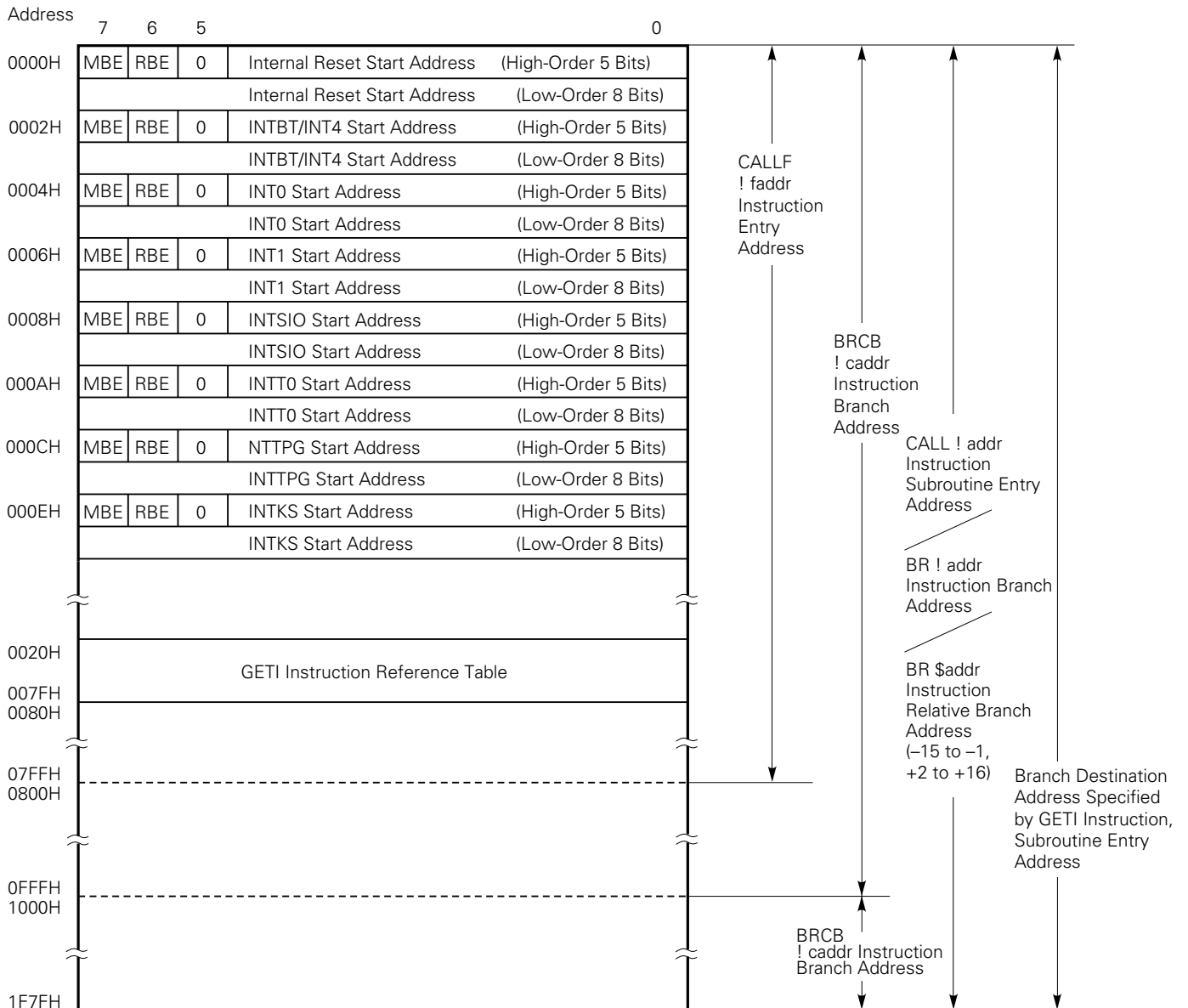
#### 4. ARCHITECTURE AND MEMORY MAP OF THE μPD75208

The μPD75208 has three architectural features:

- Bank configuration of data memory : Static RAM (448 words × 4 bits)  
Display data memory (49 words × 4 bits)  
Peripheral hardware (128 × 4 bits)
- Bank configuration of general registers: 8 × 4 banks (for operation in 4-bit units)  
4 × 4 banks (for operation in 8-bit units)
- Memory mapped I/O

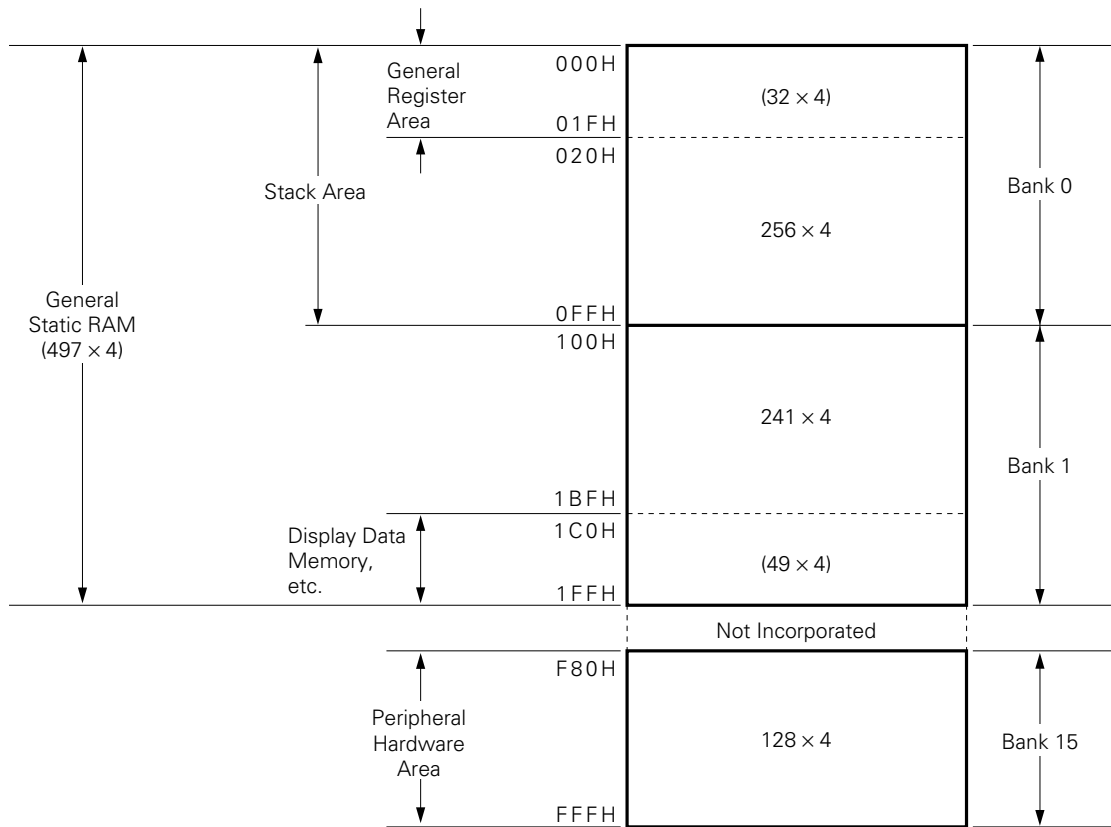
Fig. 4-1 and 4-2 show the memory maps for the μPD75208.

**Fig. 4-1 Program Memory Map**



**Remarks** In all cases other than those listed above, branch to the address with only the lower 8 bits of the PC changed is enabled by BR PCDE and BR PCXA instructions.

Fig. 4-2 Data Memory Map



## 5. PERIPHERAL HARDWARE FUNCTIONS

### 5.1 PORTS

The μPD75208 has the following three types of I/O port:

- 8 CMOS input ports
- 20 CMOS I/O ports
- 4 P-ch open-drain high-voltage, large-current output ports

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Total: 32 ports

**Table 5-1 Functions of Ports**

Port Name	Function	Operation and Feature	Remarks
PORT0	4-bit input	Always read or test possible irrespective of the dual-function pin operating mode.	Shares the pins with SI, SO, $\overline{\text{SCK}}$ and INT4.
PORT1		Always read or test possible, P10 and P11 are inputs with the noise eliminate function.	Shares the pins with INT0 to 2 and T10.
PORT2 PORT4 PORT5	4-bit input/output	Can be set to the input or output mode in 4-bit units. Ports 4 and 5 can input/output data in pairs in 8-bit units. Ports 4 and 5 can directly drive LEDs.	P23 shares the pin with BUZ.
PORT3 PORT6		Can be set bit-wise to the input or output mode. Port 6 can incorporate a pull-down resistor as a mask option.	
PORTH	4-bit output	P-ch open-drain high-voltage, high-current output port. Can drive an FIP and LED directly. Can incorporate a pull-down resistor bit-wise as a mask option.	Shares the pins with T10 to T13.

### 5.2 CLOCK GENERATOR

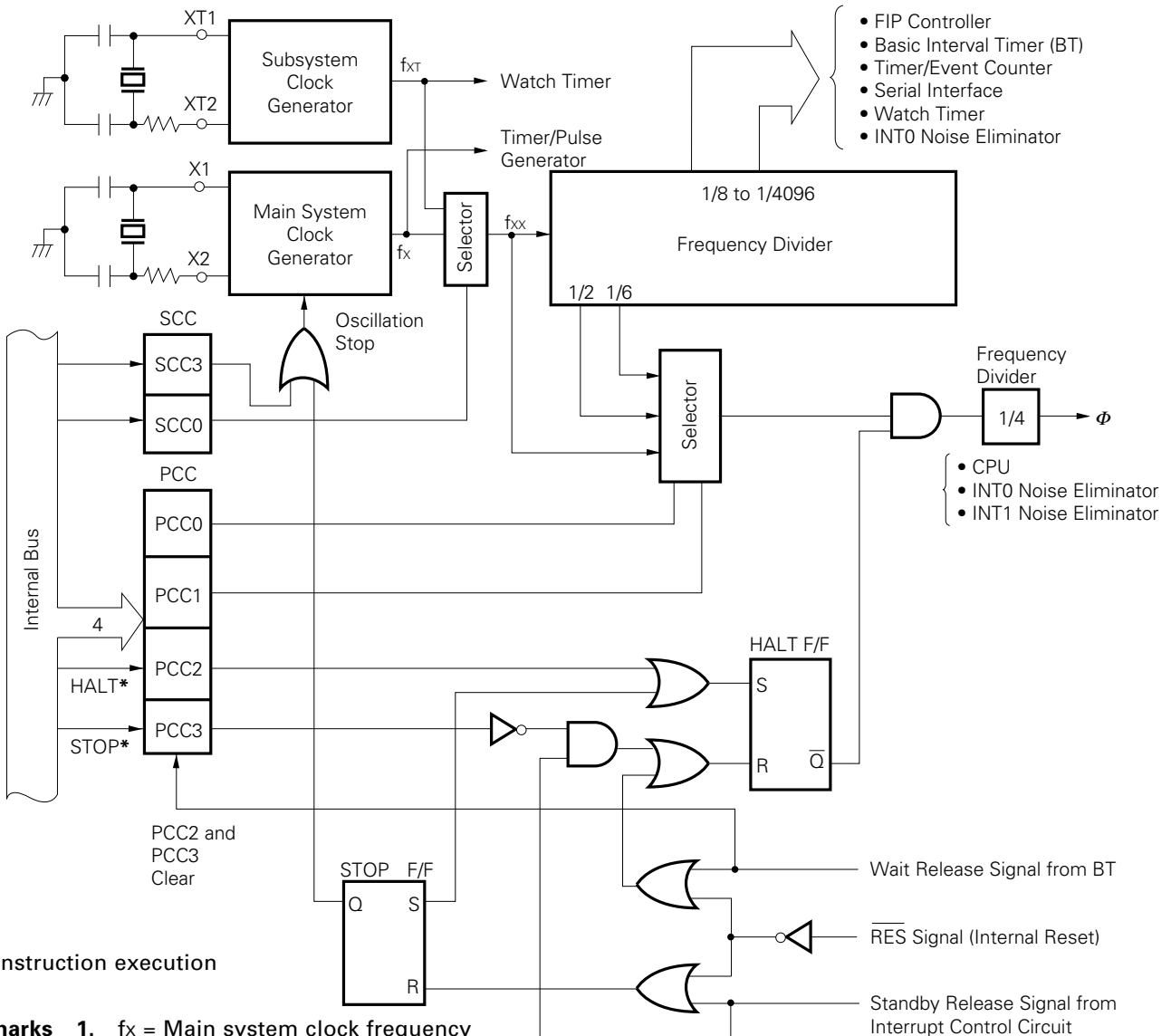
Operation of the clock generator is specified by the processor clock control register (PCC) and system clock control register (SCC).

The main system clock or subsystem clock can be selected.

The instruction execution time is variable.

- 0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz)
- 122 μs (subsystem clock: 32.768 kHz)

**Fig. 5-1 Clock Generator Block Diagram**



\* Instruction execution

- Remarks**
1. fx = Main system clock frequency
  2. f<sub>XT</sub> = Subsystem clock frequency
  3. f<sub>xx</sub> = System clock frequency
  4. φ = CPU clock
  5. PCC: Processor clock control register
  6. SCC: System clock control register
  7. 1 clock cycle (tc<sub>ϕ</sub>) of φ is 1 machine cycle of an instruction. For tc<sub>ϕ</sub>, see "AC Characteristics" in
- 12. ELECTRICAL SPECIFICATIONS.**

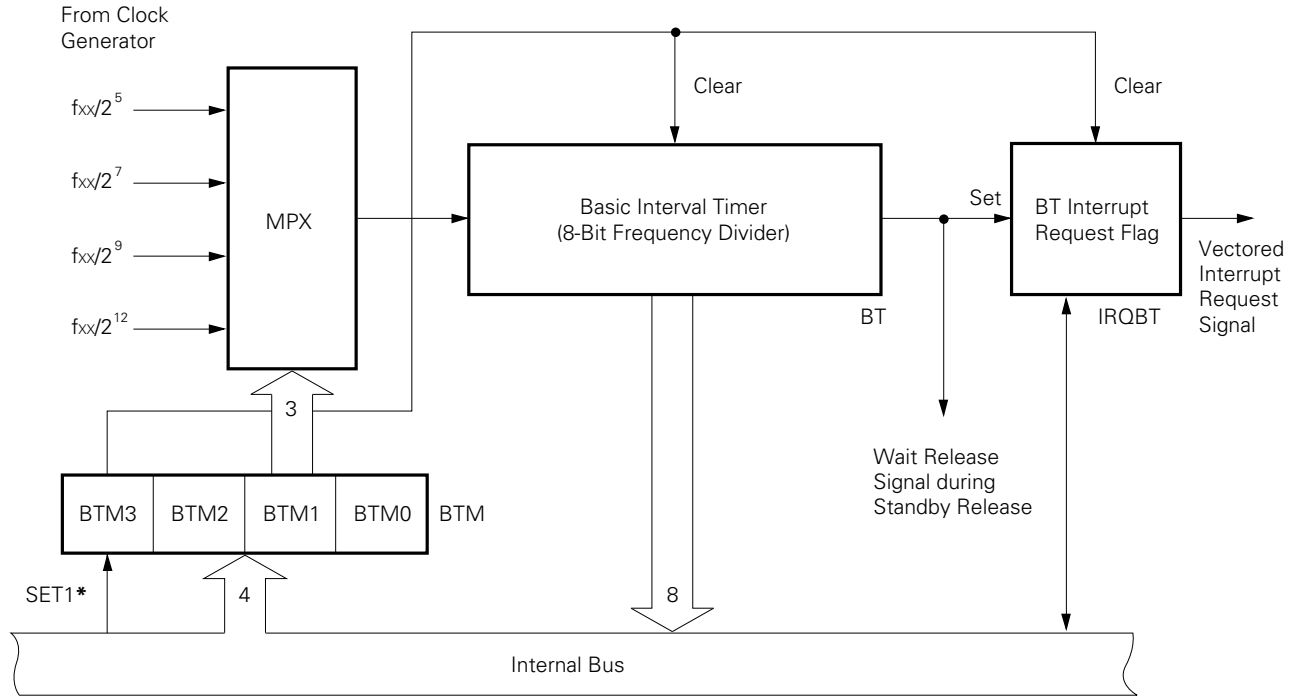


**5.3 BASIC INTERVAL TIMER**

The basic interval timer has the following functions:

- Interval timer operation to generate reference time
- Watchdog timer application to detect inadvertent program loop
- Wait time select and count upon standby mode release
- Count contents read

**Fig. 5-2 Basic Interval Timer Configuration**



\* Instruction execution

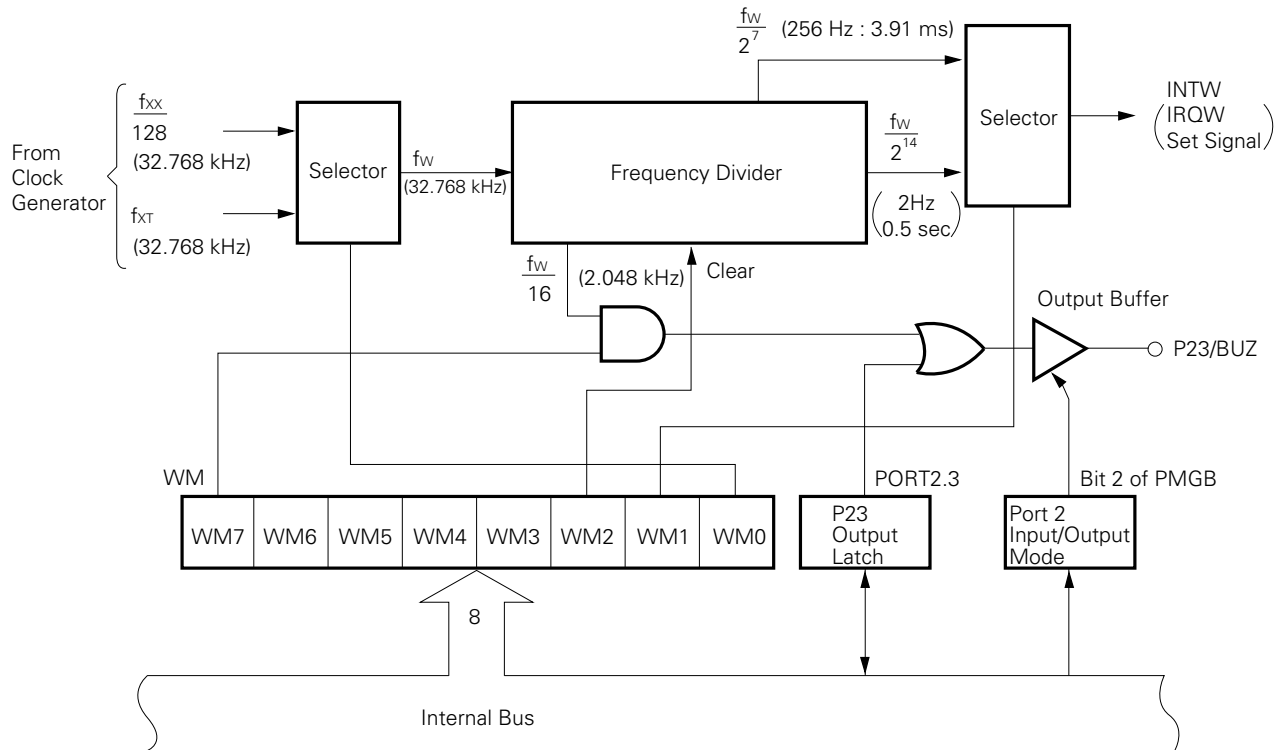


5.4 WATCH TIMER

The μPD75208 incorporates one channel of watch timer. The watch timer has the following functions:

- Sets the test flag (IRQW) at 0.5 sec intervals.  
The standby mode can be released by IRQW.
- 0.5 second interval can be set with the main system clock and subsystem clock.
- The fast mode enables to set 128-time (3.91 ms) interval useful to program debugging and inspection.
- The fixed frequencies (2.048 kHz) can be output to the P23/BUZ pin for use to generate buzzer sound and trim the system clock oscillator frequency.
- Since the frequency divider can be cleared, the watch can be started from zero second.

Fig. 5-3 Watch Timer Block Diagram



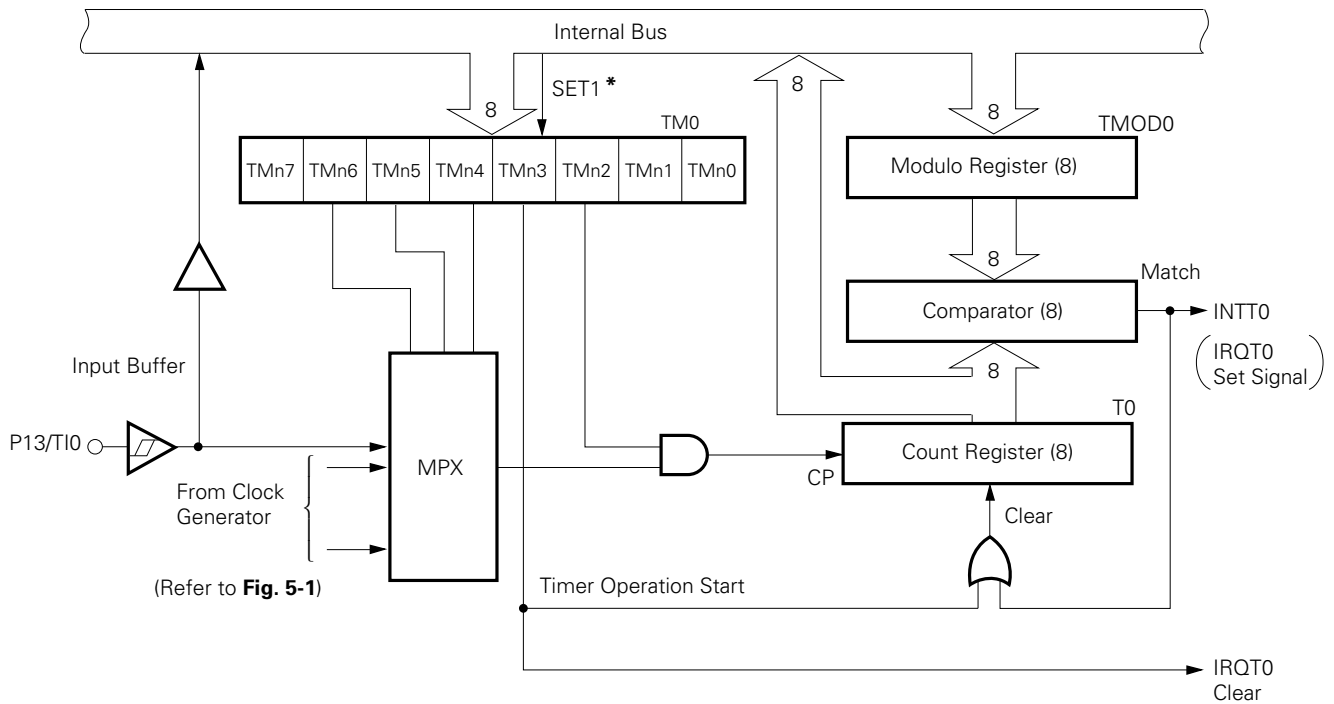
**Remarks** Values at  $f_{xx} = 4.194304$  MHz and  $f_{xt} = 32.768$  kHz are indicated in parentheses.

**5.5 TIMER/EVENT COUNTER**

The μPD75208 incorporates one channel of timer/event counter. The timer/event counter has the following functions:

- Program interval timer operation
- Event counter operation
- Count state read function

**Fig. 5-4 Timer/Event Counter Block Diagram**



\* Instruction execution

**5.6 TIMER/PULSE GENERATOR**

The μPD75208 incorporates one channel of timer/pulse generator which can be used as a timer or a pulse generator. The timer/pulse generator has the following functions:

- (a) Functions available in the timer mode
  - 8-bit interval timer operation (IRQTPG generation) enabling the clock source to be varied at 5 levels
  - Square wave output to PPO pin
- (b) Functions available in the PWM pulse generate mode
  - 14-bit accuracy PWM pulse output to the PPO pin (Used as a digital-to-analog converter and applicable to tuning)
  - Fixed time interval ( $\frac{2^{15}}{f_{xx}} = 7.81 \text{ ms}$  : at 4.19 MHz operation) interrupt generation

If pulse output is not necessary, the PPO pin can be used as a 1-bit output port.

**Note** If the STOP mode is set while the timer/pulse generator is in operation, erroneous operation may result. To prevent that from occurring, preset the timer/pulse generator to the stop state using its mode register.

**Fig. 5-5 Block Diagram of Timer/Pulse Generator (Timer Mode)**

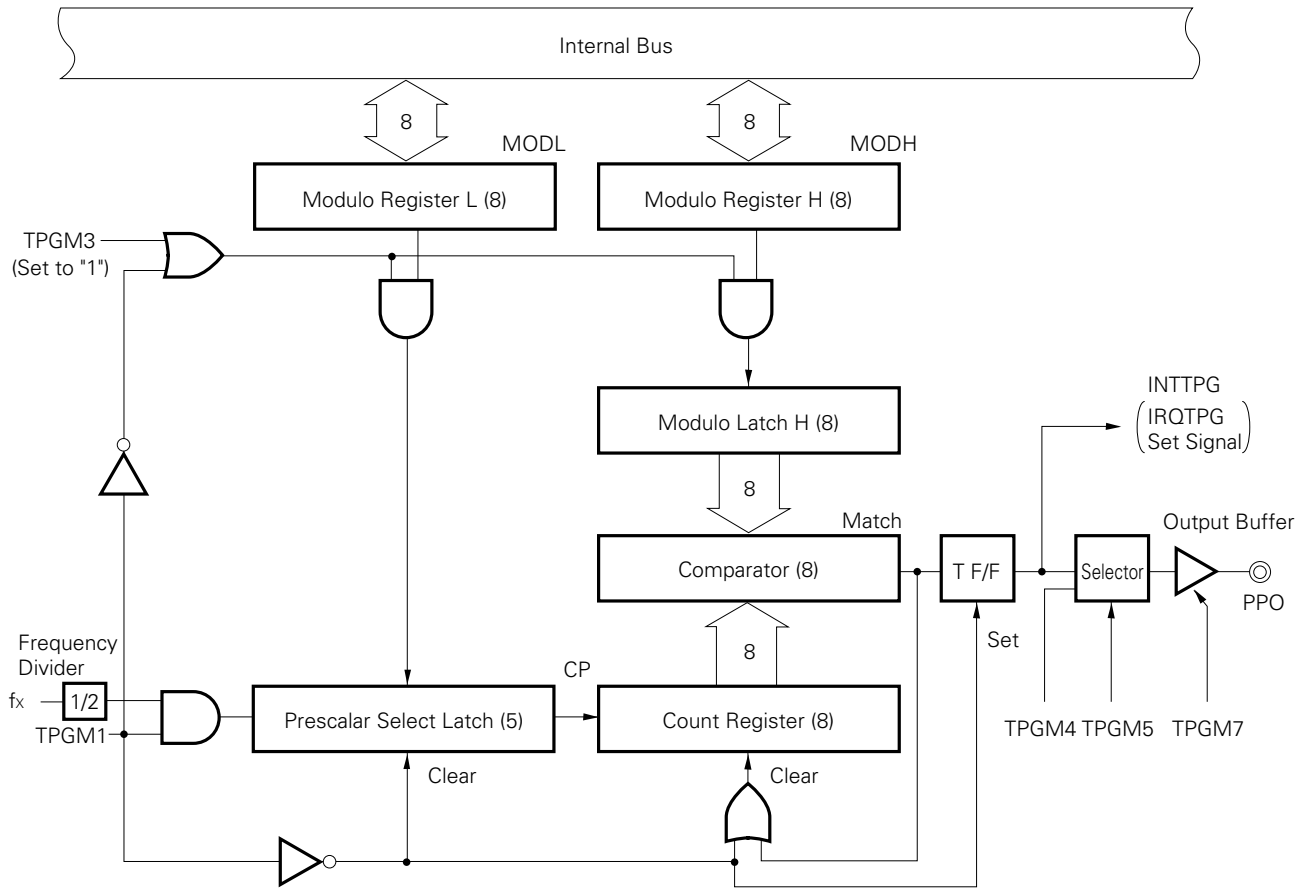
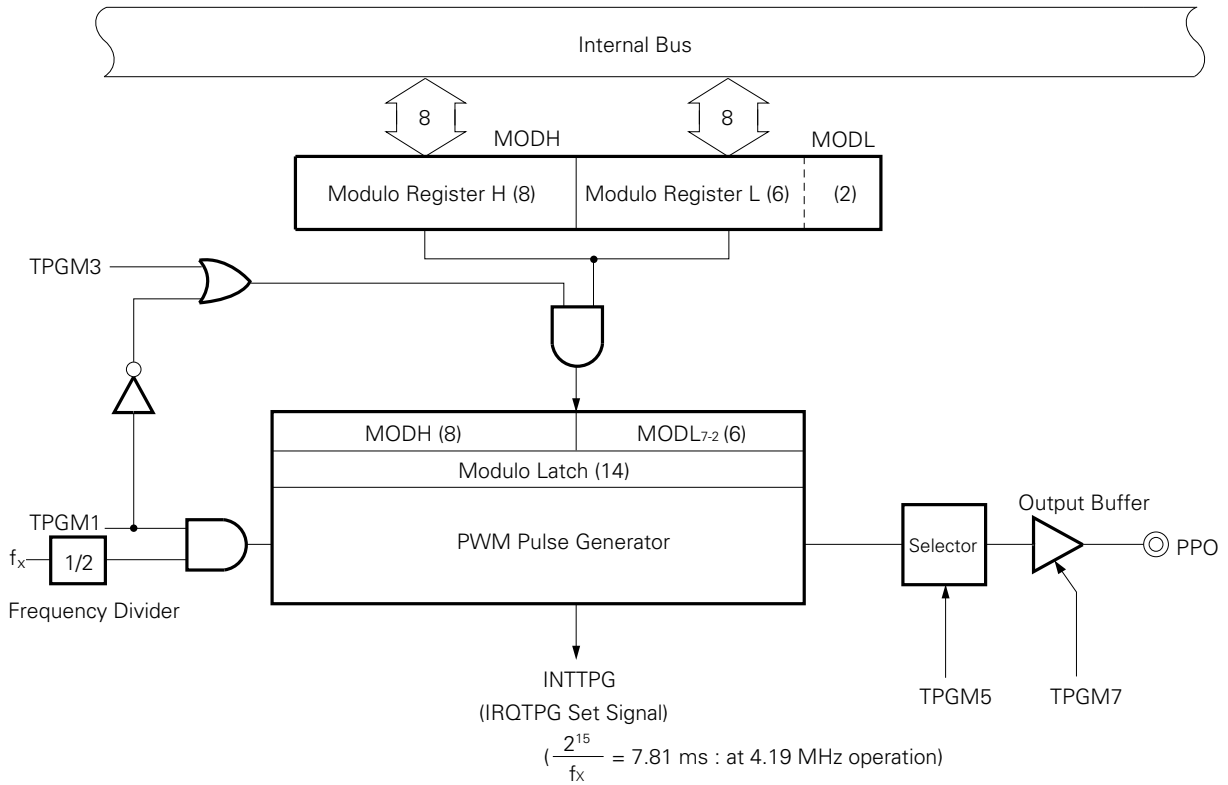


Fig. 5-6 Timer/Pulse Generator Block Diagram (PWM Pulse Generate Mode)



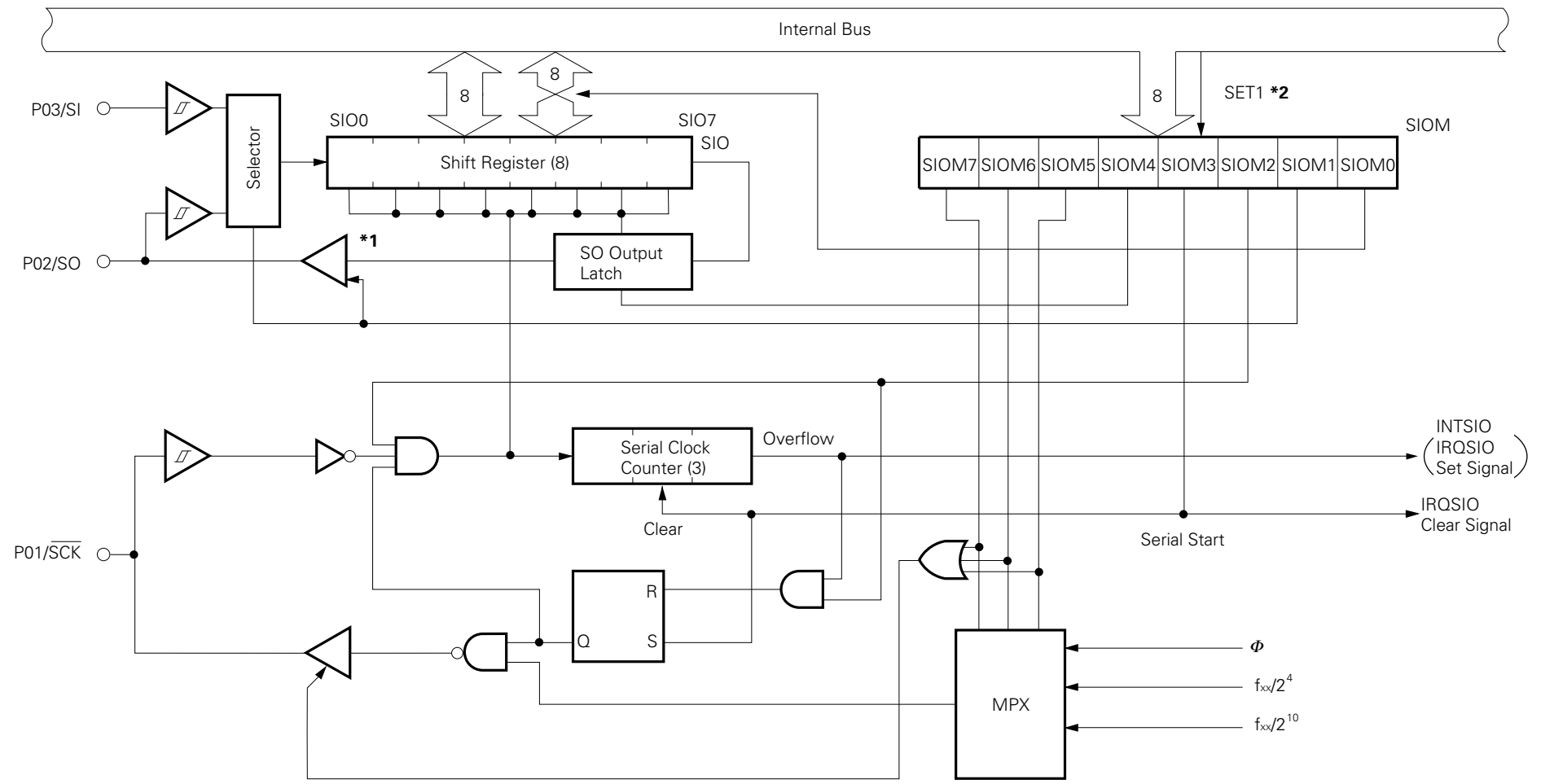
### 5.7 SERIAL INTERFACE

The serial interface has the following functions:

- Clock synchronous 8-bit send/receive operation (simultaneous send/receive)
- Clock synchronous 8-bit serial bus operation (data input/output from the SO pin. N-ch open-drain SO output)
- Start LSB/MSB switching

These functions facilitate data communication with another microcomputer of μPD7500 series or 78K series via a serial bus and coupling with peripheral devices.

Fig 5-7 Serial Interface Block Diagram



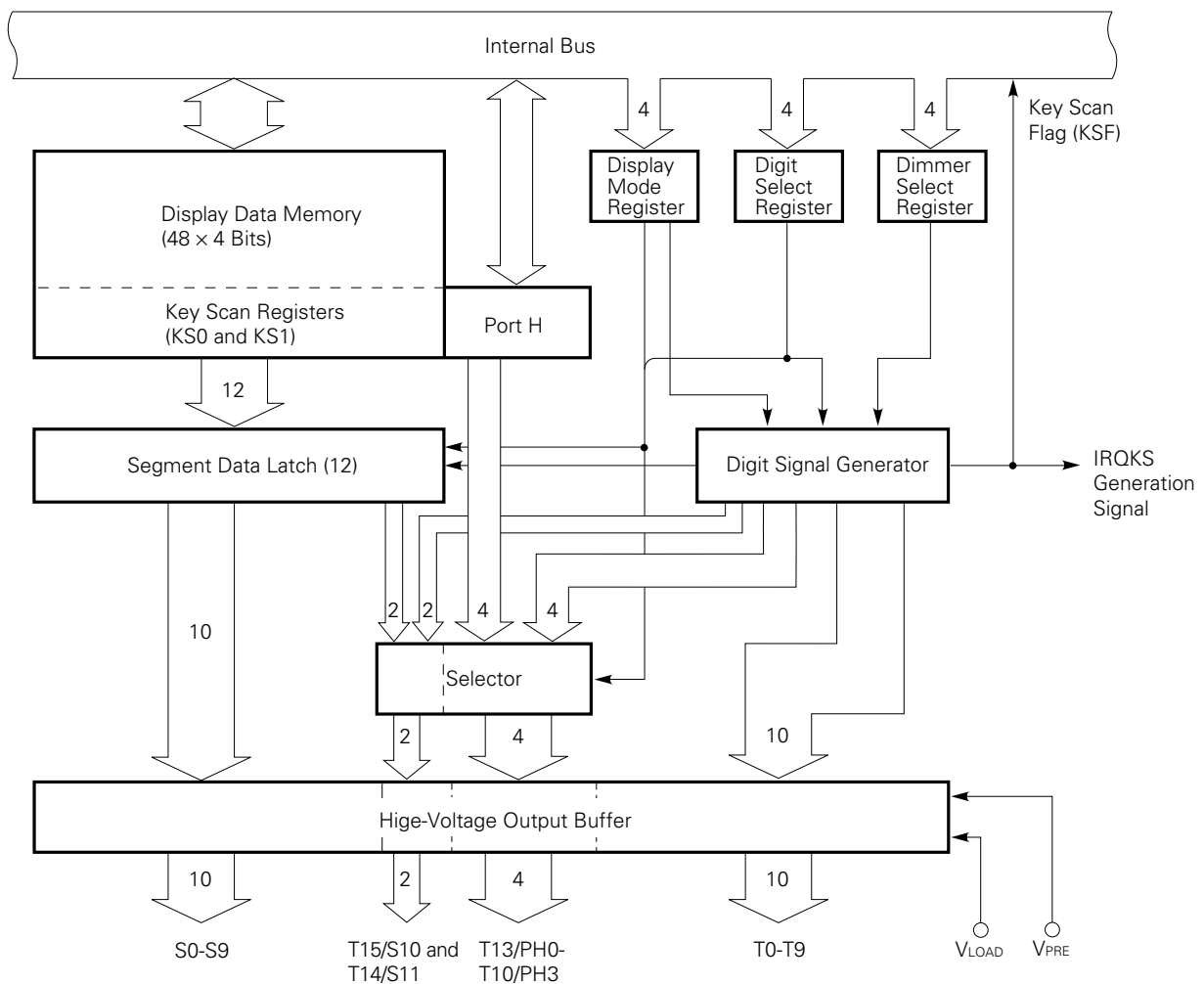
\* 1. CMOS output and N-ch open-drain output switchable output buffer.  
 2. Instruction execution

**5.8 FIP CONTROLLER/DRIVER**

The on-chip FIP controller/driver has the following functions:

- Generates the segment and digit signals by automatically reading the display data memory executing DMA operation.
- Can select up to a total of 26 display devices in the range of 9 to 12 segments and 9 to 16 digits.
- Can apply the remaining display output as static output.
- Can adjust the brightness at 8 levels using the dimmer function.
- Can apply key scan operations.
  - Generates interrupt at the key scan timing (IRQKS)
  - Can generate key scan data output from the segment output pin.
- Owns the high-voltage output pin (40 V) which can directly drive the FIP.
  - Segment special pins (S0 to S9) :  $V_{OD} = 40\text{ V}$ ,  $I_{OD} = 3\text{ mA}$
  - Digit output pins (T0 to T15) :  $V_{OD} = 40\text{ V}$ ,  $I_{OD} = 15\text{ mA}$
- Can incorporate pull-down resistors bit-wise as mask options.

**Fig. 5-8 FIP Controller/Driver Block Diagram**



**Note** The FIP controller/driver can only operate in the high and intermediate-speeds (PCC = 0011B or 0010B) of the main system clock (SCC.0 = 0). It may cause errors with any other clock or in the standby mode. Thus, be sure to stop FIP controller operation (DSPM.3 = 0) and then shift the unit to any other clock mode or the standby mode.

### 5.9 POWER-ON FLAG (MASK OPTION)

The power-on flag (PONF) is automatically set (1) when the power-on reset circuit is activated and the power-on reset signal is generated. (See **Fig. 8-1 Reset Signal Generator**)

The PONF is mapped at bit 0 of address FD1H in the data memory space and can be tested by the memory bit manipulation instructions (SKT, SKF, SKTCLR) or cleared (CLR1).

**Note** The PONF cannot be set by SET1 instruction.

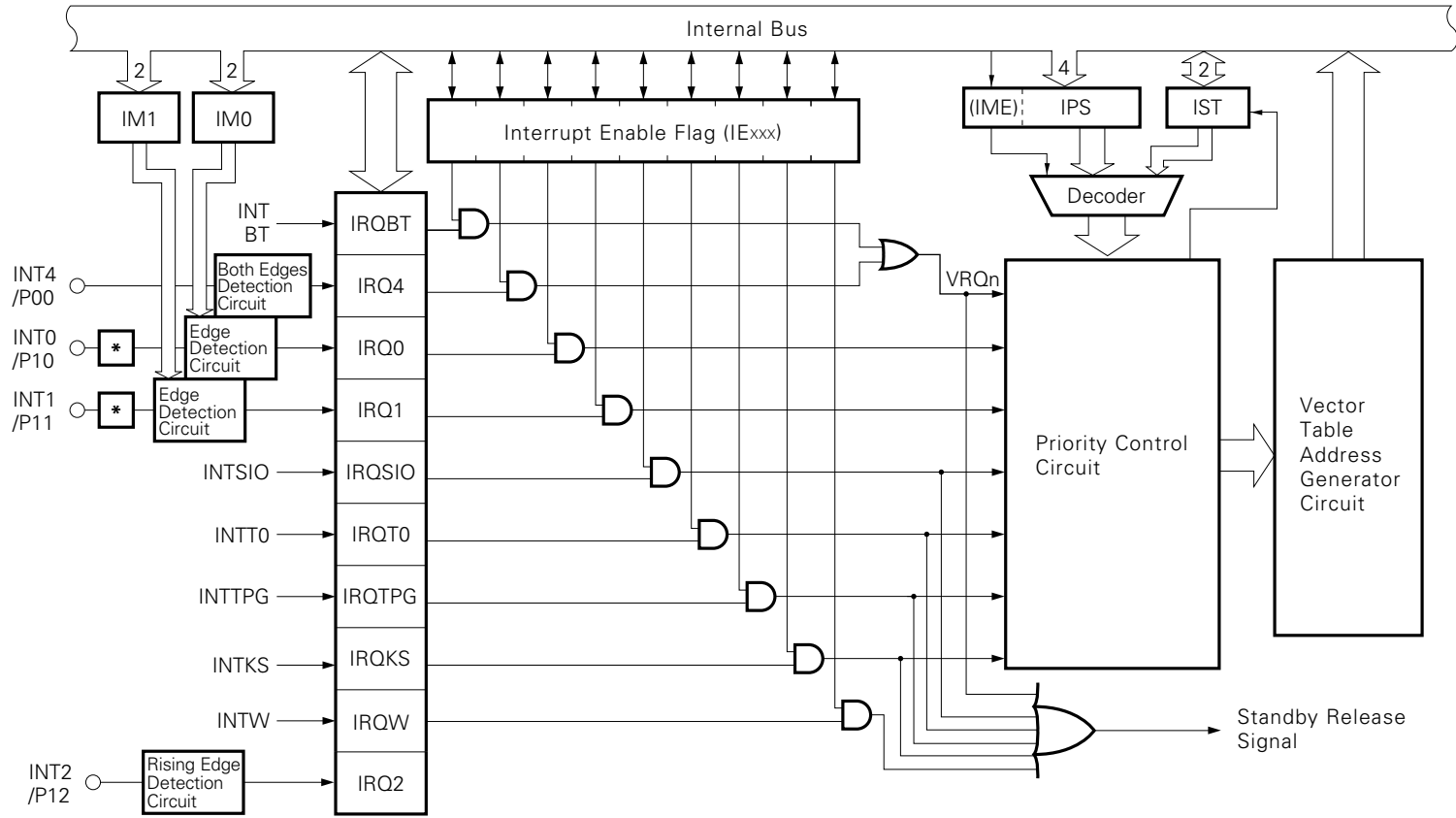
## 6. INTERRUPT FUNCTIONS

The μPD75208 has eight types of interrupt sources and can generate multiple interrupts with priority order. It is also equipped with two types of test sources. INT2 is an edge detected testable input.

The μPD75208 interrupt control circuit has the following functions:

- Hardware-controller vectored interrupt function which can control interrupt acknowledge with the interrupt enable flag (IE<sub>xxx</sub>) and the interrupt master enable flag (IME).
- Function of setting any interrupt start address.
- Multiple interrupt function which can specify priority order with the interrupt priority select register (IPS).
- Interrupt request flag (IRQ<sub>xxx</sub>) test function. (Interrupt generation can be checked by software.)
- Standby mode release function. (Interrupt to be released by interrupt enable flag can be selected.)

Fig. 6-1 Interrupt Control Circuit Block Diagram



\* Noise Eliminator



## 7. STANDBY FUNCTIONS

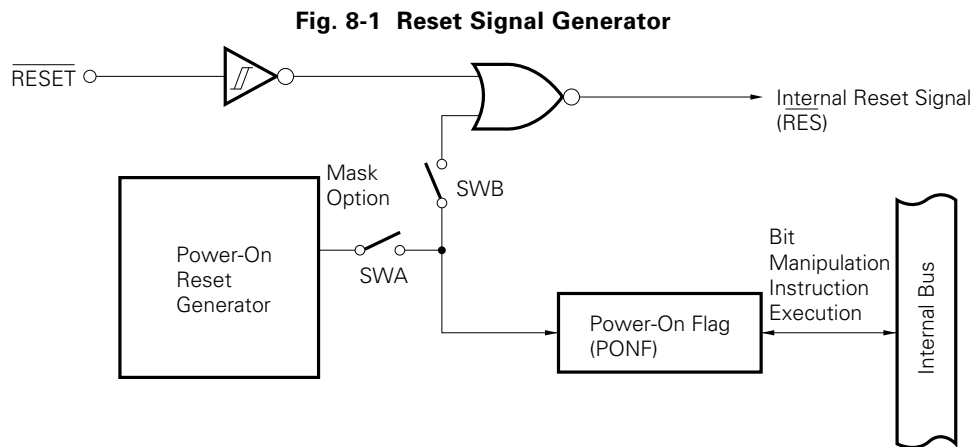
Two standby modes (STOP mode and HALT mode) are available for the μPD75208 to decrease power consumption in the program standby mode.

**Table 7-1 Operation Status in Standby Mode**

		STOP Mode	HALT Mode
Set instruction		STOP instruction	HALT instruction
System clock when set		Setting enabled only with main system clock.	Setting enabled with either main system clock or subsystem clock.
Operating State	Clock oscillator	Oscillator stops only with main system clock.	Stops only with CPU clock $\Phi$ (Oscillation continued).
	Basic interval timer	Operation stopped.	Operation (IRQBT set at reference time intervals).
	Serial interface	Operation enabled only when external $\overline{SCK}$ input is selected for serial clock.	Operation enabled when serial clock other than $\Phi$ is specified.
	Timer/event counter	Operation enabled only when T10 pin input is specified for count clock.	Operation enabled.
	Timer/pulse generator	Operation stopped.	Operation enabled.
	Watch timer	Operation enabled only fXT is selected for count clock.	Operation enabled.
	FIP controller/driver	Operation disabled (display off mode set before disabling).	
	CPU	Operation stopped.	
Release signal		Interrupt request signal (except INT0, INT1, INT2) or $\overline{RESET}$ input enabled by interrupt enable flag.	

## 8. RESET FUNCTIONS

The reset signal ( $\overline{RES}$ ) generator has a configuration shown in Fig. 8-1.



The power-on reset generator is a circuit to generate a one-shot pulse upon detection of the start-up of the power voltage. This pulse is used in three ways according to SWA, SWB mask option specification shown in Fig. 8-1. (See 10. MASK OPTION SELECTION.)

## 9. INSTRUCTION SET

### (1) Operand identifier and description

Enter an operand in the operand column of each instruction using the description method relating to the operand identifier of the instruction (refer to **RA75X Assembler Package User's Manual, Language (EEU-730)** for details). If more than one description method is available, select one. Capital alphabetic letters, plus and minus signs are keywords. Describe them as they are.

In the case of immediate data, describe appropriate numerical values or labels.

Identifier	Description Method
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL-, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label* 2-bit immediate data or label
fmem pmem	FB0H to FBFH and FF0H to FFFH immediate data or labels FC0H to FFFH immediate data or labels
addr caddr faddr	0000H to 1F7FH immediate data or labels 12-bit immediate data or label 11-bit immediate data or label
taddr	20H to 7FH immediate data (bit0 = 0) or label
PORTn IExxx RBn MBn	PORT0 to PORT6 IEBT, IESIO, IET0, IETPG, IE0, IE1, IEKS, IEW, IE4 RB0 to RB3 MB0, MB1, MB15

\* For 8-bit data processing, only even addresses can be specified.

**(2) Legend for operation description**

A	: A register; 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: Register pair (XA); 8-bit accumulator
BC	: Register pair (BC)
DE	: Register pair (DE)
HL	: Register pair (HL)
XA'	: Expanded register pair (XA')
BC'	: Expanded register pair (BC')
DE'	: Expanded register pair (DE')
HL'	: Expanded register pair (HL')
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; Bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORT <sub>n</sub>	: Port n (n = 0 to 6)
IME	: Interrupt master enable flag
IPS	: Interrupt priority select register
IE <sub>xxx</sub>	: Interrupt enable flag
RBS	: Register bank select register
MBS	: Memory bank select register
PCC	: Processor clock control register
•	: Address and bit delimiter
(xx)	: Contents addressed by xx
xxH	: Hexadecimal data

**(3) Description of symbols in the addressing area column**

* 1	MB = MBE • MBS (MBS = 0, 1, 15)	Data Memory Addressing
* 2	MB = 0	
* 3	MBE = 0 : MB = 0 (00H to 7FH) MB = 15 (80H to FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
* 4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
* 5	MB = 15, pmem = FC0H to FFFH	
* 6	addr = 0000H to 1F7FH	Program Memory Addressing
* 7	addr = (Current PC) – 15 to (Current PC) – 1, (Current PC) + 2 to (Current PC) + 16	
* 8	caddr = 0000H to 0FFFH (PC <sub>12</sub> = 0) or 1000H to 1F7FH (PC <sub>12</sub> = 1)	
* 9	faddr = 0000H to 07FFH	
* 10	taddr = 0020H to 007FH	

- Remarks**
1. MB indicates accessible memory bank.
  2. In \*2, MB = 0 irrespective of MBE and MBS.
  3. In \*4 and \*5, MB = 15 irrespective of MBE and MBS.
  4. \*6 to \*10 indicate addressable areas.

**(4) Description of the machine cycle column**

S indicates the number of machine cycles required for skip operation by an instruction having skip function.

The S value varies as follows:

- When not skipped ..... S = 0
- When 1-byte or 2-byte instructions are skipped ..... S = 1
- When 3-byte instructions are skipped (BR !addr, CALL !addr instruction) ..... S = 2

**Note** GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle(=tcy) of CPU clock  $\phi$  and three time periods are available according to PCC setting.

Note 1	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A←n4		Stack A
		reg1, #n4	2	2	reg1←n4		
		XA, #n8	2	2	XA←n8		Stack A
		HL, #n8	2	2	HL←n8		Stack B
		rp2, #n8	2	2	rp2←n8		
		A, @HL	1	1	A←(HL)	*1	
		A, @HL+	1	2 + S	A←(HL), then L←L+1	*1	L = 0
		A, @HL-	1	2 + S	A←(HL), then L←L-1	*1	L = FH
		A, @rpa1	1	1	A←(rpa1)	*2	
		XA, @HL	2	2	XA←(HL)	*1	
		@HL, A	1	1	(HL)←A	*1	
		@HL, XA	2	2	(HL)←XA	*1	
		A, mem	2	2	A←(mem)	*3	
		XA, mem	2	2	XA←(mem)	*3	
		mem, A	2	2	(mem)←A	*3	
		mem, XA	2	2	(mem)←XA	*3	
		A, reg	2	2	A←reg		
		XA, rp'	2	2	XA←rp'		
	reg1, A	2	2	reg1←A			
	rp'1, XA	2	2	rp'1←XA			
	XCH	A, @HL	1	1	A↔(HL)	*1	
		A, @HL+	1	2 + S	A↔(HL), then L←L+1	*1	L = 0
		A, @HL-	1	2 + S	A↔(HL), then L←L-1	*1	L = FH
		A, @rpa1	1	1	A↔(rpa1)	*2	
		XA, @HL	2	2	XA↔(HL)	*1	
		A, mem	2	2	A↔(mem)	*3	
		XA, mem	2	2	XA↔(mem)	*3	
		A, reg1	1	1	A↔reg1		
XA, rp'		2	2	XA↔rp'			
Note 2	MOVT	XA, @PCDE	1	3	XA←(PC <sub>12-8</sub> +DE) <sub>ROM</sub>		
		XA, @PCXA	1	3	XA←(PC <sub>12-8</sub> +XA) <sub>ROM</sub>		

- Note** 1. Instruction Group  
2. Table reference

Note	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Bit transfer	MOV1	CY, fmem.bit	2	2	$CY \leftarrow (\text{fmem.bit})$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow (\text{pmem}_{7-2} + L_{3-2}.\text{bit}(L_{1-0}))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow (\text{H+mem}_{3-0}.\text{bit})$	*1	
		fmem.bit, CY	2	2	$(\text{fmem.bit}) \leftarrow CY$	*4	
		pmem.@L, CY	2	2	$(\text{pmem}_{7-2} + L_{3-2}.\text{bit}(L_{1-0})) \leftarrow CY$	*5	
		@H+mem.bit, CY	2	2	$(\text{H+mem}_{3-0}.\text{bit}) \leftarrow CY$	*1	
Operation	ADDS	A, #n4	1	1 + S	$A \leftarrow A + n4$		carry
		XA, #n8	2	2 + S	$XA \leftarrow XA + n8$		carry
		A, @HL	1	1 + S	$A \leftarrow A + (\text{HL})$	*1	carry
		XA, rp'	2	2 + S	$XA \leftarrow XA + rp'$		carry
		rp'1, XA	2	2 + S	$rp'1 \leftarrow rp'1 + XA$		carry
	ADDC	A, @HL	1	1	$A, CY \leftarrow A + (\text{HL}) + CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA + rp' + CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1 + XA + CY$		
	SUBS	A, @HL	1	1 + S	$A \leftarrow A - (\text{HL})$	*1	borrow
		XA, rp'	2	2 + S	$XA \leftarrow XA - rp'$		borrow
		rp'1, XA	2	2 + S	$rp'1 \leftarrow rp'1 - XA$		borrow
	SUBC	A, @HL	1	1	$A, CY \leftarrow A - (\text{HL}) - CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA - rp' - CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1 - XA - CY$		
	AND	A, #n4	2	2	$A \leftarrow A \wedge n4$		
		A, @HL	1	1	$A \leftarrow A \wedge (\text{HL})$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \wedge rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \wedge XA$		
	OR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (\text{HL})$	*1	
XA, rp'		2	2	$XA \leftarrow XA \vee rp'$			
rp'1, XA		2	2	$rp'1 \leftarrow rp'1 \vee XA$			
XOR	A, #n4	2	2	$A \leftarrow A \vee n4$			
	A, @HL	1	1	$A \leftarrow A \vee (\text{HL})$	*1		
	XA, rp'	2	2	$XA \leftarrow XA \vee rp'$			
	rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \vee XA$			

**Note** Instruction Group

Note 1	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Note 2	RORC	A	1	1	$CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \bar{A}$		
Increment/decrement	INCS	reg	1	1 + S	$reg \leftarrow reg + 1$		reg = 0
		rp1	1	1 + S	$rp1 \leftarrow rp1 + 1$		rp1 = 00H
		@HL	2	2 + S	$(HL) \leftarrow (HL) + 1$	*1	(HL) = 0
		mem	2	2 + S	$(mem) \leftarrow (mem) + 1$	*3	(mem) = 0
	DECS	reg	1	1 + S	$reg \leftarrow reg - 1$		reg = FH
		rp'	2	2 + S	$rp' \leftarrow rp' - 1$		rp = FFH
Compare	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, rp'	2	2 + S	Skip if XA = rp'		XA = rp'
Carry flag manipulation	SET1	CY	1	1	$CY \leftarrow 1$		
	CLR1	CY	1	1	$CY \leftarrow 0$		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \bar{CY}$		

- Note**
1. Instruction Group
  2. Accumulator manipulation

Note	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit)←1	*3	
		fmem.bit	2	2	(fmem.bit)←1	*4	
		pmem.@L	2	2	(pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> ))←1	*5	
		@H + mem.bit	2	2	(H+mem <sub>3-0</sub> .bit)←1	*1	
	CLR1	mem.bit	2	2	(mem.bit)←0	*3	
		fmem.bit	2	2	(fmem.bit)←0	*4	
		pmem.@L	2	2	(pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> ))←0	*5	
		@H+mem.bit	2	2	(H+mem <sub>3-0</sub> .bit)←0	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> )) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H+mem <sub>3-0</sub> .bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if (pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> )) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2 + S	Skip if (H+mem <sub>3-0</sub> .bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> ))=1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H+mem <sub>3-0</sub> .bit)=1 and clear	*1	(@H+mem.bit)=1
	AND1	CY, fmem.bit	2	2	CY←CY∧(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY∧(pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> ))	*5	
		CY, @H+mem.bit	2	2	CY←CY∧(H+mem <sub>3-0</sub> .bit)	*1	
	OR1	CY, fmem.bit	2	2	CY←CY∨(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY∨(pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> ))	*5	
CY, @H+mem.bit		2	2	CY←CY∨(H+mem <sub>3-0</sub> .bit)	*1		
XOR1	CY, fmem.bit	2	2	CY←CY⊕(fmem.bit)	*4		
	CY, pmem.@L	2	2	CY←CY⊕(pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> ))	*5		
	CY, @H+mem.bit	2	2	CY←CY⊕(H+mem <sub>3-0</sub> .bit)	*1		
Branch	BR	addr	—	—	PC <sub>12-0</sub> ←addr (Optimum instruction is selected from among BR !addr, BRCB !caddr and BR \$addr by an assembler.)	*6	
		!addr	3	3	PC <sub>12-0</sub> ←addr	*6	
		\$addr	1	2	PC <sub>12-0</sub> ←addr	*7	
	BRCB	!caddr	2	2	PC <sub>12-0</sub> ←PC <sub>12</sub> +caddr <sub>11-0</sub>	*8	
	BR	PCDE	2	3	PC <sub>12-0</sub> ←PC <sub>12-8</sub> +DE		
PCXA		2	3	PC <sub>12-0</sub> ←PC <sub>12-8</sub> +XA			

Note Instruction Group



Note	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition	
Subroutine stack control	CALL	laddr	3	3	(SP-4) (SP-1) (SP-2)←PC <sub>11-0</sub> (SP-3)← MBE, RBE, 0, PC <sub>12</sub> PC <sub>12-0</sub> ←addr, SP←SP-4	*6		
	CALLF	lfaddr	2	2	(SP-4) (SP-1) (SP-2)←PC <sub>11-0</sub> (SP-3)← MBE, RBE, 0, PC <sub>12</sub> PC <sub>12-0</sub> ←00, faddr, SP←SP-4	*9		
	RET		1	3	MBE, RBE, 0, PC <sub>12</sub> ←(SP+1) PC <sub>11-0</sub> ←(SP) (SP+3) (SP+2) SP←SP+4			
	RETS		1	3 + S	MBE, RBE, 0, PC <sub>12</sub> ←(SP+1) PC <sub>11-0</sub> ←(SP) (SP+3) (SP+2) SP←SP+4 then skip unconditionally		Unconditional	
	RETI		1	3	x, x, x, PC <sub>12</sub> ←(SP+1) PC <sub>11-0</sub> ←(SP) (SP+3) (SP+2) PSW←(SP+4) (SP+5), SP←SP+6			
	PUSH	rp		1	1	(SP-1) (SP-2)←rp, SP←SP-2		
		BS		2	2	(SP-1)←MBS, (SP-2)←RBS, SP←SP-2		
	POP	rp		1	1	rp←(SP+1) (SP), SP←SP+2		
BS			2	2	MBS←(SP+1), RBS←(SP), SP←SP+2			
Interrupt control	EI		2	2	IME(IPS.3)←1			
		IE <sub>xxx</sub>	2	2	IE <sub>xxx</sub> ←1			
	DI		2	2	IME(IPS.3)←0			
		IE <sub>xxx</sub>	2	2	IE <sub>xxx</sub> ←0			
Input/output	IN *	A, PORT <sub>n</sub>	2	2	A←PORT <sub>n</sub> (n = 0 to 6)			
		XA, PORT <sub>n</sub>	2	2	XA←PORT <sub>n+1</sub> , PORT <sub>n</sub> (n = 4)			
	OUT *	PORT <sub>n</sub> , A	2	2	PORT <sub>n</sub> ←A (n = 2 to 6)			
		PORT <sub>n</sub> , XA	2	2	PORT <sub>n+1</sub> , PORT <sub>n</sub> ←XA (n = 4)			
CPU control	HALT		2	2	Set HALT Mode (PCC.2←1)			
	STOP		2	2	Set STOP Mode (PCC.3←1)			
	NOP		1	1	No Operation			
Special	SEL	RB <sub>n</sub>	2	2	RBS←n (n = 0 to 3)			
		MB <sub>n</sub>	2	2	MBS←n (n = 0, 1, 15)			

\* MBE = 0 or MBE = 1 and MBS = 15 must be set for execution of IN/OUT instruction

**Note** Instruction Group

Note	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Special	GETI *	taddr	1	3	• TBR instruction $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr+1)$	*10	
					• TCALL instruction $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, 0, PC_{12}$ $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr+1)$ $SP \leftarrow SP-4$		
					• (taddr) (taddr+1) instruction executed in the case of instruction other than TBR and TCALL instructions		Depends on instructions referred to.

\* TBR and TCALL instructions are assembled pseudo-instructions to define the GETI instruction table.

**Note** Instruction Group

### 10. MASK OPTION SELECTION

The μPD75208 has the following mask options enabling or disabling on-chip components.

**(1) Pin**

Pin	Mask Option
P60 to P63	Pull-up resistor incorporation enabled bit-wise
T0/T9	
T10/PH3 to T13/PH0	
T14/S11, T15/S10	
S0 to S9	
XT1, XT2	Deletion of subsystem clock oscillator feedback resistor possible

- Note**
- 1. In a system not using subsystem clocks, power consumption in the STOP mode can be decreased by removing the feedback resistor from the oscillator.**
  - 2. The feedback resistor must be incorporated when the subsystem clock is used.**

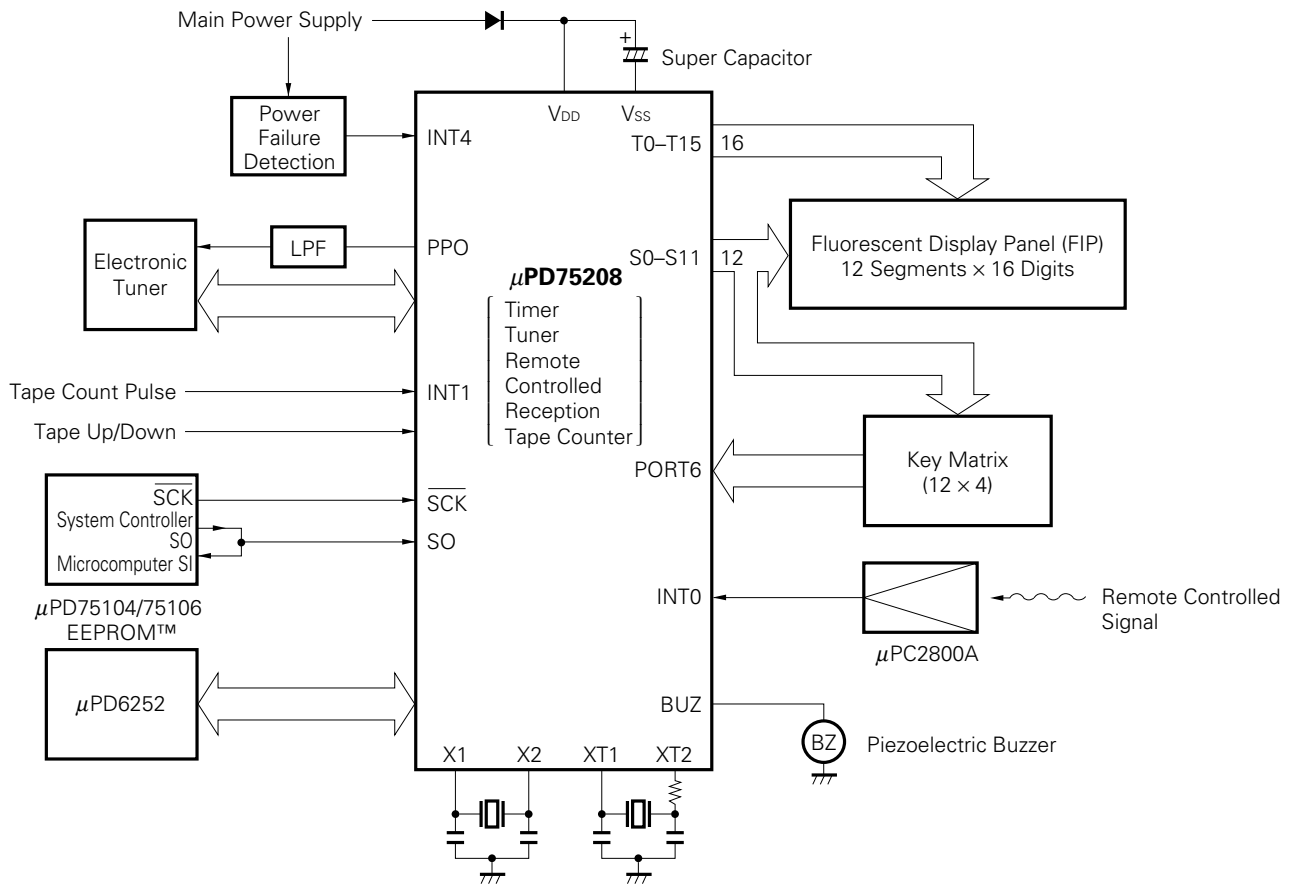
**(2) Power-on reset generator, power-on flag (PONF)**

One of the following three can be selected.

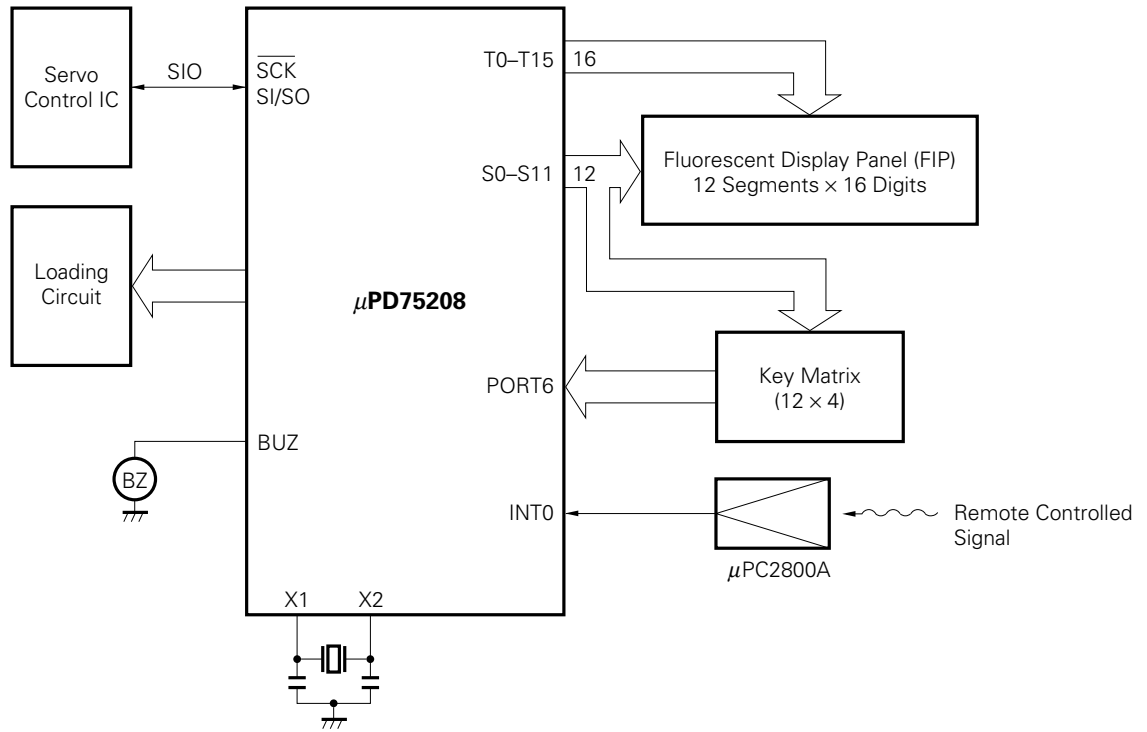
Switch Selection (See Fig. 8-1)		Power-On Reset Generator	Power-On Flag (PONF)	Internal Reset Signal ( $\overline{\text{RES}}$ )
SWA	SWB			
ON	ON	Incorporated	Incorporated	Generate automatically
ON	OFF	Incorporated	Incorporated	Not generate automatically
OFF	OFF	Not incorporated	Not incorporated	—

### 11. APPLICATION BLOCK DIAGRAM

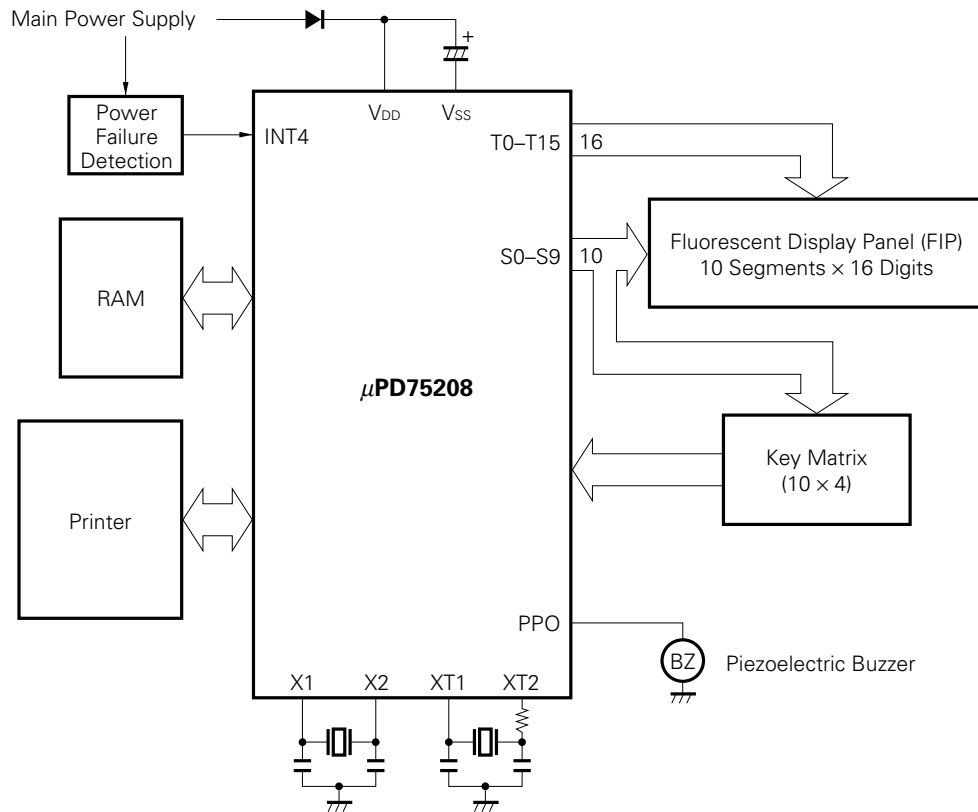
#### 11.1 VCR TIMER TUNER



11.2 COMPACT DISK PLAYER



11.3 ECR



**12. ELECTRICAL SPECIFICATIONS**

**ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)**

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Power supply voltage	V <sub>DD</sub>		-0.3 to +7.0	V
	V <sub>LOAD</sub>		V <sub>DD</sub> -40 to V <sub>DD</sub> +0.3	V
	V <sub>PRE</sub>		V <sub>DD</sub> -12 to V <sub>DD</sub> +0.3	V
Input voltage	V <sub>I</sub>		-0.3 to V <sub>DD</sub> +0.3	V
Output voltage	V <sub>O</sub>	Pins except display output pins	-0.3 to V <sub>DD</sub> +0.3	V
	V <sub>OD</sub>	Display output pins	V <sub>DD</sub> -40 to V <sub>DD</sub> +0.3	V
Output current high	I <sub>OH</sub>	1 pins except display output pins	-15	mA
		S0 to S9 1 pin	-15	mA
		T0 to T15 1 pin	-30	mA
		Total of pins except display output pins	-20	mA
		Total of display output pins	-120	mA
Output current low	I <sub>OL</sub>	1 pin	17	mA
		Total of pins	60	mA
Total loss*1	P <sub>T</sub>	Plastic QFP	450	mW
		Plastic shrink DIP	600	mW
Operating temperature	T <sub>opt</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-65 to +150	°C

**POWER SUPPLY VOLTAGE RANGE (Ta = -40 to +85 °C)**

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
CPU *2		*3	6.0	V
Display controller		4.5	6.0	V
Time/pulse generator		4.5	6.0	V
Other hardware *2		2.7	6.0	V

\* 1. Calculation of total loss

Design so that the sum of the following three power consumption values for the μPD75208CW/GF will be less than the total loss P<sub>T</sub> (It is recommended to use the system with 80 % or less of the rating).

- ① CPU loss : Given as V<sub>DD</sub> (MAX.) × I<sub>DD1</sub> (MAX.)
- ② Output pin loss : There are normal output pin loss and display output pin loss. It is necessary to add a loss derived from the flow of maximum current to each output pin.
- ③ Pull-down register loss : Power loss due to a pull-down resistor incorporated in the display output pin by mask option.

**Example** Suppose 4-LED output with 9<sub>SEG</sub> × 11<sub>DIGIT</sub>, V<sub>DD</sub> = 5 V + 10 % and 4.19 MHz oscillation and let a maximum of 3 mA, 15 mA and 10 mA flow to the segment pin, timing pin and LED output pin, respectively. Further, let the voltage of fluorescent display tube (V<sub>LOAD</sub> voltage) be -30 V and normal voltage be small.

- ① CPU loss : 5.5 V × 9.0 mA = 49.5 mW
- ② Pin loss : Segment pin ..... 2 V × 3 mA × 9 = 54 mW  
Timing pin ..... 2 V × 15 mA = 30 mW  
  
LED output .....  $\left(\frac{10}{15} \times 2 \text{ V}\right) \times 10 \text{ mA} \times 4 = 53 \text{ mW}$
- ③ Pull-down resistor loss .....  $\frac{(30 + 5.5 \text{ V})^2}{40 \text{ k}\Omega} \times 10 = 315 \text{ mW}$

P<sub>T</sub> = ① + ② + ③ = 501.5 mW

In this example, the power consumption of 501.5 mW is less than the allowable total loss for the shrink DIP package (600 mW). However, since the allowable total loss is 450 mW for the QFP package, it is necessary to decrease power consumption by decreasing the number of on-chip pull-down resistors. In this example, power consumption can be adjusted to 344 mW by incorporating pull-down resistors in only 11 digit outputs and 4 segment outputs and externally mounting pull-down resistors to the 5 remaining segment outputs.

- 2. Except the system clock oscillator, display controller and timer/pulse generator.
- 3. The operating voltage range varies depending on the cycle time. Refer to the section describing AC characteristics.

**MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)**

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator*1		Oscillator frequency (f <sub>xx</sub> ) *2	V <sub>DD</sub> = Oscillation voltage range	2.0		5.0*4	MHz
		Oscillation stabilization time *3	After V <sub>DD</sub> reaches the minimum value in the oscillation voltage range			4	ms
Crystal resonator*1		Oscillator frequency (f <sub>xx</sub> ) *2		2.0	4.19	5.0 *4	MHz
		Oscillation stabilization time *3	V <sub>DD</sub> = 4.5 to 6.0 V			10	ms
External clock		X1 input frequency (f <sub>x</sub> ) *2		2.0		5.0*4	MHz
		X1 input high and low level widths (t <sub>xH</sub> , t <sub>xL</sub> )		100		250	ns

- \* 1. Resonators are shown in the following page.
- 2. Oscillator characteristics only. Refer to the description of AC characteristics for details of instruction execution time.
- 3. Time required for oscillation to become stabilized after V<sub>DD</sub> application or STOP mode release.
- ★ 4. When oscillator frequency is " 4.19 < f<sub>x</sub> ≤ 5.0 MHz ", do not select " PCC = 0011 " as instruction execution time. If " PCC = 0011 " is selected, 1 machine cycle becomes less than 0.95 μs, with the result that the specified MIN. value of 0.95 μs cannot be observed.

**SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)**

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator*1		Oscillator frequency (f <sub>XT</sub> ) *2		32	32.768	35	kHz
		Oscillation stabilization time *3	V <sub>DD</sub> = 4.5 to 6.0 V			1.0	2
External clock		XT1 input frequency (f <sub>XT</sub> )		32		100	kHz
		XT1 input high and low level widths (t <sub>xTH</sub> , t <sub>xTL</sub> )		10		32	μs

- \* 1. Recommended resonators are shown in the following page.
- 2. Oscillator characteristics only. Refer to the description of AC characteristics for instruction execution time.
- 3. Oscillation stabilization time is a time required for oscillation to become stabilized after V<sub>DD</sub> application or STOP mode release.



**CAPACITANCE (Ta = 25 °C, VDD = 0 V)**

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance		C <sub>IN</sub>	f = 1 MHz Unmeasured pin returned to 0V			15	pF
Output capacitance	Except display output	C <sub>OUT</sub>				15	pF
	Display output					35	pF
Input /output capacitance		C <sub>IO</sub>				15	pF

**RECOMMENDED OSCILLATOR CONSTANTS**

**MAIN SYSTEM CLOCK : CERAMIC RESONATOR (Ta = -40 to +85 °C)**

MANUFACTURER	PRODUCT NAME	EXTERNAL CAPACITANCE (pF)		OSCILLATION VOLTAGE RANGE (V)	
		C1	C2	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSA 4.19MG	30	30	4.0	6.0
Kyocera Corp.	KBR-2.09MS	68	68	4.0	6.0
	KBR-3.58MS	33	33		
	KBR-4.19MS				
	KBR-4.9M				

**MAIN SYSTEM CLOCK : CRYSTAL RESONATOR (Ta = -40 to +85 °C)**

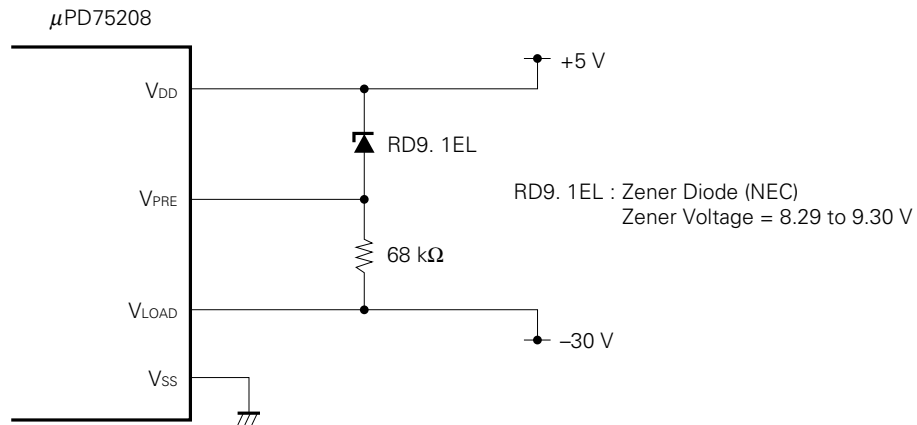
MANUFACTURER	FREQUENCY (MHz)	HOLDER	EXTERNAL CAPACITANCE (pF)		OSCILLATION VOLTAGE RANGE (V)	
			C1	C2	MIN.	MAX.
Kinseki	4.19	HC-49/U	15	15	2.7	6.0

**Note** Carry out fine adjustment of crystal resonator frequency with external capacitance C1 of 10 to 33 pF.

DC CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Input voltage high	V <sub>IH1</sub>	Except below		0.7V <sub>DD</sub>		V <sub>DD</sub>	V	
	V <sub>IH2</sub>	Ports 0, 1, RESET		0.75V <sub>DD</sub>		V <sub>DD</sub>	V	
	V <sub>IH3</sub>	X1, X2, XT1		V <sub>DD</sub> -0.4		V <sub>DD</sub>	V	
	V <sub>IH4</sub>	Port 6	V <sub>DD</sub> = 4.5 to 6.0 V		0.65V <sub>DD</sub>		V <sub>DD</sub>	V
			0.7V <sub>DD</sub>		V <sub>DD</sub>	V		
Input Voltage low	V <sub>IL1</sub>	Except below		0		0.3V <sub>DD</sub>	V	
	V <sub>IL2</sub>	Ports 0, 1, 6, RESET		0		0.2V <sub>DD</sub>	V	
	V <sub>IL3</sub>	X1, X2, XT1		0		0.4	V	
Output voltage high	V <sub>OH</sub>	All output pins	V <sub>DD</sub> = 4.5 to 6.0V, I <sub>OH</sub> = -1 mA	V <sub>DD</sub> -1.0			V	
			I <sub>OH</sub> = -100 μA	V <sub>DD</sub> -0.5			V	
Output voltage low	V <sub>OL</sub>	Ports 4, 5	V <sub>DD</sub> = 4.5 to 6.0V, I <sub>OL</sub> = 15 mA		0.4	2.0	V	
		All output pins	V <sub>DD</sub> = 4.5 to 6.0V, I <sub>OL</sub> = 1.6 mA			0.4	V	
			I <sub>OL</sub> = 400 μA			0.5	V	
Input leakage current high	I <sub>LIH1</sub>	Except X1,X2,XT1	V <sub>IN</sub> = V <sub>DD</sub>			3	μA	
	I <sub>LIH2</sub>	X1, X2, XT1				20	μA	
Input leakage current low	I <sub>LIL1</sub>	Except X1,X2,XT1	V <sub>IN</sub> = 0 V			-3	μA	
	I <sub>LIL2</sub>	X1, X2, XT1				-20	μA	
Output leakage current high	I <sub>LOH</sub>	All output pins	V <sub>OUT</sub> = V <sub>DD</sub>			3	μA	
Output leakage current low	I <sub>LOL1</sub>	Except display output	V <sub>OUT</sub> = 0 V			-3	μA	
	I <sub>LOL2</sub>	Display output	V <sub>OUT</sub> = V <sub>LOAD</sub> = V <sub>DD</sub> - 35 V			-10	μA	
Display output current	I <sub>OD</sub>	S0 to S9	V <sub>DD</sub> = 4.5 to 6.0 V	V <sub>PRE</sub> = V <sub>DD</sub> - 9 ± 1 V*1	-3	-5.5	mA	
			V <sub>PRE</sub> = 0 V	-1.5	-3.5	mA		
		T0 to T15	V <sub>DD</sub> = V <sub>DD</sub> - 2 V	V <sub>PRE</sub> = V <sub>DD</sub> - 9 ± 1 V*1	-15	-22	mA	
			V <sub>PRE</sub> = 0 V	-7	-15	mA		
Built-in pull-down resistor (mask option)	R <sub>P6</sub>	Port 6 V <sub>IN</sub> = V <sub>DD</sub>	V <sub>DD</sub> = 4.5 to 6.0 V	30	80	200	kΩ	
				30		1000	kΩ	
	R <sub>L</sub>	Display output	V <sub>OD</sub> - V <sub>LOAD</sub> = 35 V	40	70	120	kΩ	
Supply current*2	I <sub>DD1</sub>	4.19 MHz crystal oscillation C1 = C2 = 15pF	V <sub>DD</sub> = 5 V ± 10 %*3			3.0	9.0	mA
			V <sub>DD</sub> = 3 V ± 10 %*4			0.55	1.5	mA
	I <sub>DD2</sub>	HALT mode	V <sub>DD</sub> = 5 V ± 10 %			600	1800	μA
			V <sub>DD</sub> = 3 V ± 10 %			200	600	μA
	I <sub>DD3</sub>	32 kHz crystal oscillation*5	V <sub>DD</sub> = 3 V ± 10 %			40	120	μA
	I <sub>DD4</sub>		HALT mode	V <sub>DD</sub> = 3 V ± 10 %			5	15
I <sub>DD5</sub>	XT1 = 0 V STOP mode	V <sub>DD</sub> = 5 V ± 10 %			0.5	20	μA	
		V <sub>DD</sub> = 3 V ± 10 %			0.1	10	μA	

\* 1. The following external circuit is recommended.

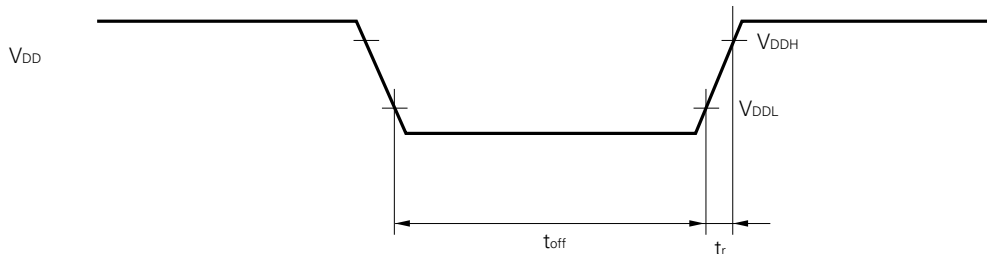


2. Current to the on-chip pull-down resistor and power-on reset circuit (mask option) is not included.
3. When the processor clock control register (PCC) is set to 0011 and is operated in the high-speed mode.
4. When the PCC register is set to 0000 and is operated in the low-speed mode.
5. When the system clock control register (SCC) is set to 1001 and is operated with the subsystem clock with main system clock oscillation stopped.

**POWER-ON RESET CIRCUIT CHARACTERISTICS (MASK OPTION) (Ta = -40 to +85 °C)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-on reset operating voltage high	V <sub>DDH</sub>		4.5		6.0	V
Power-on reset operating voltage low	V <sub>DDL</sub>		0		0.2	V
Power supply voltage rise time	t <sub>r</sub>		10		*1	μs
Power supply voltage off time	t <sub>off</sub>		1			s
Power-on reset circuit*2 current consumption	I <sub>DDPR</sub>	V <sub>DD</sub> = 5 V ±10 %		10	100	μA
		V <sub>DD</sub> = 2.7 V		2	20	μA

- \* 1. 2<sup>17</sup>/f<sub>xx</sub> (31.3 ms at f<sub>xx</sub> = 4.19 MHz)
2. Current with on-chip power-on reset circuit or power-on flag.

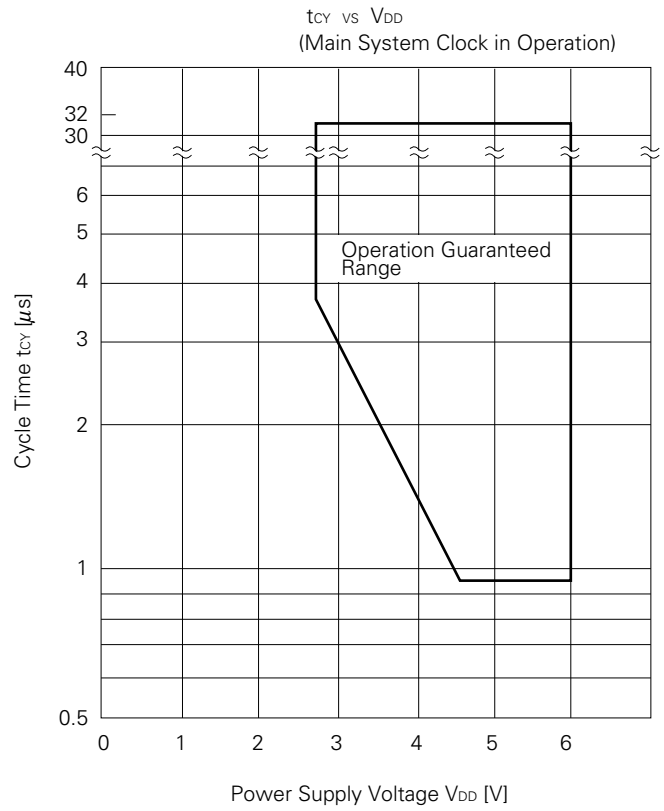


**Remarks** Start the power supply smoothly.

AC CHARACTERISTICS (Ta = -40 to +85 °C , VDD = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time = 1 machine cycle) *1	t <sub>cy</sub>	Operation with main system clock	V <sub>DD</sub> = 4.5 to 6.0 V	0.95		32	μs
				3.8		32	μs
		Operation with sub- system clock		114	122	125	μs
TIO input frequency	f <sub>TI</sub>	V <sub>DD</sub> = 4.5 to 6.0 V		0		0.6	MHz
				0		165	kHz
TIO input high and low- level widths	t <sub>TIH</sub> , t <sub>TIL</sub>	V <sub>DD</sub> = 4.5 to 6.0 V		0.83			μs
				3			μs
SCK cycle time	t <sub>kcy</sub>	V <sub>DD</sub> = 4.5 to 6.0 V	Input	0.8			μs
			Output	0.95			μs
			Input	3.2			μs
			Output	3.8			μs
SCK high and low-level widths	t <sub>KH</sub> , t <sub>KL</sub>	V <sub>DD</sub> = 4.5 to 6.0 V	Input	0.4			μs
			Output	t <sub>kcy</sub> /2-50			ns
		Input	1.6			μs	
		Output	t <sub>kcy</sub> /2-150			ns	
SI setup time (to SCK↑)	t <sub>SIK</sub>			100			ns
SI hold time (from SCK↑)	t <sub>SI</sub>			400			ns
SO output delay time from SCK↓	t <sub>KSO</sub>	V <sub>DD</sub> = 4.5 to 6.0 V				300	ns
						1000	ns
Interrupt input high and low-level widths	t <sub>INTH</sub> , t <sub>INTL</sub>			INT0	*2		μs
				INT1	2t <sub>cy</sub>		μs
				INT2, 4	10		μs
RESET low-level width	t <sub>RSL</sub>			10			μs

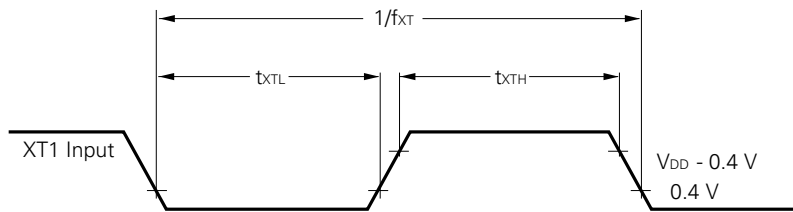
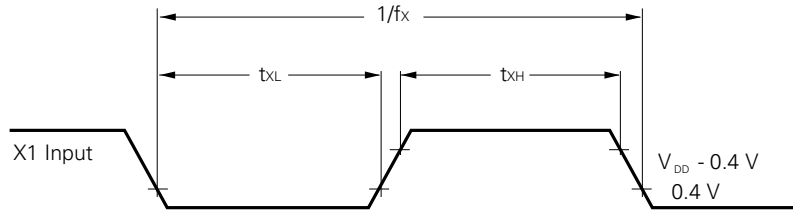
- \* 1. CPU clock ( $\Phi$ ) cycle time is determined by the oscillator frequency of the connected resonator, the system clock control register (SCC) and the processor clock control register (PCC). The cycle time  $t_{CY}$  characteristics for power supply voltage  $V_{DD}$  when the main system clock is in operation is shown below.
- 2.  $2t_{CY}$  or  $128/f_{XX}$  is set by interrupt mode register (IM0) setting.



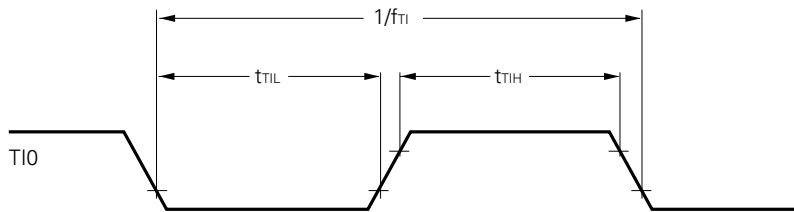
**AC Timing Measurement Values (Except X1 and XT1 Inputs)**



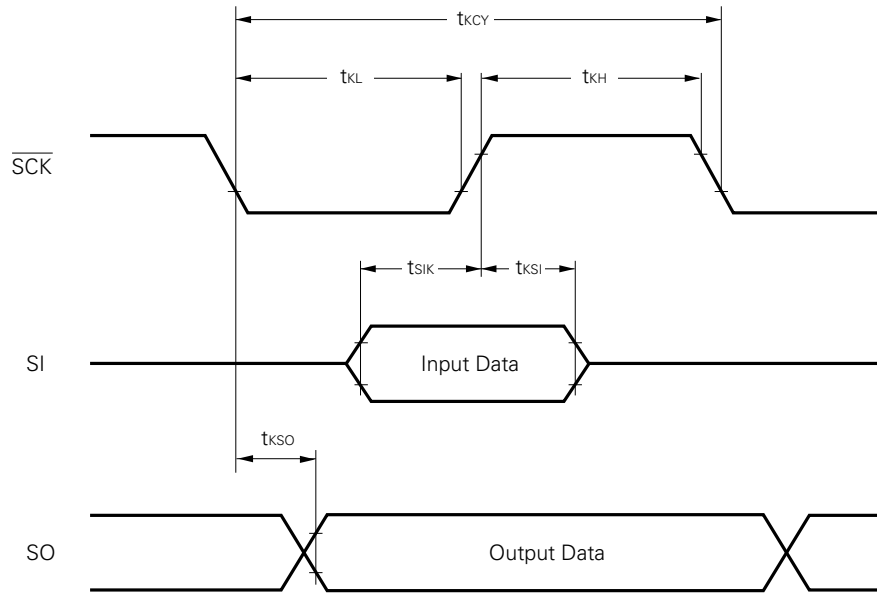
**Clock Timing**



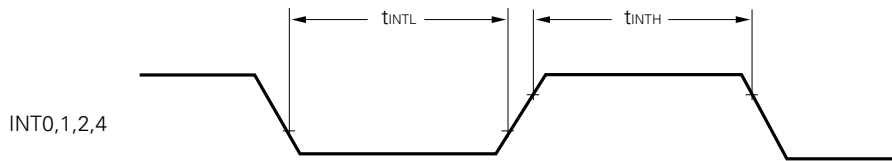
**T10 Timing**



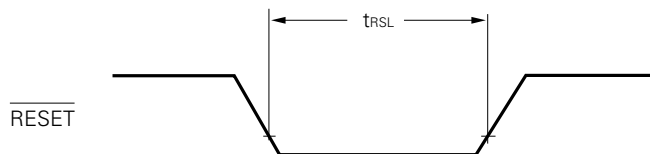
**Serial Transfer Timing**



**Interrupt Input Timing**



**$\overline{\text{RESET}}$  Input Timing**



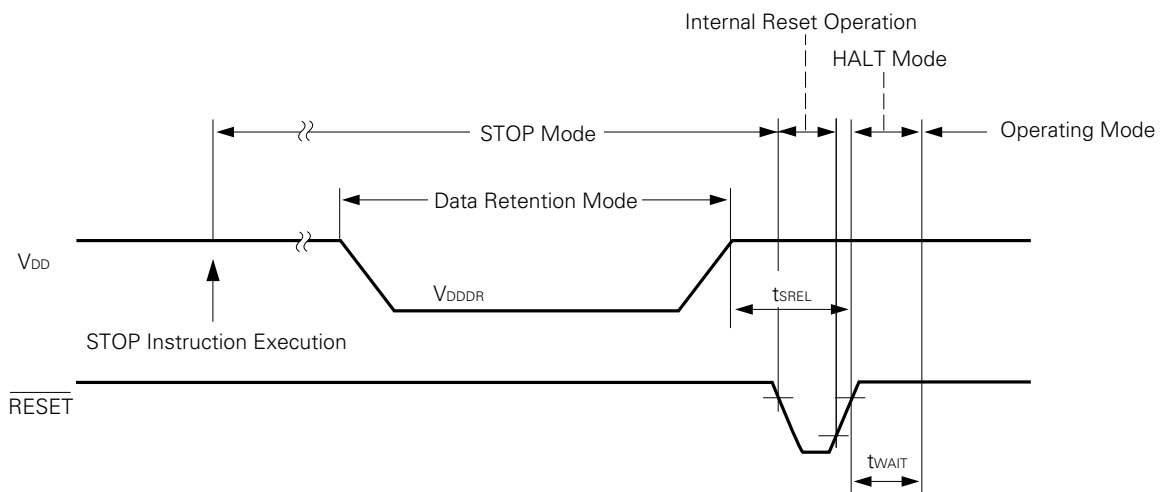
**DATA MEMORY STOP MODE LOW POWER SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = -40 to +85 °C)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention power supply voltage	V <sub>DDDR</sub>		2.0		6.0	V
Data retention power supply current *1	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 2.0V		0.1	10	μA
Release signal set time	t <sub>SREL</sub>		0			μs
Oscillation stabilization wait time *2	t <sub>WAIT</sub>	Release by $\overline{\text{RESET}}$		2 <sup>17</sup> /f <sub>x</sub>		ms
		Release by interrupt request		*3		ms

- \* 1. Current to the on-chip pull-down resistor and power-on reset circuit (mask option) is not included.
- 2. Oscillation stabilization wait time is time to stop CPU operation to prevent unstable operation upon oscillation start.
- 3. According to the setting of the basic interval timer mode register (BTM) (see below).

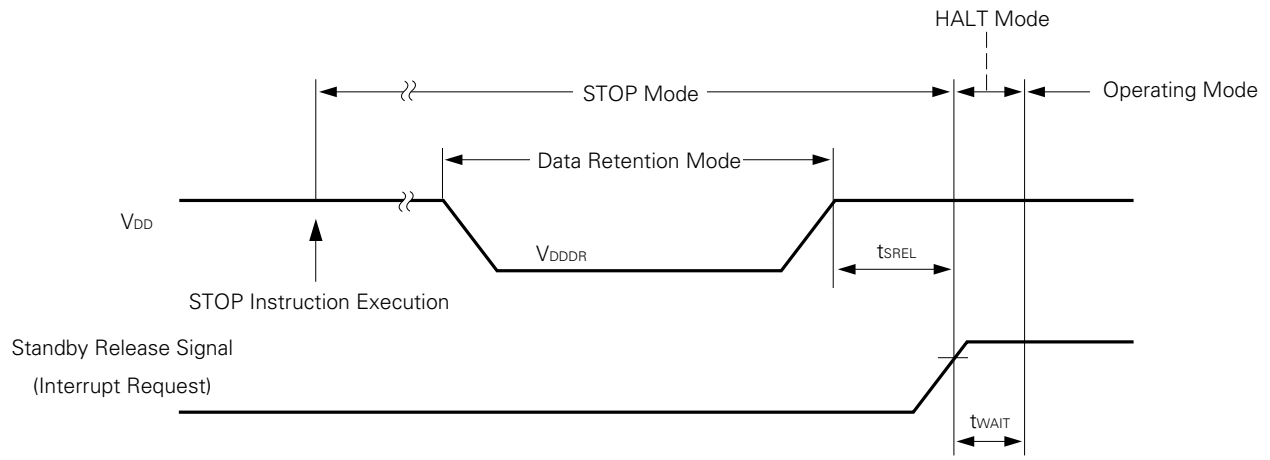
BTM3	BTM2	BTM1	BTM0	Wait Time (Values at f <sub>xx</sub> = 4.19 MHz in parentheses)
—	0	0	0	2 <sup>20</sup> /f <sub>x</sub> (approx. 250 ms)
—	0	1	1	2 <sup>17</sup> /f <sub>x</sub> (approx. 31.3 ms)
—	1	0	1	2 <sup>15</sup> /f <sub>x</sub> (approx. 7.82 ms)
—	1	1	1	2 <sup>13</sup> /f <sub>x</sub> (approx. 1.95 ms)

**Data Retention Timing (STOP Mode Release by  $\overline{\text{RESET}}$ )**

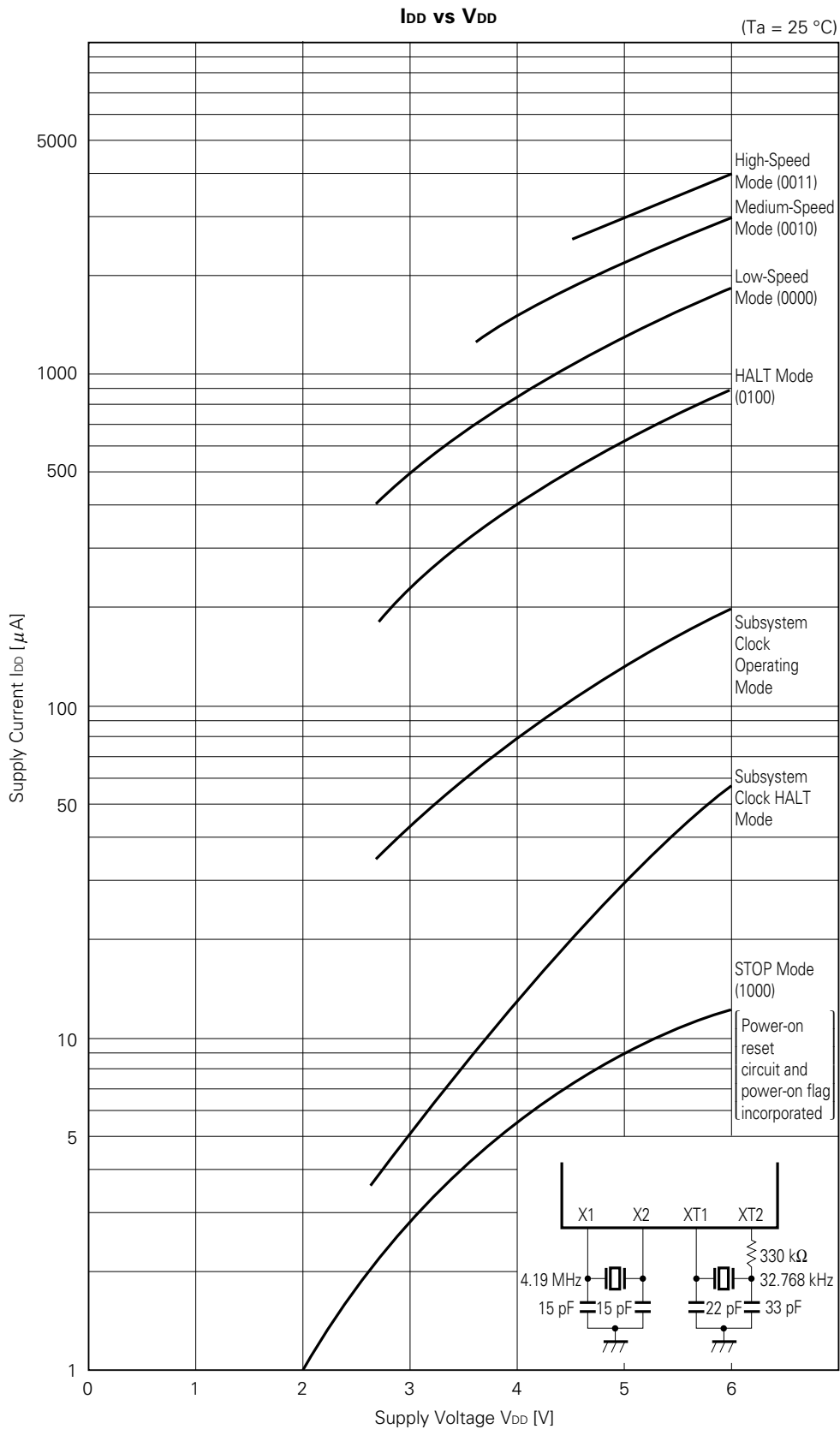




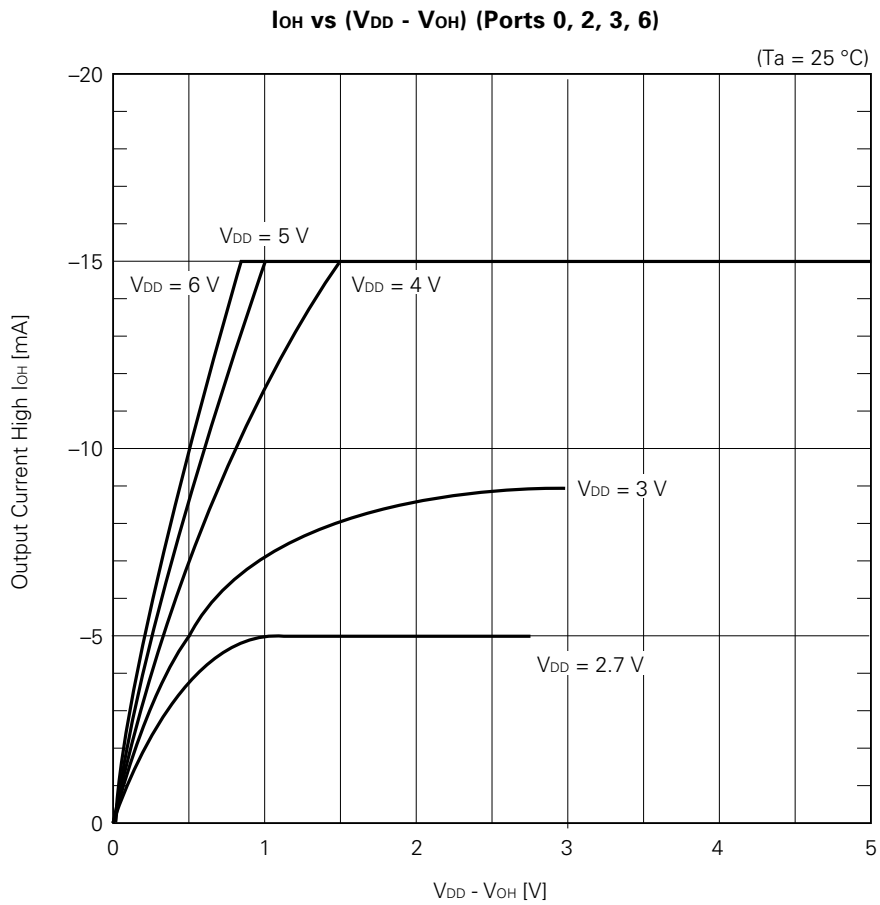
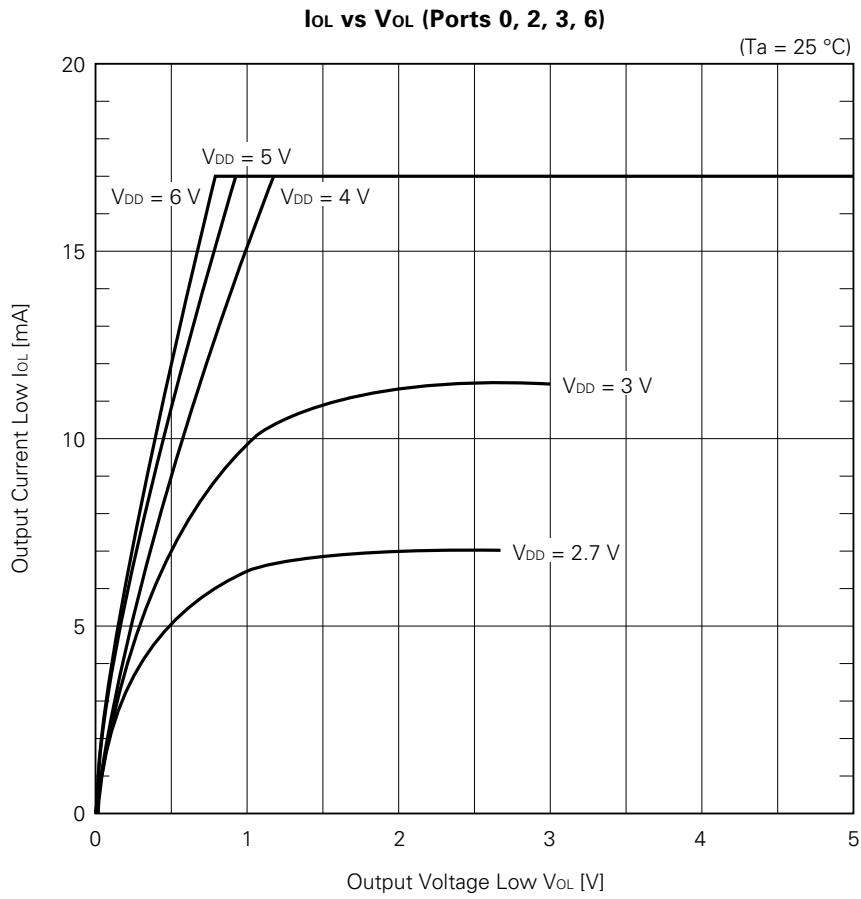
**Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)**



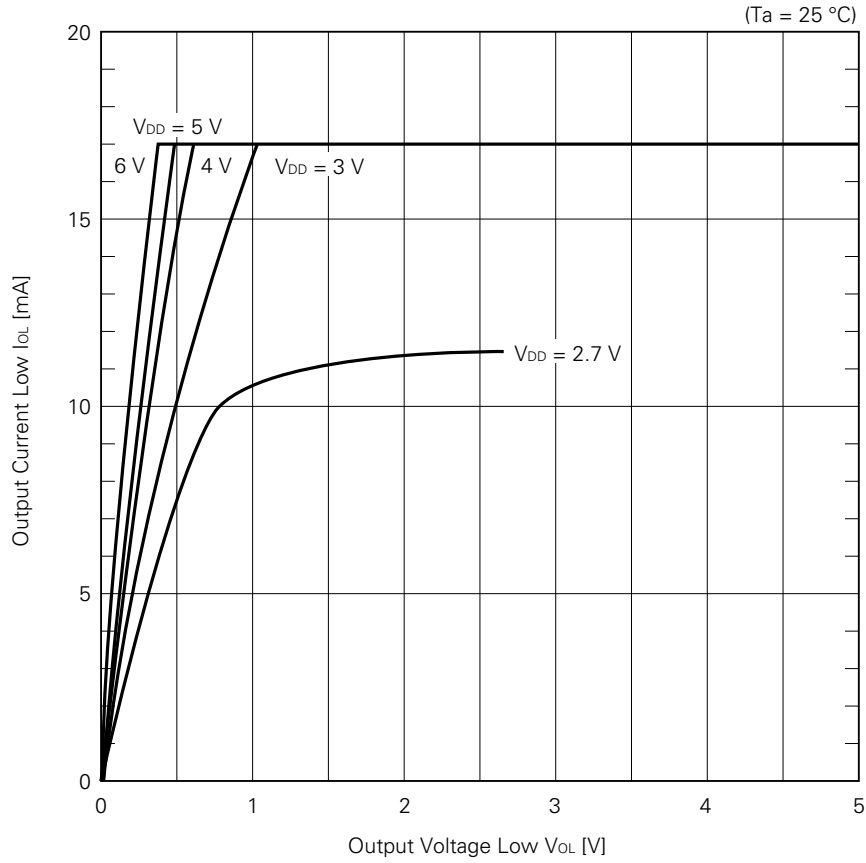
13. CHARACTERISTIC CURVES



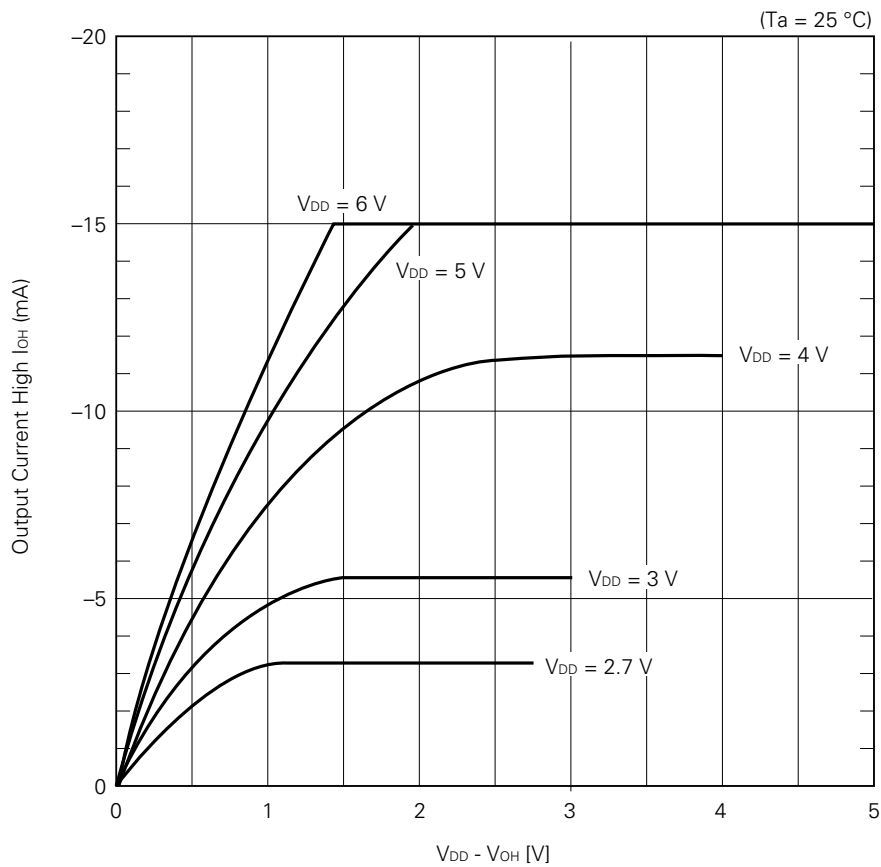
**Remarks** Values of the processor clock control register (PCC) is indicated in parenthesis.



**I<sub>OL</sub> vs V<sub>OL</sub> (Ports 4, 5)**

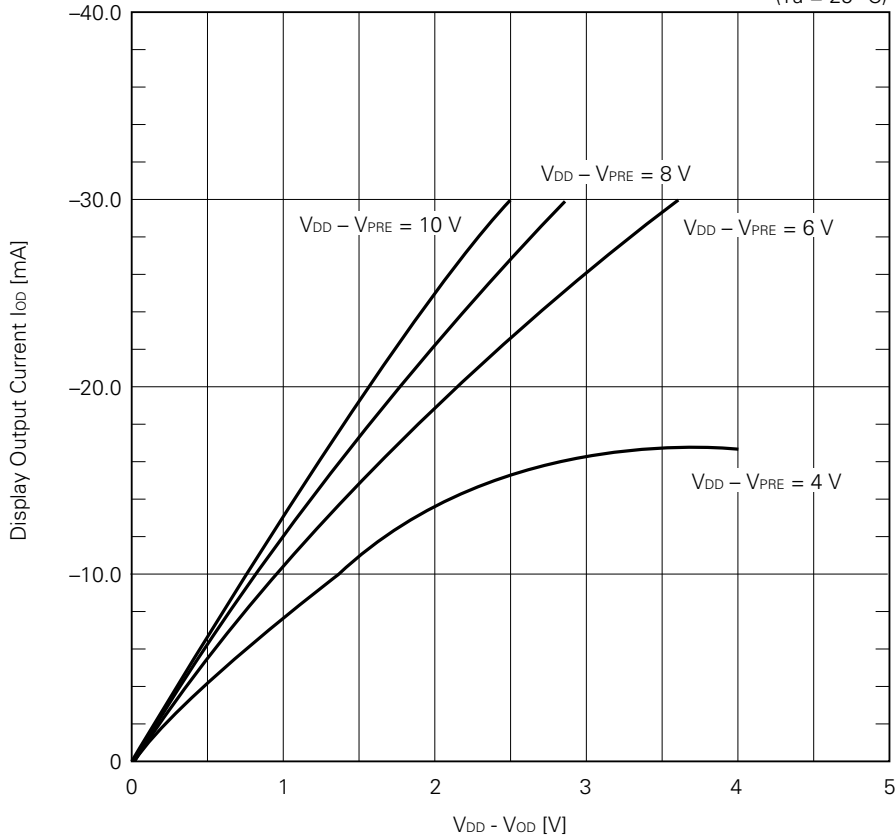


**I<sub>OH</sub> vs (V<sub>DD</sub> - V<sub>OH</sub>) (Ports 4, 5)**



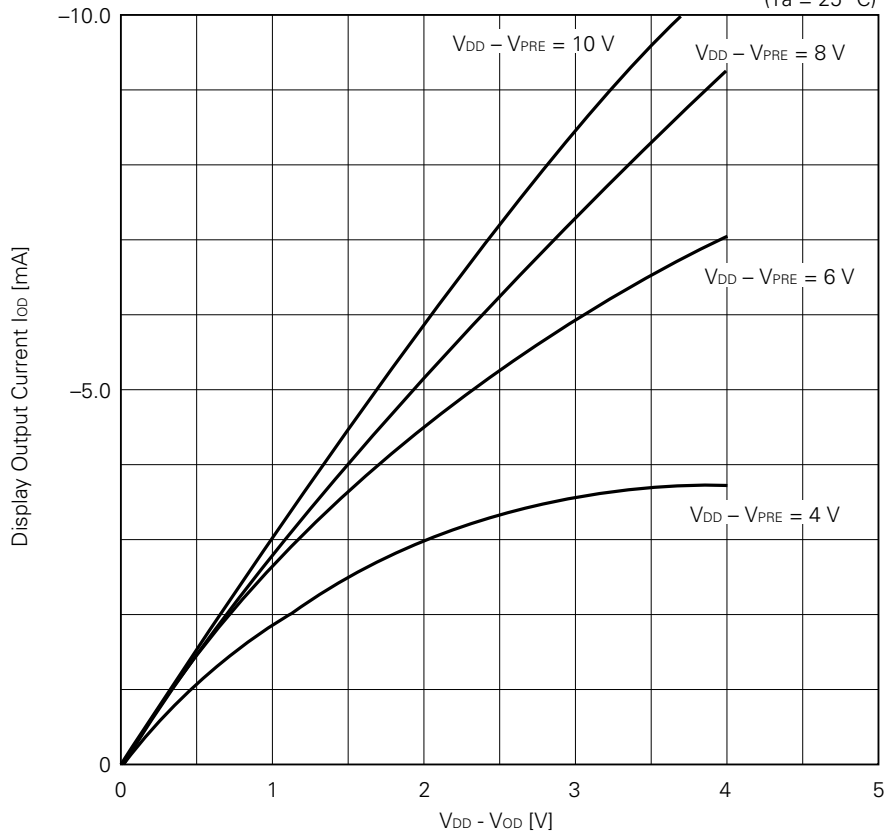
**I<sub>OD</sub> vs (V<sub>DD</sub> - V<sub>OD</sub>) (T0 to T15)**

(T<sub>a</sub> = 25 °C)



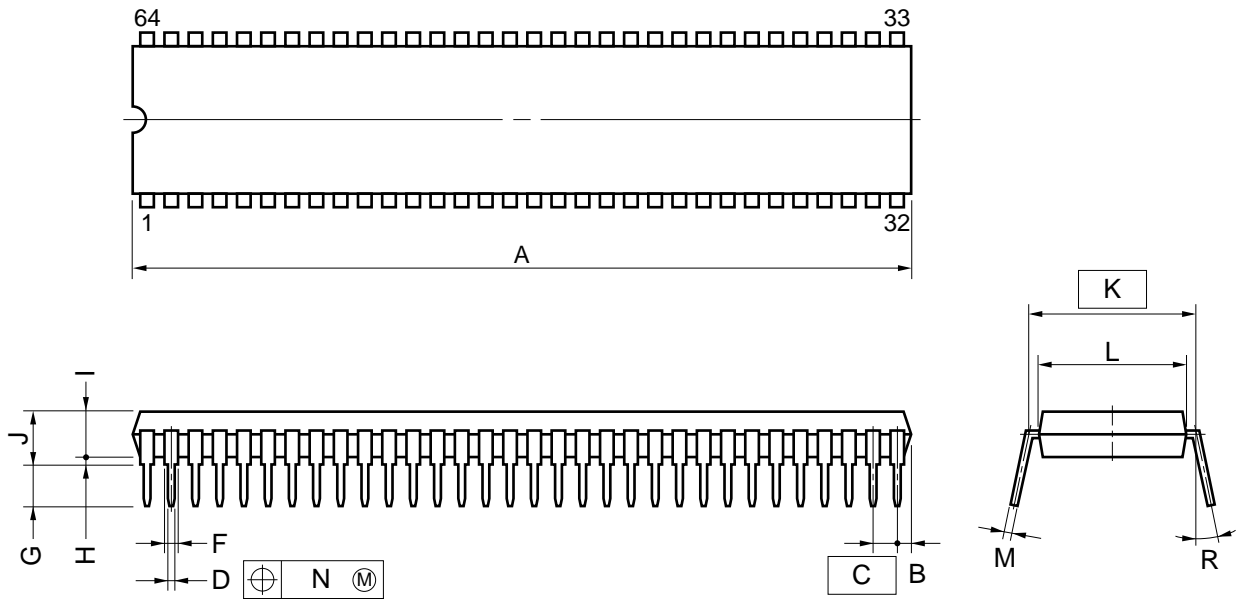
**I<sub>OD</sub> vs (V<sub>DD</sub> - V<sub>OD</sub>) (S0 to S9)**

(T<sub>a</sub> = 25 °C)



14. PACKAGE INFORMATION

64 PIN PLASTIC SHRINK DIP (750 mil)



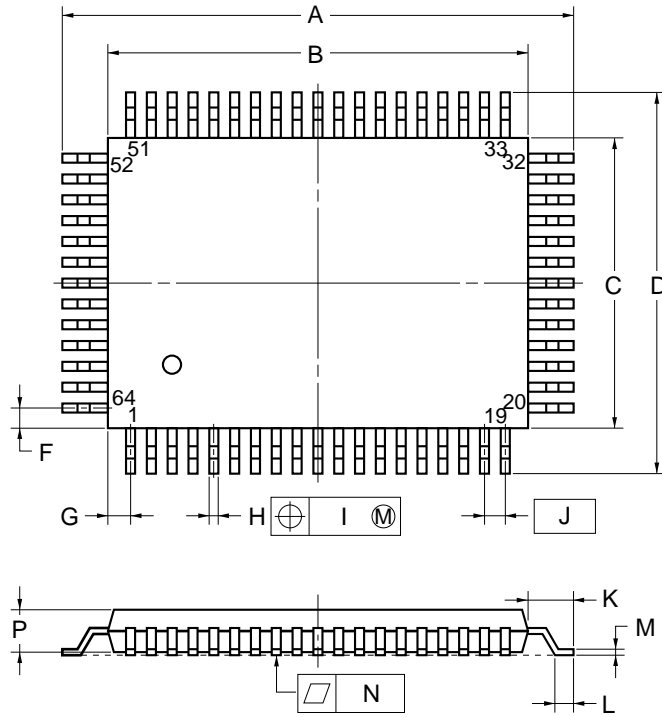
NOTE

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.010 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (14×20)



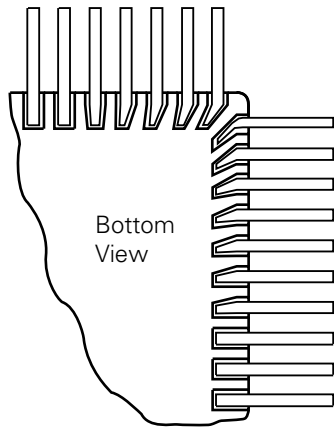
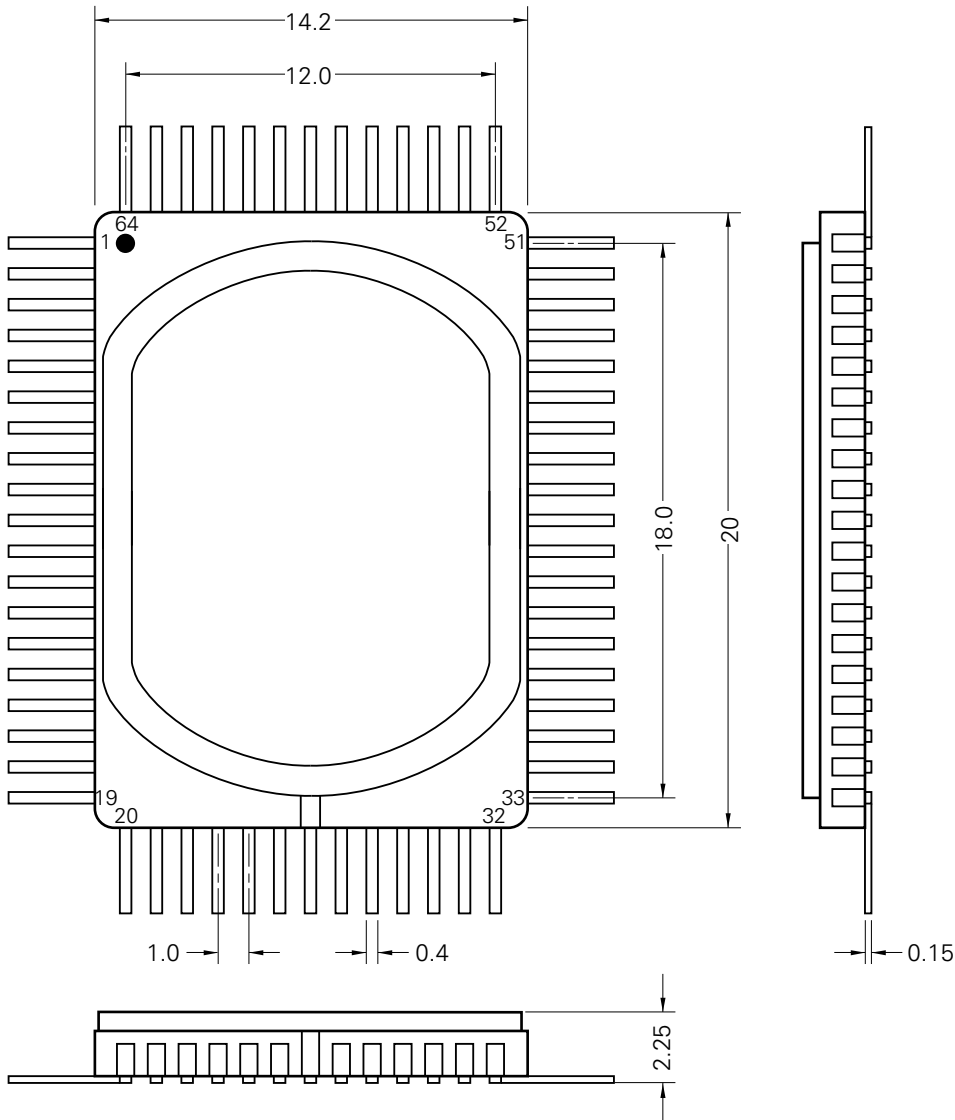
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 <sup>+0.008</sup> <sub>-0.009</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	0.016 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	0.071 <sup>+0.008</sup> <sub>-0.009</sub>
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P64GF-100-3B8,3BE,3BR-2

64-pin ceramic QFP for ES (reference) (unit : mm)



- Note**
1. Care is needed since the metal cap is connected to pin 26 and set to the positive power supply level.
  2. Care is needed since the lead of the base is formed obliquely.
  3. The lead length is not stipulated since the cutting of the lead ends is not progress-controlled.





**15. RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions for the surface mounting type, refer to the document “Semiconductor Device Mount Technology” (IEI-1207).

For soldering methods and conditions other than those recommended below, contact our salesman.

**Table 15-1 Surface Mounting Type Conditions**

**μPD75208GF-xxx-3BE : 64-pin plastic QFP (body 14 × 20 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Wave soldering	Solder bath temperature: 260 °C or less, Duration: 10 sec. max. Number of times: Once, Time limit: 7 days* (thereafter 10 hours prebaking required at 125 °C) Preheating temperature : 120 °C max. (package surface temperature)	WS60-107-1
Infrared reflow	Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Once, Time limit: 7 days*(thereafter 10 hours prebaking required at 125 °C)	IR30-107-1
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Once, Time limit: 7 days* (thereafter 10 hours prebaking required at 125 °C)	VP15-107-1
Pin part heating	Pin part temperature: 300 °C or below , Duration: 3 sec. max. (per device side)	—

\* For the storage period after dry-pack decompression storage conditions are max. 25 °C, 65 % RH.

**Note Use of more than one soldering method should be avoided (except in the case of pin part heating).**

**Table 15-2 Insertion Type Soldering Conditions**

**μPD75208CW-xxx : 64-pin plastic shrink DIP (750 mil)**

Soldering Method	Soldering Conditions
Wave soldering (lead part only)	Solder bath temperature: 260 °C or below , Duration: 10 sec. max.
Pin part heating	Pin part temperature: 260 °C or below , Duration: 10 sec. max.

**Note Ensure that the application of wave soldering is limited to the lead part and no solder touches the main unit directly.**

★ APPENDIX A DEVELOPMENT TOOLS

The following development tools are provided for developing systems including the μPD75208:

Hardware	IE-75000-R *1 IE-75001-R	In-circuit emulator for the 75X series
	IE-75000-R-EM *2	Emulation board for the IE-75000-R and IE-75001-R
	EP-75216ACW-R	Emulation probe for the μPD75216ACW
	EP-75216AGF-R EV-9200G-64	Emulation probe for the μPD75216AGF. A 64-pin conversion socket, the EV-9200G-64, is attached to the probe.
	PG-1500	PROM programmer
	PA-75P216ACW	PROM programmer adapter for the μPD75P216ACW and μPD75P218CW. Connected to the PG-1500.
	PA-75P218GF	PROM programmer adapter for the μPD75P218GF. Connected to the PG-1500.
	PA-75P218KB	PROM programmer adapter for the μPD75P218KB. Connected to the PG-1500.
Software	IE control program	Host machine <ul style="list-style-type: none"> <li>• PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A *3)</li> <li>• IBM PC series (PC DOS™ Ver. 3.1)</li> </ul>
	PG-1500 controller	
	RA75X relocatable assembler	

- \* 1. Maintenance service only  
 2. Not contained in the IE-75001-R  
 3. These software cannot use the task swap function, which is available in MS-DOS Ver. 5.00 and Ver. 5.00A.



**APPENDIX B RELATED DOCUMENTS**

**Documents related to the device**

Document Name	Document No.
User's manual	IEU-1294
Application note	IEM-1294
75X series selection guide	IF-1027

**Documents related to development tools**

Document Name				Document No.
Hardware	IE-75000-R User's Manual			EEU-1297
	IE-75001-R User's Manual			EEU-1416
	IE-75000-R-EM User's Manual			EEU-1294
	EP-75216ACW-R User's Manual			EEU-1321
	EP-75216AGF-R User's Manual			EEU-1309
	PG-1500 User's Manual			EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	PC-9800 series (MS-DOS) base IBM PC series (PC DOS) base	EEU-1346
		Language		EEU-1363
	PG-1500 Controller User's Manual			EEU-1291

**Other documents**

Document Name	Document No.
PACKAGE MANUAL	IEI-1213
SMD SURFACE MOUNT TECHNOLOGY MANUAL	IEI-1207
QUALITY GRADES ON NEC SEMICONDUCTOR DEVICES	IEI-1209
NEC SEMICONDUCTOR DEVICE RELIABILITY/QUALITY CONTROL SYSTEM	IEI-1203
ELECTROSTATIC DISCHARGE (ESD) TEST	IEI-1201
GUIDE TO QUALITY ASSURANCE FOR SEMICONDUCTOR DEVICES	MEI-1202

**Note** The above documents may be revised without notice. Use the latest versions when you design an application system.

### Cautions on CMOS Devices

#### ① Countermeasures against static electricity for all MOSs

**Caution** When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

#### ② CMOS-specific handling of unused input pins

**Caution** Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the  $V_{DD}$  or GND pin through a resistor. If handling of unused pins is documented, follow the instructions in the document.

#### ③ Statuses of all MOS devices at initialization

**Caution** The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

**[MEMO]**

**[MEMO]**

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Application examples recommended by NEC Corporation

Standard : Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special : Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

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