FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27230-3E

*ASSP For Power Manegement Applications (DC/DC Converter for DSC/Camcorder)*

# 4-ch DC/DC Converter IC
## for low voltage

# MB39A103

## ■ DESCRIPTION

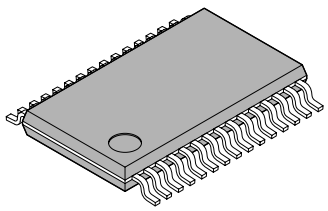
The MB39A103 is a 4-channel DC/DC converter IC using pulse width modulation (PWM). This IC is ideal for up conversion, down conversion, and up/down conversion.
Achievement of low voltage start-up (1.7 V or more) enables operation from low voltage.
4ch is built in TSSOP-30P/package. Each channel can be controlled, and soft-start.
This is an ideal power supply for high-performance portable devices such as digital still cameras.
This product is covered by US Patent Number 6,147,477.

## ■ FEATURES

- Supports for down-conversion and up/down Zeta conversion (CH1)
- Supports for up-conversion and up/down Sepic conversion (CH2 to CH4)
- Low voltage start-up (CH4): 1.7 V
- Power supply voltage range : 2.5 V to 11 V
- Reference voltage : 2.0 V ± 1 %
- Error amplifier threshold voltage : 1.24 V ± 1.5 %
- Built-in totem-pole type output for MOS FET
- Built-in soft-start circuit independent of loads
- High-frequency operation capability: 1.5 MHz (Max)
- External short-circuit detection capability by –INS terminal

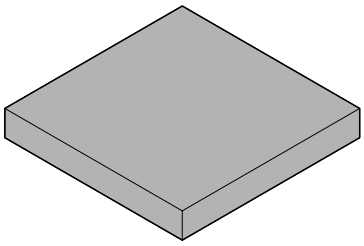
## ■ PACKAGES

30-pin plastic TSSOP



(FPT-30P-M04)

32-pad plastic BCC



(LCC-32P-M15)



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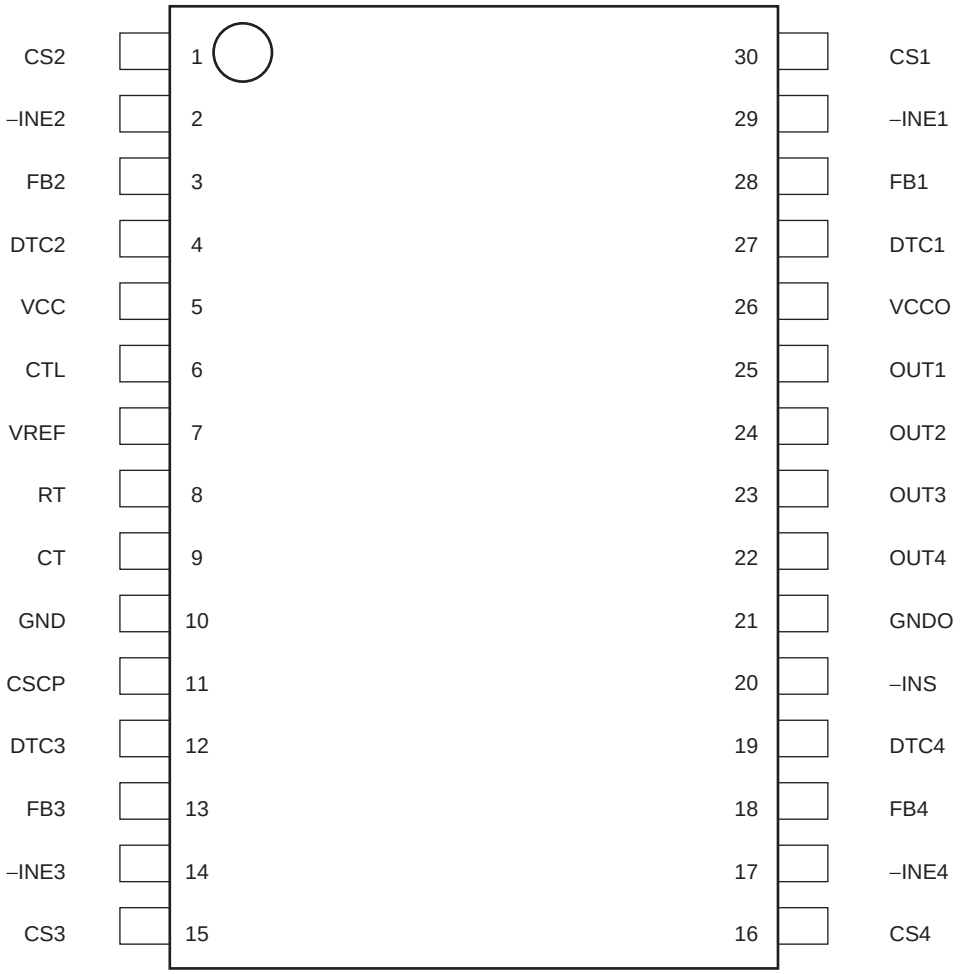
## ■ PIN ASSIGNMENTS

(TOP VIEW)




(FPT-30P-M04)

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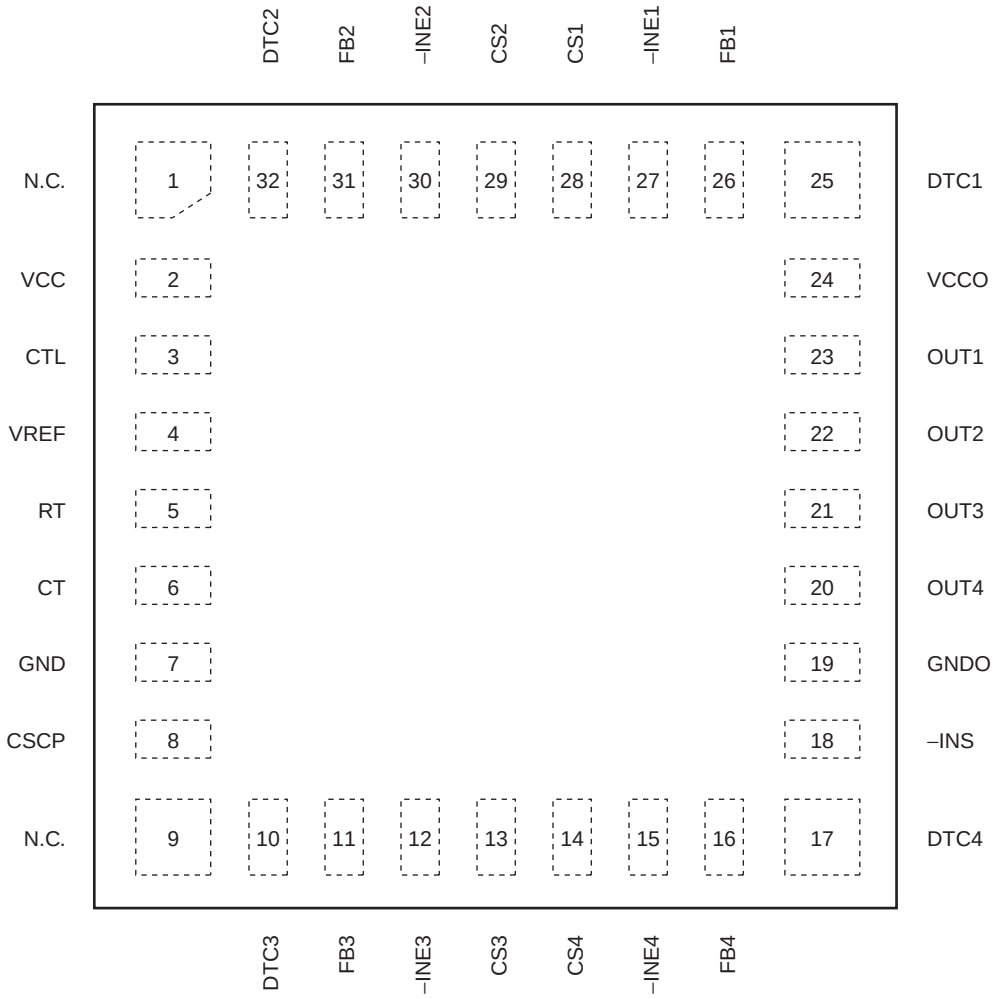
(TOP VIEW)
(Penetration diagram from surface)

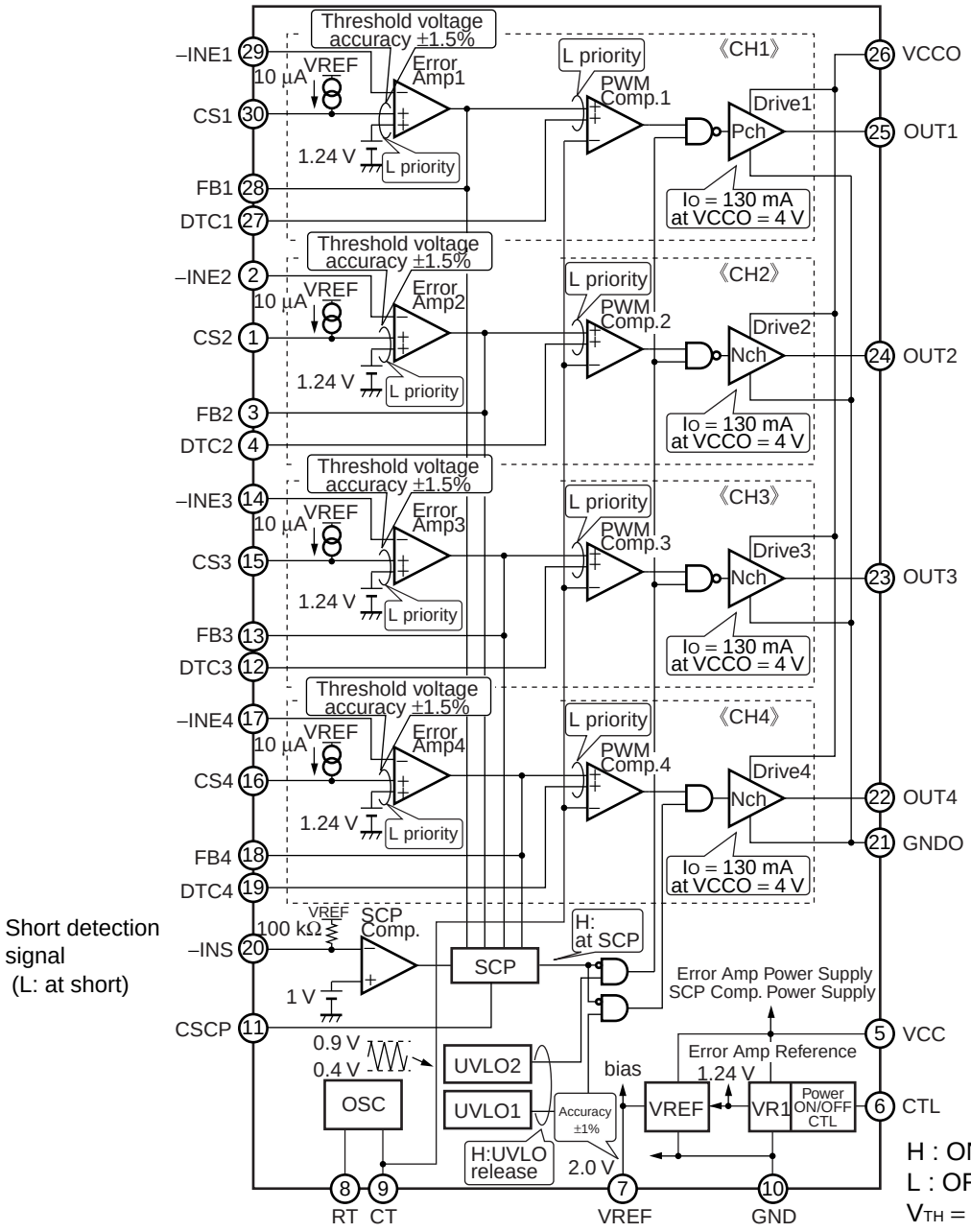



(LCC-32P-M15)

## ■ PIN DESCRIPTION

| Block | Pin No. | | Symbol | I/O | Descriptions |
|---|---|---|---|---|---|
| | TSSOP | BCC | | | |
| CH1 | 27 | 25 | DTC1 | I | Dead time control terminal |
| | 28 | 26 | FB1 | O | Error amplifier output terminal |
| | 29 | 27 | –INE1 | I | Error amplifier inverted input terminal |
| | 30 | 28 | CS1 | — | Soft-start setting capacitor connection terminal |
| | 25 | 23 | OUT1 | O | Totem pole type output terminal |
| CH2 | 4 | 32 | DTC2 | I | Dead time control terminal |
| | 3 | 31 | FB2 | O | Error amplifier output terminal |
| | 2 | 30 | –INE2 | I | Error amplifier inverted input terminal |
| | 1 | 29 | CS2 | — | Soft-start setting capacitor connection terminal |
| | 24 | 22 | OUT2 | O | Totem pole type output terminal |
| CH3 | 12 | 10 | DTC3 | I | Dead time control terminal |
| | 13 | 11 | FB3 | O | Error amplifier output terminal |
| | 14 | 12 | –INE3 | I | Error amplifier inverted input terminal |
| | 15 | 13 | CS3 | — | Soft-start setting capacitor connection terminal |
| | 23 | 21 | OUT3 | O | Totem pole type output terminal |
| CH4 | 19 | 17 | DTC4 | I | Dead time control terminal |
| | 18 | 16 | FB4 | O | Error amplifier output terminal |
| | 17 | 15 | –INE4 | I | Error amplifier inverted input terminal |
| | 16 | 14 | CS4 | — | Soft-start setting capacitor connection terminal |
| | 22 | 20 | OUT4 | O | Totem pole type output terminal |
| OSC | 9 | 6 | CT | — | Triangular wave frequency setting capacitor connection terminal |
| | 8 | 5 | RT | — | Triangular wave frequency setting resistor connection terminal |
| Control | 6 | 3 | CTL | I | Power supply control terminal |
| | 11 | 8 | CSCP | — | Short-circuit detection circuit capacitor connection terminal |
| | 20 | 18 | –INS | I | Short-circuit detection comparator inverted input terminal |
| Power | 26 | 24 | VCCO | — | Output block power supply terminal |
| | 5 | 2 | VCC | — | Power supply terminal |
| | 7 | 4 | VREF | O | Reference voltage output terminal |
| | 21 | 19 | GNDO | — | Output block ground terminal |
| | 10 | 7 | GND | — | Ground terminal |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Power supply voltage | $V_{CC}$ | VCC, VCCO terminals | — | 12 | V |
| Output current | $I_O$ | OUT1 to OUT4 terminals | — | 20 | mA |
| Peak output current | $I_{OP}$ | OUT1 to OUT4 terminals<br>Duty ≤ 5% (t = 1/$f_{OSC}$×Duty) | — | 400 | mA |
| Power dissipation | $P_D$ | $T_A$ ≤ +25 °C (TSSOP-30P) | — | 1390* | mW |
| | | $T_A$ ≤ +25 °C (BCC-32P) | — | 980* | mW |
| Storage temperature | $T_{STG}$ | — | –55 | +125 | °C |

* : The packages are mounted on the epoxy board (10 cm × 10 cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Start power supply voltage | $V_{CC}$ | VCC, VCCO terminals (CH4) | 1.7 | — | 11 | V |
| Power supply voltage | $V_{CC}$ | VCC, VCCO terminal s (CH1 to CH4) | 2.5 | 4 | 11 | V |
| Reference voltage output current | $I_{REF}$ | VREF terminal | –1 | — | 0 | mA |
| Input voltage | $V_{INE}$ | –INE1 to –INE4 terminals | 0 | — | $V_{CC}$ – 0.9 | V |
| | | –INS terminal | 0 | — | $V_{REF}$ | V |
| | $V_{DTC}$ | DTC1 to DTC4 terminals | 0 | — | $V_{REF}$ | V |
| Control input voltage | $V_{CTL}$ | CTL terminal | 0 | — | 11 | V |
| Output current | $I_O$ | OUT1 to OUT4 terminals | –15 | — | +15 | mA |
| Oscillation frequency | $f_{OSC}$ | * | 100 | 500 | 1500 | kHz |
| Timing capacitor | $C_T$ | — | 39 | 100 | 560 | pF |
| Timing resistor | $R_T$ | — | 11 | 24 | 130 | kΩ |
| Soft-start capacitor | $C_S$ | CS1 to CS4 terminals | — | 0.1 | 1.0 | µF |
| Short-circuit detection capacitor | $C_{SCP}$ | — | — | 0.1 | 1.0 | µF |
| Reference voltage output capacitor | $C_{REF}$ | — | — | 0.1 | 1.0 | µF |
| Operating ambient temperature | $T_A$ | — | –30 | +25 | +85 | °C |

* : See “■ SETTING THE TRIANGULAR OSCILLATION FREQUENCY”.

Note: Pin numbers referred after this part are present on TSSOP-30P PKG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

(VCC = VCCO = 4 V, $T_A$ = +25 °C)

| Parameter | | Symbol | Pin No | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Reference voltage block [Ref] | Output voltage | $V_{REF}$ | 7 | — | 1.98 | 2.00 | 2.02 | V |
| | Output voltage temperature stability | $\Delta V_{REF}/V_{REF}$ | 7 | $T_A$ = –30 °C to +85 °C | — | 0.5* | — | % |
| | Input stability | Line | 7 | VCC = 2.5 V to 11 V | –10 | — | +10 | mV |
| | Load stability | Load | 7 | VREF = 0 mA to –1 mA | –10 | — | +10 | mV |
| Under voltage lockout protection circuit block (CH4) [UVLO1] | Threshold voltage | $V_{TH}$ | 22 | VCC = ↗ | 1.4 | 1.5 | 1.65 | V |
| | Hysteresis width | $V_H$ | 22 | — | 0.02 | 0.05 | 0.1 | V |
| Under voltage lockout protection circuit block (CH1 to CH3) [UVLO2] | Threshold voltage | $V_{TH}$ | 25 | VCC = ↗ | 1.7 | 1.8 | 1.95 | V |
| | Hysteresis width | $V_H$ | 25 | — | 0.05 | 0.1 | 0.2 | V |
| Short-circuit detection block [SCP] | Threshold voltage | $V_{TH}$ | 11 | — | 0.65 | 0.70 | 0.75 | V |
| | Input source current | $I_{CSCP}$ | 11 | — | –1.4 | –1.0 | –0.6 | µA |
| | Reset voltage | $V_{RST}$ | 25 | VREF = ↘ | 1.3 | 1.45 | 1.63 | V |
| Triangular wave oscillator block [OSC] | Oscillation frequency | $f_{OSC}$ | 22, 23, 24, 25 | CT = 100 pF, RT = 24 kΩ | 450 | 500 | 550 | kHz |
| | Frequency temperature stability | $\Delta f_{OSC}/f_{OSC}$ | 22, 23, 24, 25 | $T_A$ = –30 °C to +85 °C | — | 1* | — | % |
| Soft-start block [CS1 to CS4] | Charge current | $I_{CS}$ | 1, 15, 16, 30 | CS1 to CS4 = 0 V | –14 | –10 | –6 | µA |
| Error amplifier block [Error Amp1 to Error Amp4] | Threshold voltage | $V_{TH}$ | 3, 13, 18, 28 | FB1 to FB4 = 0.65 V | 1.222 | 1.240 | 1.258 | V |
| | Input bias current | $I_B$ | 2, 14, 17, 29 | –INE1 to –INE4 = 0 V | –120 | –30 | — | nA |
| | Voltage gain | $A_V$ | 3, 13, 18, 28 | DC | — | 100* | — | dB |
| | Frequency bandwidth | BW | 3, 13, 18, 28 | $A_V$ = 0 dB | — | 1.6* | — | MHz |

* : Standard design value

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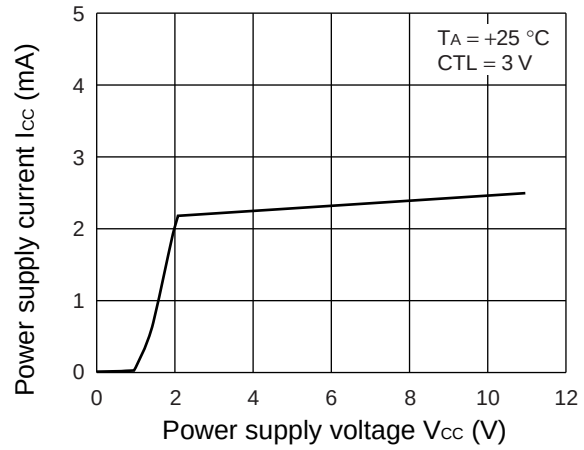
(VCC = VCCO = 4 V, $T_A$ = +25 °C)

| Parameter | | Symbol | Pin No | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Error amplifier block [Error Amp1 to Error Amp4] | Output voltage | $V_{OH}$ | 3, 13, 18, 28 | — | 1.7 | 1.9 | — | V |
| | | $V_{OL}$ | 3, 13, 18, 28 | — | — | 40 | 200 | mV |
| | Output source current | $I_{SOURCE}$ | 3, 13, 18, 28 | FB1 to FB4 = 0.65 V | — | –2 | –1 | mA |
| | Output sink current | $I_{SINK}$ | 3, 13, 18, 28 | FB1 to FB4 = 0.65 V | 150 | 200 | — | µA |
| PWM comparator block [PWM Comp.1 to PWM Comp.4] | Threshold voltage | $V_{T0}$ | 22, 23, 24, 25 | Duty cycle = 0 % | 0.3 | 0.4 | — | V |
| | | $V_{T100}$ | 22, 23, 24, 25 | Duty cycle = Dtr | — | 0.9 | 1.0 | V |
| | Input current | $I_{DTC}$ | 4, 12, 19, 27 | DTC1 to DTC4 = 0.4 V | –2.0 | –0.6 | — | µA |
| Output block [Drive1 to Drive4] | Output source current | $I_{SOURCE}$ | 22, 23, 24, 25 | Duty ≤ 5 %<br>(t = 1/$f_{OSC}$×Duty)<br>OUT1 to OUT4 = 0 V | — | –130 | –75 | mA |
| | Output sink current | $I_{SINK}$ | 22, 23, 24, 25 | Duty ≤ 5 %<br>(t = 1/$f_{OSC}$×Duty)<br>OUT1 to OUT4 = 4 V | 75 | 130 | — | mA |
| | Output ON resistor | $R_{OH}$ | 22, 23, 24, 25 | OUT1 to OUT4 = –15 mA | — | 18 | 27 | Ω |
| | | $R_{OL}$ | 22, 23, 24, 25 | OUT1 to OUT4 = 15 mA | — | 18 | 27 | Ω |
| Short-circuit detection comparator block [SCP Comp.] | Threshold voltage | $V_{TH}$ | 25 | — | 0.97 | 1.00 | 1.03 | V |
| | Input bias current | $I_B$ | 20 | –INS = 0 V | –25 | –20 | –17 | µA |
| Control block [CTL] | CTL input voltage | $V_{IH}$ | 6 | IC Active mode | 1.7 | — | 11 | V |
| | | $V_{IL}$ | 6 | IC Standby mode | 0 | — | 0.8 | V |
| | Input current | $I_{CTLH}$ | 6 | CTL = 3 V | 5 | 30 | 60 | µA |
| | | $I_{CTLL}$ | 6 | CTL = 0 V | — | — | 1 | µA |
| General | Standby current | $I_{CCS}$ | 5 | CTL = 0 V | — | 0 | 2 | µA |
| | | $I_{CCSO}$ | 26 | CTL = 0 V | — | 0 | 2 | µA |
| | Power supply current | $I_{CC}$ | 5 | CTL = 3 V | — | 2.3 | 4.5 | mA |

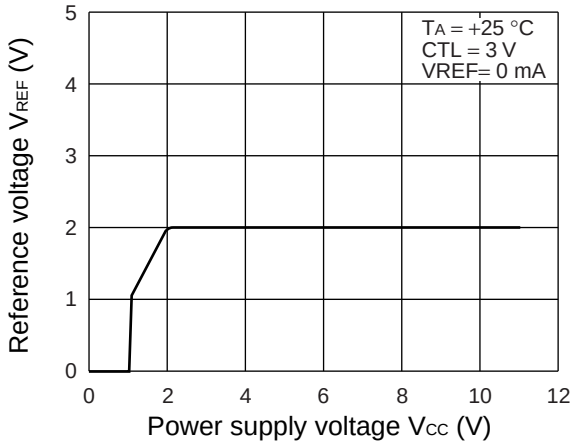
*: Standard design value.

## ■ TYPICAL CHARACTERISTICS

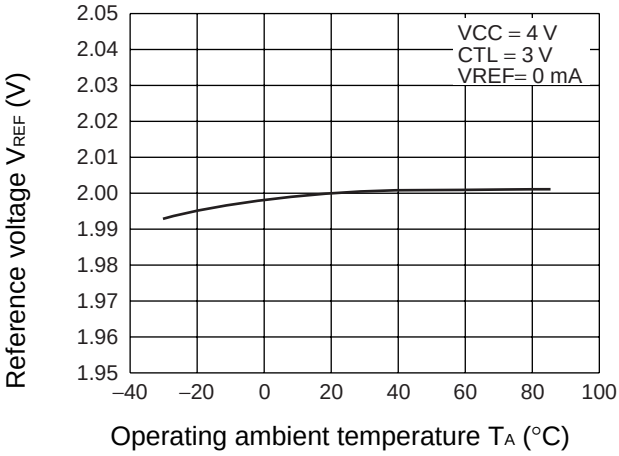
Power Supply Current vs. Power Supply Voltage



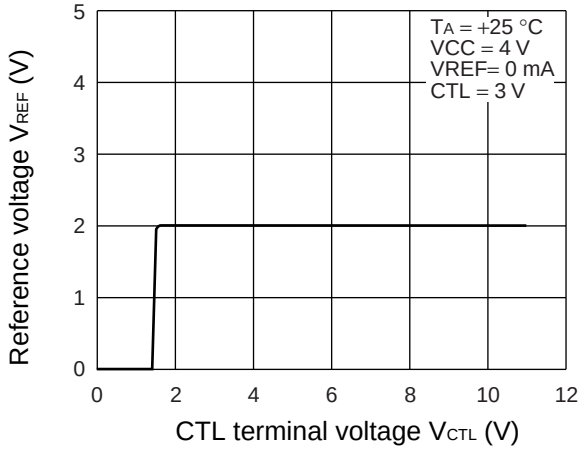

Reference Voltage vs. Power Supply Voltage



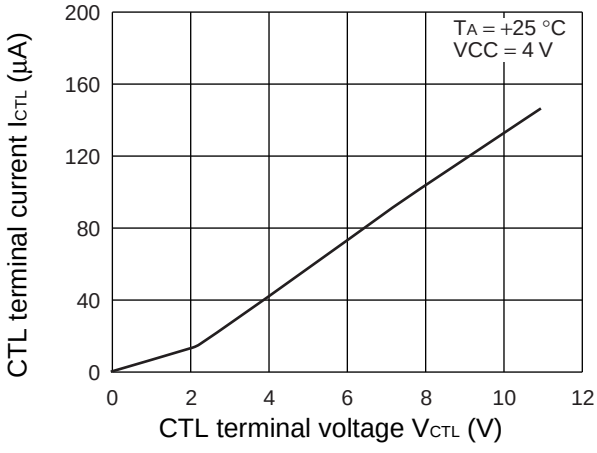

Reference Voltage vs.
Operating Ambient Temperature




Reference Voltage vs. CTL terminal Voltage




CTL terminal Current vs. CTL terminal Voltage

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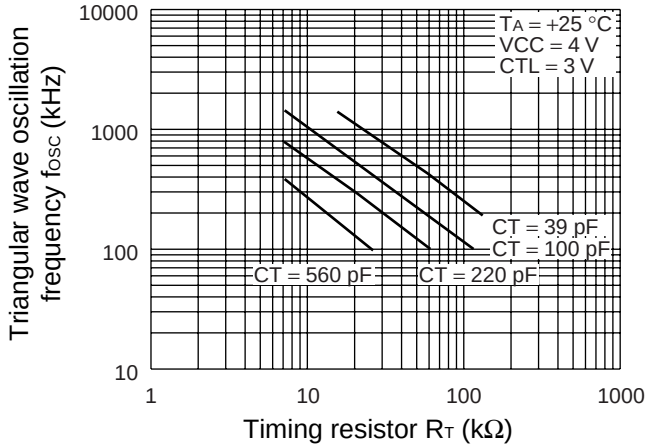
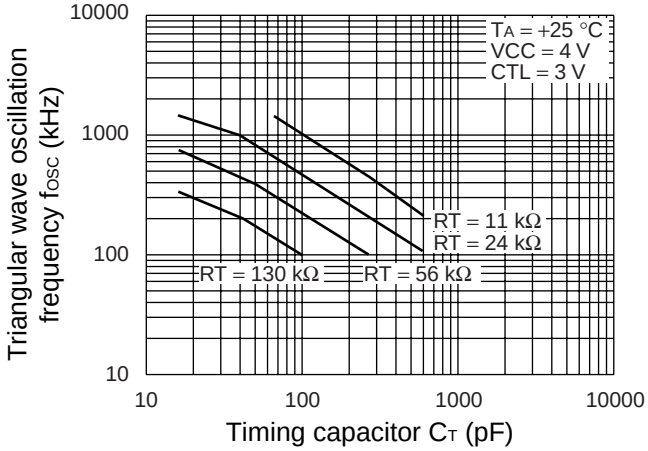
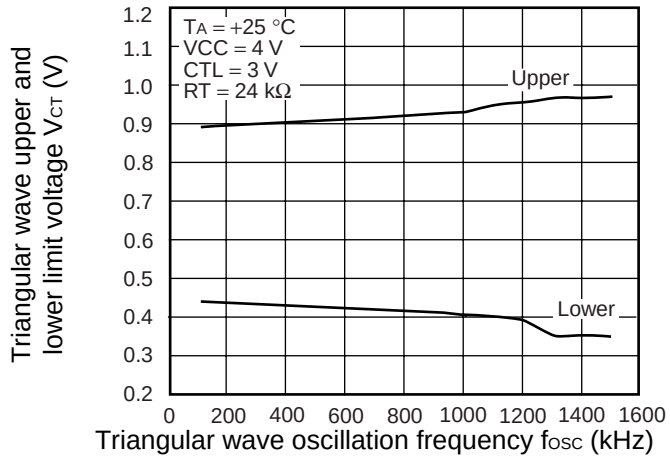
Triangular Wave Oscillation Frequency vs. Timing Resistor



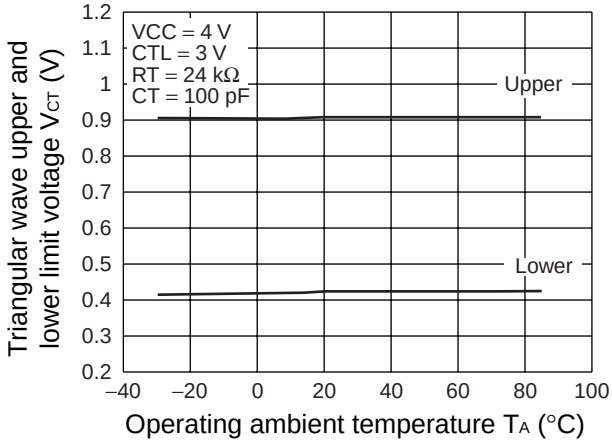

Triangular Wave Oscillation Frequency vs. Timing Capacitor



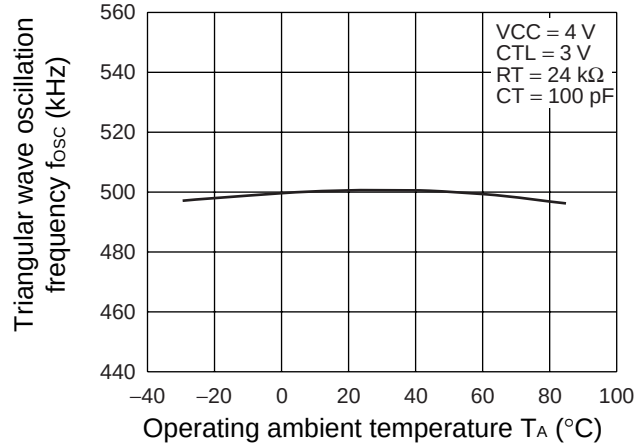

Triangular Wave Upper and Lower Limit Voltage vs. Triangular Wave Oscillation Frequency




Triangular Wave Upper and Lower Limit Voltage vs. Operating Ambient Temperature




Triangular Wave Oscillation Frequency vs. Operating Ambient Temperature

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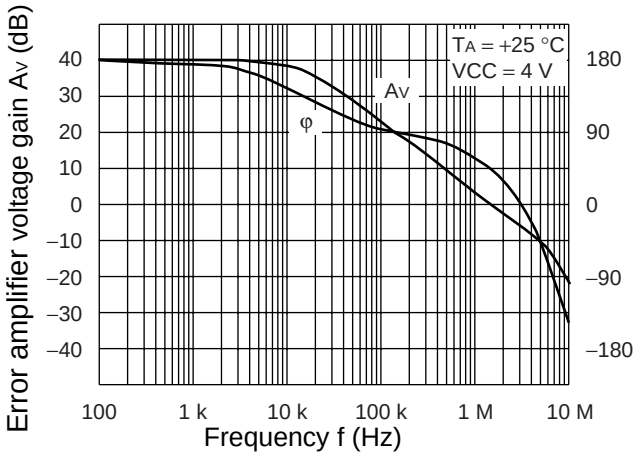
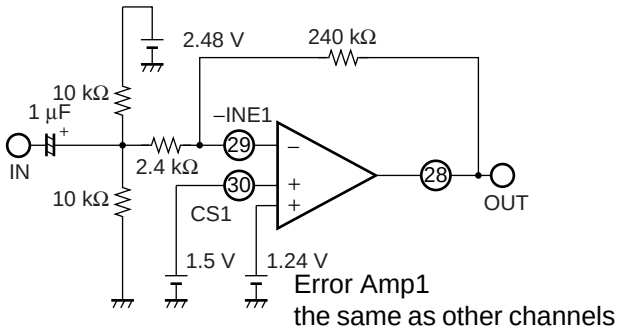
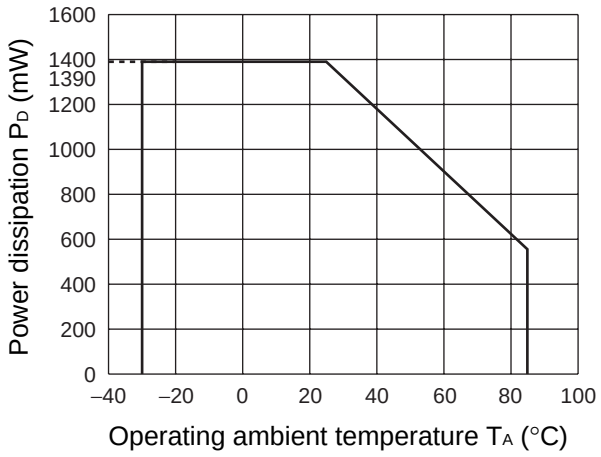
Error Amplifier Voltage Gain, Phase vs. Frequency

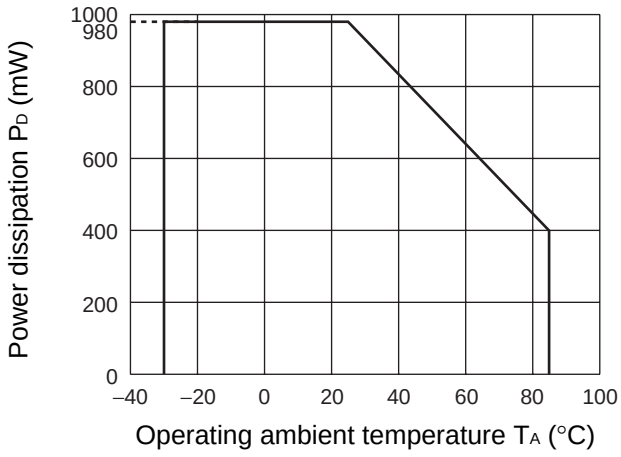



Power Dissipation vs.
Operating Ambient Temperature
(TSSOP-30P)




Power Dissipation vs.
Operating Ambient Temperature
(BCC-32P)



## ■ FUNCTIONS

### 1. DC/DC Converter Functions

#### (1) Reference voltage block (Ref)

The reference voltage circuit generates a temperature-compensated reference voltage (2.0 V Typ) from the voltage supplied from the VCC terminal (pin 5). The voltage is used as the reference voltage for the IC's internal circuitry.
The reference voltage can supply a load current of up to 1 mA to an external device through the VREF terminal (pin 7).

#### (2) Triangular-wave oscillator block (OSC)

The triangular wave oscillator incorporates a timing capacitor and a timing resistor connected respectively to the CT terminal (pin 9) and RT terminal (pin 8) to generate triangular oscillation waveform amplitude of 0.4 V to 0.9 V.
The triangular waveforms are input to the PWM comparator in the IC.

#### (3) Error amplifier block (Error Amp1 to Error Amp4)

The error amplifier detects the DC/DC converter output voltage and outputs PWM control signals. In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the output terminal to inverted input terminal of the error amplifier, enabling stable phase compensation to the system.
Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with the CS1 terminal (pin 30) to CS4 terminal (pin 16) which are the non-inverted input terminal for Error Amp. The use of Error Amp for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load on the DC/DC converter.

#### (4) PWM comparator block (PWM Comp.1 to PWM Comp.4)

The PWM comparator is a voltage-to-pulse width modulator that controls the output duty depending on the input/output voltage.
The output transistor turns on while the error amplifier output voltage and DTC voltage remain higher than the triangular wave voltage.

#### (5) Output block (Drive1 to Drive4)

The output block is in the totem pole type, capable of driving an external P-channel MOS FET (channel 1), and N-channel MOS FET (channels 2 to 4).

## 2. Channel Control Function

The main or each channel is turned on and off depending on the voltage levels at the CTL terminal (pin 6), CS1 terminal (pin 30), CS2 terminal (pin 1), CS3 terminal (pin 15), and CS4 terminal (pin 16).

Channel On/Off Setting Conditions

| CTL | CS1 | CS2 | CS3 | CS4 | Power | CH1 | CH2 | CH3 | CH4 |
|---|---|---|---|---|---|---|---|---|---|
| L | —* | —* | —* | —* | OFF | OFF | OFF | OFF | OFF |
| H | GND | GND | GND | GND | ON | OFF | OFF | OFF | OFF |
| H | High-Z | GND | GND | GND | ON | ON | OFF | OFF | OFF |
| H | GND | High-Z | GND | GND | ON | OFF | ON | OFF | OFF |
| H | GND | GND | High-Z | GND | ON | OFF | OFF | ON | OFF |
| H | GND | GND | GND | High-Z | ON | OFF | OFF | OFF | ON |
| H | High-Z | High-Z | High-Z | High-Z | ON | ON | ON | ON | ON |

*: Undefined

## 3. Protective Functions

### (1) Timer-latch short-circuit protection circuit (SCP, SCP Comp.)

The short-circuit detection comparator detects the Error Amp output voltage level of each channel, and if any channel output voltage of Error Amp reaches the short-circuit detection voltage, the timer circuits are actuated to start charging the external capacitor $C_{SCP}$ connected to the CSCP terminal (pin 11).

When the capacitor ($C_{SCP}$) voltage reaches about 0.7 V, the circuit is turned off the output transistor and sets the dead time to 100 %.

In addition, the short-circuit detection from external input is capable by using –INS terminal (pin 20) on short-circuit detection comparator (SCP Comp.) .

To release the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the “L” level to lower the VREF terminal (pin 7) voltage to 1.3 V (Min) or less. (See “■SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT”.)

### (2) Under voltage lockout protection circuit (UVLO)

The transient state or a momentary decrease in supply voltage, which occurs when the power supply is turned on, may cause the IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, under voltage lockout protection circuit detects a decrease in internal reference voltage with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP terminal (pin 11) at the “L” level.

The circuit restores the output transistor to normal when the supply voltage reaches the threshold voltage of the undervoltage lockout protection circuit.

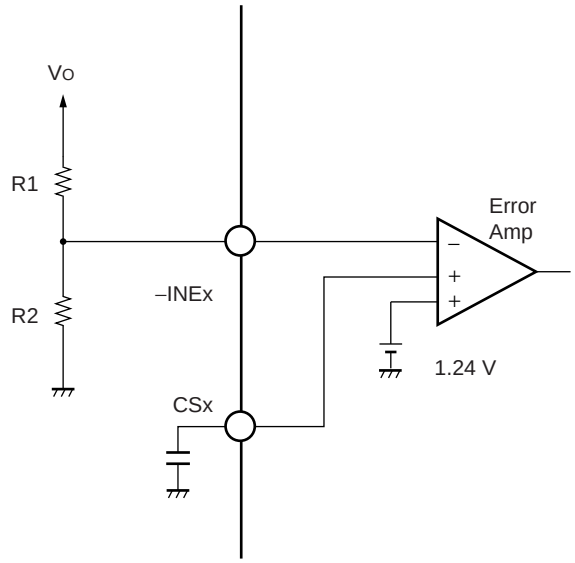
## ■ PROTECTION CIRCUIT OPERATING FUNCTION TABLE

This table refers to output condition when protection circuit is operating.

| Operating circuit | OUT1 | OUT2 | OUT3 | OUT4 |
|---|---|---|---|---|
| Short-circuit protection circuit | H | L | L | L |
| Under voltage lockout protection circuit | H | L | L | L |

## ■ SETTING THE OUTPUT VOLTAGE

**• CH1 to CH4**




$$V_O\ (V) = \frac{1.24}{R2}\ (R1 + R2)$$

x: Each channel No.

## ■ SETTING THE TRIANGULAR OSCILLATION FREQUENCY

The triangular oscillation frequency is determined by the timing capacitor ($C_T$) connected to the CT terminal (pin 9), and the timing resistor ($R_T$) connected to the RT terminal (pin 8).
Moreover, it shifts more greatly than the calculated values according to the constant of timing resistor ($R_T$) when the triangular wave oscillation frequency exceeds 1 MHz. Therefore, set it referring to “Triangular Wave Oscillation Frequency vs. Timing Resistor” and “Triangular Wave Oscillation Frequency vs. Timing Capacitor” in “■ TYPICAL CHARACTERISTICS”.

Triangular oscillation frequency : $f_{OSC}$

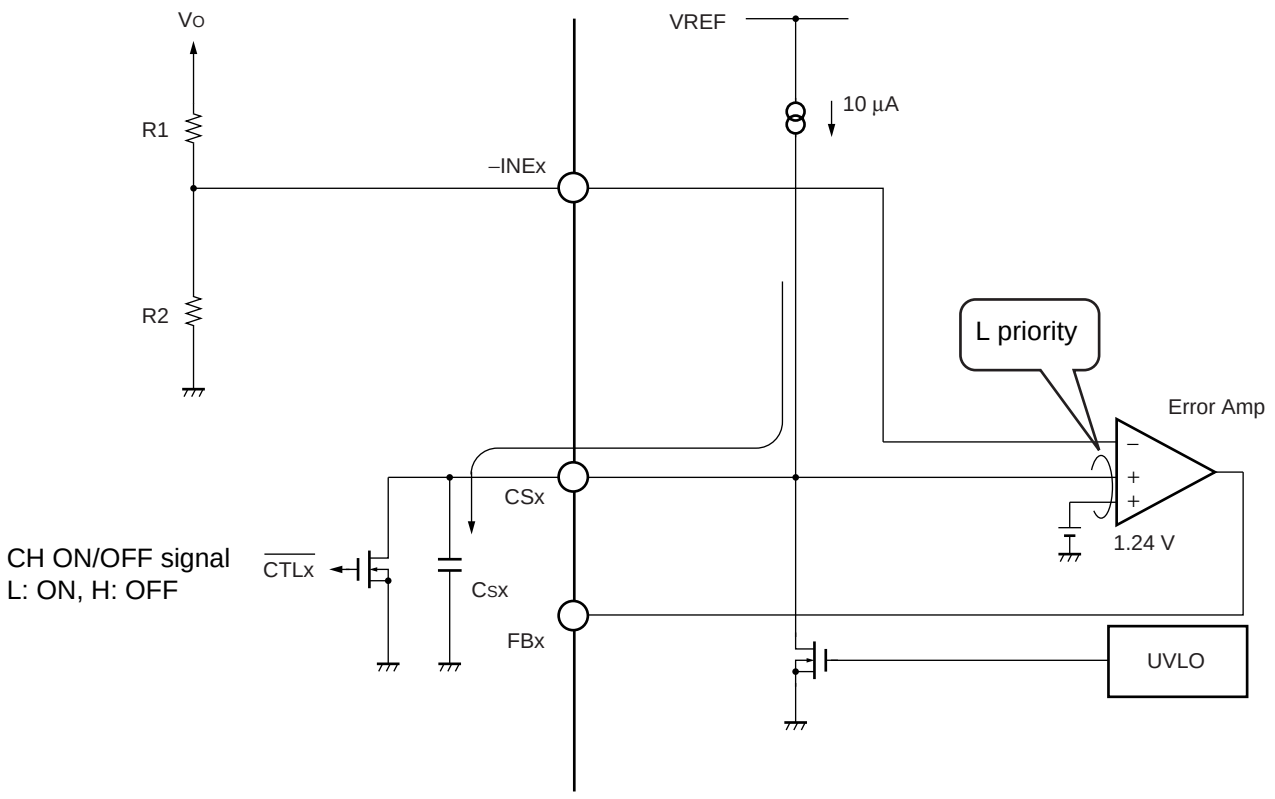
$$f_{OSC}\ (kHz) \fallingdotseq \frac{1200000}{C_T\ (pF) \bullet R_T\ (k\Omega)}$$

## ■ SETTING THE SOFT-START TIME

To prevent rush currents when the IC is turned on, you can set a soft-start by connecting soft-start capacitors ($C_{S1}$ to $C_{S4}$) to the CS1 terminal (pin 30) to the CS4 terminal (pin 16), respectively.
Setting each $\overline{CTLx}$ from "H" to "L" switches to charge the external soft-start capacitors ($C_{S1}$ to $C_{S4}$) connected to the CS1 terminal (pin 30) to CS4 terminal (pin 16) at 10 µA.
The error amplifier output (FB1 to FB4) is determined by comparison between the lower one of the potentials at two non-inverted input terminals (1.24 V, CS terminal voltages) and the inverted input terminal voltage (–INE1 to –INE4).
The FB terminal voltage during the soft-start period (CS terminal voltage < 1.24 V) is therefore determined by comparison between the –INE terminal and CS terminal voltages. The DC/DC converter output voltage rises in proportion to the CS terminal voltage as the soft-start capacitor connected to the CS terminal is charged.
The soft-start time is obtained from the following formula:

Soft-start time: ts (time to output 100%)
$ts\ (s) \fallingdotseq 0.124 \times C_{SX}\ (\mu F)$

**• Soft-Start Circuit**

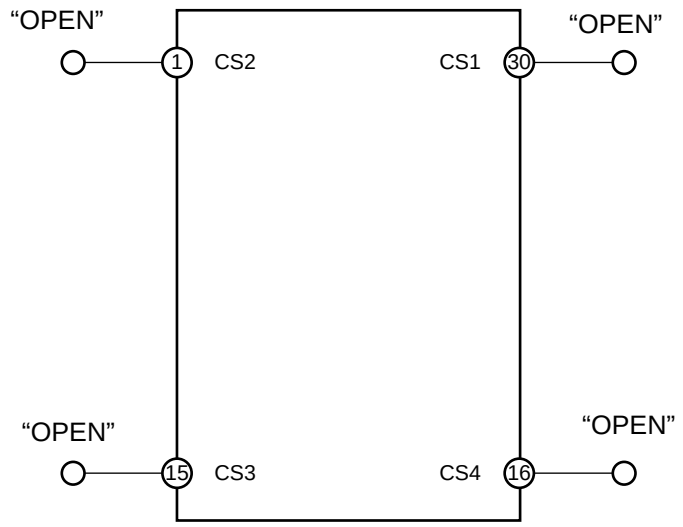



x: Each channel No.

## ■ TREATMENT WITHOUT USING CS TERMINAL

When not using the soft-start function, open the CS1 terminal (pin 30), the CS2 terminal (pin 1), the CS3 terminal (pin 15), the CS4 terminal (pin 16).

• **Without Setting Soft-Start Time**



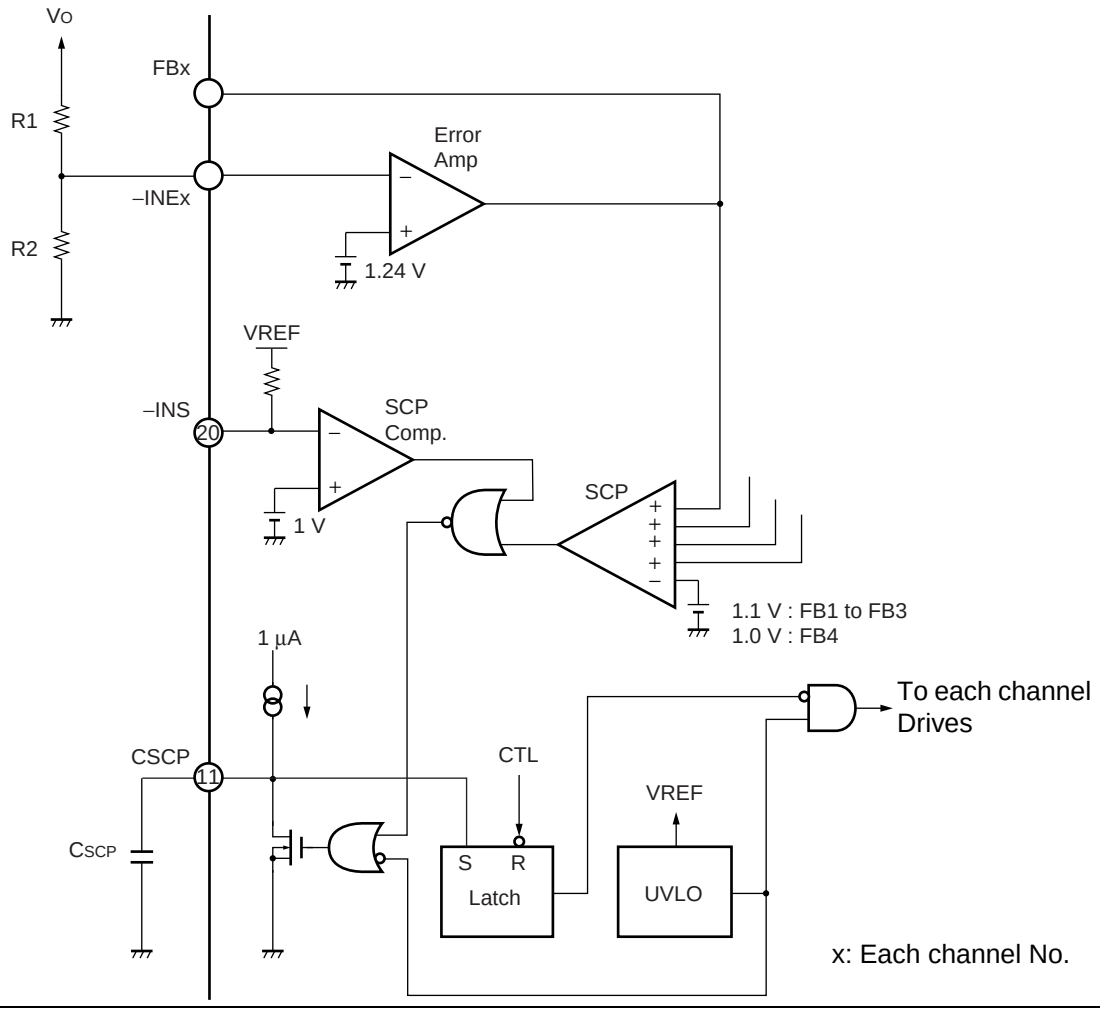
## ■ SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT

Each channel uses the short-circuit detection comparator (SCP) to always compare the error amplifier's output level to the reference voltage.
While DC/DC converter load conditions are stable on all channels, the short-circuit detection comparator output remains at "L" level, and the CSCP terminal (pin 11) is held at "L" level.
If the load condition on a channel changes rapidly due to a short-circuit of the load, causing the output voltage to drop, the output of the short-circuit detection comparator on that channel goes to "H" level. This causes the external short-circuit protection capacitor $C_{SCP}$ connected to the CSCP terminal (pin 11) to be charged at 1 µA.
Short-circuit detection time : $t_{SCP}$

$t_{SCP}$ (s) ≒ 0.70 × $C_{SCP}$ (µF)

When the capacitor $C_{SCP}$ is charged to the threshold voltage ($V_{TH}$ ≒ 0.70 V), the latch is set and the external FET is turned off (dead time is set to 100%). At this time, the latch input is closed and the CSCP terminal (pin 11) is held at "L" level.
In addition, the short-circuit detection from external input is capable by using –INS terminal (pin 20) on the short-circuit detection comparator (SCP Comp.). The short-circuit detection operation starts when –INS terminal voltage is less than threshold voltage ($V_{TH}$ ≒ 1 V).
When the power supply is turn off and on again or VREF terminal (pin 7) voltage is less than 1.3 V (Min) by setting CTL terminal (pin 6) to "L" level, the latch is released.

• **Timer-latch short-circuit protection circuit**

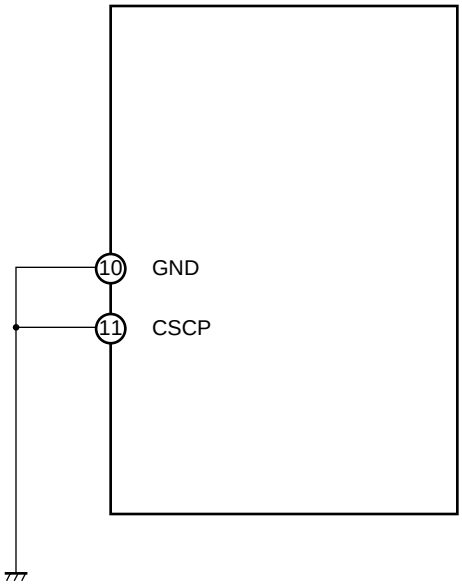



Note : When using self-power supply configuration in which the output from the CH4 DC/DC converter is connected to the VCC, note that short-circuit detection is not possible in the CH4 DC/DC converter output.

## ■ TREATMENT WITHOUT USING CSCP TERMINAL

When not using the timer-latch short-circuit protection circuit, connect the CSCP terminal (pin 11) to GND (pin 10) with the shortest distance.

• **Treatment without using CSCP terminal**



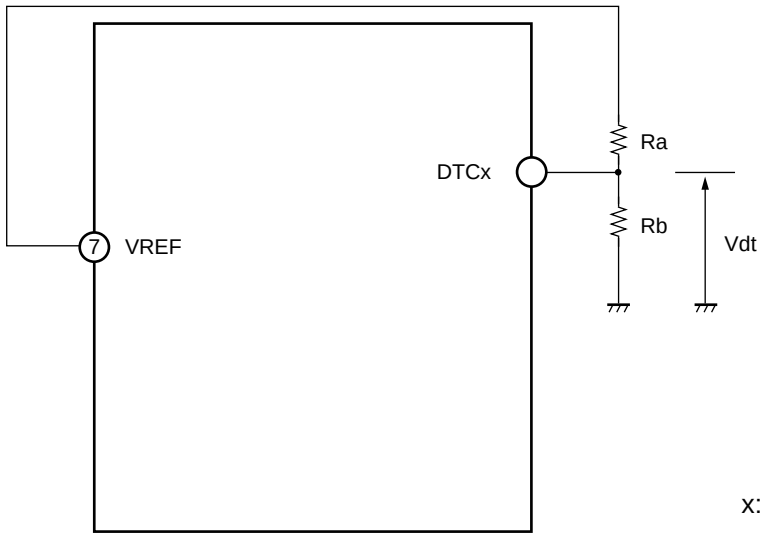
## ■ SETTING THE DEAD TIME

When the device is set for step-up or inverted output based on the step-up or step-up/down Zeta conversion, step-up/down Sepic conversion or flyback conversion, the FB terminal voltage may reach and exceed the triangular wave voltage due to load fluctuation. If this is the case, the output transistor is fixed to a full-ON state (ON duty = 100 %). To prevent this, set the maximum duty of the output transistor. To set it, set the voltage at the DTC terminal by applying a resistive voltage divider to the VREF voltage as shown below.
When the DTC terminal voltage is higher than the triangular wave voltage, the output transistor is turned on. The maximum duty calculation formula assuming that triangular wave amplitude ≒ 0.5 V and triangular wave lower voltage ≒ 0.4 V is given below.

$$\text{DUTY (ON) Max} \fallingdotseq \frac{\text{Vdt} - 0.4\ \text{V}}{0.5\ \text{V}} \times 100\ (\%)\ ,\ \text{Vdt (V)} = \frac{\text{Rb}}{\text{Ra} + \text{Rb}} \times \text{VREF}$$

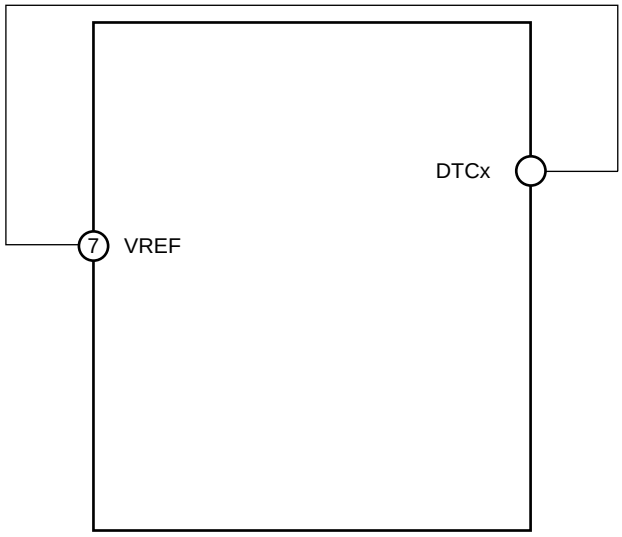
When the DTC terminal is not used, connect it directly to the VREF terminal (pin 7) as shown below (when no dead time is set).

• **When using DTC to set dead time**




x: Each channel No.

• **When no dead time is set**

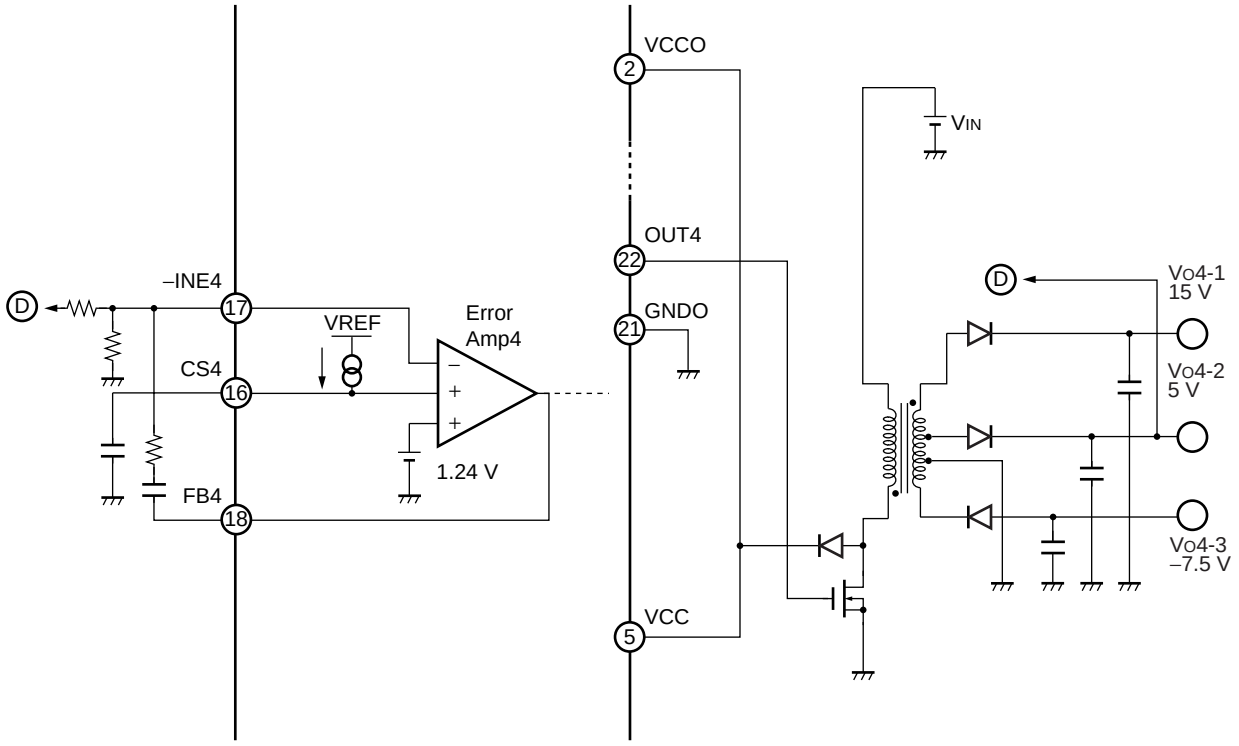



x: Each channel No.

## ■ POWERR SUPPLY EXAMPLE USING CH4 FOR SELF-POWER SUPPLY

The MB39A103 can be started with the low input voltage ($V_{IN} \geq 1.7$ V) if the CH4 is used as a self-power supply. An example of supply the power using the transformer is shown below.

• **Power supply example using CH4 for self-power supply**




Setting shown in the "■(APPLICATION EXAMPLE" is as follows:

- Number of windings for VCC and VCCO is set to the value equivalent to $V_{IN}$ + 2.5 V.

CH1 to CH3 are operational on VCC ≥ 2.5 V; in order for the CH1 to CH3 to operate on $V_{IN} \geq 1.7$ V, the number of windings should be set equivalent to $V_{IN}$ + 0.8 V or more for VCC and VCCO.

## ■ OPERATION EXPLANATION WHEN CTL TURNING ON AND OFF

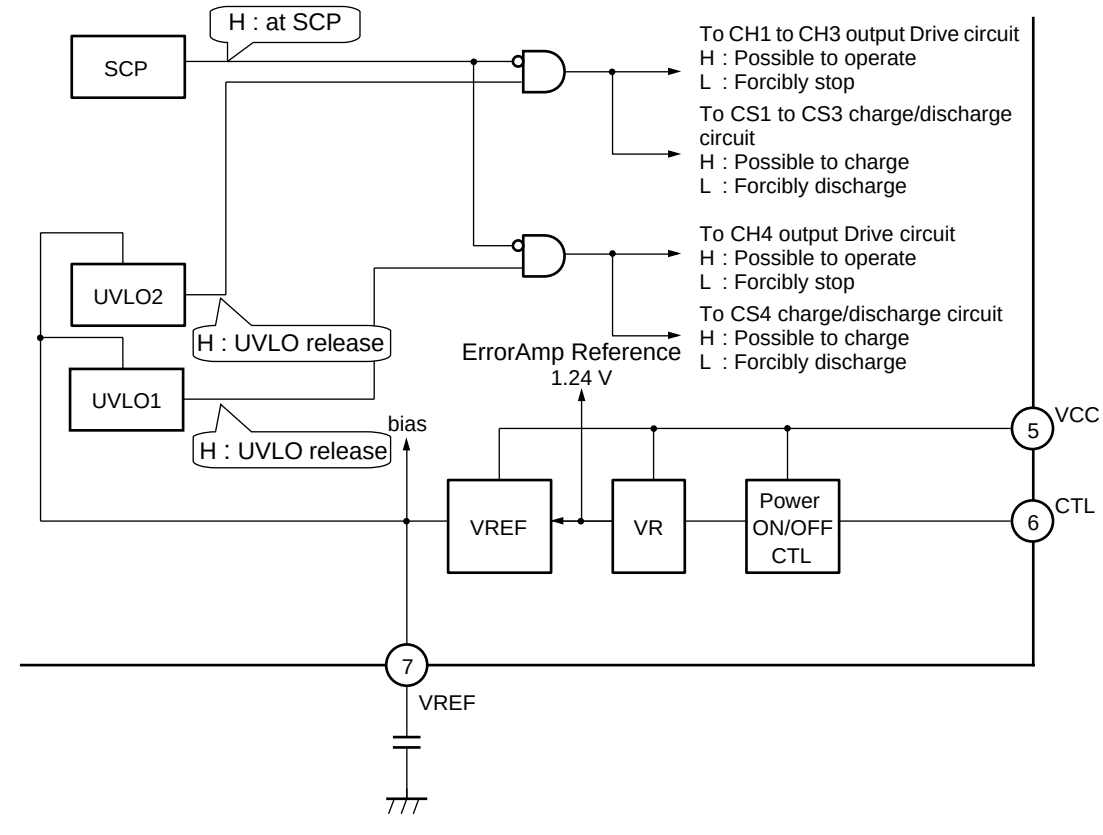
When CTL is turned on, internal reference voltage VR and VREF generate. When VREF exceeds each threshold voltage (VTH1, VTH2) of UVLO1 and UVLO2 (under voltage lockout protection circuit), UVLO1 and UVLO2 are released, and the operation of output Drive circuit of each channel becomes possible.

When CTL is off, VR and VREF fall. When VREF decreases and UVLO1 and UVLO2 fall below each reset voltage (VRST1, VRST2), UVLO operates and output Drive circuit of each channel is forcibly done the operation stop, and makes the output off state.

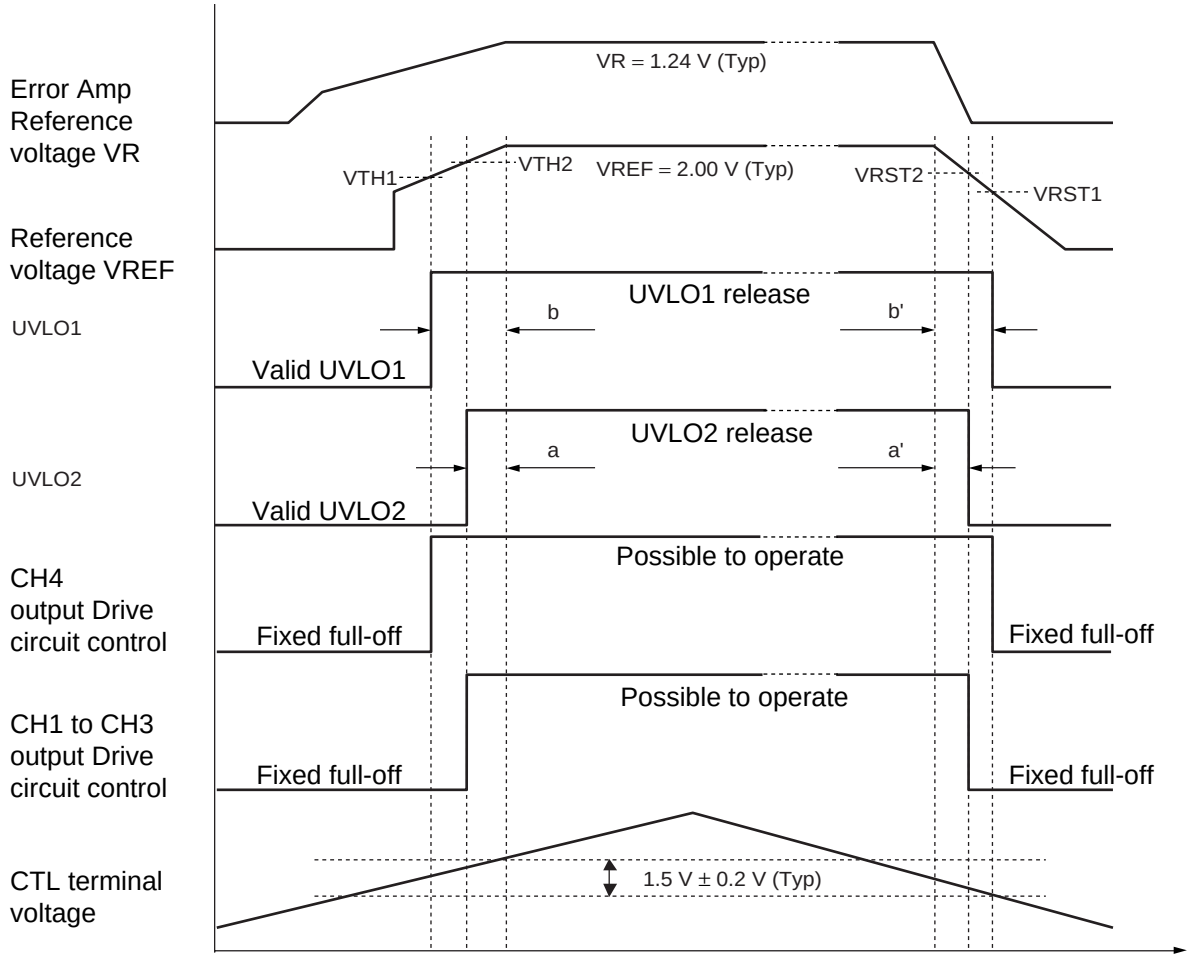
For the period to reach to 2.0 V by VREF voltage after UVLO1 and UVLO2 are released by turning on CTL (refer to a and b in "• Timing Chart") and the period when VREF decreases from 2.0 V after turning off CTL until UVLO1 and UVLO2 operate (refer to a' and b' in "• Timing Chart"), VREF which is the reference voltage does not reach 2.0 V. Therefore, the bias voltage and the bias current in IC do not reach a prescribed value, and the speed of response for IC has decreased.

Note : For this reason, when the input sudden change and the load sudden change occur in this period, IC cannot respond immediately and the output might overshoot.
Therefore, impress the voltage to CTL terminal by which the VREF terminal voltage never stays in the above-mentioned period.

• **CTL Block Equivalent Circuit**

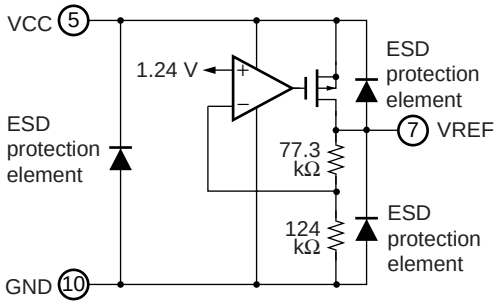


- **Timing Chart**

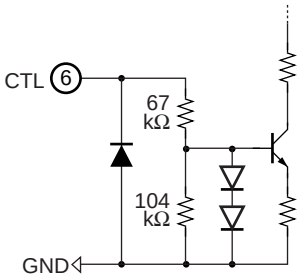


## ■ I/O EQUIVALENT CIRCUIT

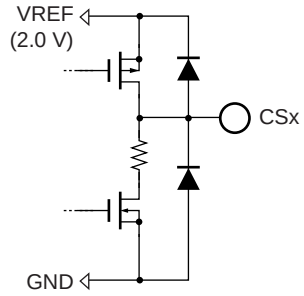
⟨⟨Reference voltage block⟩⟩



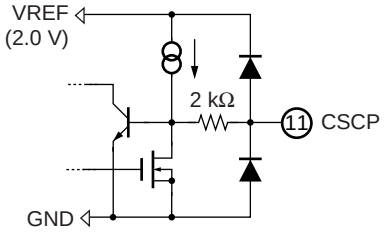

⟨⟨Control block⟩⟩



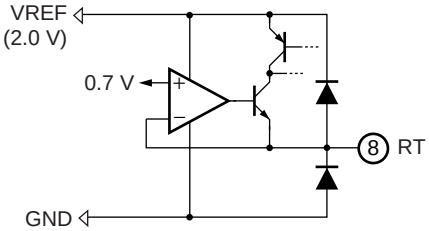

⟨⟨Soft-start block⟩⟩



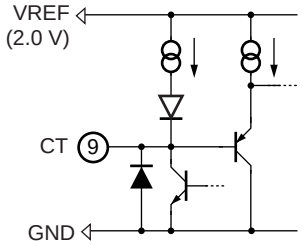

⟨⟨Short-circuit detection block⟩⟩



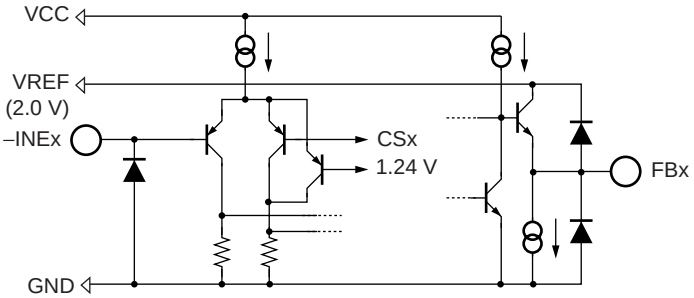

⟨⟨Triangular wave oscillator block (RT) ⟩⟩



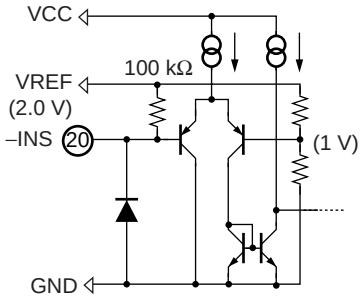

⟨⟨Triangular wave oscillator block (CT)⟩⟩



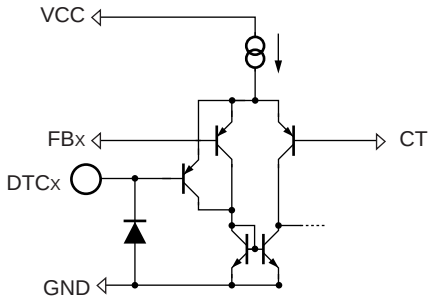

⟨⟨Error amplifier block (CH1 to CH4) ⟩⟩



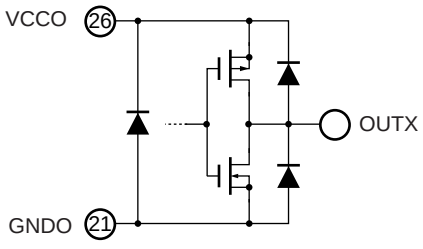

⟨⟨Short-circuit detection comparator block⟩⟩




⟨⟨PWM comparator block (CH1 to CH4) ⟩⟩

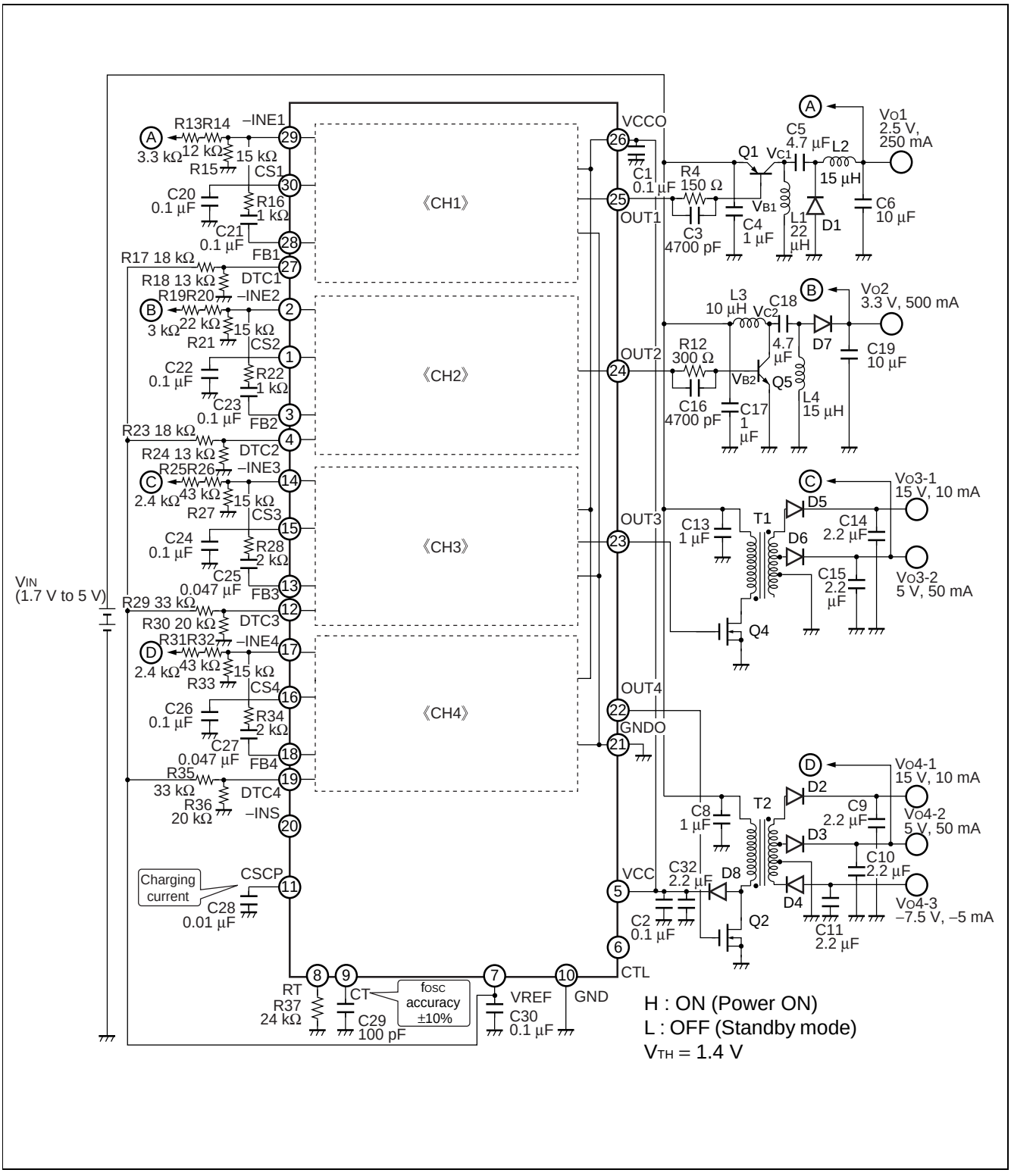



⟨⟨Output block (CH1 to CH4) ⟩⟩




x: Each channel No.

## ■ APPLICATION EXAMPLE



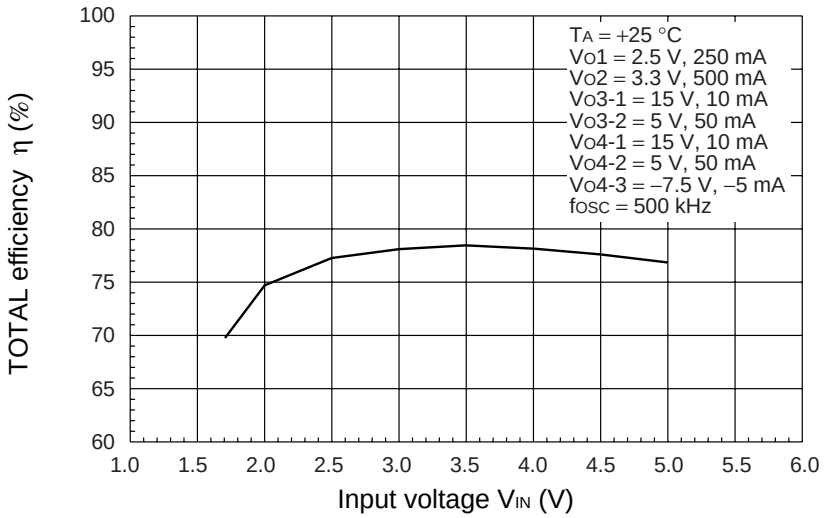
## ■ PARTS LIST

| COMPONENT | ITEM | SPECIFICATION | | VENDOR | PARTS No. |
|---|---|---|---|---|---|
| Q1, | PNP Tr | VCEO = –12 V, IC = –3 A | | SANYO | CPH3106 |
| Q2, Q4 | Nch FET | VDS = 20 V, ID = 1.8 A | | SANYO | MCH3405 |
| Q5 | NPN Tr | VCEO = 15 V, IC = 3 A | | SANYO | CPH3206 |
| D1, D7, D8 | Diode | VF = 0.4 V (Max) , at IF = 1 A | | SANYO | SBS004 |
| D2 to D6 | Diode | VF = 0.55 V (Max) , at IF = 0.5 A | | SANYO | SB05-05CP |
| L1 | Inductor | 22 µH | 0.63 A, 160 mΩ | TDK | RLF5018T-220MR63 |
| L2 | Inductor | 15 µH | 0.76 A, 120 mΩ | TDK | RLF5018T-150MR76 |
| L3 | Inductor | 10 µH | 0.94 A, 67 mΩ | TDK | RLF5018T-100MR94 |
| L4 | Inductor | 15 µH | 0.76 A, 120 mΩ | TDK | RLF5018T-150MR76 |
| T1, T2 | Transformer | — | — | SUMIDA | CLQ52 5388-T095 |
| C1, C2, C30 | Ceramics Condenser | 0.1 µF | 50 V | TDK | C1608JB1H104K |
| C3, C16 | Ceramics Condenser | 4700 pF | 50 V | TDK | C1608JB1H472K |
| C4, C8, C13 | Ceramics Condenser | 1 µF | 25 V | TDK | C3216JB1E105K |
| C5, C18 | Ceramics Condenser | 4.7 µF | 10 V | TDK | C3216JB1A475M |
| C6, C19 | Ceramics Condenser | 10 µF | 6.3 V | TDK | C3216JB0J106K |
| C9 to C11 | Ceramics Condenser | 2.2 µF | 16 V | TDK | C3216JB1C225K |
| C13, C17 | Ceramics Condenser | 1 µF | 25 V | TDK | C3216JB1E105K |
| C14, C15 | Ceramics Condenser | 2.2 µF | 16 V | TDK | C3216JB1C225K |
| C20 to C24, C26 | Ceramics Condenser | 0.1 µF | 50 V | TDK | C1608JB1H104K |
| C25, C27 | Ceramics Condenser | 0.047 µF | 50 V | TDK | C1608JB1H473K |
| C28 | Ceramics Condenser | 0.01 µF | 50 V | TDK | C1608JB1H103K |
| C29 | Ceramics Condenser | 100 pF | 50 V | TDK | C1608CH1H101J |
| R4 | Resistor | 150 Ω | 0.5% | ssm | RR0816P-151-D |
| R12 | Resistor | 300 Ω | 0.5% | ssm | RR0816P-301-D |
| R13 | Resistor | 3.3 kΩ | 0.5% | ssm | RR0816P-332-D |
| R14 | Resistor | 12 kΩ | 0.5% | ssm | RR0816P-123-D |
| R15, R21, R27 | Resistor | 15 kΩ | 0.5% | ssm | RR0816P-153-D |
| R16, R22 | Resistor | 1 kΩ | 0.5% | ssm | RR0816P-102-D |
| R17 | Resistor | 18 kΩ | 0.5% | ssm | RR0816P-183-D |
| R18 | Resistor | 13 kΩ | 0.5% | ssm | RR0816P-133-D |
| R19 | Resistor | 3 kΩ | 0.5% | ssm | RR0816P-302-D |
| R20 | Resistor | 22 kΩ | 0.5% | ssm | RR0816P-223-D |
| R23 | Resistor | 18 kΩ | 0.5% | ssm | RR0816P-183-D |
| R24 | Resistor | 13 kΩ | 0.5% | ssm | RR0816P-133-D |
| R25, R31 | Resistor | 2.4 kΩ | 0.5% | ssm | RR0816P-242-D |
| R26 | Resistor | 43 kΩ | 0.5% | ssm | RR0816P-433-D |
| R28, R34 | Resistor | 2 kΩ | 0.5% | ssm | RR0816P-202-D |
| R29, R35 | Resistor | 33 kΩ | 0.5% | ssm | RR0816P-333-D |
| R30, R36 | Resistor | 20 kΩ | 0.5% | ssm | RR0816P-203-D |
| R32 | Resistor | 43 kΩ | 0.5% | ssm | RR0816P-433-D |
| R33 | Resistor | 15 kΩ | 0.5% | ssm | RR0816P-153-D |
| R37 | Resistor | 24 kΩ | 0.5% | ssm | RR0816P-243-D |

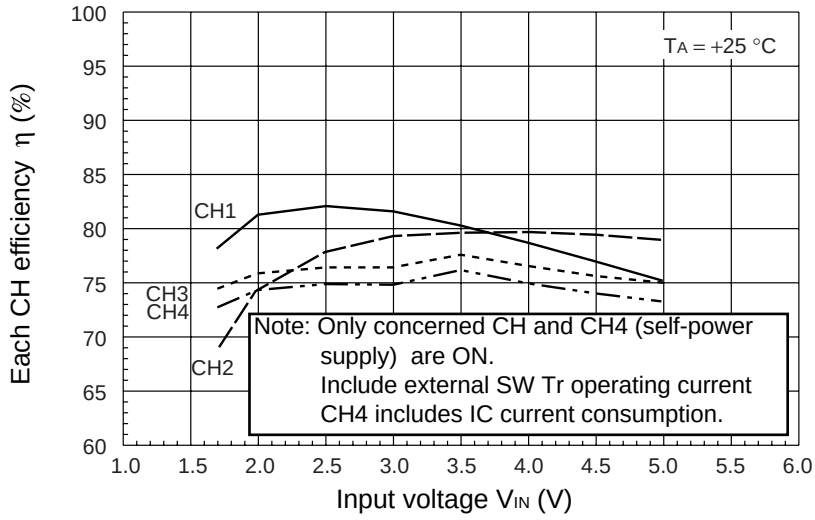
Note : SANYO : SANYO Electric Co., Ltd.
TDK : TDK Corporation
SUMIDA : SUMIDA Electric Co., Ltd.
ssm : SUSUMU Co., Ltd.

## ■ REFERENCE DATA

TOTAL Efficiency vs. Input Voltage




Each CH Efficiency vs. Input Voltage

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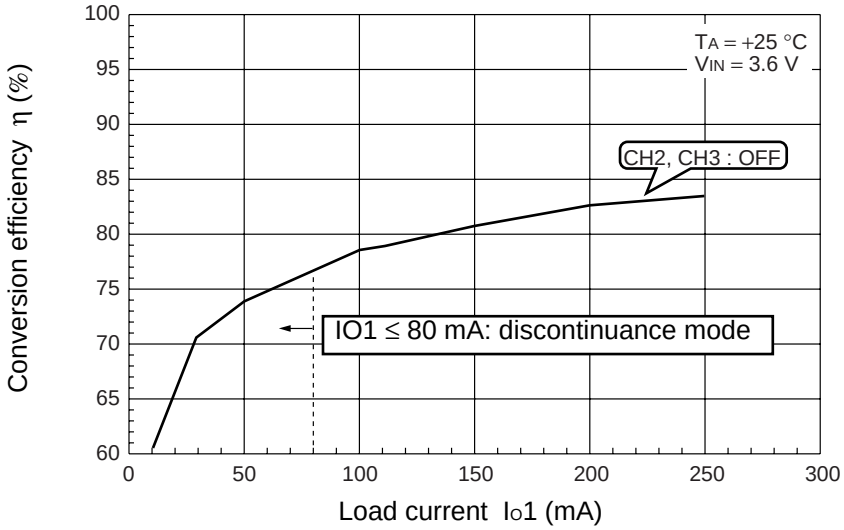
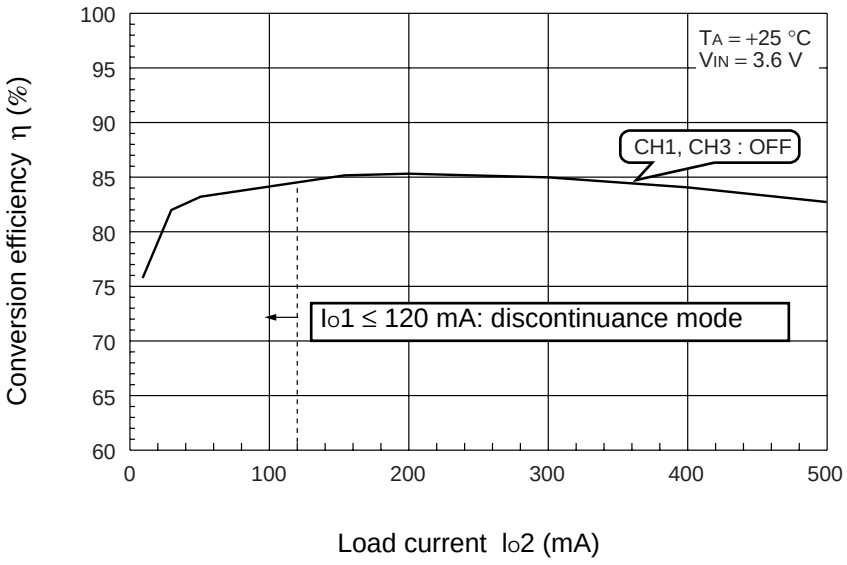
Conversion Efficiency vs. Load Current (CH1)




Conversion Efficiency vs. Load Current (CH2)

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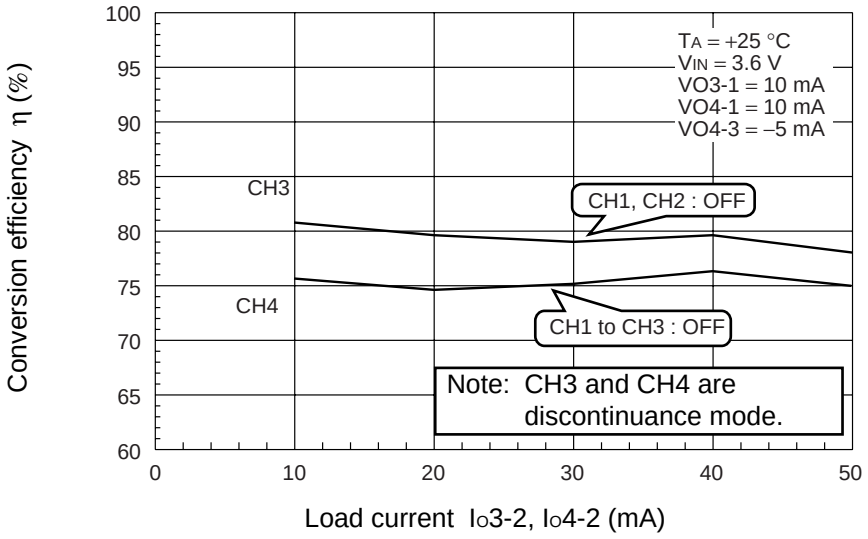
Conversion Efficiency vs. Load Current (CH3, CH4)

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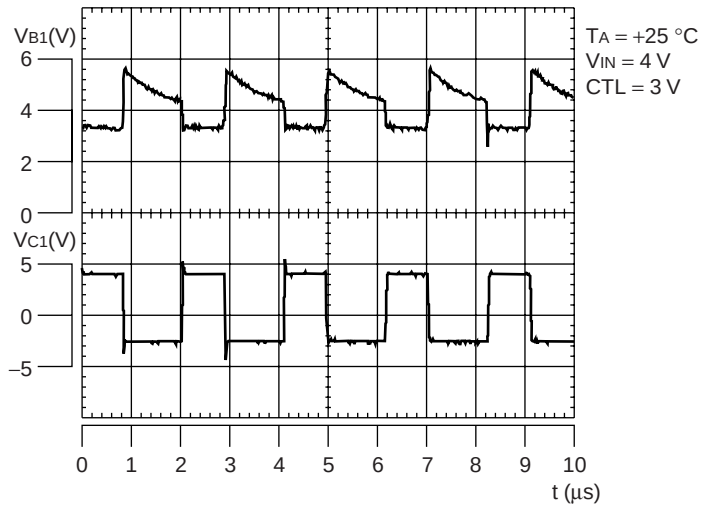
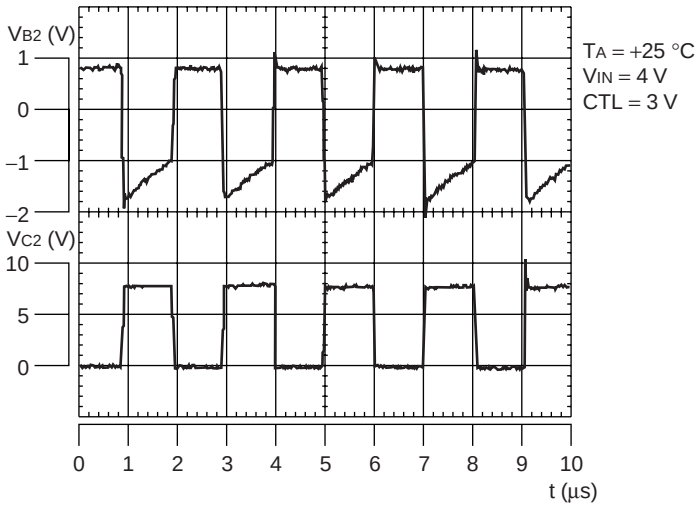
Switching Wave Form (CH1)




Switching Wave Form (CH2)



## ■ USAGE PRECAUTION

- **Printed circuit board ground lines should be set up with consideration for common impedance.**

- **Take appropriate static electricity measures.**
  - Containers for semiconductor materials should have anti-static protection or be made of conductive material.
  - After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
  - Work platforms, tools, and instruments should be properly grounded.
  - Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

- **Do not apply negative voltages.**

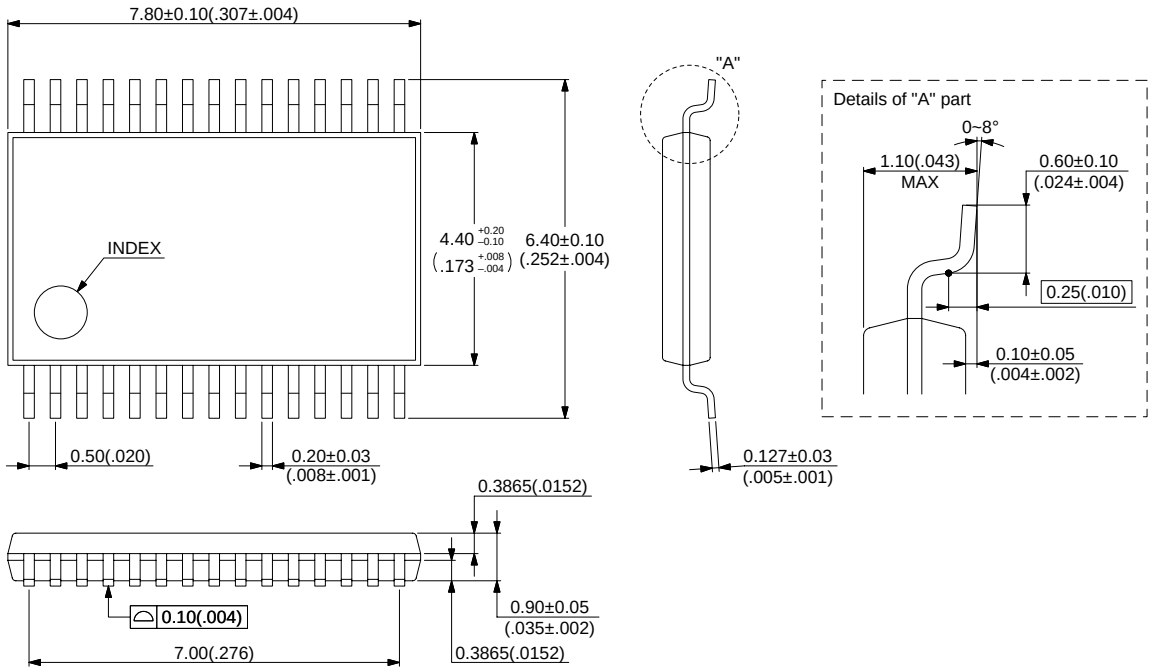
  The use of negative voltages below –0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB39A103PFT | 30-pin plastic TSSOP<br>(FPT-30P-M04) | |
| MB39A103PV3 | 32-pad plastic BCC<br>(LCC-32P-M15) | |

## ■ PACKAGE DIMENSIONS

30-pin plastic TSSOP
(FPT-30P-M04)



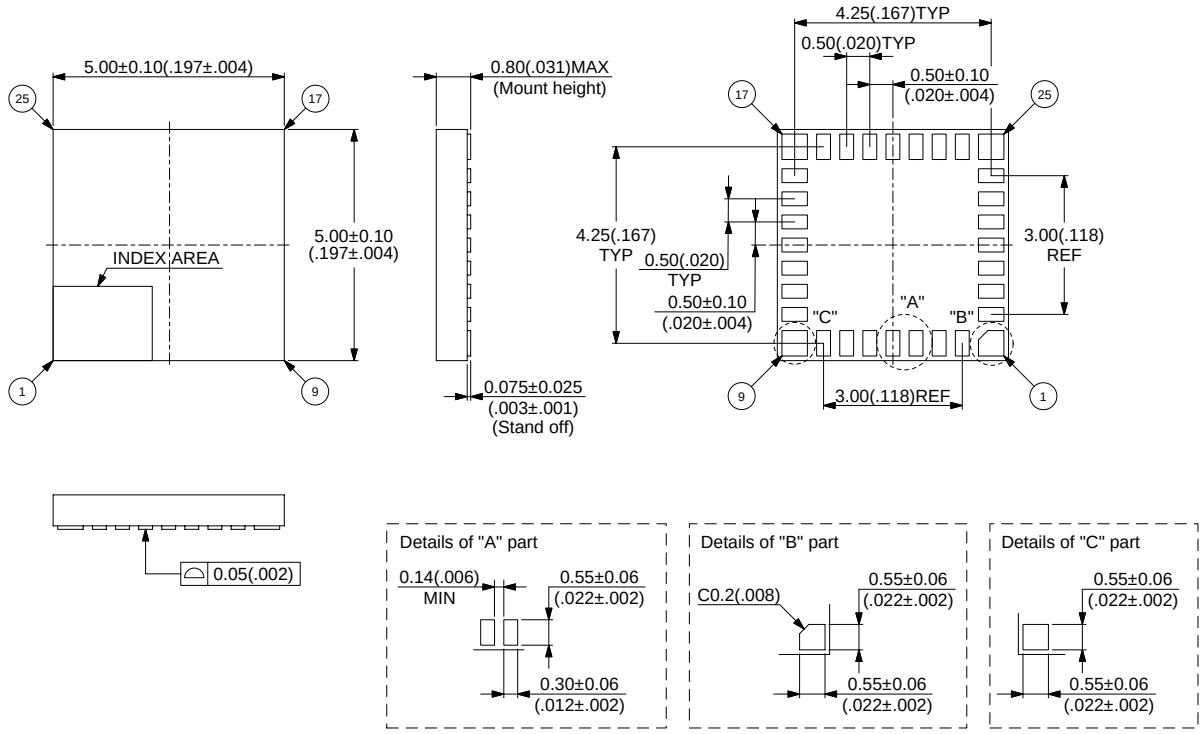



Dimensions in mm (inches)
Note: The values in parentheses are reference values.

*(Continued)*

*(Continued)*

32-pad plastic BCC
(LCC-32P-M15)






Dimensions in mm (inches)
Note: The values in parentheses are reference values.

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