FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27234-1E

ASSP For Power Supply Applications (Secondary Battery)

DC/DC Converter IC for Charging Li-ion Battery with Synchronous Rectifier

MB39A107

■ DESCRIPTION

The MB39A107 is a DC/DC converter IC suitable for down-conversion, using pulse-width modulation (PWM) charging and enabling output voltage to be set to any desired level from 1 cell to 4 cells.

The MB39A107 adopts output for Nch MOS drive of synchronous rectification type.

The MB39A107 can be used to monitor the current in an AC adapter or battery, as it contains a current amplifier that can set an offset voltage.
It can also be used for applications such as setting the charging voltages for 2 batteries.

The MB39A107 provides a broad power supply voltage range and low standby current as well as high efficiency, making it ideal for use as a built-in charging device in products such as notebook PC.

■ FEATURES

- Built-in low-current control circuits in two systems (supporting dynamically controlled charging)
- The charge current value can be analog controlled (+INE1 and +INE2 terminal)
- Built-in synchronous rectification system output for Nch MOS FET
- Built-in charge pump for driving high-side Nch MOS, providing 100% on-duty support
- Built-in AC adapter detection function
- Output voltage setting accuracy : 4.2 V ± 0.74 % (Ta = − 10 °C to + 85 °C)

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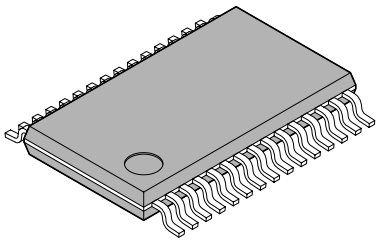
■ PACKAGE

30-pin plastic TSSOP



(FPT-30P-M04)

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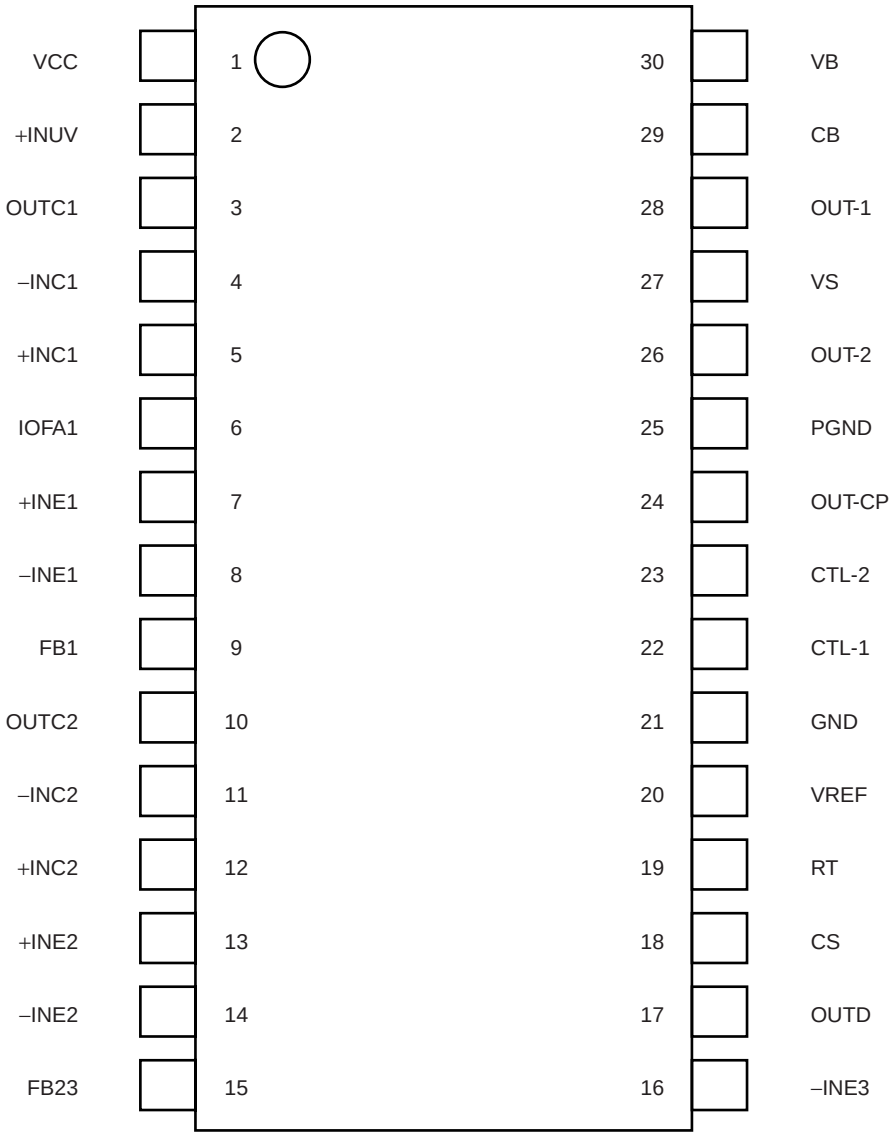
- Built-in high accuracy current detection amplifier : ± 5 % (input voltage difference at 100 mV)
  : ±15 % (input voltage difference at 20 mV)
- Output voltage setting using external resistor : 1 cell to 4 cells
- Oscillation frequency range : 100 kHz to 1 MHz
- In standby mode, leave output voltage setting resistor open to prevent inefficient current loss.
- Built-in standby current function : 0 μA (Typ)
- Built-in soft-start function independent of loads

■ PIN ASSIGNMENT

(TOP VIEW)

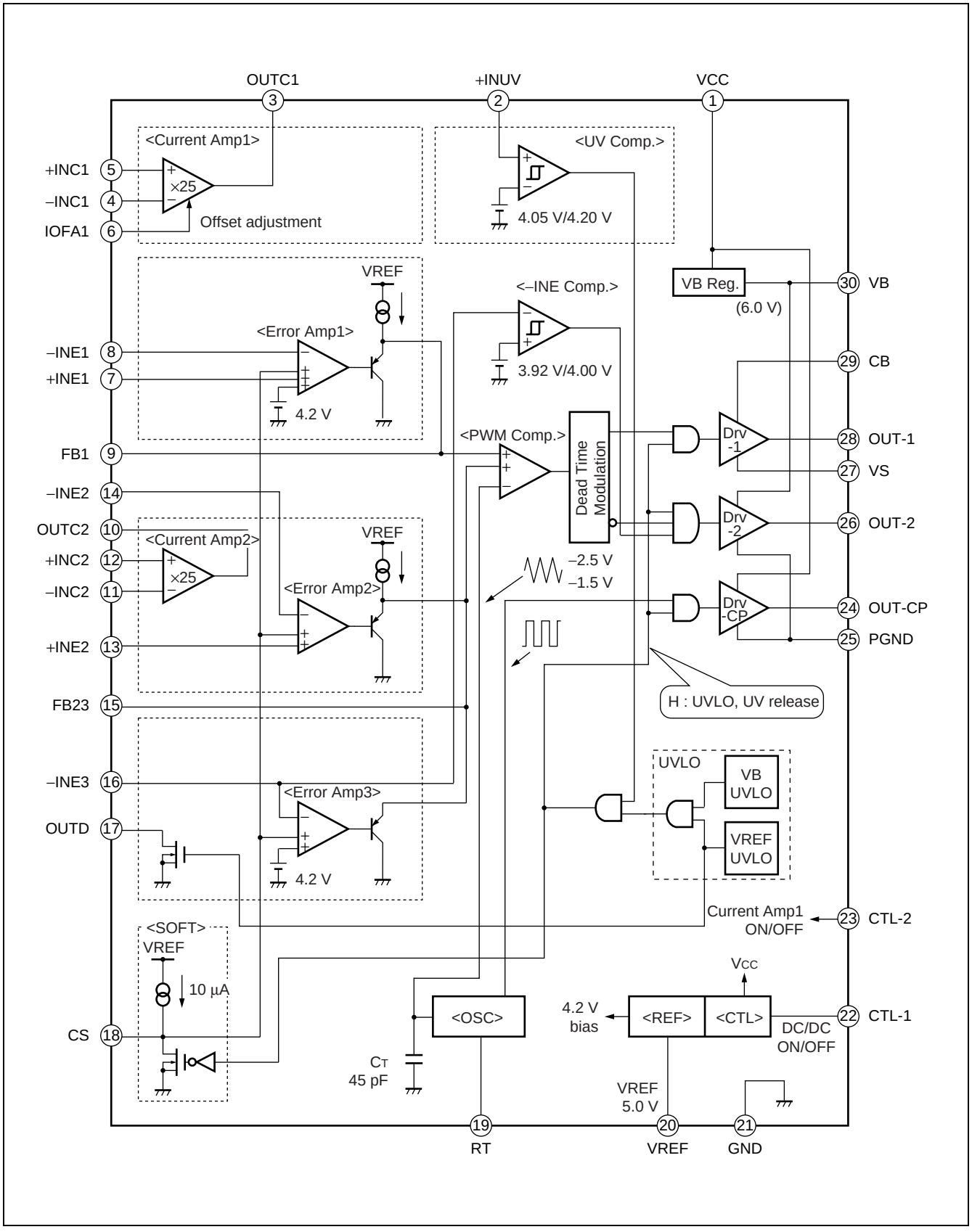


(FPT-30P-M04)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Descriptions
1	VCC	—	Reference voltage, control circuit power supply terminal
2	+ INUV	I	Low input voltage detection comparater (UV Comp.) input terminal
3	OUTC1	O	Current detection amplifier (Current Amp1) output terminal
4	− INC1	I	Current detection amplifier (Current Amp1) input terminal
5	+ INC1	I	Current detection amplifier (Current Amp1) input terminal
6	IOFA1	I	Current detection amplifier (Current Amp1) offset voltage input terminal
7	+ INE1	I	Error amplifier (Error Amp1) non-inverted input terminal
8	− INE1	I	Error amplifier (Error Amp1) inverted input terminal
9	FB1	O	Error amplifier (Error Amp1) output terminal
10	OUTC2	O	Current detection amplifier (Current Amp2) output terminal
11	− INC2	I	Current detection amplifier (Current Amp2) input terminal
12	+ INC2	I	Current detection amplifier (Current Amp2) input terminal
13	+ INE2	I	Error amplifier (Error Amp2) non-inverted input terminal
14	− INE2	I	Error amplifier (Error Amp2) inverted input terminal
15	FB23	O	Error amplifier (Error Amp2, 3) output terminal
16	− INE3	I	Error amplifier (Error Amp3) inverted input terminal
17	OUTD	O	With IC in standby mode, this terminal is set to Hi-Z to prevent loss of current through output voltage setting resistance. Set CTL terminal to “H” level to output “L” level.
18	CS	—	Soft-start capacitor connection terminal
19	RT	—	Triangular waveform oscillation frequency setting resistor connection terminal
20	VREF	O	Reference voltage output terminal
21	GND	—	Ground terminal
22	CTL-1	I	DC/DC converter block power supply control terminal
23	CTL-2	I	Current detection amplifier (Current Amp1) power supply control terminal
24	OUT-CP	O	External main-side FET charge pump output terminal for driving gate
25	PGND	—	Ground teriminal
26	OUT-2	O	External synchronous rectification-side FET output terminal for driving gate
27	VS	—	External main-side FET source connection terminal
28	OUT-1	O	External main-side FET output terminal for driving gate
29	CB	—	This terminal generates a voltage of “VCC + about 5 V” with a capacitor and an SBD connected to the OUT-CP, VB, and CB terminals.
30	VB	O	Output circuit bias output terminal

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	—	—	27	V
Boot voltage	V_{CB}	CB terminal	—	32	V
Control input voltage	V_{CTL}	CTL-1 terminal, CTL-2 terminal	—	27	V
Output current	I_{OUT}	—	—	60	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	1390*	mW
Storage temperature	T_{STG}	—	− 55	+125	°C

* : The packages are mounted on the dual-sided epoxy board (10 cm × 10 cm) .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	—	7	—	25	V
Boot voltage	V_{CB}	CB terminal	—	—	30	V
Reference voltage output current	I_{REF}	VREF terminal	− 1	—	0	mA
Bias output current	I_{VB}	VB terminal	− 1	—	0	mA
Input voltage	V_{INE}	+ INE1, + INE2, + INE3, − INE1, − INE2 terminal	0	—	V_{CC} − 1.8	V
	V_{INC}	+ INC1, + INC2, − INC1, − INE2 terminal	0	—	V_{CC}	V
	V_{INUV}	+ INUV terminal	0	—	V_{CC}	V
IOFA1 terminal input voltage	V_{IOFA1}	—	0	—	5	V
OUTD terminal output voltage	V_{OUTD}	—	0	—	17	V
OUTD terminal output current	I_{OUTD}	—	0	—	2	mA
CTL terminal input voltage	V_{CTL}	—	0	—	25	V
Output current	I_{OUT}	—	− 45	—	+ 45	mA
Peak output current	I_{OUT}	Main side Duty ≤ 5% (t = 1/fosc × Duty)	− 800	—	+ 800	mA
	I_{OUT}	Synchronous rectification side Duty ≤ 5% (t = 1/fosc × Duty)	− 1200	—	+ 1200	mA
Oscillation frequency	f_{OSC}	—	100	500	1000	kHz
Timing resistor	R_T	—	22	47	200	kΩ
Soft-start capacitor	C_S	—	—	0.022	1.0	µF
Charge pump capacitor	C_{CP}	—	—	0.33	—	µF
CB terminal capacitor	C_{CB}	—	0.47	1.0	—	µF
Bias output capacitor	C_{VB}	—	0.47	1.0	—	µF
Reference voltage output capacitor	C_{REF}	—	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	− 30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = 19 V, VB = 0 mA, VREF = 0 mA, Ta = + 25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Reference Voltage Block [Ref]	Output voltage	V_{REF1}	20	Ta = + 25 °C	4.967	5.000	5.041	V
		V_{REF2}	20	Ta = − 10 °C to + 85 °C	4.95	5.00	5.05	V
	Input stability	Line	20	VCC = 7 V to 25 V	—	3	10	mV
	Load stability	Load	20	VREF = 0 mA to − 1 mA	—	1	10	mV
	Short-circuit output current	Ios	20	VREF = 1 V	− 50	− 25	− 12	mA
Under Voltage (VCC) Lockout Circuit Block [UVLO]	Threshold voltage	V_{TLH}	30	VB = ↑	3.80	4.00	4.20	V
		V_{THL}	30	VB = ↓	3.10	3.30	3.50	V
	Hysteresis width	V_H	30	—	0.49	0.70	0.91	V
	Threshold voltage	V_{TLH}	20	VREF = ↑	2.6	2.8	3.0	V
		V_{THL}	20	VREF = ↓	2.4	2.6	2.8	V
	Hysteresis width	V_H	20	—	0.05	0.20	0.35	V
Soft-start Circuit Block [SOFT]	Charge current	I_{CS}	18	—	− 14	− 10	− 6	µA
Triangular Wave Oscillator Block [OSC]	Oscillation frequency	f_{OSC}	28	RT = 47 kΩ	450	500	550	kHz
	Frequency temperature variation	$\Delta f_{OSC}/f_{OSC}$	28	Ta = − 30 °C to +85 °C	—	1*	—	%
Error Amp Block [Error Amp1]	Threshold voltage	V_{TH1}	8, 9	FB1 = 2 V, Ta = +25 °C	4.179	4.200	4.221	V
		V_{TH2}	8, 9	FB1 = 2 V, Ta = − 10 °C to +85 °C	4.169	4.200	4.231	V
	Input offset voltage	V_{IO}	7, 8	FB1 = 2 V	—	1	5	mV
	Input bias current	I_B	7, 8	− INE1 = + INE1 = 0 V	− 100	− 30	—	nA
	Voltage gain	A_V	7, 8, 9	DC	—	100*	—	dB
	Frequency bandwidth	BW	7, 8, 9	A_V = 0 dB	—	1.2*	—	MHz
	Output voltage	V_{FBH}	9	—	4.8	5.0	—	V
		V_{FBL}	9	—	—	0.8	0.9	V
	Output source current	I_{SOURCE}	9	FB1 = 2 V	—	− 120	− 60	µA
	Output sink current	I_{SINK}	9	FB1 = 2 V	2.0	4.0	—	mA

* : Standard design value

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(VCC = 19 V, VB = 0 mA, VREF = 0 mA, Ta = + 25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Error Amp Block [Error Amp2]	Input offset voltage	V_{IO}	13, 14	FB23 = 2 V	—	1	5	mV
	Input bias current	I_B	13, 14	− INE2 = + INE2 = 0 V	− 100	− 30	—	nA
	Voltage gain	A_V	13, 14, 15	DC	—	100*	—	dB
	Frequency bandwidth	BW	13, 14, 15	A_V = 0 dB	—	1.2*	—	MHz
	Output voltage	V_{FBH}	15	—	4.8	5.0	—	V
		V_{FBL}	15	—	—	0.8	0.9	V
	Output source current	I_{SOURCE}	15	FB23 = 2 V	—	− 120	− 60	µA
	Output sink current	I_{SINK}	15	FB23 = 2 V	2.0	4.0	—	mA
Error Amp Block [Error Amp3]	Threshold voltage	V_{TH1}	15, 16	FB23 = 2 V, Ta = +25 °C	4.179	4.200	4.221	V
		V_{TH2}	15, 16	FB23 = 2 V, Ta = − 10 °C to +85 °C	4.169	4.200	4.231	V
	Voltage gain	A_V	15, 16	DC	—	100*	—	dB
	Frequency bandwidth	BW	15, 16	A_V = 0 dB	—	1.2*	—	MHz
	Output voltage	V_{FBH}	15	—	4.8	5.0	—	V
		V_{FBL}	15	—	—	0.8	0.9	V
	Output source current	I_{SOURCE}	15	FB23 = 2 V	—	− 120	− 60	µA
	Output sink current	I_{SINK}	15	FB23 = 2 V	2.0	4.0	—	mA
	OUTD terminal output leakage current	I_{LEAK}	17	OUTD = 17 V	—	0	1	µA
	OUTD terminal output ON resistor	R_{ON}	17	OUTD = 1 mA	—	35	50	Ω
Current Detection Amp Block [Current Amp1]	Current detection voltage	V_{OUTC1}	3	+ INC1 = 9 V to VCC, ΔV_{IN} = − 100 mV, IOFA1 = 0 V	2.375	2.5	2.625	V
		V_{OUTC2}	3	+ INC1 = 9 V to VCC, ΔV_{IN} = − 20 mV, IOFA1 = 0 V	0.425	0.5	0.575	V
		V_{OUTC3}	3	+ INC1 = 0 V to 9 V, ΔV_{IN} = − 100 mV, IOFA1 = 0 V	2.25	2.5	2.75	V
		V_{OUTC4}	3	+ INC1 = 0 V to 9 V, ΔV_{IN} = − 100 mV, IOFA1 = 0 V	0.25	0.5	0.75	V
	Voltage gain	A_V	3, 4, 5	+ INC1 = 3 V to VCC, ΔV_{IN} = − 20 mV, IOFA1 = 0 V	24.25	25	25.75	V/V

* : Standard design value

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(VCC = 19 V, VB = 0 mA, VREF = 0 mA, Ta = + 25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Current Detection Amp Block [Current Amp1]	Input current	I_{INC1}	4, 5	+ INC1 = − INC1 = 19 V	—	50	75	µA
		I_{INC2}	4, 5	CTL-2 = 0 V, + INC1 = − INC1 = 19 V	—	0	1	µA
	Frequency bandwidth	BW	3, 4, 5	A_V = 0 dB	—	0.2*	—	MHz
	IOFA1 terminal input current	I_{OFA1}	6	IOFA1 = 2.5 V	− 100	− 30	—	nA
	Output voltage	V_{OUTCH}	3	—	5.3	5.6	—	V
		V_{OUTCL}	3	—	—	20	200	mV
	Output source current	I_{SOURCE}	3	OUTC = 2 V	—	− 2	− 1	mA
	Output sink current	I_{SINK}	3	OUTC = 2 V	150	300	—	µA
Current Detection Amp Block [Current Amp2]	Current detection voltage	V_{OUTC1}	10	+ INC2 = 9 V to VCC, ΔV_{IN} = − 100 mV, IOFA1 = 0 V	2.375	2.5	2.625	V
		V_{OUTC2}	10	+ INC2 = 9 V to VCC, ΔV_{IN} = − 20 mV, IOFA1 = 0 V	0.425	0.5	0.575	V
		V_{OUTC3}	10	+ INC2 = 0 V to 9 V, ΔV_{IN} = − 100 mV, IOFA1 = 0 V	2.25	2.5	2.75	V
		V_{OUTC4}	10	+ INC2 = 0 V to 9 V, ΔV_{IN} = − 100 mV, IOFA1 = 0 V	0.25	0.5	0.75	V
	Voltage gain	A_V	10, 11, 12	+ INC2 = 3 V to VCC, ΔV_{IN} = − 100 mV	24.25	25	25.75	V/V
	Input current	I_{INC1}	11, 12	+ INC2 = − INC2 = 19 V	—	50	75	µA
		I_{INC2}	11, 12	CTL-1 = 0 V, + INC2 = − INC2 = 19 V	—	0	1	µA
	Frequency bandwidth	BW	10, 11, 12	A_V = 0 dB	—	0.2*	—	MHz
	Output voltage	V_{OUTCH}	10	—	5.3	5.6	—	V
		V_{OUTCL}	10	—	—	20	200	mV
	Output source current	I_{SOURCE}	10	OUTC2 = 2 V	—	− 2	− 1	mA
	Output sink current	I_{SINK}	10	OUTC2 = 2 V	150	300	—	µA
PWM Comparator Block [PWM Comp.]	Threshold voltage	V_{TL}	9, 15	Duty cycle = 0%	1.4	1.5	—	V
		V_{TH}	9, 15	Duty cycle = 100%	—	2.5	2.6	V

* : Standard design value

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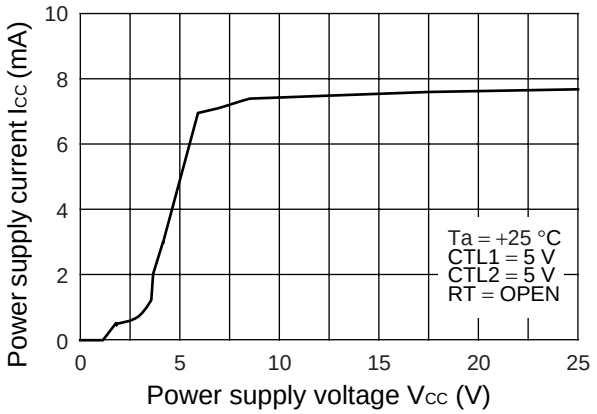
(VCC = 19 V, VB = 0 mA, VREF = 0 mA, Ta = + 25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Output Block [Drv-1, 2]	Output source current	I_{SOURCE}	28	Main side, Duty ≤ 5% (t = 1/fosc × Duty)	—	– 600*	—	mA
		I_{SOURCE}	26	Synchronous rectification side, Duty ≤ 5% (t = 1/fosc × Duty)	—	– 800*	—	mA
	Output sink current	I_{SINK}	28	Main side, Duty ≤ 5% (t = 1/fosc × Duty)	—	800*	—	mA
		I_{SINK}	26	Synchronous rectification side, Duty ≤ 5% (t = 1/fosc × Duty)	—	1000*	—	mA
	Dead time	t_{D1}	26, 28	—	—	100*	—	ns
		t_{D2}	26, 28	—	—	100*	—	ns
Charge Pump Block [Drv-CP]	Output ON resistor	R_{OH}	24	OUT-CP = – 45 mA	—	2	10	Ω
	Output sink current	I_{SINK}	24	OUT-CP = 10 V	—	200*	—	mA
Low Input Voltage Detection Comparator Block [UV Comp.]	Threshold voltage	V_{TLH}	2, 28	+ INUV = ↗	4.12	4.2	4.28	V
		V_{THL}	2, 28	+ INUV = ↘	3.97	4.05	4.13	V
	Hysteresis width	V_H	2, 28	—	—	0.15	—	V
	Input bias current	I_{INUV}	2	+ INUV = 0 V	– 200	– 100	—	nA
Battery Voltage Detection Comparator Block [– INE Comp.]	Threshold voltage	V_{TLH}	16	– INE3 = ↗	3.89	3.93	3.97	V
		V_{THL}	16	– INE3 = ↘	3.85	3.89	3.93	V
	Hysteresis width	V_H	16	—	—	0.04	—	V
Bias Voltage Block [VB]	Output voltage	V_B	30	—	5.9	6	6.1	V
Control Block [CTL]	ON condition	V_{ON}	22, 23	CTL-1, CTL-2 terminal	2	—	25	V
	OFF condition	V_{OFF}	22, 23	CTL-1, CTL-2 terminal	0	—	0.8	V
	Input current	I_{CTLH}	22, 23	CTL-1 = CTL-2 = 5 V	—	100	150	µA
		I_{CTLL}	22, 23	CTL-1 = CTL-2 = 0 V	—	0	1	µA
General	Standby current	I_{CCS}	1	CTL-1 = CTL-2 = 0 V	—	0	10	µA
	Power supply current	I_{CC1}	1	CTL-1 = CTL-2 = 5 V	—	12	18	mA
		I_{CC2}	1	CTL-1 = 5 V, CTL-2 = 0 V	—	10.5	15.8	mA
		I_{CC3}	1	CTL-1 = 0 V, CTL-2 = 5 V	—	2.1	3.2	mA

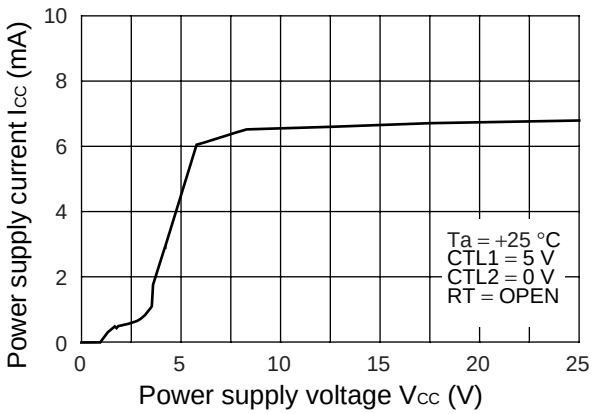
* : Standard design value

■ TYPICAL CHARACTERISTICS

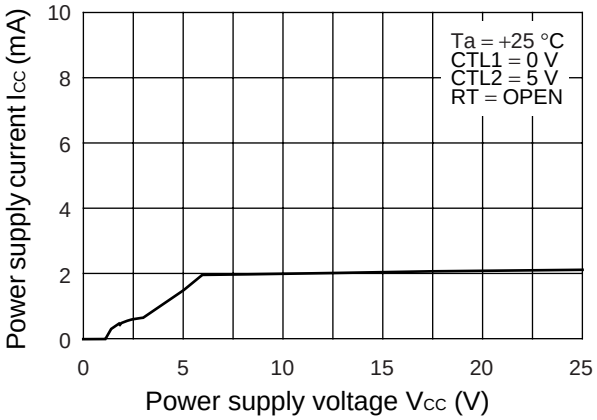
Power Supply Current vs. Power Supply Voltage



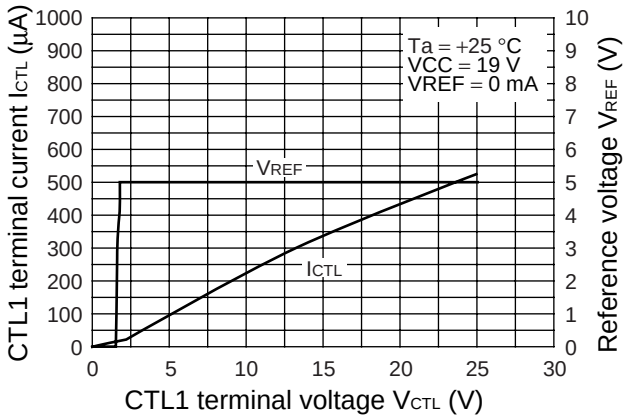
Power Supply Current vs. Power Supply Voltage



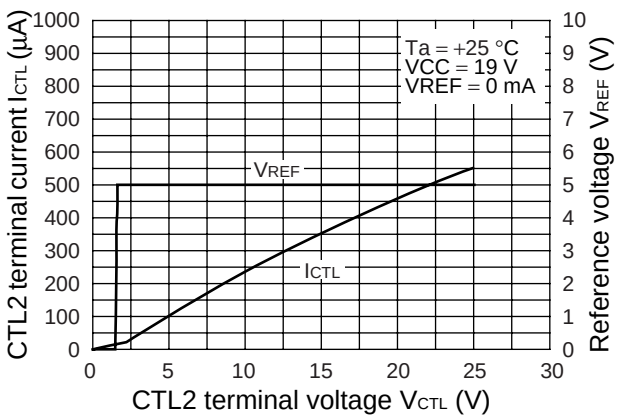
Power Supply Current vs. Power Supply Voltage



CTL1 Terminal Current, Reference Voltage vs. CTL1 Terminal Voltage



CTL2 Terminal Current, Reference Voltage vs. CTL2 Terminal Voltage



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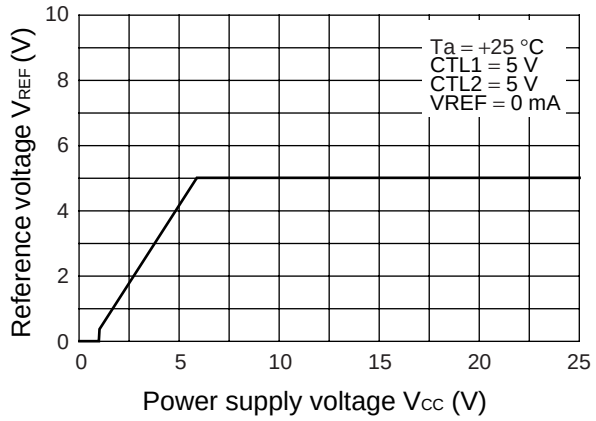
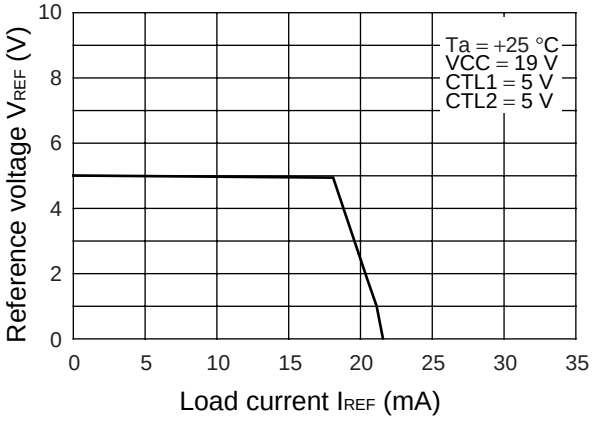
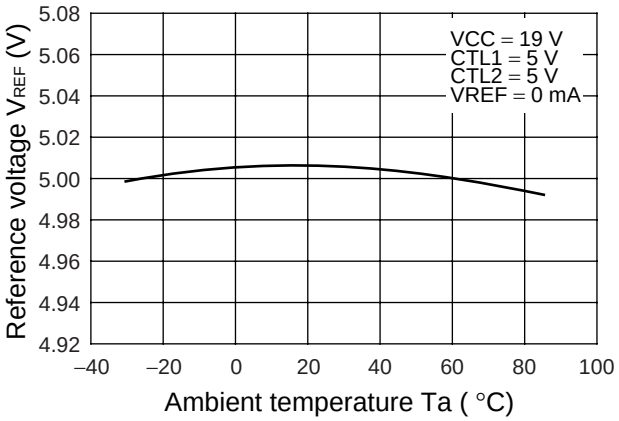
Reference Voltage vs. Power Supply Voltage



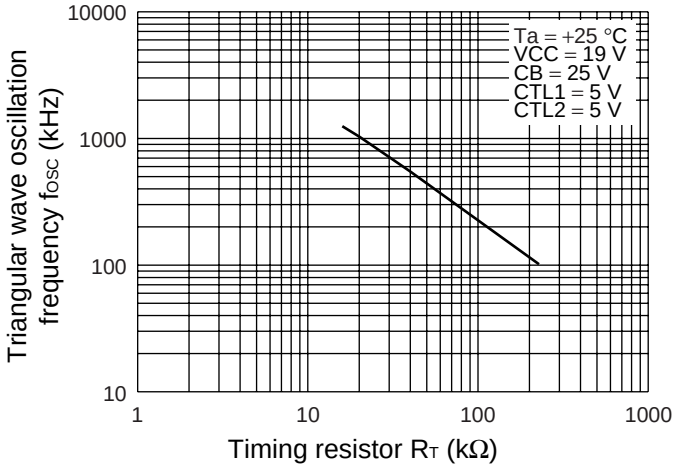
Reference Voltage vs. Load Current



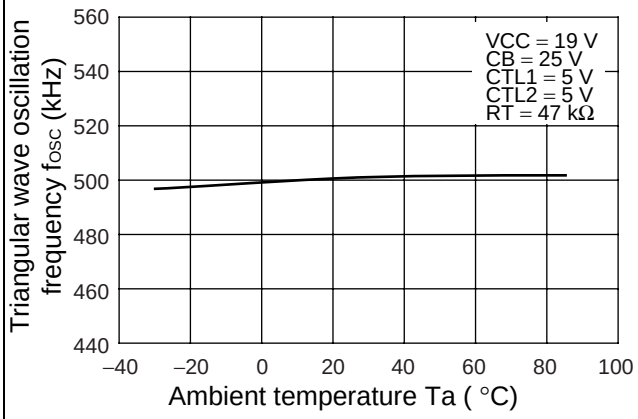
Reference Voltage vs. Ambient Temperature



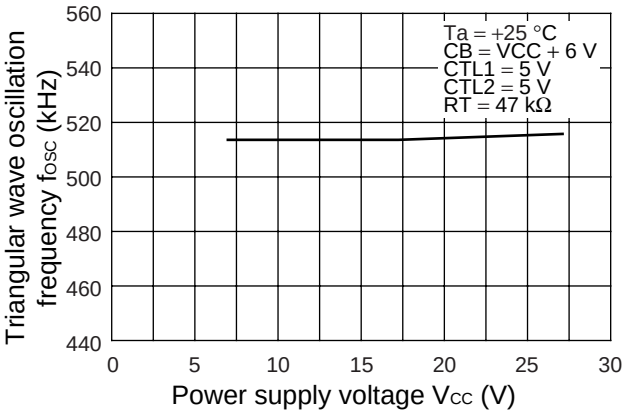
Triangular Wave Oscillation Frequency vs. Timing Resistor



Triangular Wave Oscillation Frequency vs. Ambient Temperature



Triangular Wave Oscillation Frequency vs. Power Supply Voltage



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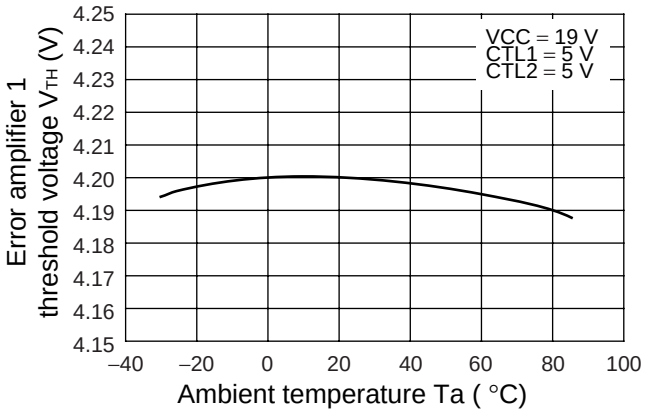
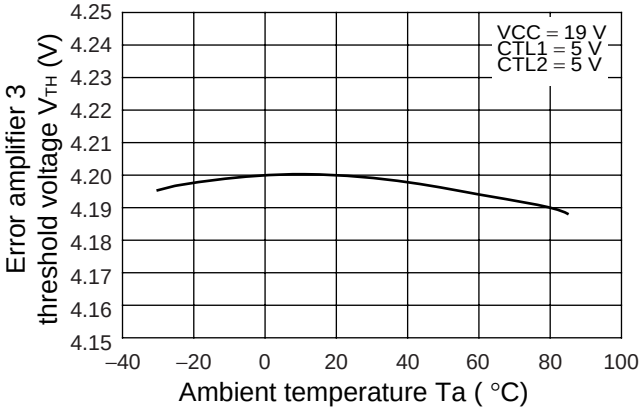
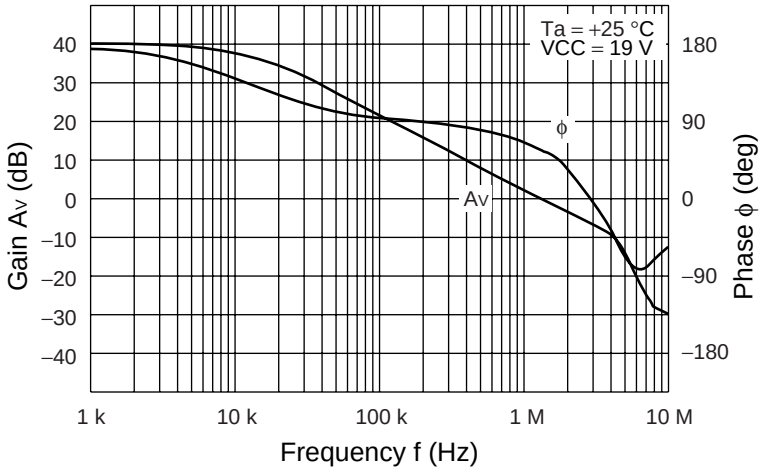
Error Amplifier 1 Threshold Voltage vs. Ambient Temperature

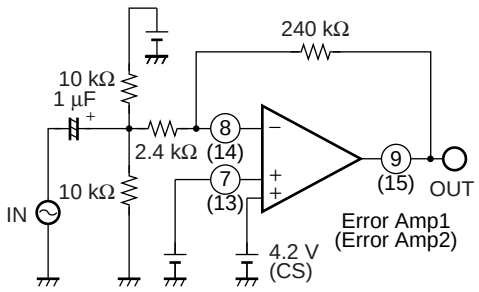


Error Amplifier 3 Threshold Voltage vs. Ambient Temperature

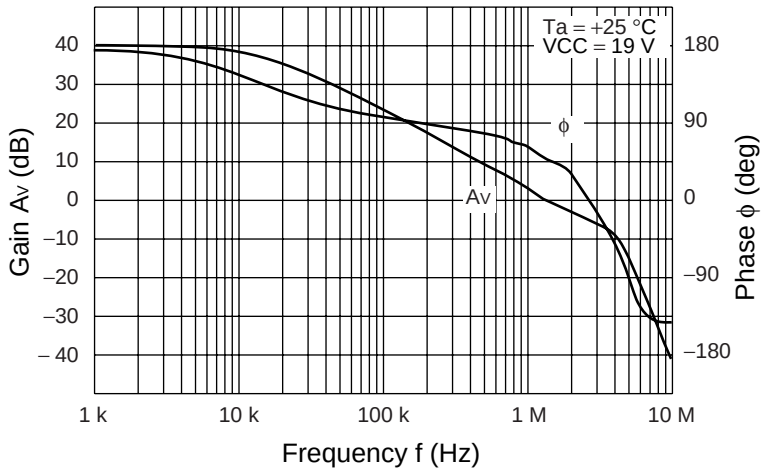


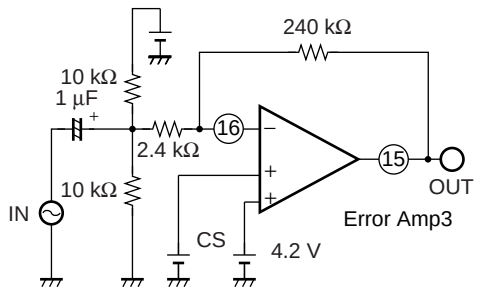
Error Amplifer, Gain and Phase vs. Frequency





Error Amplifier, Gain and Phase vs. Frequency





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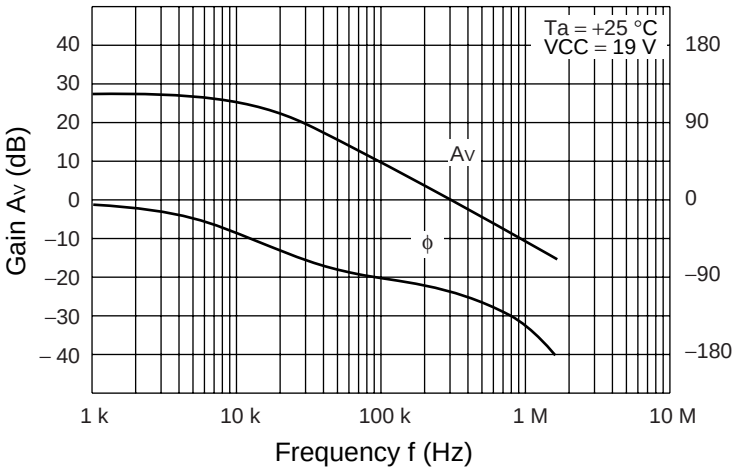
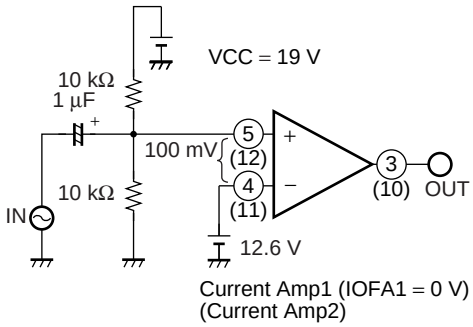
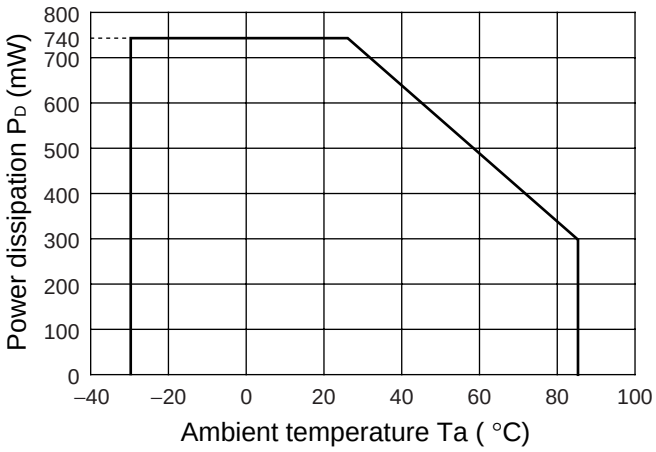
Current Detection Amplifier, Gain and Phase vs. Frequency





Power Dissipation vs. Ambient Temperature



■ FUNCTIONAL DESCRIPTION

1. DC/DC Converter Functions

(1) Reference voltage block (REF)

The reference voltage circuit generates a temperature-compensated reference voltage (5.0 V Typ) using the voltage supplied from the VCC terminal (pin 1) . The voltage is used as the reference voltage for the IC's internal circuit.

The reference voltage can be used to supply a load current of up to 1 mA to an external device through the VREF terminal (pin 20) .

(2) Triangular wave oscillator block (OSC)

The triangular wave oscillator incorporates a triangular oscillation frequency setting capacitor connected

respectively to the RT terminal (pin 19) to generate triangular oscillation waveforms.

The triangular oscillation waveforms are input to the IC's internal PWM comparator.

(3) Error amplifier block (Error Amp1)

The error amplifier detects output signal of current detection amplifier (Current Amp2) and outputs PWM control signal by comparison with +INE1 terminal (pin 7), also controls charge current.

Charge current controls by this amplifier and by the error amplifier (Error Amp2) allow two constant current values to be set to offer fail-safe control.

By connecting a feedback resistor and capacitor between FBI terminal (pin 9) and − INE1 terminal (pin 8), it is possible to create any desired level of loop gain, thereby providing stable phase compensation to the system.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with the CS terminal (pin 18).

The use of Error amplifier for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load.

The amplifier can serve for constant current control in combination with the current detection amplifier (Current Amp1) .

(4) Error amplifier block (Error Amp2)

The error amplifier detects output signal of current detection amplifier (Current Amp2) and outputs PWM control signal by comparison with +INE2 terminal (pin 13), also controls charge current.

By connecting a feedback resistor and capacitor between FB23 terminal (pin 15) and − INE2 terminal (pin 14), it is possible to create any desired level of loop gain, thereby providing stable phase compensation to the system.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with the CS terminal (pin 18).

The use of Error amplifier for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load.

(5) Error amplifier block (Error Amp3)

The error amplifier (Error Amp3) detects the DC/DC converter output voltage and outputs PWM control signals.

An arbitrary output voltage can be set for 1 to 4 cells by connecting external output voltage setting resistors to the error amplifier inverting input pins.

By connecting a feedback resistor and capacitor between FB23 terminal (pin 15) and − INE3 terminal (pin 16), it is possible to create any desired level of loop gain, thereby providing stable phase compensation to the system.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with the CS terminal (pin 18).

The use of Error amplifier for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load.

(6) Current detection amplifier block (Current Amp1)

The current detection amplifier (Current Amp1) uses the +INC1 terminal (pin 5) and −INC1 terminal (pin 4) to detect a voltage drop which occurs between both ends of the sense resistor (R_{S2}) due to the flow of the AC adapter current and outputs the signal amplified 25 times to the OUTC1 terminal (pin 3) .
It is also possible to set an offset voltage equal to the voltage applied to the IOFA1 terminal (pin 6) .

(7) Current detection amplifier block (Current Amp2)

The current detection amplifier (Current Amp2) uses the +INC2 terminal (pin 12) and −INC2 terminal (pin 11) to detect a voltage drop which occurs between both ends of the output sense resistor (R_{S1}) due to the flow of the charge current and outputs the signal amplified 25 times to the OUTC2 terminal (pin 10) .

(8) PWM comparator block (PWM Comp.)

The PWM comparator is a voltage-pulse width modulator that controls the output duty depending on the output voltage of error amplifier (Error Amp1, Error Amp2 and Error Amp3).

The PWM comparator compares the triangular wave voltage generated by the triangular wave oscillator with the error amplifier output voltage. Then it turns on the output transistor on the main side and turns off the output transistor on the synchronous rectification side during the interval in which the triangular wave voltage is lower than the error amplifier output voltage.

(9) Output block (Drv-1, Drv-2)

The output circuit on the main side and on the synchronous rectification side are both in the totem pole configuration, capable of driving an external Nch MOS FET.

(10) Charge pump block (Drv-CP)

The CB terminal is a power supply terminal of output circuit (Drv-1) for the main side external Nch MOS FET drive. The CB terminal generates “VCC + about 5 V” in the OUT-CP terminal (pin 24) , VB terminal (pin 30) , and CB terminal (pin 29) by connecting the capacitor with SBD.

(11) Power supply control block

Setting the CTL-1 terminal (pin 22) and CTL-2 terminal (pin 23) “L” level in the standby mode. (The supply current is 10 μA at maximum in the standby mode.) Setting the CTL-1 and CTL-2 terminals “H” level allows the DC/DC converter and current detection amplifier (Current Amp1) to operate independently of each other.

CTL function table

CTL-1	CTL-2	DC/DC converter block	Current Amp1
L	L	OFF	OFF
H	L	ON	OFF
L	H	OFF	ON
H	H	ON	ON

(12) Bias voltage block

6 V (Typ) is as a power supply of the output circuit and potential for the charge pump output voltage setting.

(13) Battery voltage detection comparator block (– INEComp.)

At least 95% of the battery set voltage is detected to turn off the output transistor of the output block (Drv-2) on the synchronous rectification side.

2. Protection Functions

(1) Under voltage lockout protection circuit block (VREF-UVLO)

The momentary decrease in internal reference voltage (VREF) may cause malfunctions in the control IC, resulting in breakdown or degradation of the system.

To prevent such malfunctions, under voltage lockout protection circuit detects internal reference voltage drop and fixes OUT-1 terminal (pin 28) and OUT-2 terminal (pin 26) to "L" level.

The system restores voltage supply when the internal reference voltage reaches the threshold voltage of the under voltage lockout protection circuit.

Protection circuit (VREF-UVLO)operation function table

At UVLO operating (VRFE voltage is lower than UVLO threshold voltage.)
The logic of following terminal is fixed.

OUTD	OUT-1	OUT-2	OUT-CP	CS	VB
Hi-Z	L	L	L	L	L

(2) Under voltage lockout protection circuit (VB-UVLO)

The transient state or a momentary decrease in supply voltage, which occurs when the bias voltage (VB) for output circuit is turned on, may cause malfunction in the control IC, resulting in breakdown or degradation of the system.

To prevent such malfunctions, under voltage lockout protection circuit detects a bias voltage drop, and fixes OUT-1 terminal (pin 28) and OUT-2 terminal (pin 26) to "L" level.

The system restores voltage supply when the power supply voltage or the internal reference voltage reaches the threshold voltage of the under voltage lockout protection circuit.

Protection circuit (VB-UVLO)operation function table

At UVLO operating (VB voltage is lower than UVLO threshold voltage.)
The logic of following terminals is fixed.

OUT-1	OUT-2	OUT-CP	CS
L	L	L	L

(3) Under input voltage detection comparator block (UVComp.)

Decrease of input voltage is detected and OUT-1 terminal (pin 28) and OUT-2 terminal (pin 26) are fixed to “L” level. In addition, an arbitrary detection voltage value can be set with an external resistor.
The system restores voltage supply when the input voltage reaches or exceeds the threshold voltage of the under input voltage detection comparator.

Protection circuit (UVComp.)operation function table

At under input voltage detection (Input voltage is lower than UVComp. threshold voltage.)
The logic of following terminals is fixed.

OUT-1	OUT-2	OUT-CP	CS
L	L	L	L

3. Soft-start function

Soft-start block (SOFT)

Connecting a capacitor to the CS terminal (pin 18) prevents rush currents from flowing upon activation of the power supply.

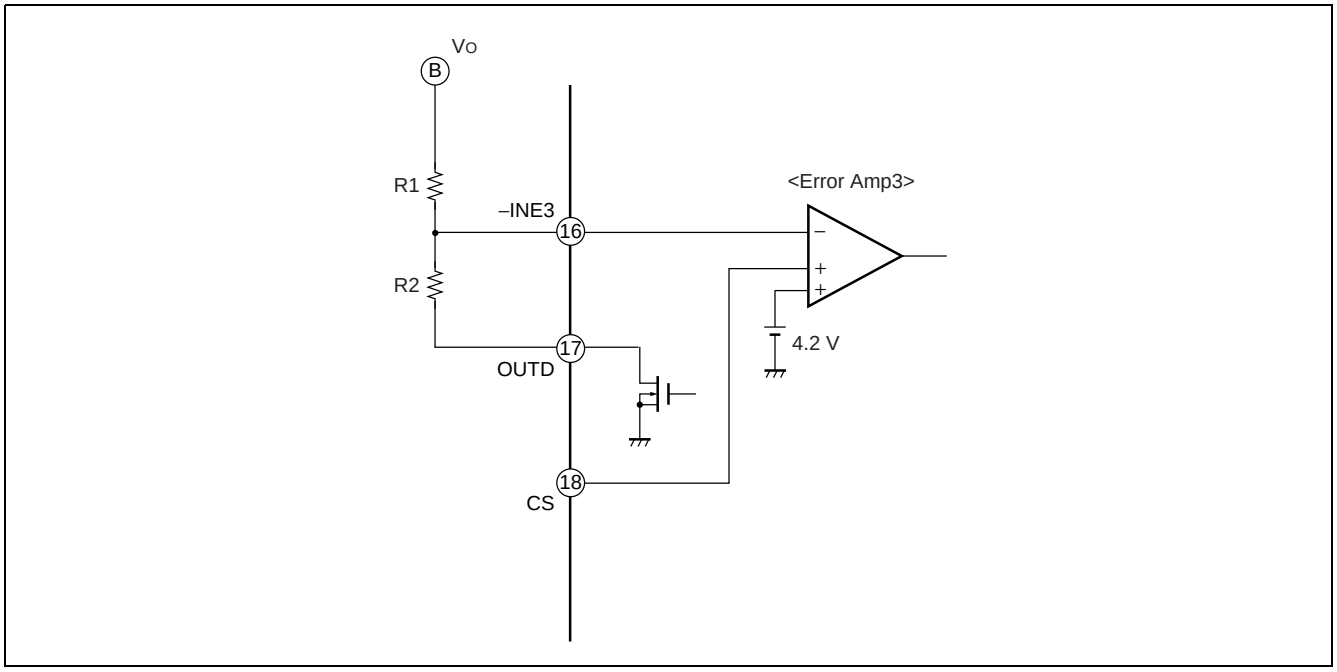
Using the error amplifier to detect a soft-start allows to soft-start at constant setting time intervals independent of the output load of the DC/DC converter.

■ SETTING THE CHARGING VOLTAGE

The charging voltage (DC/DC output voltage) can be set by connecting an external output voltage setting resistors (R1, R2) to the –INE3 terminal (pin 16) .
Select a resistance value at which the ON resistance (35 Ω at 1 mA) of the built-in FET connected to the OUTD terminal (pin 17) can be ignored.

Battery charging voltage : Vo

$$Vo\ (V) = \frac{R1 + R2}{R2} \times -INE3\ (V)$$



■ SETTING THE CHARGING CURRENT

The charge current value (output limit current) can be set depending on the voltage value at the +INE2 terminal (pin 13) .

If a current exceeding the setting value attempts to flow, the charging voltage drops according to the setting current value.

Battery charge current setting voltage : + INE2

$$+INE2\ (V) = 25 \times Ichg\ (A) \times Rs\ (\Omega)$$

■ SETTING THE TRIANGULAR WAVE OSCILLATION FREQUENCY

The triangular wave oscillation frequency can be set by the timing resistor (R_T) connected to the RT terminal (pin 19) .

Triangular oscillation frequency : f_{OSC}

$$f_{OSC}\ (kHz) \fallingdotseq \frac{23500}{R_T\ (k\Omega)}$$

■ SETTING THE SOFT-START TIME

(1) Setting constant voltage mode soft-start

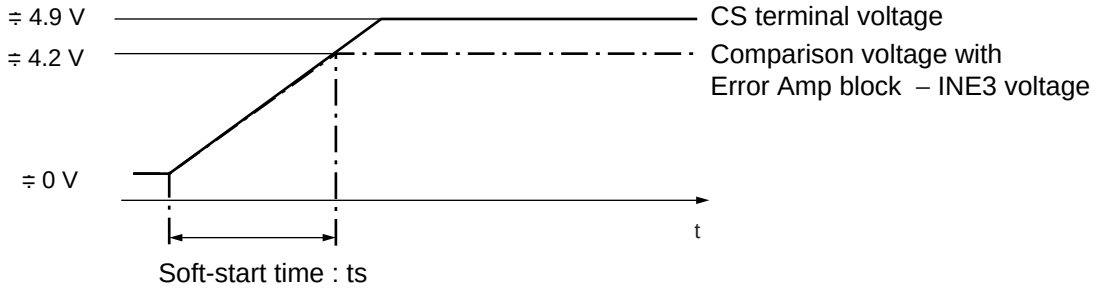
For preventing rush current upon activation of IC, the IC allows soft-start using the capacitor (C_S) connected to the CS terminal (pin 18) .
When the CTL-1 terminal (pin 22) is placed under “H” level and IC is activated (threshold voltage of VCC ≥ UVLO) , and Q2 is turned off and the external soft-start capacitor (C_S) connected to the CS terminal is charged at 10 μA.

The Error Amp3 output (FB23 terminal (pin 15)) is determined by comparison between the lower voltage of the two non-inverted input terminal voltages (4.2 V and − CS terminal voltage) , and the inverted input terminal voltage (at the –INE3 terminal (pin 16)) . FB23 during soft-start intervals (CS terminal voltage < 4.2 V) is therefore determined through comparison between the –INE3 terminal voltage and CS terminal voltage and the DC/DC converter output voltage is proportional to the CS terminal voltage rising as the external soft-start capacitor connected to the CS terminal is charged.

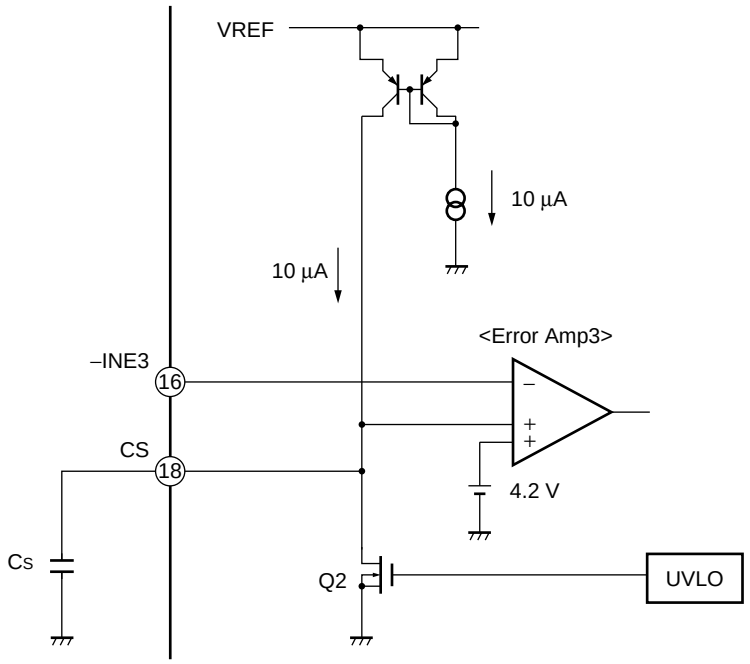
The soft-start time is obtained by the following formula.

Soft start time : ts (time to output voltage 100%)

$$ts\ (s) \fallingdotseq 0.42 \times Cs\ (\mu F)$$



• Soft-start circuit



(2) Setting constant current mode soft-start

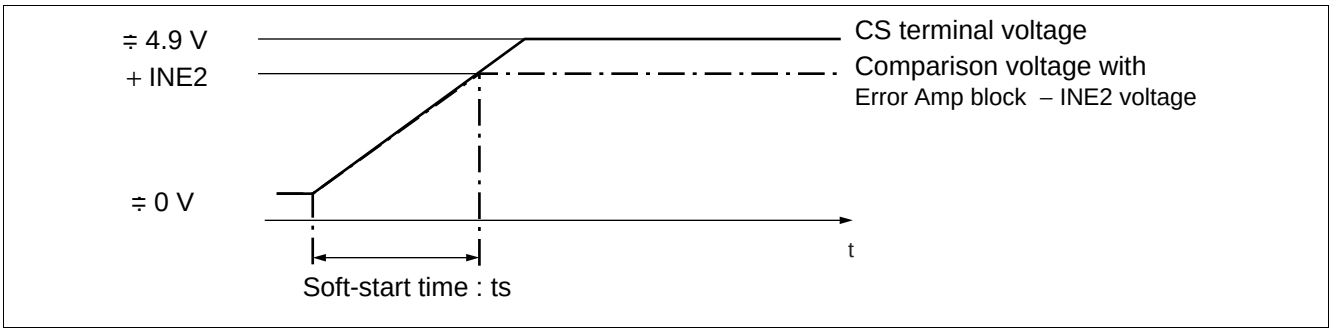
For preventing rush current upon activation of IC, the IC allows soft-start using the capacitor (C_S) connected to the CS terminal (pin 18) .
When the CTL-1 terminal (pin 22) is placed under “H” level and IC is activated (threshold voltage of VCC ≥ UVLO) , and Q2 is turned off and the external soft-start capacitor (C_S) connected to the CS terminal is charged at 10 μA.

The error Amp2 output (FB23 terminal (pin 15)) is determined by comparison between the lower voltage of the two non-inverted input terminal voltages (at the +INE2 terminal (pin 13) and CS terminal) , and the inverted input terminal voltage (at the –INE2 terminal (pin 14)) . FB23 during soft-start intervals (CS terminal voltage < +INE2) is therefore determined through comparison between the –INE2 terminal voltage and CS terminal voltage and the DC/DC converter output current is proportional to the CS terminal voltage rising as the external soft-start capacitor connected to the CS terminal is charged.

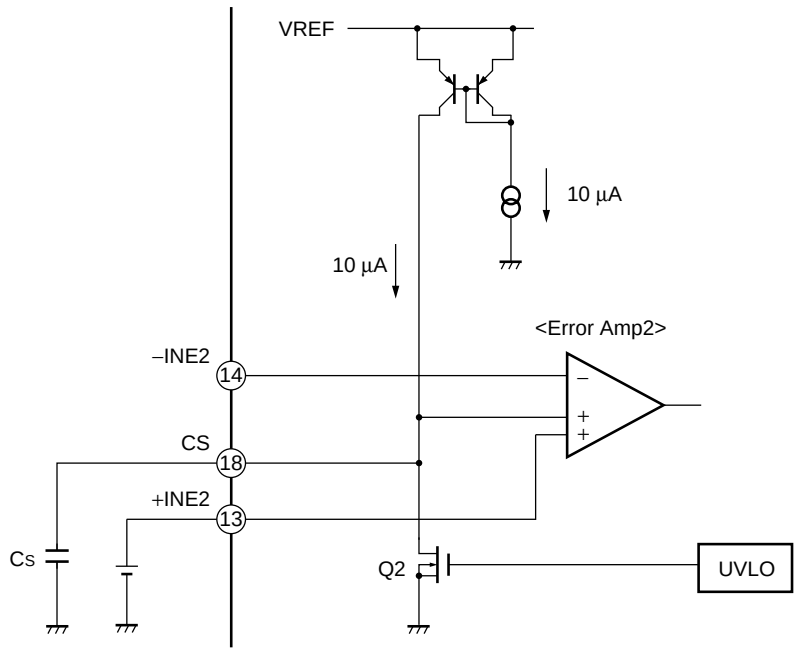
The soft-start time is obtained by the following formula.

Soft start time : ts (time to output voltage 100%)

$$ts\ (s) \fallingdotseq \frac{+\mathrm{INE2}}{10\ \mu A} \times Cs\ (\mu F)$$



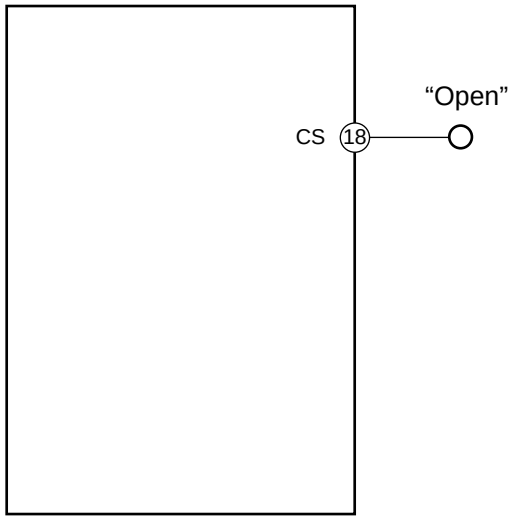
• Soft-start circuit



■ PROCESSING WITHOUT USING OF THE SOFT-START FUNCTION

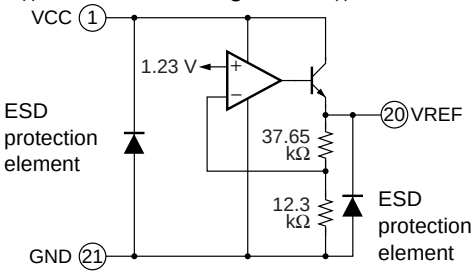
When soft-start function is not used, leave the CS terminal (pin 18) open.

- When no soft-start function is specified

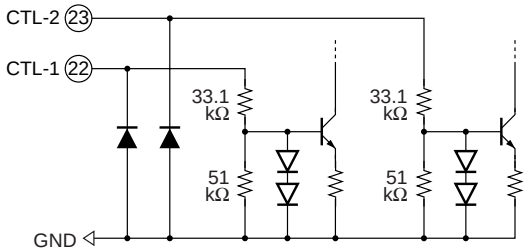


■ I/O EQUIVALENT CIRCUIT

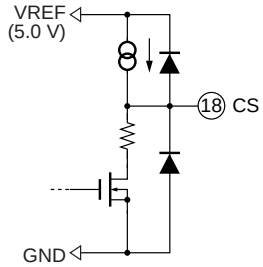
⟨⟨ Reference voltage block ⟩⟩



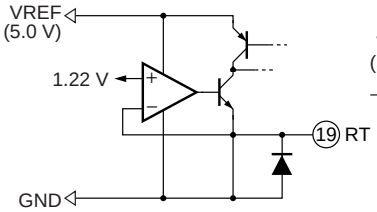
⟨⟨ Control block ⟩⟩



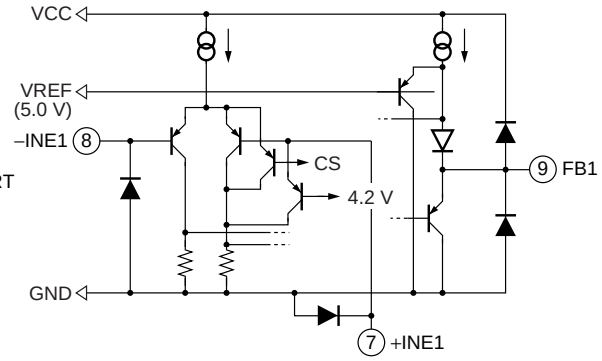
⟨⟨ Soft-start block ⟩⟩



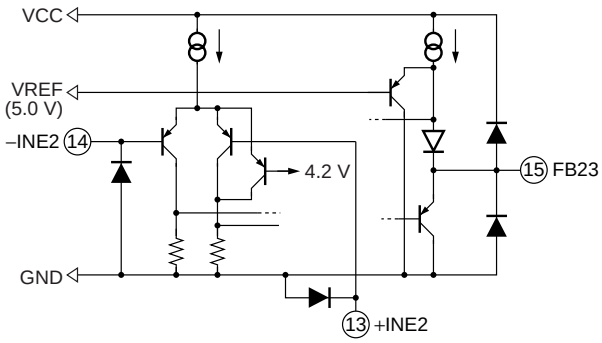
⟨⟨ Triangular wave oscillator block ⟩⟩



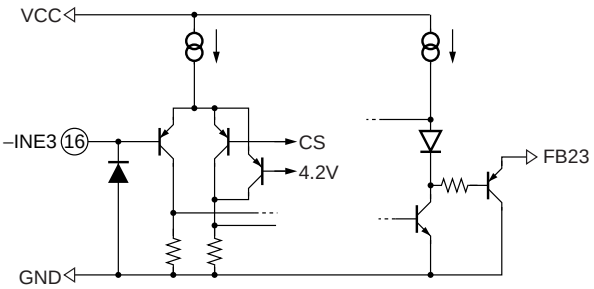
⟨⟨ Error amplifier block (Error Amp1) ⟩⟩



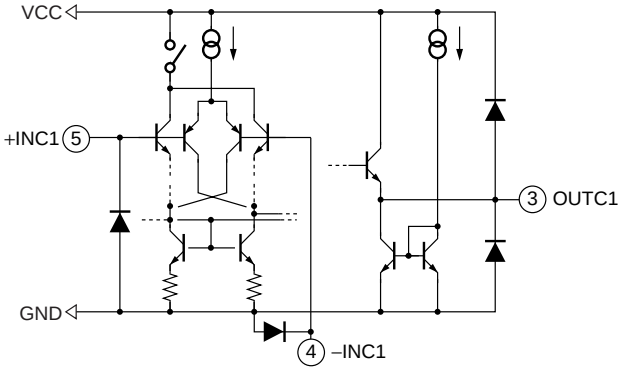
⟨⟨ Error amplifier block (Error Amp2) ⟩⟩



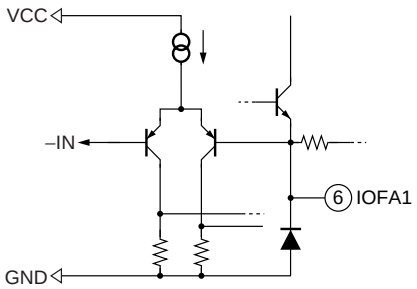
⟨⟨ Error amplifier block (Error Amp3) ⟩⟩



⟨⟨ Current detection amplfier block (Current Amp1) ⟩⟩



⟨⟨ Current detection amplfier block (Current Amp1 offset adjustment block) ⟩⟩



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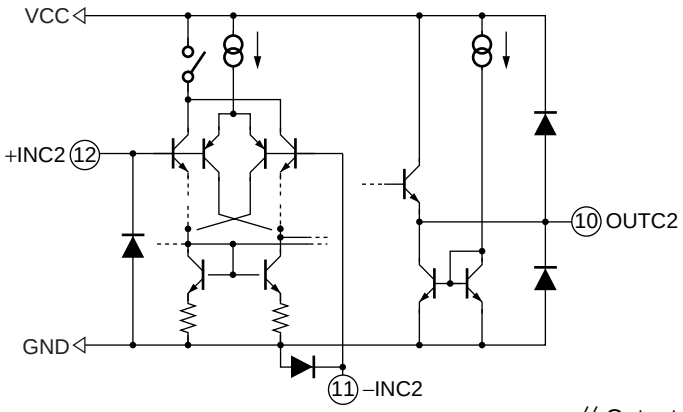
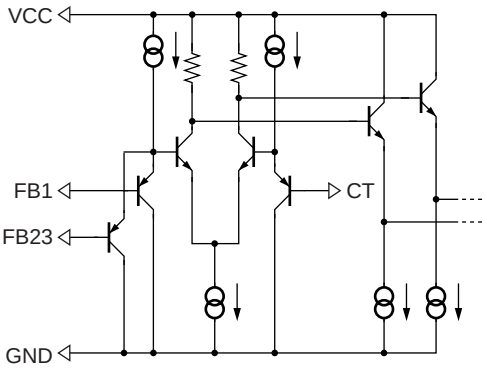
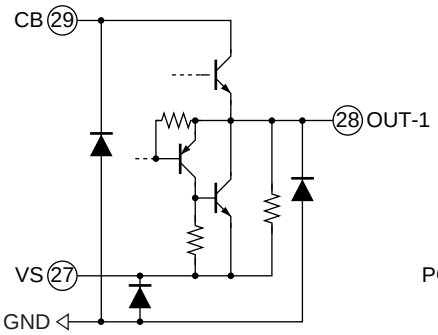
⟨⟨ Current detection amplfier block (Current Amp2) ⟩⟩



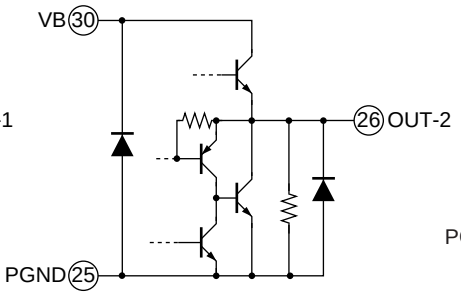
⟨⟨ PWM comparator block ⟩⟩



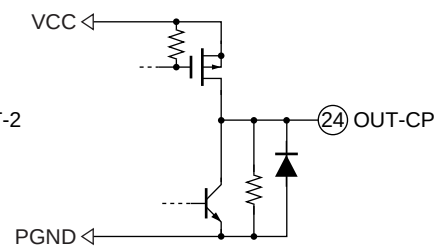
⟨⟨ Output block (Main side) ⟩⟩



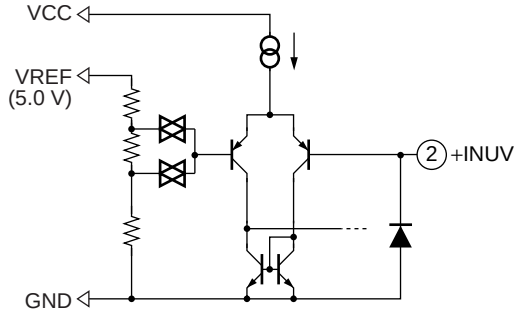
⟨⟨ Output block (synchronous rectification-side) ⟩⟩



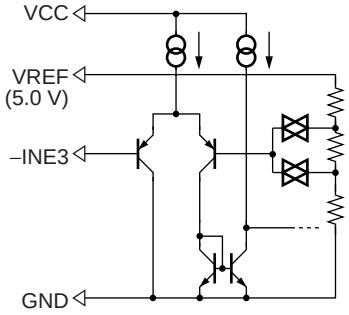
⟨⟨ Charge pump block ⟩⟩



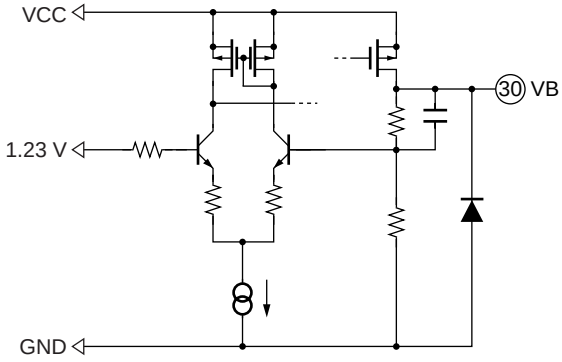
⟨⟨ Under input voltage detection comparator block ⟩⟩



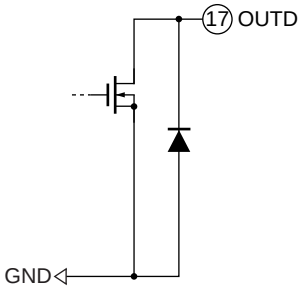
⟨⟨ Battery voltage detection comparator block ⟩⟩



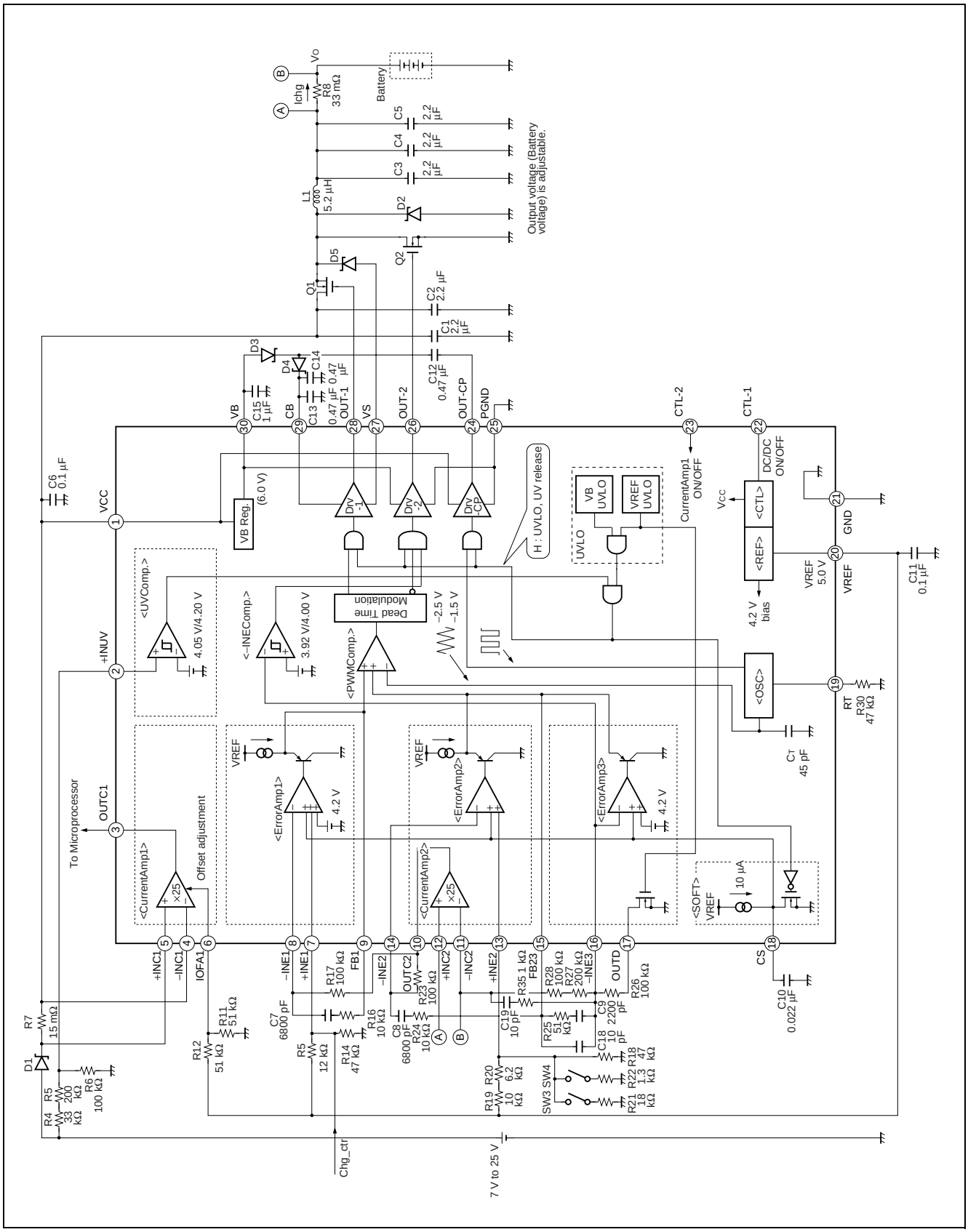
⟨⟨ Bias voltage block ⟩⟩



⟨⟨ Prevent inefficient current block ⟩⟩



■ APPLICATION EXAMPLE 1

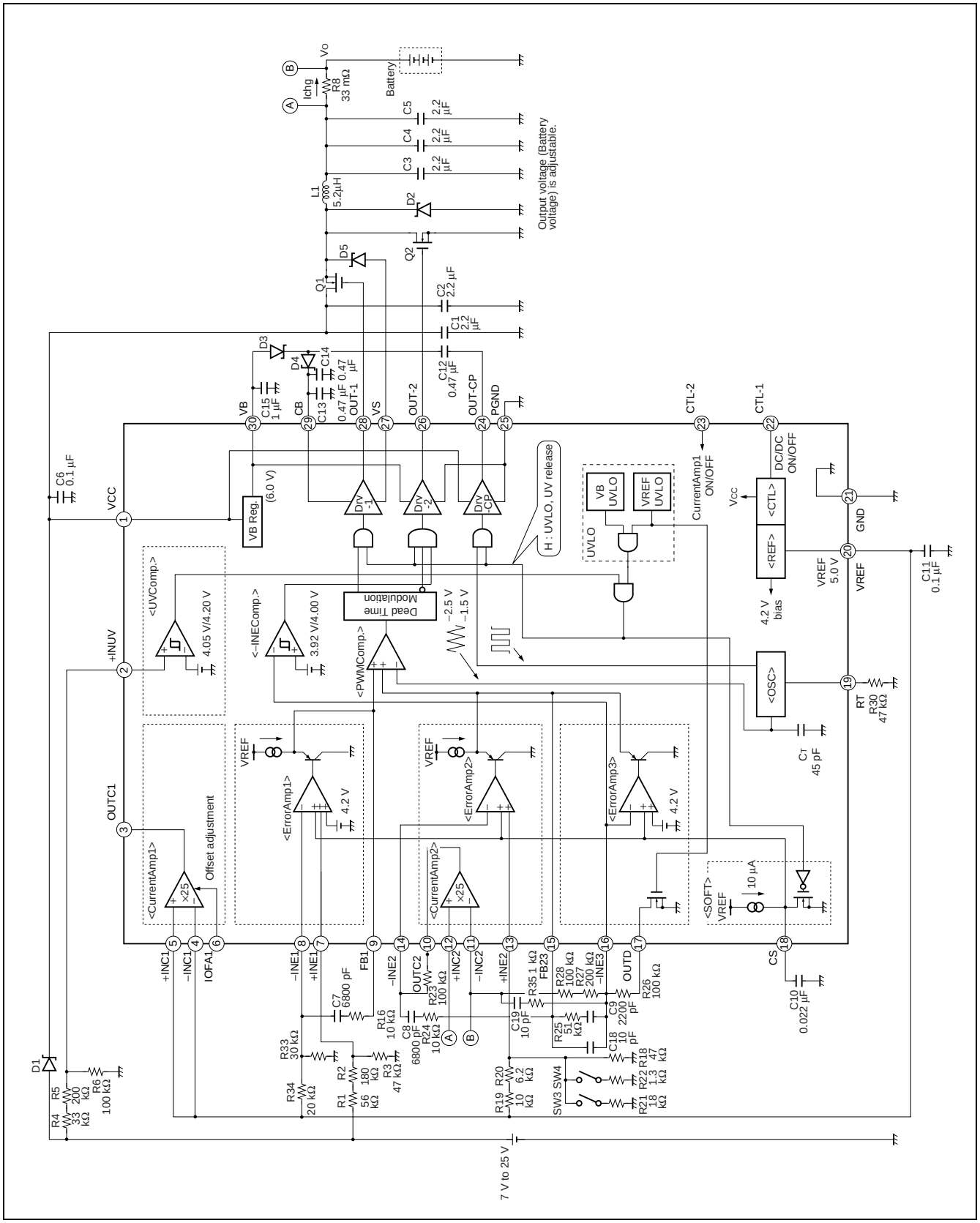


■ PARTS LIST 1

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1, Q2,	Nch FET	VDS = 30 V, ID = 8.0 A		NEC	μPA2752
D1 D2, D5 D3, D4	Diode Diode Diode	VF = 0.4 V (Max) , At IF = 2.5 A VF = 0.42 V (Max) , At IF = 3 A VF = 0.45 V (Max) , At IF = 100 mA		SHINDENGEN ROHM ORIGIN	DEP5PC3 RB053L-30 FQ4JP3
L1	Inductor	5.2 μH	5.5 A, 22 mΩ	SUMIDA	CDRH104R-5R2
C1, C2	Ceramics Condenser	2.2 μF	25 V	TDK	C3216JB1E225K
C3 to C5	Ceramics Condenser	2.2 μF	25 V	TDK	C3225JB1H225K
C6, C11	Ceramics Condenser	0.1 μF	50 V	TDK	C1608JB1H104K
C7, C8	Ceramics Condenser	6800 pF	50 V	TDK	C1608JB1H682K
C9	Ceramics Condenser	2200 pF	50 V	TDK	C1608JB1H222K
C10	Ceramics Condenser	0.022 μF	50 V	TDK	C1608JB1H223K
C12	Ceramics Condenser	0.47 μF	25 V	TDK	C3216JB1E474K
C13, C14	Ceramics Condenser	0.47 μF	50 V	TDK	C3216JB1H474K
C15	Ceramics Condenser	1 μF	25 V	TDK	C3216JB1E105K
C18, C19	Ceramics Condenser	10 pF	50 V	TDK	C1608JB1H100K
R4	Resistor	33 kΩ	0.5%	ssm	RR0816P-333-D
R5	Resistor	200 kΩ	0.5%	ssm	RR0816P-204-D
R6	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R7	Resistor	15 mΩ	1%	KOA	SL1TTE15LOF
R8	Resistor	33 mΩ	1%	KOA	SL1TTE33LOF
R11, R12	Resistor	51 kΩ	0.5%	ssm	RR0816P-513-D
R14	Resistor	47 kΩ	0.5%	ssm	RR0816P-473-D
R15	Resistor	12 kΩ	0.5%	ssm	RR0816P-123-D
R16, R24	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R17, R23, R26	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R18, R30	Resistor	47 kΩ	0.5%	ssm	RR0816P-473-D
R19	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R20	Resistor	6.2 kΩ	0.5%	ssm	RR0816P-622-D
R21	Resistor	18 kΩ	0.5%	ssm	RR0816P-183-D
R22	Resistor	1.3 kΩ	0.5%	ssm	RR0816P-132-D
R25	Resistor	51 kΩ	0.5%	ssm	RR0816P-513-D
R27	Resistor	200 kΩ	0.5%	ssm	RR0816P-204-D
R28	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R35	Resistor	1 kΩ	0.5%	ssm	RR0816P-102-D

Note : NEC : NEC corporation
SHINDENGEN : Shindengen Electric Manufacturing. Co., Ltd.
ROHM : ROHM CO., LTD
ORIGIN : Origin Electric Co., Ltd.
SUMIDA : SUMIDA Corporation
TDK : TDK Corporation
ssm : SUSUMU CO., LTD
KOA : KOA Corporation

■ APPLICATION EXAMPLE 2



■ PARTS LIST 2

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1, Q2	Nch FET	VDS = 30 V, ID = 8.0 A		NEC	μPA2752
D1 D2, D5 D3, D4	Diode Diode Diode	VF = 0.4 V (Max) , At IF = 2.5 A VF = 0.42 V (Max) , At IF = 3 A VF = 0.45 V (Max) , At IF = 100 mA		SHINDENGEN ROHM ORIGIN	DEP5PC3 RB053L-30 FQ4JP3
L1	Inductor	5.2 μH	5.5 A, 22 mΩ	SUMIDA	CDRH104R-5R2
C1, C2	Ceramics Condenser	2.2 μF	25 V	TDK	C3216JB1E225K
C3 to C5	Ceramics Condenser	2.2 μF	25 V	TDK	C3225JB1H225K
C6, C11	Ceramics Condenser	0.1 μF	50 V	TDK	C1608JB1H104K
C7, C8	Ceramics Condenser	6800 pF	50 V	TDK	C1608JB1H682K
C9	Ceramics Condenser	2200 pF	50 V	TDK	C1608JB1H222K
C10	Ceramics Condenser	0.022 μF	50 V	TDK	C1608JB1H223K
C12	Ceramics Condenser	0.47 μF	25 V	TDK	C3216JB1E474K
C13, C14	Ceramics Condenser	0.47 μF	50 V	TDK	C3216JB1H474K
C15	Ceramics Condenser	1 μF	25 V	TDK	C3216JB1E105K
C18, C19	Ceramics Condenser	10 pF	50 V	TDK	C1608JB1H100K
R1	Resistor	56 kΩ	0.5%	ssm	RR0816P-563-D
R2	Resistor	180 kΩ	0.5%	ssm	RR0816P-184-D
R3	Resistor	47 kΩ	0.5%	ssm	RR0816P-473-D
R4	Resistor	33 kΩ	0.5%	ssm	RR0816P-333-D
R5	Resistor	200 kΩ	0.5%	ssm	RR0816P-204-D
R6	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R8	Resistor	33 mΩ	1%	KOA	SL1TTE33LOF
R16, R24	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R18, R30	Resistor	47 kΩ	0.5%	ssm	RR0816P-473-D
R19	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R20	Resistor	6.2 kΩ	0.5%	ssm	RR0816P-622-D
R21	Resistor	18 kΩ	0.5%	ssm	RR0816P-183-D
R22	Resistor	1.3 kΩ	0.5%	ssm	RR0816P-132-D
R23, R26	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R25	Resistor	51 kΩ	0.5%	ssm	RR0816P-513-D
R27	Resistor	200 kΩ	0.5%	ssm	RR0816P-204-D
R28	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R33	Resistor	30 kΩ	0.5%	ssm	RR0816P-303-D
R34	Resistor	20 kΩ	0.5%	ssm	RR0816P-203-D
R35	Resistor	1 kΩ	0.5%	ssm	RR0816P-102-D

Note : NEC : NEC corporation
SHINDENGEN : Shindengen Electric Manufacturing. Co., Ltd.
ROHM : ROHM CO., LTD
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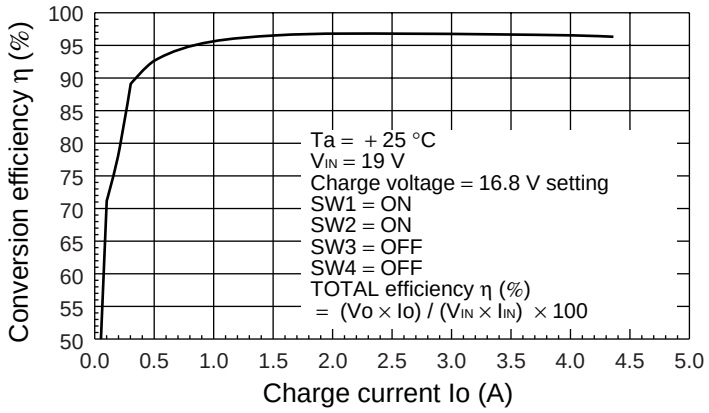
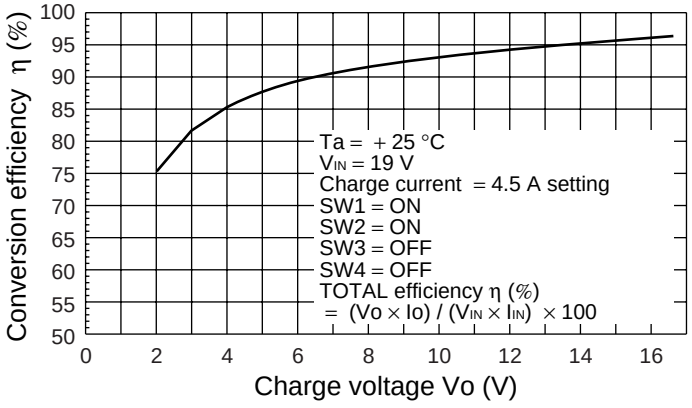
■ REFERENCE DATA

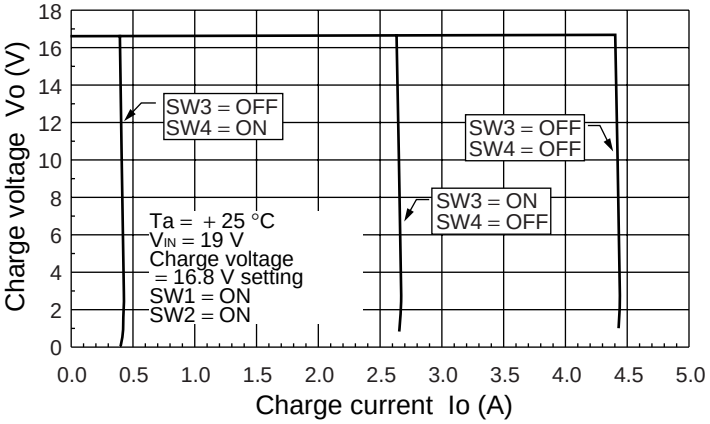
Conversion Efficiency vs. Charge Current (constant voltage mode)



Conversion Efficiency vs. Charge Voltage (constant current mode)



Charge Voltage vs. Charge Current (16.8 V setting)



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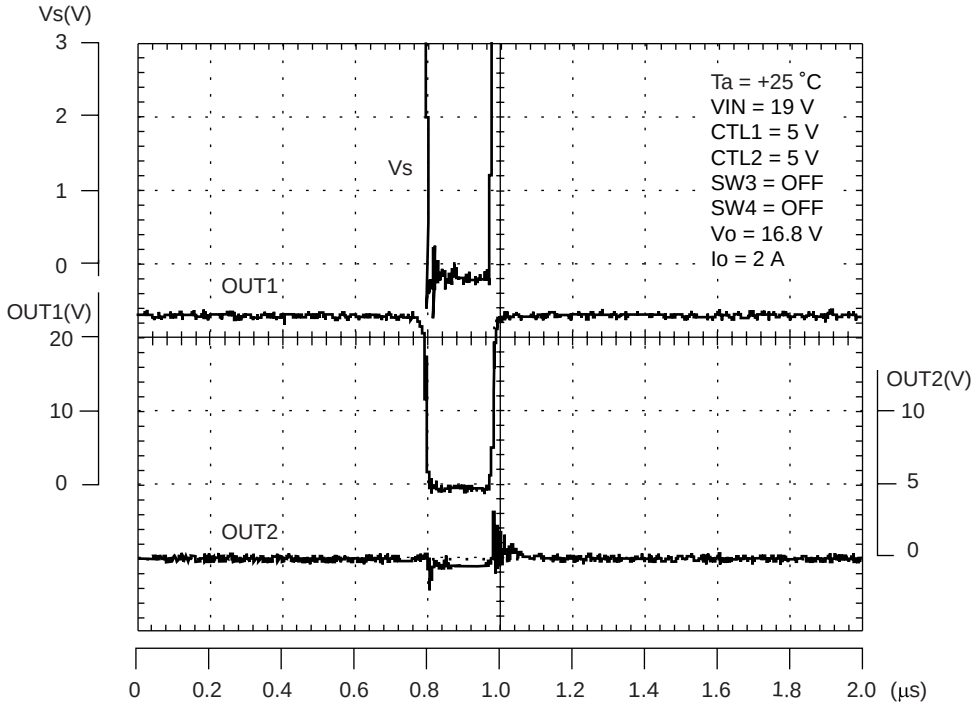
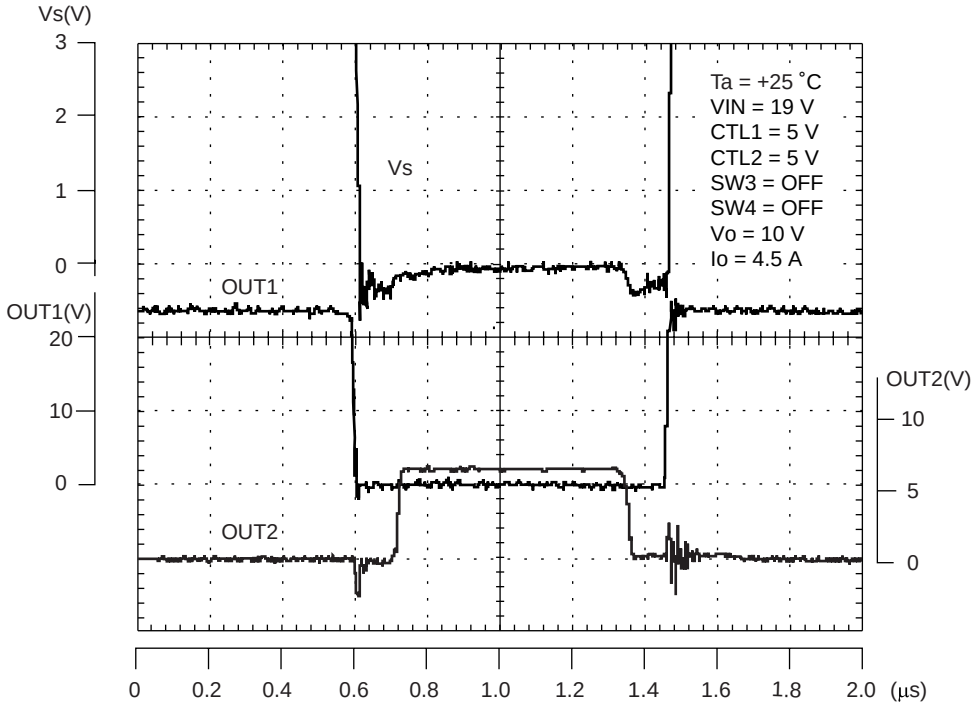
• Switching Waveform (constant voltage mode)

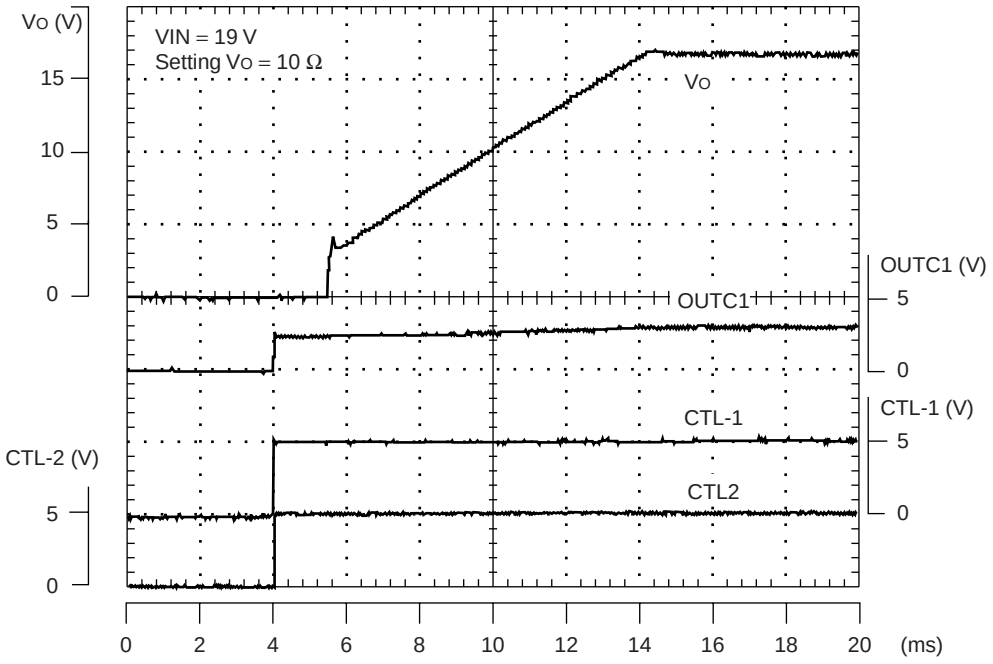


• Switching Waveform (constant current mode)

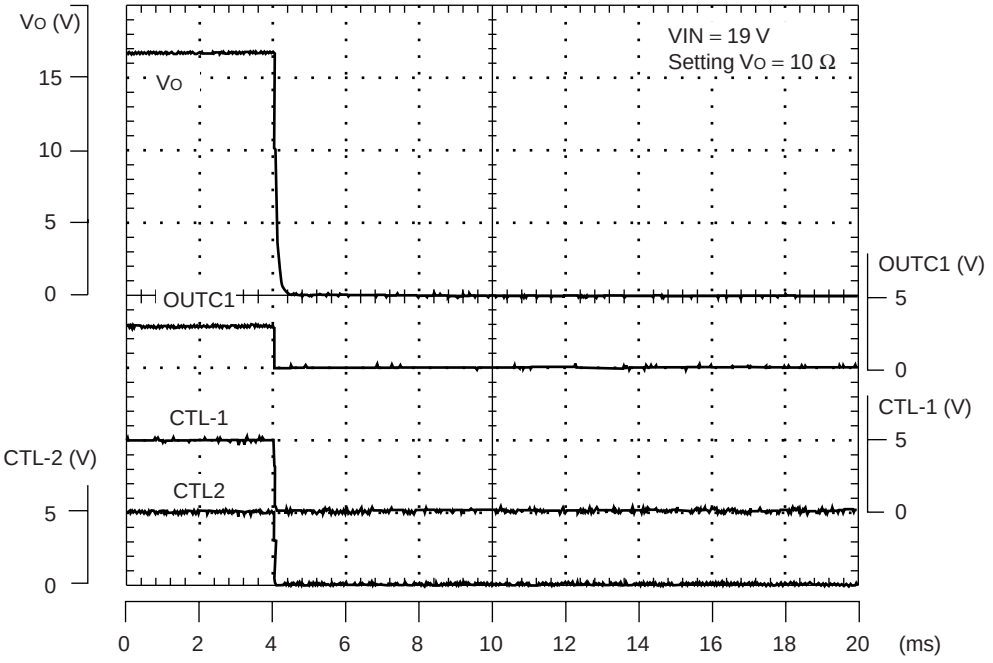


• CTL function

• CTL1, CTL2 = L→H constant voltage mode



• CTL1, CTL2 = H→L constant voltage mode



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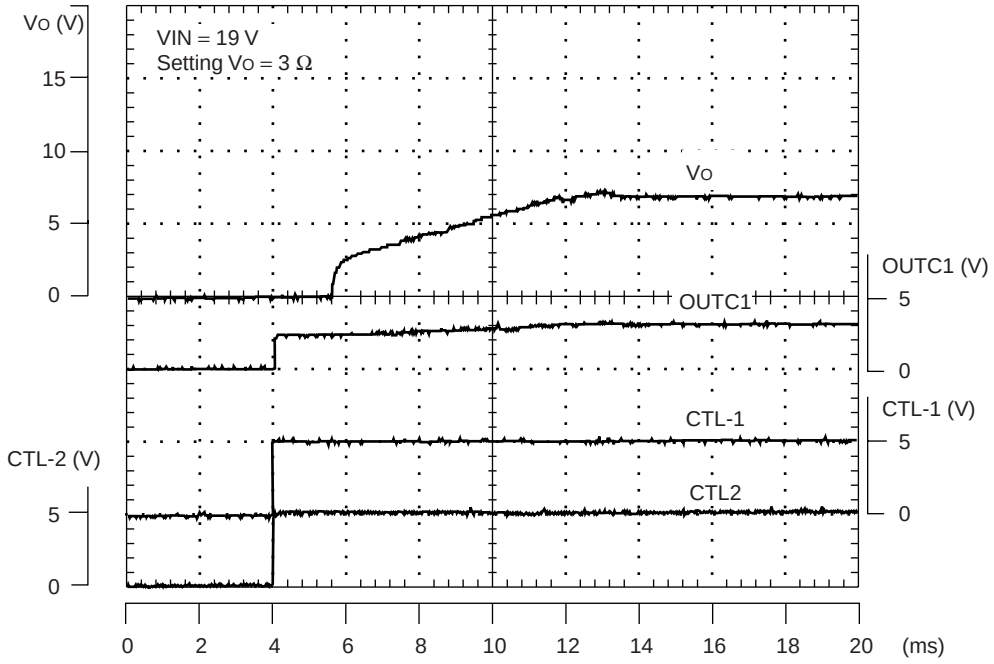
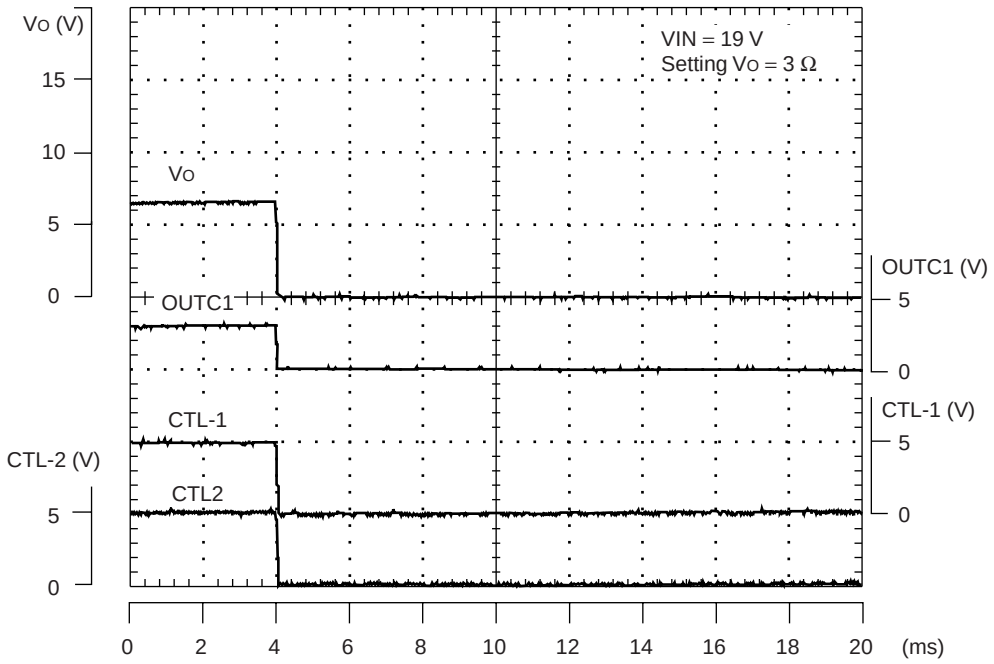
• CTL1, CTL2 = L→H constant current mode



• CTL1, CTL2 = H→L constant current mode



■ SELECTION OF COMPONENTS

• Nch MOS FET

The Nch MOS FET for switching use should be rated for at least + 20% more than the maximum input voltage. To minimize continuity loss, use a FET with low $R_{DS\ (ON)}$ between the drain and source. For high input voltage and high frequency operation, on/off-cycle switching loss will be higher so that power dissipation must be considered. In this application, the μPA2752 (NEC products) is used. Continuity loss, on/off switching loss and total loss are determined by the following formulas. The selection must ensure that peak drain current does not exceed rated values.

Continuity loss : Pc

$$P_C = I_D^2 \times R_{DS\ (ON)} \times \text{Duty}$$

On-cycle switching loss : $P_{S\ (ON)}$

$$P_{S\ (ON)} = \frac{V_{D\ (Max)} \times I_D \times tf \times f_{OSC}}{6}$$

Off-cycle switching loss : $P_{S\ (OFF)}$

$$P_{S\ (OFF)} = \frac{V_{D\ (Max)} \times I_{D\ (Max)} \times tf \times f_{OSC}}{6}$$

Total loss : P_T

$$P_T = P_C + P_{S\ (ON)} + P_{S\ (OFF)}$$

Example) Using the μPA2752
Setting 16.8V
Main side

Input voltage $V_{IN\ (Max)}$ = 25 V, output voltage V_O = 16.8 V, drain current I_D = 4.5 A, oscillation frequency f_{OSC} = 500 kHz, L = 5.2 μH, drain-source on resistance $R_{DS\ (ON)}$ ≒ 20 mΩ, tr = 6.2 ns, tf = 5.8 ns

Drain current (Max) : $I_{D\ (Max)}$

$$I_{D\ (Max)} = Io + \frac{V_{IN\ (Max)} - Vo}{2L} \text{ ton}$$

$$= 4.5 + \frac{25 - 16.8}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.672$$

$$\fallingdotseq \underline{5.56\ A}$$

Drain current (Min) : $I_{D\ (Min)}$

$$I_{D\ (Min)} = Io - \frac{V_{IN\ (Max)} - Vo}{2L} \text{ ton}$$

$$= 4.5 - \frac{25 - 16.8}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.672$$

$$\fallingdotseq \underline{3.44\ A}$$

$$P_C = I_D^2 \times R_{DS\,(ON)} \times Duty$$
$$= 4.5^2 \times 0.02 \times 0.672$$
$$\fallingdotseq \underline{0.272\ W}$$

$$P_{S\,(ON)} = \frac{V_{D\,(Max)} \times I_D \times tr \times f_{OSC}}{6}$$
$$= \frac{25 \times 4.5 \times 6.2 \times 10^{-9} \times 500 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.058\ W}$$

$$P_{S\,(OFF)} = \frac{V_{D\,(Max)} \times I_{D\,(Max)} \times tf \times f_{OSC}}{6}$$
$$= \frac{25 \times 5.56 \times 5.8 \times 10^{-9} \times 500 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.067\ W}$$

$$P_T = P_C + P_{S\,(ON)} + P_{S\,(OFF)}$$
$$\fallingdotseq 0.272 + 0.058 + 0.067$$
$$\fallingdotseq \underline{0.397\ W}$$

The above power dissipation figures for the µPA2752 are satisfied with ample margin at 2 W (Ta = + 25 °C).

Synchronous rectification side

Input voltage $V_{IN\,(Max)}$ = 25 V, output voltage Vo = 16.8 V, drain current I_D = 4.5 A, oscillation frequency f_{OSC} = 500 kHz, L = 5.2 µH, drain-source on resistance $R_{DS\,(ON)} \fallingdotseq$ 20 mΩ, tr = 6.2 ns, tf = 5.8 ns

Drain current (Max) : $I_{D\,(Max)}$

$$I_{D\,(Max)} = Io + \frac{Vo}{2L}\,toff$$
$$= 4.5 + \frac{16.8}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times (1 - 0.672)$$
$$\fallingdotseq \underline{5.56\ A}$$

Drain current (Min) : $I_{D\,(Min)}$

$$I_{D\,(Min)} = Io - \frac{Vo}{2L}\,toff$$
$$= 4.5 - \frac{16.8}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times (1 - 0.672)$$
$$\fallingdotseq \underline{3.44\ A}$$

$$P_C = I_D^2 \times R_{DS\,(ON)} \times Duty_{(OFF)}$$
$$= 4.5^2 \times 0.02 \times (1 - 0.672)$$
$$\fallingdotseq \underline{0.133\ W}$$

$$P_{S\,(ON)} = \frac{V_F \times I_D \times tr \times f_{OSC}}{6}$$
$$= \frac{0.45 \times 4.5 \times 6.2 \times 10^{-9} \times 500 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.001\ W}$$

$$P_{S\,(OFF)} = \frac{V_F \times I_{D\,(Max)} \times tf \times f_{OSC}}{6}$$
$$= \frac{0.45 \times 5.56 \times 5.8 \times 10^{-9} \times 500 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.001\ W}$$

$$P_T = P_C + P_{S\,(ON)} + P_{S\,(OFF)}$$
$$\fallingdotseq 0.133 + 0.001 + 0.001$$
$$\fallingdotseq \underline{0.135\ W}$$

The above power dissipation figures for the μPA2752 are satisfied with ample margin at 2 W (Ta = + 25 °C).

Setting 12.6V
Main side

Input voltage $V_{IN\,(Max)}$ = 20 V, output voltage Vo = 12.6 V, drain current I_D = 4.5 A, oscillation frequency f_{OSC} = 500 kHz, L = 5.2 μH, drain-source on resistance $R_{DS\,(ON)} \fallingdotseq$ 20 mΩ, tr = 6.2 ns, tf = 5.8 ns

Drain current (Max) : $I_{D\,(Max)}$

$$I_{D\,(Max)} = Io + \frac{V_{IN\,(Max)} - Vo}{2L} ton$$
$$= 4.5 + \frac{20 - 12.6}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.63$$
$$\fallingdotseq \underline{5.40\ A}$$

Drain current (Min) : $I_{D\,(Min)}$

$$I_{D\,(Min)} = Io - \frac{V_{IN\,(Max)} - Vo}{2L} ton$$
$$= 4.5 - \frac{20 - 12.6}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.63$$
$$\fallingdotseq \underline{3.60\ A}$$

$$P_C = I_D^2 \times R_{DS\,(ON)} \times \text{Duty}$$
$$= 4.5^2 \times 0.02 \times 0.63$$
$$\fallingdotseq \underline{0.255\ \text{W}}$$

$$P_{S\,(ON)} = \frac{V_{D\,(Max)} \times I_D \times tr \times f_{OSC}}{6}$$
$$= \frac{20 \times 4.5 \times 6.2 \times 10^{-9} \times 500 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.047\ \text{W}}$$

$$P_{S\,(OFF)} = \frac{V_{D\,(Max)} \times I_{D\,(Max)} \times tf \times f_{OSC}}{6}$$
$$= \frac{20 \times 5.40 \times 5.8 \times 10^{-9} \times 500 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.052\ \text{W}}$$

$$P_T = P_C + P_{S\,(ON)} + P_{S\,(OFF)}$$
$$\fallingdotseq 0.255 + 0.047 + 0.052$$
$$\fallingdotseq \underline{0.354\ \text{W}}$$

The above power dissipation figures for the µPA2752 are satisfied with ample margin at 2 W (Ta = + 25 °C).

Synchronous rectification side

Input voltage $V_{IN\,(Max)}$ = 20 V, output voltage Vo = 12.6 V, drain current I_D = 4.5 A, oscillation frequency f_{OSC} = 500 kHz, L = 5.2 µH, drain-source on resistance $R_{DS\,(ON)} \fallingdotseq$ 20 mΩ, tr = 6.2 ns, tf = 5.8 ns

Drain current (Max) : $I_{D\,(Max)}$

$$I_{D\,(Max)} = Io + \frac{Vo}{2L}\,toff$$
$$= 4.5 + \frac{12.6}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times (1 - 0.63)$$
$$\fallingdotseq \underline{5.40\ \text{A}}$$

Drain current (Min) : $I_{D\,(Min)}$

$$I_{D\,(Min)} = Io - \frac{Vo}{2L}\,toff$$
$$= 4.5 - \frac{12.6}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times (1 - 0.63)$$
$$\fallingdotseq \underline{3.60\ \text{A}}$$

$$P_C = I_D^2 \times R_{DS\,(ON)} \times Duty_{(OFF)}$$
$$= 4.5^2 \times 0.02 \times (1 - 0.63)$$
$$\fallingdotseq \underline{0.150\ W}$$

$$P_{S\,(ON)} = \frac{V_F \times I_D \times tr \times f_{OSC}}{6}$$
$$= \frac{0.45 \times 4.5 \times 6.2 \times 10^{-9} \times 500 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.001\ W}$$

$$P_{S\,(OFF)} = \frac{V_F \times I_{D\,(Max)} \times tf \times f_{OSC}}{6}$$
$$= \frac{0.45 \times 5.40 \times 5.8 \times 10^{-9} \times 500 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.001\ W}$$

$$P_T = P_C + P_{S\,(ON)} + P_{S\,(OFF)}$$
$$\fallingdotseq 0.15 + 0.001 + 0.001$$
$$\fallingdotseq \underline{0.152\ W}$$

The above power dissipation figures for the μPA2752 are satisfied with ample margin at 2 W (Ta = + 25 °C).

- Inductor

In selecting inductors, it is of course essential not to apply more current than the rated capacity of the inductor, but also to note that the lower limit for ripple current is a critical point that if reached will cause discontinuous operation and a considerable drop in efficiency. This can be prevented by choosing a higher inductance value, which will enable continuous operation under light loads. Note that if the inductance value is too high, however, direct current resistance (DCR) is increased and this will also reduce efficiency. The inductance must be set at the point where efficiency is greatest.

Note also that the DC superimposition characteristic become worse as the load current value approaches the rated current value of the inductor, so that the inductance value is reduced and ripple current increases, causing loss of efficiency.

The selection of rated current value and inductance value will vary depending on where the point of peak efficiency lies with respect to load current.

Inductance values are determined by the following formulas.

The L value for all load current conditions is set so that the peak to peak value of the ripple current is 1/2 the load current or less.

Inductance value : L

$$L \geq \frac{2\,(V_{IN} - V_O)}{I_O}\ ton$$

16.8 V output
Example :

$$L \geq \frac{2\,(V_{IN\,(Max)} - V_O)}{I_O}\,ton$$

$$\geq \frac{2 \times (25 - 16.8)}{4.5} \times \frac{1}{500 \times 10^3} \times 0.672$$

$$\geq \underline{4.9\ \mu H}$$

12.6 V output
Example :

$$L \geq \frac{2\,(V_{IN\,(Max)} - V_O)}{Io}\,ton$$

$$\geq \frac{2 \times (20 - 12.6)}{4.5} \times \frac{1}{500 \times 10^3} \times 0.63$$

$$\geq \underline{4.1\ \mu H}$$

Inductance values derived from the above formulas are values that provide sufficient margin for continuous operation at maximum load current, but at which continuous operation is not possible at light loads. It is therefore necessary to determine the load level at which continuous operation becomes possible. In this application, the SUMIDA CDRH104R-5R2 is used. The following formula is available to obtain the load current as a continuous current condition when 5.2 µH is used.

Load current value under continuous operating conditions : Io

$$I_O \geq \frac{V_O}{2L}\,toff$$

Example : Using the CDRH104R-5R2

5.2 µH (tolerance ± 20%), rated current = 5.5 A

16.8 V output

$$I_O \geq \frac{V_O}{2L}\,toff$$

$$\geq \frac{16.8}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times (1 - 0.672)$$

$$\geq \underline{1.06\ A}$$

12.6 V output

$$I_O \geq \frac{V_O}{2L} \text{ toff}$$

$$\geq \frac{12.6}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times (1 - 0.63)$$

$$\geq \underline{0.897A}$$

To determine whether the current through the inductor is within rated values, it is necessary to determine the peak value of the ripple current as well as the peak-to-peak values of the ripple current that affect the output ripple voltage.

The peak value and peak-to-peak value of the ripple current can be determined by the following formulas.

Peak Value : I_L

$$I_L \geq Io + \frac{V_{IN} - V_O}{2L} \text{ ton}$$

Peak-Peak Value : ΔI_L

$$\Delta I_L = \frac{V_{IN} - V_O}{L} \text{ ton}$$

Example : Using the CDRH104R-5R2

5.2 µH (tolerance ± 20%), rated current = 5.5 A

Peak Value

16.8 V output

$$I_L \geq Io + \frac{V_{IN\,(Max)} - V_O}{2L} \text{ ton}$$

$$\geq 4.5 + \frac{25 - 16.8}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.672$$

$$\geq \underline{5.56 \text{ A}}$$

12.6 V output

$$I_L \geq I_O + \frac{V_{IN\,(Max)} - V_O}{2L} \text{ ton}$$

$$\geq 4.5 + \frac{20 - 12.6}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.63$$

$$\geq \underline{5.40 \text{ A}}$$

Peak-Peak Value

16.8 V output

$$\Delta I_L = \frac{V_{IN\,(Max)} - Vo}{L} \text{ ton}$$

$$= \frac{25 - 16.8}{5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.672$$

$$\fallingdotseq \underline{2.12\ A}$$

12.6 V output

$$\Delta I_L = \frac{V_{IN\,(Max)} - Vo}{L} \text{ ton}$$

$$= \frac{20 - 12.6}{5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.63$$

$$\fallingdotseq \underline{1.79\ A}$$

- Diode for charge pump

  Using a low-leak diode increases efficiency a little; but using a signal diode is satisfactory. It is recommended to use a low-VF one. Also, use a capacitor for the charge pump, which is sufficiently larger value than the gate capacitor for the main-side FET. It is recommended to use a component between 0.1 μF to 1.0 μF.

■ NOTES ON USE

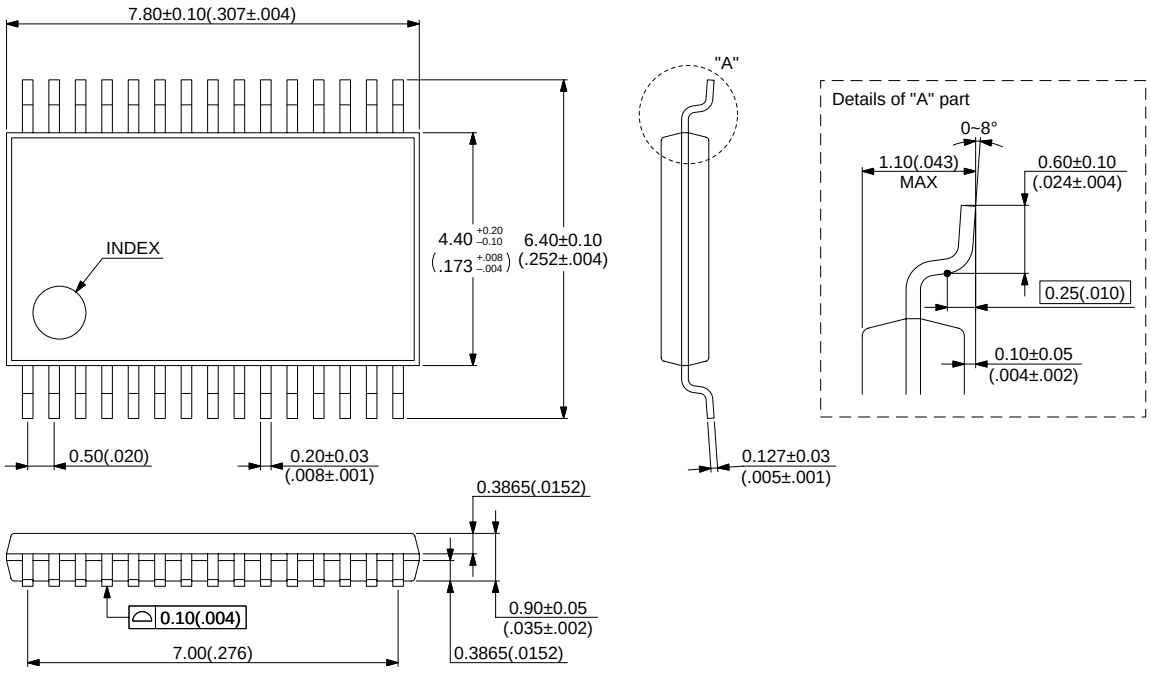
- Take account of common impedance when designing the earth line on a printed wiring board.
- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools, and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.
- Do not apply a negative voltage.
  - Applying a negative voltage of −0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB39A107PFT	30-pin plastic TSSOP (FPT-30P-M04)	

■ PACKAGE DIMENSION

30-pin plastic TSSOP
(FPT-30P-M04)



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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