ViVA2+ HD3D Sound **BBE**   **BBE** DIGITAL   **BBE** Mach3Bass   **eala**

Digital Signal Processor for TV

■**Package**

■ General Description

The NJU26102 is a digital signal processor that provides Delay, eala, ViVA2+, PEQ, and AGC.

The NJU26102 is suitable for audio products such as TV, CD radio- cassette, speakers system, and others.

■ FEATURES

NJU26102FR1

- Software

- 3D sound : eala (NJRC Original Surround),
            BBE ViVA, BBE ViVA+
- Sound Enhancement: : BBE, BBE Mach3Bass
- AGC
- 5Band PEQ
- Tone Control
- Audio Delay (fs=48kHz : Max. 25ms, fs=44.1kHz : Max. 27ms, fs=32kHz : Max. 37ms)
- Master Volume
- WatchDog Clock Output

- Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency   : 38MHz Max.
- Digital Audio Interface   : 3 Input ports / 3 Output ports
- Digital Audio Format   : I^2S 24bit, Left- justified, Right-justified,   BCK : 32/64fs
- Master / Slave Mode   : Master Mode MCK   1/2 fclk, 1/3 fclk
                                        ex. MCK = 384Fs(1/2)   or   MCK = 256Fs(1/3)   at fclk=768Fs
- Power Supply   : 2.5V
- Input terminal   : 3.3V Input tolerant
- Package   : QFP32-R1 (Pb-Free)
- Two kinds of micro computer interface : I^2C bus (standard-mode/100kbps)
                                        : Serial interface (4 lines: clock, enable, input data, output data)

The detail hardware specification is described in the " NJU26100 Series Hardware Data Sheet".

New Japan Radio Co., Ltd.
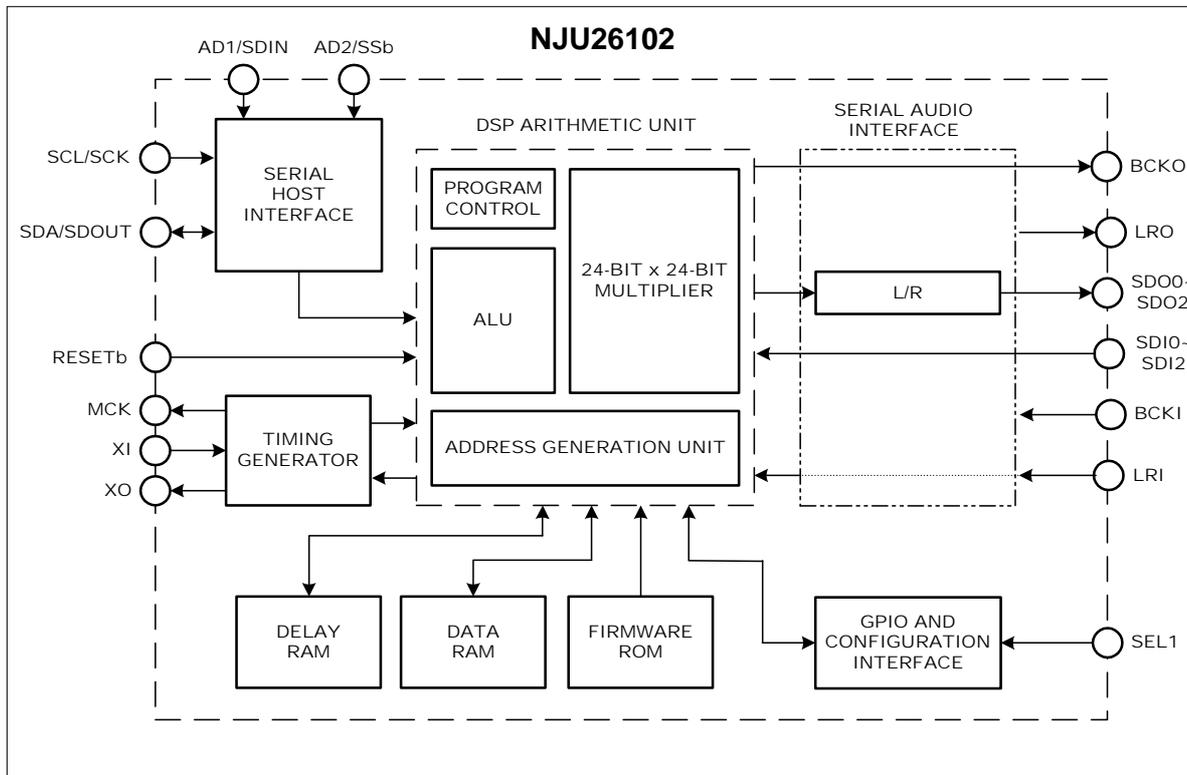
NJU26102

■ Function Block Diagram

Fig. 1   NJU26102 Block Diagram

■ DSP Block Diagram

Note 1. only one AGCs(*1, *2, *3) should be used.
Note 2. Do not use *1AGC and *3AGC during BBE ViVA2 being in use.
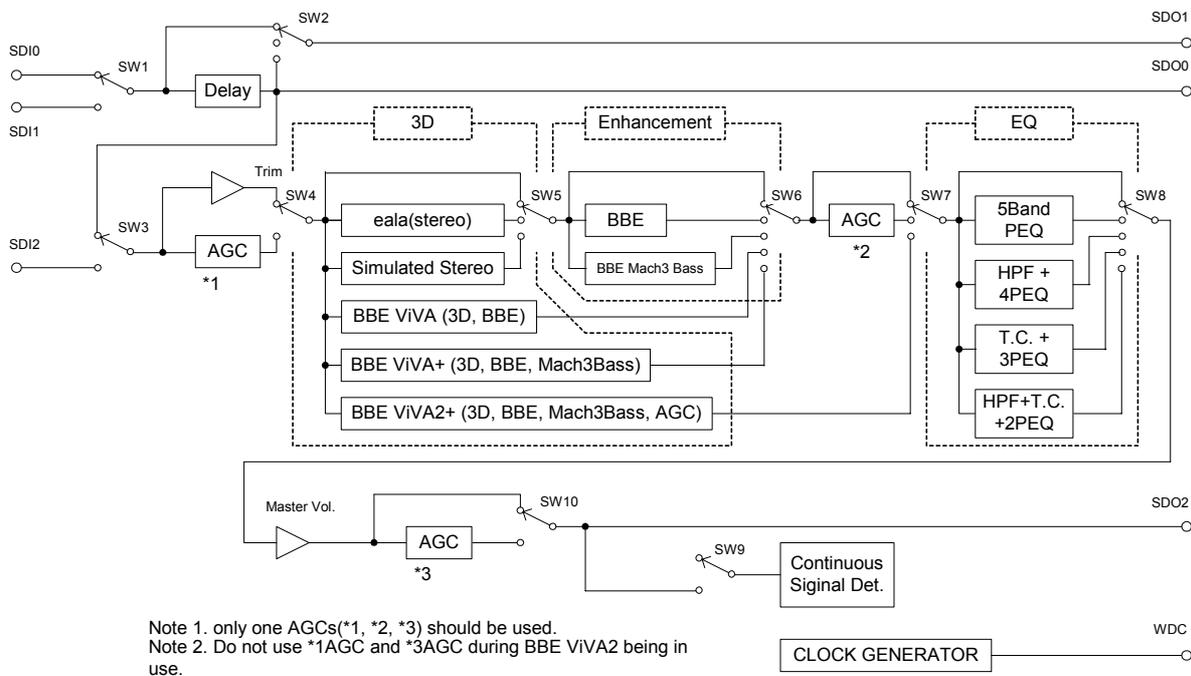
Fig. 2   NJU26102 Function Diagram

New Japan Radio Co.,Ltd.
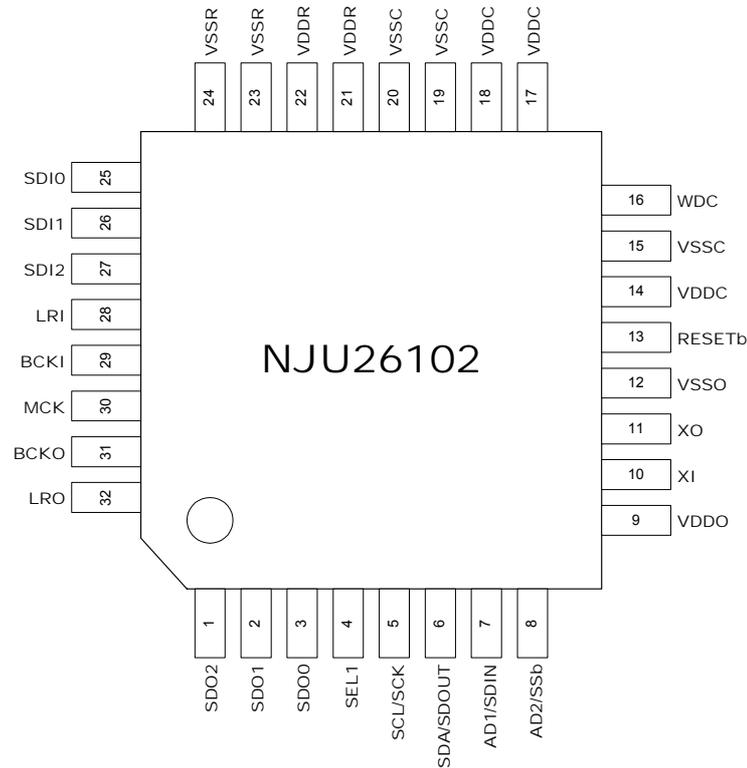
■ Pin Configuration

Fig. 3   NJU26102 Pin Configuration

■ Pin Description

Table 1   Pin Description

No.	Symbol	I/O	Description	No.	Symbol	I/O	Description
1	SDO2	O	Audio Data Output 2 L/R	17	VDDC	--	Core Power Supply +2.5V
2	SDO1	O	Audio Data Output 1 L/R	18			
3	SDO0	O	Audio Data Output 0 L/R	19	VSSC	--	Core GND
4	SEL1 *1	I	Select I²C or Serial bus	20			
5	SCL/SCK	I	I²C Clock / Serial Clock	21	VDDR	--	I/O Power Supply +2.5V
6	SDA/SDOUT	I/O	I²C I/O / Serial Output. This pin requires a pull-up resistance.	22			
7	AD1/SDIN	I	I²C Address / Serial Input	23	VSSR	--	I/O GND
8	AD2/SSb	I	I²C Address / Serial Enable	24			
9	VDDO	--	OSC Power Supply +2.5V	25	SDI0	I	Audio Data Input 0 L/R
10	XI	I	X'tal Clock Input	26	SDI1	I	Audio Data Input 1 L/R
11	XO	O	OSC Output	27	SDI2	I	Audio Data Input 2 L/R
12	VSSO	--	OSC GND	28	LRI	I	LR Clock Input
13	RESETb	I	RESET (active Low)	29	BCKI	I	Bit Clock Input
14	VDDC	--	Core Power Supply +2.5V	30	MCK	O	Master Clock Output
15	VSSC	--	Core GND	31	BCKO	O	Bit Clock Output
16	WDC *2	O	Clock for Watch Dog Timer	32	LRO	O	LR Clock Output

*   I : Input,

   O : Output,

   I/O: Bi-directional

*1   SEL1 : Input

*2   WDC : Output

NJU26102

■ Digital Audio Interface

The NJU26102 audio interface provides industry standard serial data formats of I^2S, MSB-first left-justified or MSB-first right-justified. The NJU26102 audio interface provides three data inputs, SDI0, SDI1, SDI2 and three data outputs, SDO0, SDO1, SDO2 as shown in table 2, table 3 and Fig.2. An audio interface input and output data format become the same data format.

Table 2   Serial Audio Input Pin

Pin No.	Symbol	Description
25	SDI0	Audio Data Input 0 L / R
26	SDI1	Audio Data Input 1 L / R
27	SDI2	Audio Data Input 2 L / R

Table 3   Serial Audio Output Pin

Pin No.	Symbol	Description
3	SDO0	Audio Data Output 0 L / R
2	SDO1	Audio Data Output 1 L / R
1	SDO2	Audio Data Output 2 L / R

■ Host Interface

The NJU26102 can be controlled via Serial Host Interface (SHI) using either of two serial bus format : 4-Wire serial bus or I^2C bus.(Table 4)   Data transfers are in 8 bit packets (1 byte) when using either format.
Serial Host Interface Pin Description.(Table 5)

Table 4   Serial Host Interface Pin Description

Pin No.	Symbol	Setting	Host Interface
4	SEL1	"Low"	I^2C bus
		"High"	4-Wire serial bus

Table 5   Serial Host Interface Pin Description

Pin No.	Symbol (I^2C bus / Serial)	I^2C bus Format	4-Wire Serial bus Format
5	SCL / SCK	Serial Clock	Serial Clock
6	SDA / SDOUT	Serial Data Input/Output (Open Drain Input/Output)	Serial Data Output (CMOS)
7	AD1 / SDIN	I^2C bus address Bit1	Serial Data Input
8	AD2 / SSb	I^2C bus address Bit2	Serial enable

Note : SDA /SDOUT pin is a bi-directional open drain.

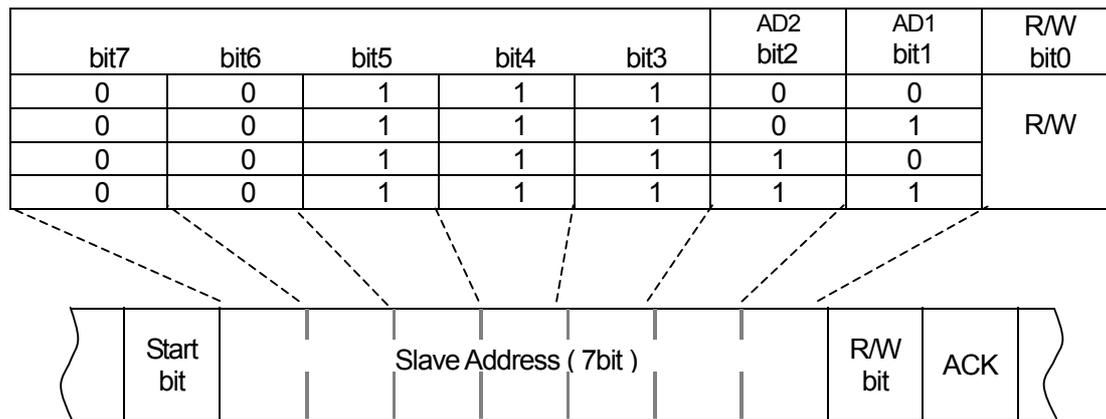   SDA /SDOUT output is normal CMOS output in case of 4-Wire Serial bus mode and SSb="Low".

    SDA /SDOUT output is Hi-Z state in case of 4-Wire Serial bus mode and SSb="High". This pin requires a pull-up resister in both 4-Wire serial and I^2C bus mode.

■ I²C bus

When the NJU26102 is configured for I²C bus communication during the Reset initialization sequence. I²C bus interface transfers data to the SDA pin and clocks data to the SCL pin.

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6) This offers additional flexibility to a system design by four different SLAVE addresses of the NJU26102. An address can be arbitrarily set up by the AD1 and AD2 pins. The I²C address of AD1/AD2 is decided by connection of AD1/AD2 pins.

Table 6   I²C bus SLAVE Address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	
0	0	1	1	1	0	1	R/W
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	

Start bit	Slave Address (7bit)	R/W bit	ACK

* SLAVE address is 0 when AD1/2 is "Low". SLAVE address is 1 when AD1/2 is "High".

Note : In case of the NJU26102, <u>only single-byte transmission is available</u>. The serial host interface supports "Standard-Mode (100kbps)" I²C bus data transfer.

■ 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1 pin ="High" during the Reset initialization sequence.

SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin. Data transfers are MSB first and are enabled by setting the Slave Select pin Low (SSb=0). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transitions of SSb.

SDOUT is Hi-Z in case of SSb = "High". SDOUT is CMOS output in case of SSb = "Low". SDOUT needs a pull-up resistor when SDOUT is Hi-Z.
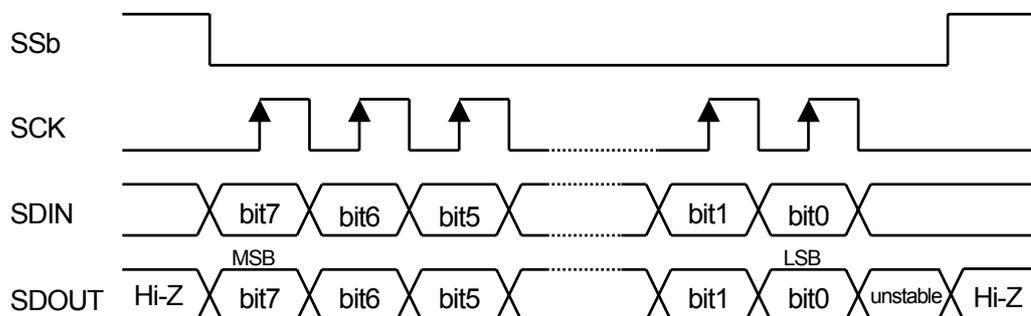
Fig. 4   4-Wire Serial Interface Timing

Note: When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb="High". When the data-clock is more than 8 clocks, the last 8 bit data becomes valid. After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes "High". SDOUT is Hi-Z in case of SSb = "High". SDOUT is CMOS output in case of SSb = "Low". SDOUT needs a pull-up resistor to prevent SDOUT from becoming floating level.

NJU26102

■ WatchDog Clock

The NJU26102 outputs clock pulse through WDC (No.16) pin during normal operation. The output toggle cycle (Low/High) from a WDC pin changes with sampling frequencies. (Table 7)

Table7   WatchDog Clock Output Cycle

Sampling Frequencies	WDC Output Cycle (Low/High) Time
32 KHz	276ms
44.1KHz	200ms
48 KHz	184ms

The NJU26102 generates a clock pulse through the WDC terminal after resetting the NJU26102. The WDC clock is useful to check the status of the NJU26102 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26102. When the WDC clock pulse is lost or not normal clock cycle, the NJU26102 does not operate correctly. Then reset the NJU26102 and set up the NJU26102 again.

Note: If input and output of a audio signal stop and an audio interface stops, WDC can't output.
That is because it has controlled based on the signal of an audio interface.

■ NJU26102 Command Table

Table 8   NJU26102 Command

No.	Command
1	System State
2	Firmware Version No. Request
3	Firmware Mode Select
4	Input Select / Fs Select
5	Input Trim
6	Master Volume
7	Channel Balance
8	AGC Threshold Level
9	eala Gain
10	BBE ViVA / ViVA+ Surround Gain
11	BBE
12	BBE ViVA2+ AGC
13	BBE Mach3Bass
14	EQ Mode
15	PEQ f0 / HPF fc
16	Delay Time
17	Continuous Signal Detect
18	NOP

Notes : In respect to detail command information, request New Japan Radio Co., Ltd. and permission of a licenser (BBE Sound, Inc.) is required.

.

NJU26102

■ License Information

1. The NJU26102 is manufactured by New Japan Radio Co.,Ltd. under license from BBE Sound Inc. BBE is a registered trademark of BBE Sound Inc. A license from BBE Sound Inc. must be required before the NJU26102 can be purchased from New Japan Radio Co.,Ltd.

    BBE Sound, Inc.
    5381 Production Drive
    Huntington Beach, CA 92649 USA
    Tel: 714-897-6766   Fax: 714-896-0736   http://www.bbesound.com

[CAUTION]
  The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

New Japan Radio Co.,Ltd.