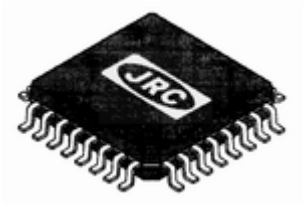
# Digital Signal Processor for TV

■Package



NJU26105FR1

## ■ General Description

The NJU26105 is a high performance 24-bit digital signal processor.
The NJU26105 provides 'eala' 3D Surround function, 'eala BASS' Dynamic Bass Boost function, 5Band PEQ, AGC, and Tone Control. These kinds of sound functions are suitable for TV, mini-component, CD radio-cassette, speakers system and other audio products.

## ■ FEATURES

**- Software**

- 3D sound : eala (NJRC Original Surround)
- Sound Enhancement: : ealaBASS (NJRC Original Dynamic Bass Boost)
- AGC
- 5Band PEQ
- Tone Control
- Master Volume
- WatchDog Clock Output

**- Hardware**

- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency : 38MHz Max.
- Digital Audio Interface : 2 Input ports / 2 Output ports
- Digital Audio Format : $I^2S$ 24bit, Left- justified, Right-justified, BCK : 32/64fs
- Master / Slave Mode : Master Mode MCK 1/2 fclk, 1/3 fclk
  ex. MCK = 384Fs(1/2) or MCK = 256Fs(1/3) at fclk=768Fs
- Power Supply : 2.5V
- Input terminal : 3.3V Input tolerant
- Package : QFP32-R1 (Pb-Free)
- Two kinds of micro computer interface : $I^2C$ bus (standard-mode/100kbps)
  : Serial interface (4 lines: clock, enable, input data, output data)

The detail hardware specification is described in the " NJU26100 Series Hardware Data Sheet".

## ■ Function Block Diagram

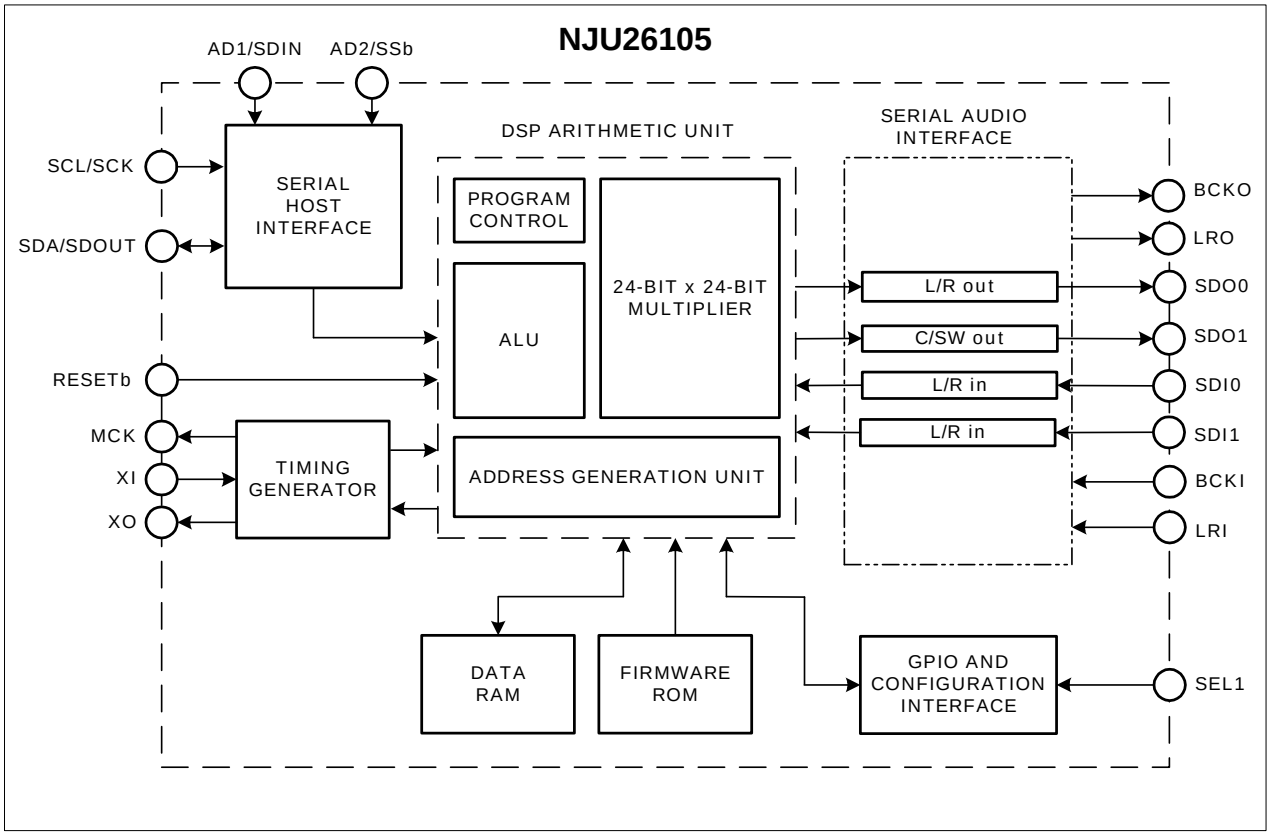



**Fig. 1 NJU26105 Block Diagram**

## ■ DSP Block Diagram

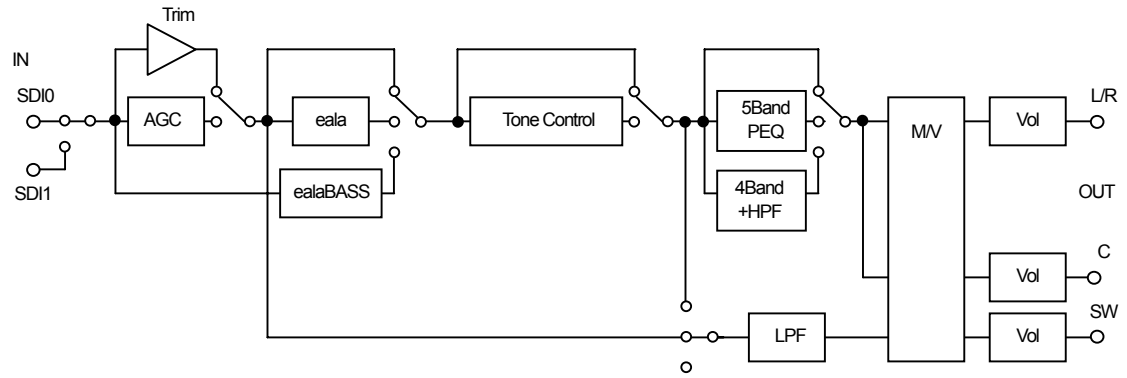



**Fig. 2 NJU26105 Function Diagram**

## ■ Pin Configuration

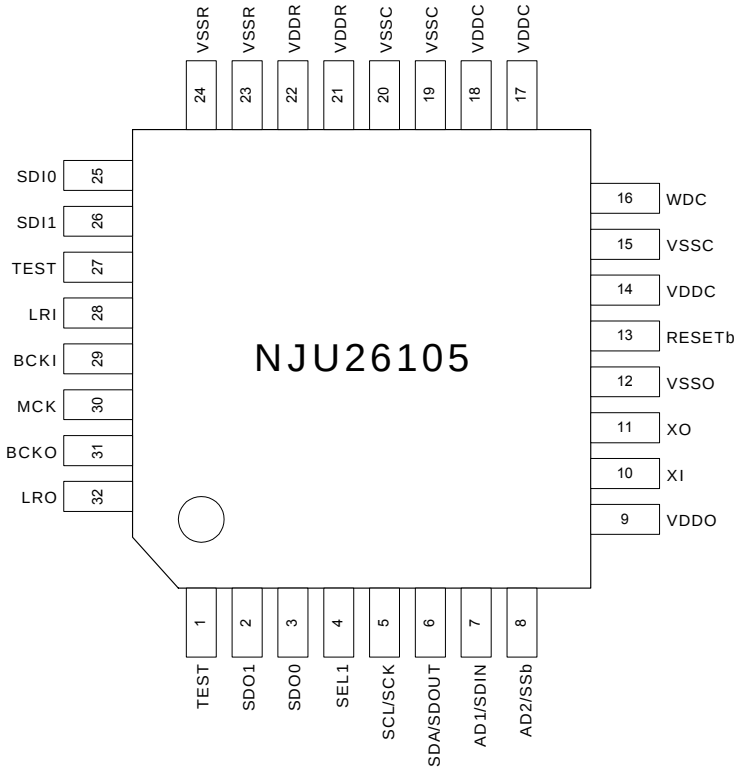



**Fig. 3 NJU26105 Pin Configuration**

## ■ Pin Description

**Table 1 Pin Description**

| No. | Symbol | I/O | Description |
|---|---|---|---|
| 1 | TEST | O | Open |
| 2 | SDO1 | O | Audio Data Output 1 C/SW |
| 3 | SDO0 | O | Audio Data Output 0 L/R |
| 4 | SEL1 *1 | I | Select $I^2C$ or Serial bus |
| 5 | SCL/SCK | I | $I^2C$ Clock / Serial Clock |
| 6 | SDA/SDOUT | I/O | $I^2C$ I/O / Serial Output |
| 7 | AD1/SDIN | I | $I^2C$ Address / Serial Input |
| 8 | AD2/SSb | I | $I^2C$ Address / Serial Enable |
| 9 | VDDO | -- | OSC Power Supply +2.5V |
| 10 | XI | I | X'tal Clock Input |
| 11 | XO | O | OSC Output |
| 12 | VSSO | -- | OSC GND |
| 13 | RESETb | I | RESET (active Low) |
| 14 | VDDC | -- | Core Power Supply +2.5V |
| 15 | VSSC | -- | Core GND |
| 16 | WDC *2 | O | Clock for Watch Dog Timer |

| No. | Symbol | I/O | Description |
|---|---|---|---|
| 17<br>18 | VDDC | -- | Core Power Supply +2.5V |
| 19<br>20 | VSSC | -- | Core GND |
| 21<br>22 | VDDR | -- | I/O Power Supply +2.5V |
| 23<br>24 | VSSR | -- | I/O GND |
| 25 | SDI0 | I | Audio Data Input 0 L/R |
| 26 | SDI1 | I | Audio Data Input 1 L/R |
| 27 | TEST | I | Connect to GND |
| 28 | LRI | I | LR Clock Input |
| 29 | BCKI | I | Bit Clock Input |
| 30 | MCK | O | Master Clock Output |
| 31 | BCKO | O | Bit Clock Output |
| 32 | LRO | O | LR Clock Output |

* I : Input,
O : Output,
I/O: Bi-directional

*1 SEL1 : Input

*2 WDC : Output

## ■ Digital Audio Interface

The NJU26105 audio interface provides industry standard serial data formats of $I^2S$, MSB-first left-justified or MSB-first right-justified. The NJU26105 audio interface provides two data inputs, SDI0, SDI1 and two data outputs, SDO0, SDO1 as shown in table 2, table 3 and Fig.2. An audio interface input and output data format become the same data format.

**Table 2 Serial Audio Input Pin**

| Pin No. | Symbol | Description |
|---|---|---|
| 25 | SDI0 | Audio Data Input 0 L / R |
| 26 | SDI1 | Audio Data Input 1 L / R |

**Table 3 Serial Audio Output Pin**

| Pin No. | Symbol | Description |
|---|---|---|
| 3 | SDO0 | Audio Data Output 0 L / R |
| 2 | SDO1 | Audio Data Output 1 C / SW |

## ■ Host Interface

The NJU26105 can be controlled via Serial Host Interface (SHI) using either of two serial bus format : 4-Wire serial bus or $I^2C$ bus.(Table 4) Data transfers are in 8 bit packets (1 byte) when using either format.
Serial Host Interface Pin Description.(Table 5)

**Table 4 Serial Host Interface Pin Description**

| Pin No. | Symbol | Setting | Host Interface |
|---|---|---|---|
| 4 | SEL1 | "Low" | $I^2C$ bus |
| | | "High" | 4-Wire serial bus |

**Table 5 Serial Host Interface Pin Description**

| Pin No. | Symbol ($I^2C$ bus / Serial) | $I^2C$ bus Format | 4-Wire Serial bus Format |
|---|---|---|---|
| 5 | SCL / SCK | Serial Clock | Serial Clock |
| 6 | SDA / SDOUT | Serial Data Input/Output (Open Drain Input/Output) | Serial Data Output (CMOS) |
| 7 | AD1 / SDIN | $I^2C$ bus address Bit1 | Serial Data Input |
| 8 | AD2 / SSb | $I^2C$ bus address Bit2 | Serial enable |

**Note :** SDA /SDOUT pin is a bi-directional open drain.
SDA /SDOUT output is normal CMOS output in case of 4-Wire Serial bus mode and SSb="Low".
SDA /SDOUT output is Hi-Z state in case of 4-Wire Serial bus mode and SSb="High". This pin requires a pull-up resister in both 4-Wire serial and $I^2C$ bus mode.

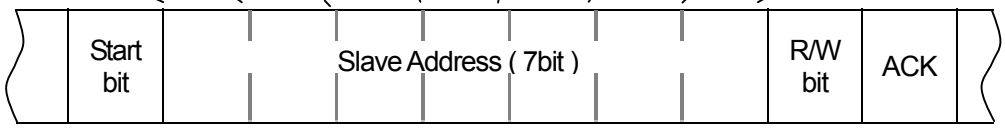
## ■ I²C bus

When the NJU26105 is configured for I²C bus communication during the Reset initialization sequence. I²C bus interface transfers data to the SDA pin and clocks data to the SCL pin.

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6) This offers additional flexibility to a system design by four different SLAVE addresses of the NJU26105. An address can be arbitrarily set up by the AD1 and AD2 pins. The I²C address of AD1/AD2 is decided by connection of AD1/AD2 pins.

**Table 6 I²C bus SLAVE Address**

| bit7 | bit6 | bit5 | bit4 | bit3 | AD2 bit2 | AD1 bit1 | R/W bit0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | R/W |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | |




* SLAVE address is 0 when AD1/2 is “Low”. SLAVE address is 1 when AD1/2 is “High”.

**Note :** In case of the NJU26105, only single-byte transmission is available. The serial host interface supports “Standard-Mode (100kbps)” I²C bus data transfer.

## ■ 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1 pin =”High” during the Reset initialization sequence.

SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin. Data transfers are MSB first and are enabled by setting the Slave Select pin Low ( SSb=0 ). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transitions of SSb.

SDOUT is Hi-Z in case of SSb = “High”. SDOUT is CMOS output in case of SSb = “Low”. SDOUT needs a pull-up resistor when SDOUT is Hi-Z.

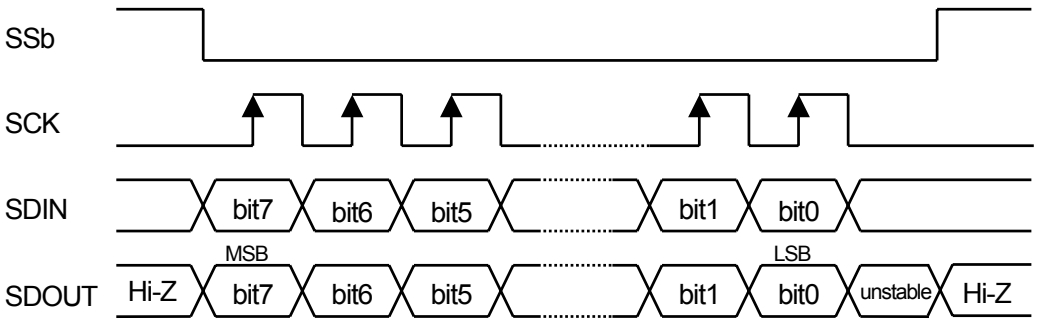



**Fig. 4 4-Wire Serial Interface Timing**

**Note:** When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb=”High”. When the data-clock is more than 8 clocks, the last 8 bit data becomes valid. After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes “High”. SDOUT is Hi-Z in case of SSb = “High”. SDOUT is CMOS output in case of SSb = “Low”. SDOUT needs a pull-up resistor to prevent SDOUT from becoming floating level.

## ■ WatchDog Clock

The NJU26105 outputs clock pulse through WDC (No.16) pin during normal operation. The output toggle cycle (Low/High) from a WDC pin changes with sampling frequencies. (Table 7)

**Table7 WatchDog Clock Output Cycle**

| Sampling Frequencies | WDC Output Cycle (Low/High) Time |
|---|---|
| 32 KHz | 128ms |
| 44.1KHz | 92ms |
| 48 KHz | 85ms |

The NJU26105 generates a clock pulse through the WDC terminal after resetting the NJU26105. The WDC clock is useful to check the status of the NJU26105 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26105. When the WDC clock pulse is lost or not normal clock cycle, the NJU26105 does not operate correctly. Then reset the NJU26105 and set up the NJU26105 again.

**Note:** If input and output of a audio signal stop and an audio interface stops, WDC can't output.
That is because it has controlled based on the signal of an audio interface.

## ■ NJU26105 Command Table

**Table 8 NJU26105 Command**

| No. | Command |
|---|---|
| 1 | Start Command |
| 2 | System State |
| 3 | Firmware mode select |
| 4 | Fs Select / Input Select |
| 5 | Master Volume |
| 6 | Master Volume Boost |
| 7 | Master Volume Smooth Control |
| 8 | Channel Balance |
| 9 | Output Channel Trim L/R |
| 10 | Output Channel Trim C/SW |
| 11 | AGC Threshold Level |
| 12 | AGC Noise Compressor Threshold Level |
| 13 | AGC Attack Time / Release Time |
| 14 | AGC Ratio / Boost |
| 15 | AGC Output Trim |
| 16 | AGC BYPASS Trim |
| 17 | eala Surround Gain |

| No. | Command |
|---|---|
| 18 | eala BASS Bass fo |
| 19 | eala BASS Bass volume |
| 20 | eala BASS Treble fo |
| 21 | eala BASS Treble gain |
| 22 | eala BASS Output Trim |
| 23 | eala BASS Attack Time / Release Time |
| 24 | Tone Control Bass/Treble Gain |
| 25 | EQ Band1 mode |
| 26 | PEQ1 to 5 / HPF fo |
| 27 | PEQ1 to 5 Q |
| 28 | PEQ1 to 5 Gain |
| 29 | SW fc |
| 30 | Version No. Request |
| 31 | Status Read |
| 32 | AGC Input Level Request |
| 33 | AGC Gain Reduction Level Request |
| 34 | No Operation |

**Notes :** In respect to detail command information, request New Japan Radio Co., Ltd.