8031AH

Single-Chip 8-Bit Microcontroller

MILITARY INFORMATION

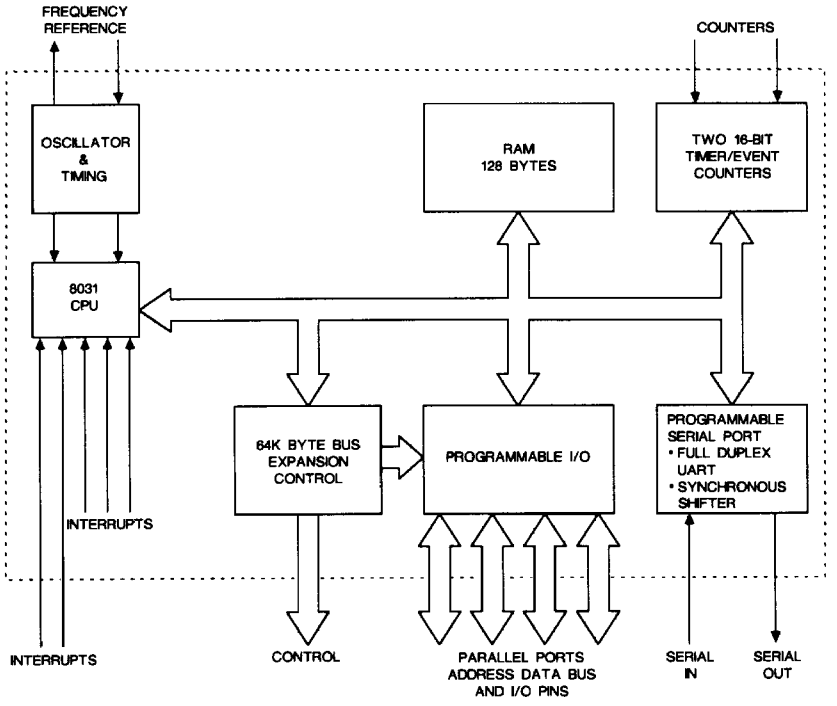
DISTINCTIVE CHARACTERISTICS

- 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- 64K addressable Program Memory
- All versions are pin-compatible
- Boolean processor
- Programmable Serial Port
- Five interrupt sources/two priority levels
- On-chip Oscillator/Clock Circuit
- 64K addressable Data Memory

GENERAL DESCRIPTION

The 8031AH is optimized for control applications. Byte processing and numerical operations on small data structures are facilitated by a variety of fast addressing modes for accessing the internal RAM. The instruction set provides a convenient menu of 8-bit arithmetic instructions, including multiply and divide instructions. Extensive on-chip support is provided for 1-bit variables as a separate data type. This allows direct bit manipulation and testing in control and logic systems that require Boolean processing. Efficient use of program memory results from an instruction set consisting of 44% 1-byte, 41% 2-byte, and 15% 3-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1 μs, 40% in 2 μs, and multiply and divide require only 4 μs.

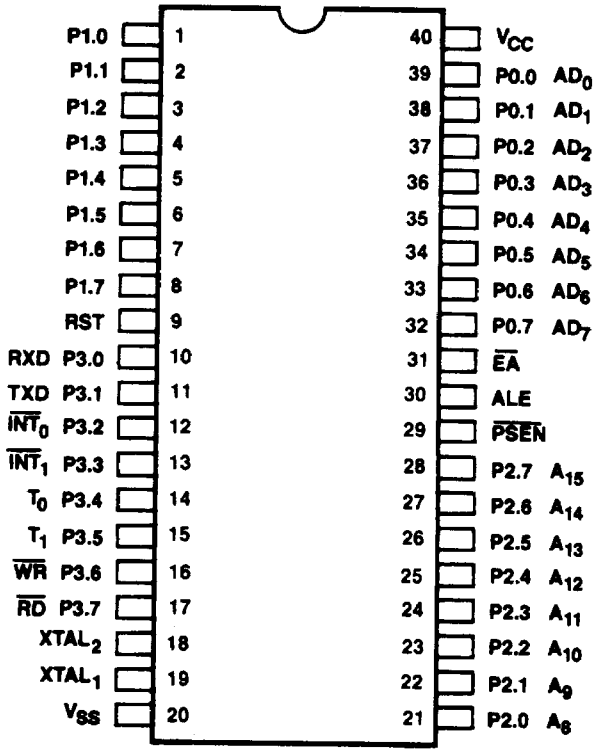
BLOCK DIAGRAM



BD007261

Publication # 09399 Rev. A Amendment /0
Issue Date: December 1987

CONNECTION DIAGRAM
Top View



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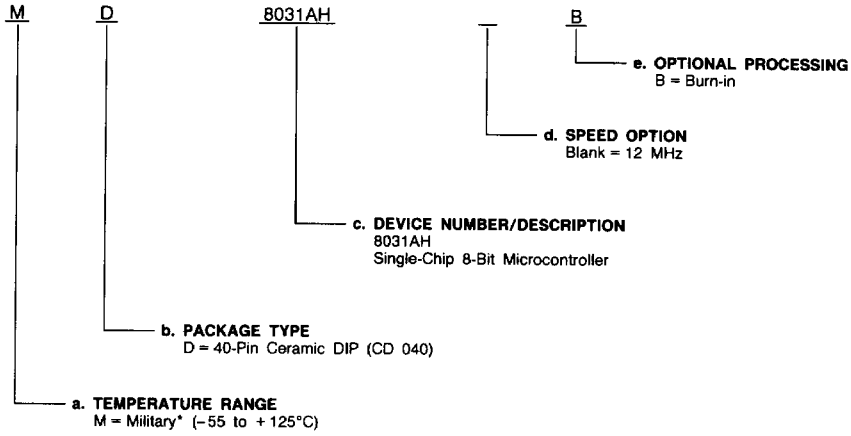
Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Temperature Range**
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing



Valid Combinations	
MD	8031AHB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

*Military temperature range products are NPL (Non-Compliant Products List) or Non-MIL-STD-883C Compliant Products only.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
with Respect to Ground ..... −0.5 to +7.0 V
Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V
Ground (V_{SS}) ..... 0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		−0.5	0.7	V
V_{IH}	Input HIGH Voltage (Except RST/V_{PD} and $XTAL_2$)		2.2	V_{CC} +0.5	V
V_{IH1}	Input HIGH Voltage to RST/V_{PD}, $XTAL_2$	$XTAL_1 = V_{SS}$	2.8	V_{CC} +0.5	V
V_{PD}	Power-Down Voltage to RST/V_{PD}	V_{CC} = 0 V	4.5	5.5	V
V_{OL}	Output LOW Voltage, Ports 1, 2, 3 (Note 1)	I_{OL} = 1.2 mA		0.45	V
V_{OL1}	Output LOW Voltage, Port 0, ALE, $\overline{PSEN}$ (Note 1)	I_{OL} = 2.4 mA		0.45	V
V_{OH}	Output HIGH Voltage, Ports 1, 2, 3	I_{OH} = −60 μA	2.4		V
V_{OH1}	Output HIGH Voltage, Port 0, ALE, $\overline{PSEN}$	I_{OH} = −400 μA	2.4		V
I_{IL}	Logical 0 Input Current, Ports 1, 2, 3	V_{IL} = 0.45 V		−800	μA
I_{IL2}	Logical 0 Input Current for $XTAL_2$	$XTAL_1 = V_{SS}$ V_{IN} = 0.45 V		−3.2	mA
I_{IH1}	Input HIGH Current to RST/V_{PD} for Reset	$V_{IN} < (V_{CC} - 1.5\ V)$		600	μA
I_{LI}	Input Leakage Current to Port 0, $\overline{EA}$	0.45 < V_{IN} < V_{CC}		±10	μA
I_{CC}	Power-Supply Current	$\overline{EA}$ = V_{CC}		140	mA
I_{PD}	Power-Down Current	V_{CC} = 0 V; V_{PD} = 5.0 V		15	mA
C_{IO}	Capacitance of I/O Buffer	fc = 1 MHz		10	pF

Notes: 1. Capacitive load on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

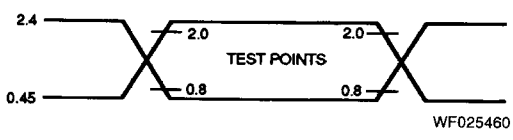
SWITCHING CHARACTERISTICS over operating range (Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

Parameter Symbol	Parameter Description	12-MHz Clock		Variable Clock		Unit
		Min.	Max.	Min.	Max.	
TCY 1/TCLCL	Oscillator Frequency			3.5TCLCL	12TCLCL	MHz
TLHLL	ALE Pulse Width	112		2TCLCL–55		ns
TAVLL	Address Setup to ALE	28		TCLCL–55		ns
TLLAX	Address Hold After ALE	33		TCLCL–50		ns
TLLIV	ALE to Valid Instruction In		218		4TCLCL–115	ns
TLLPL	ALE to $\overline{PSEN}$	43		TCLCL–40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	190		3TCLCL–60		ns
TPLIV	$\overline{PSEN}$ to Valid Instruction In				3TCLCL–140	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		48		TCLCL–35	ns
TPXAV	Address Valid After $\overline{PSEN}$	58		TCLCL–25		ns
TAVIV	Address to Valid Instruction In		287		5TCLCL–130	ns
TPLAZ	Address Float After $\overline{PSEN}$		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL–100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL–100		ns
TRLDV	$\overline{RD}$ to Valid Data In		232		5TCLCL–185	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		82		2TCLCL–85	ns
TLLDV	ALE to Valid Data In		497		8TCLCL–170	ns
TAVDV	Address to Valid Data In		565		9TCLCL–185	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	185	315	3TCLCL–65	3TCLCL+65	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	188		4TCLCL–145		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	8		TCLCL–75		ns
TQVWH	Data Setup Before $\overline{WR}$	508		7TCLCL–75		ns
TWHQX	Data Hold After $\overline{WR}$	18		TCLCL–65		ns
TRLAZ	Address Float After $\overline{RD}$		20		20	ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ HIGH to ALE HIGH	18	148	TCLCL–65	TCLCL+65	ns

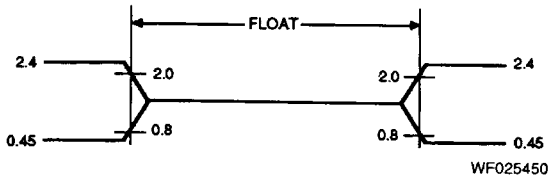
EXTERNAL CLOCK DRIVE

Parameter Symbol	Parameter Description	Min.	Max.	Units
1/TCLCL	Oscillator Frequency	3.5	12	MHz
TCHCX	HIGH Time	20		ns
TCLCX	LOW Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

AC TESTING



Input/Output Waveform



Float Waveform

AC inputs during testing are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0". For timing purposes, the float state is defined as the point at which a P0 pin sinks 2.4 mA or sources 400 μA at the voltage test levels.