SONY **SBX1602A**

Serial Interface/Transmission Decoder

Description

The SBX1602A is a Hybrid IC that receives serial data of the SMPTE T14.224 encoded by the SBX1601A and decodes into parallel data.

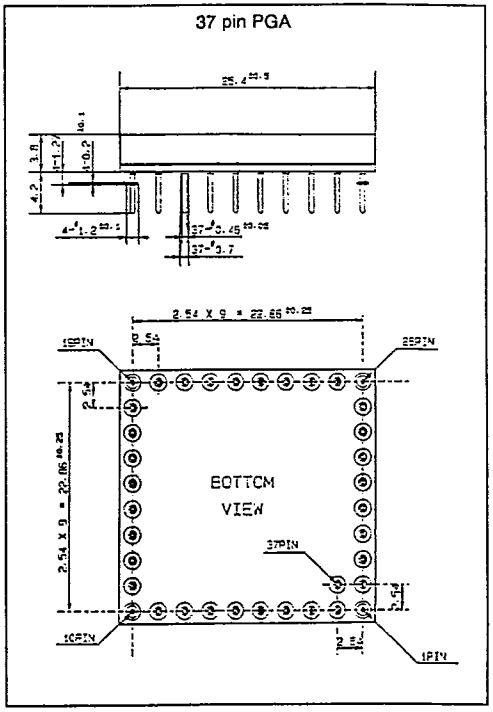
Features

Built-in automatic equalizer for up to 300m using Belden 8281 or equivalent coaxial cable (30dB loss at 135MHz), PLL circuit for reclocking, and serial-parallel conversion circuit.

This serial transmission decoder can be used with only a few external components. Other related IC's include SBX1601A serial transmission encoder (parallel to serial conversion) and CXA1389AQ coaxial cable driver.

Package Outline

Unit : mm



1. Structure

Hybrid IC

2. Applications

- Decoder for 100 to 270 Mbps Serial data.
- Examples of application:

  Serial Interface/Transmission for

4 : 2 : 2	270Mbps
4fsc PAL	177Mbps
4fsc NTSC	143Mbps.

3. Functions

- Automatic cable equalizer
  (Maximum gain: 30dB at 135MHz).
- PLL for serial clock generation.
- Reclocked repeater output (active loop through).
- Descrambler: Modulo-2 Multiplication by G (X)=(X^9+X^4+1) (X+1).
- Serial to parallel conversion.
- SYNC monitor output.
- Eye pattern monitoring.
- Input signal detector.

E90722A'6 - ST

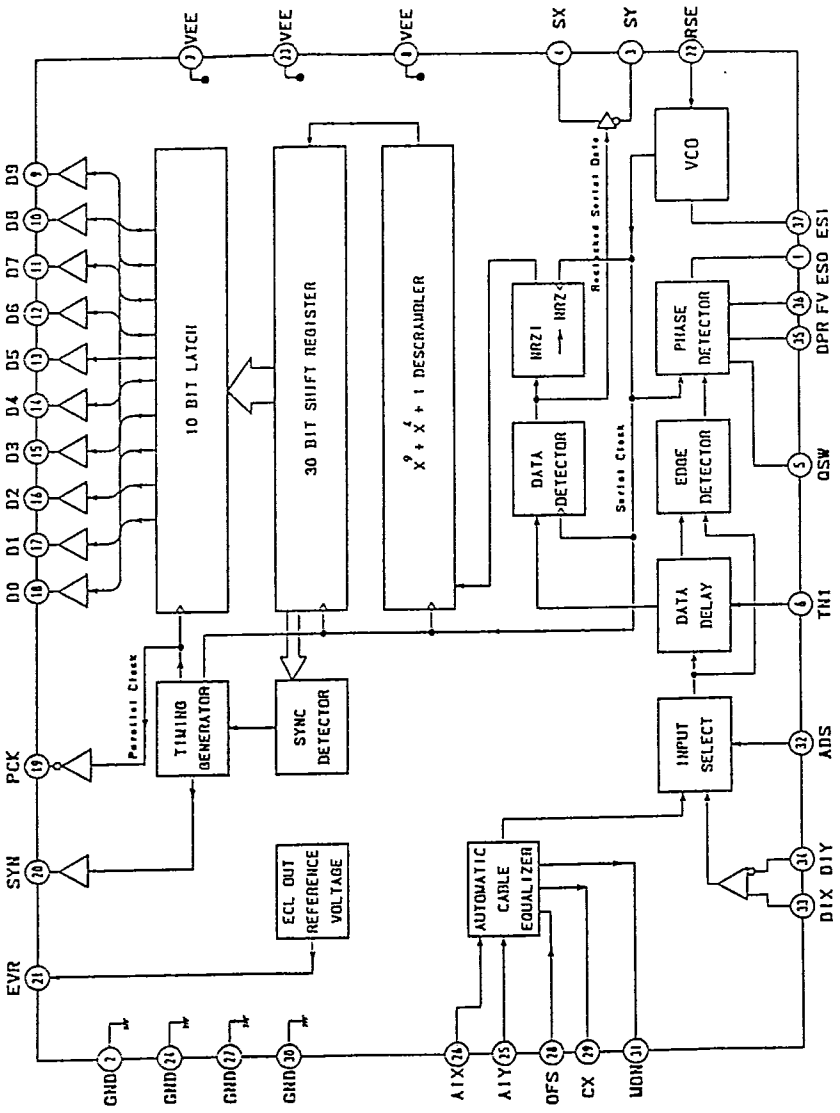
4. Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Supply voltage	V_{EE}	−6	V
Input voltage	V_{IN}	V_{EE} to 0	V
Output current	I_{OUT}	−30	mA
Operating temperature	Top	0 to 65	°C
Storage temperature	Tstg	−50 to +125	°C
Allowable power dissipation	P_D	2.0	W

5. Recommended Operating Conditions

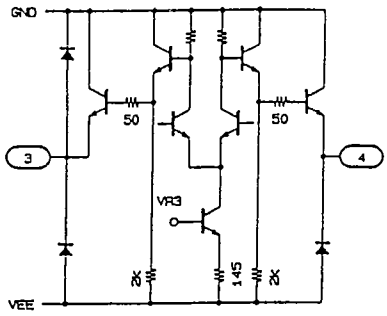
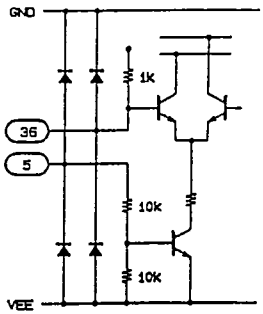
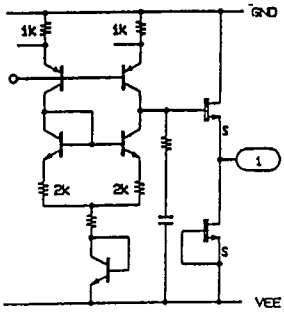
Item	Symbol	Ratings	Unit
Supply voltage	V_{EE}	−4.8 to −5.2	V
Operating temperature	Top	0 to 65	°C

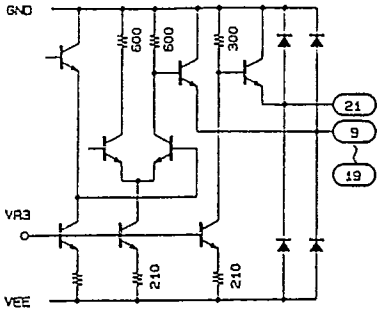
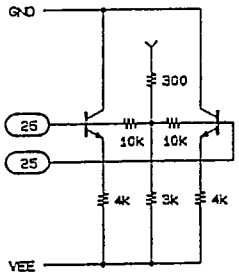
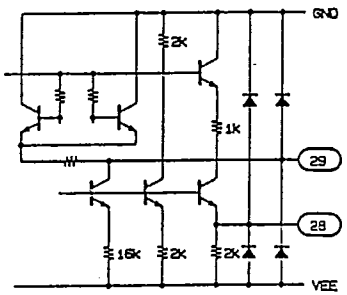
6. Block Diagram

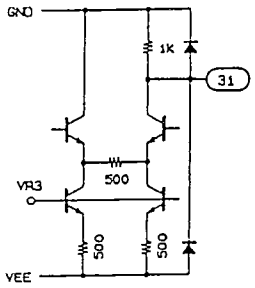
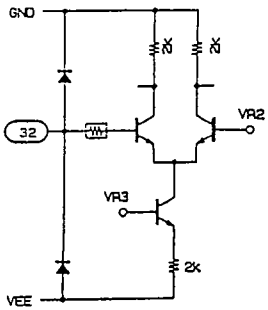
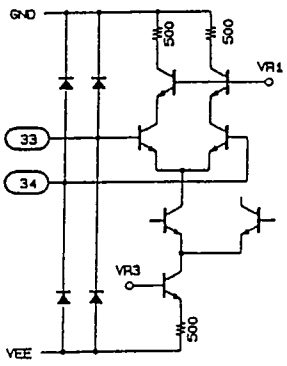


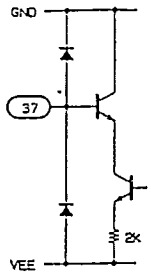
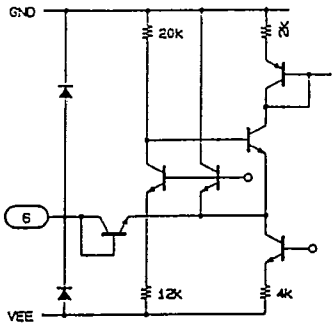
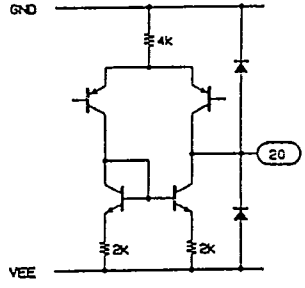
Block diagram of SBX1602A

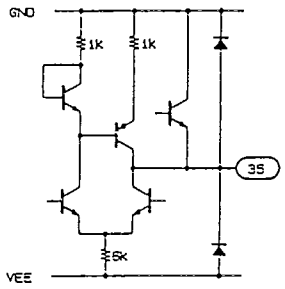
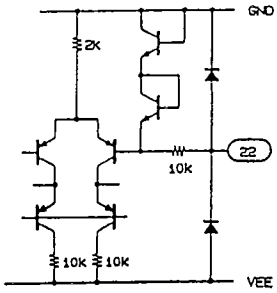
7. Pin Description

Pin No.	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
3	SY		Reclocked serial output: While TN1 is kept H, reclocked output is disabled maintaining SX to H SY to L. H L	O		 –1.6 –2.4		 V V
4	SX							
5	QSW (GND)		This node is reserved: Connect to GND for this version.					
36	FV		Adjusting VCO free run frequency:	I				
1	ES0		Output of phase comparator: Shall be connected to ES1 with shortest distance.	O		–3.2		V

Pin No.	Symbol	Equivalent circuit	Description	I/O	Standard Min.	Typ.	Max.	Unit
9 to 18	D9 to D0		Parallel data outputs. H L	O		 –0.8 –1.6		 V V
19	PCK		Internal parallel clock: Rising edge coincides with a mid point of data. H L			 –0.8 –1.6		 V V
21	EVR		Data output reference potential.	O		–1.2		V
26	AIX		Equalizer input. (Analog input)	I		–2.0		V
25	AIY		Equalizer input return.					
28	NC		Leave it open.	I		–4.6		V
29	CX		AGC output. Without input signal With input signal	O		 –2.4 –2.0		 V V

Pin No.	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
31	MON		Eye pattern monitor: Connect 75Ω resistor between MON and GND. Use DC input of the scope with 75Ω coaxial cable and its termination.	O		15		mV (pp)
32	ADS		Input select: H: Digital input DIX/DIY L: Analog input AIX/AIY H L	I	 –0.5		 –1.5	 V V
33	DIX		Digital differential input: Selected when ADS is at H. H L	I	 –1.0		 –1.6	 V V
34	DIY							

Pin No.	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
37	ESI		PLL error signal input: Shall be connected to ES0 with the shortest distance.	I		–3.2		V
6	TN1		Test node: H: Serial input signal is disabled and VCO is set for free run. L: Normal operation. H L	I	 –1.0	 	 –4.0	 V V
20	SYN		SYNC monitor: Output state toggles between H and L at every SYNC word detection. H L	O	 –1.0	 	 –4.0	 V V

Pin No.	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
35	DPR		Input signal monitor: H signifies a presence of input signal while L does an absence. H L	O	 –1.0	 	 –4.0	 V V
22	RSE		Rate selection: Selects VCO oscillation frequency range: H: High Range 140 to 270MHz L: Low Range 100 to 145MHz H L	I	 –0.4	 	 –4.0	 V V
7 23	V_{EE}		–5V supply I/O buffer PLL, equalizer.		–5.2	–5.0	–4.8	V
8	V_{EE}		–5V supply Logic part: Leave open in "repeater" mode for power saving.		–5.2	–5.0	–4.8	V
2 24 27 30	GND		GND					

8. Electrical Characteristics

8-1. DC Characteristics

(V_{EE}=–5V, Ta=25°C)

Item	Symbol	Test conditions	Test circuit Fig.	Min.	Typ.	Max.	Unit
Supply current	I_{EE}	V_{EE}=5V	Fig. 8-3		185		mA
Input voltage	V_{IH}	Pin used: ADS		–0.4			V
	V_{IL}					–1.5	V
	V_{IH}	Pin used: RSE	Fig. 8-9	–0.4			V
	V_{IL}					–4.0	V
	V_{IH}	Pin used: DIX, DIY		–1.0			V
	V_{IL}					–1.6	V
Input current	I_{IH}	Pin used: DIX, DIY	Fig. 8-4			+5.0	μA
	I_{IL}			–1.0		+1.0	μA
Input voltage	V_{IH}	Pin used: TN1	Fig. 8-8	–1.0			V
	V_{IL}					–4.0	V
Output voltage	V_{OH}	Pin used: PCK, Dn R_P=1kΩ			–0.8		V
	V_{OL}				–1.6		V
	V_M	Pin used: EVR R_P=1kΩ			–1.2		V
	V_{OH}	Pin used: DPR, SYN I_{OH}=–10 μA, I_{OL}=+10 μA	Fig. 8-6	–1.0			V
	V_{OL}		Fig. 8-7			–4.0	V
	V_{OH}	Pin used: SX, SY R_P=220Ω			–1.6		V
	V_O				–2.4		V

8-2. AC Characteristics

PLL

(V_{EE}=–5V, Ta=25°C)

Item	Symbol	Test conditions	Test circuit Fig.	Min.	Typ.	Max.	Unit
VCO oscillation frequency 1 *	f_{MAX1}	RSE= "H"	Fig. 8-5	30.0			MHz
	f_{MIN1}					14.0	MHz
VCO oscillation frequency 2 *	f_{MAX2}	RSE= "L"		15.0			MHz
	f_{MIN2}					10.0	MHz
PLL pull in range *	f_{HP1}	f signal=270MHz RSE= "H"	Fig. 8-2			27.7	MHz
	f_{LP1}			25.5			MHz
	f_{HP2}	f signal=177MHz RSE= "H"				18.5	MHz
	f_{LP2}			16.8			MHz
	f_{HP3}	f signal=143MHz RSE= "L"				15.0	MHz
	f_{LP3}			13.3			MHz

* Measured through PCK (Pin 19): 1/10 of serial clock.

Switching Characteristics

(V_{EE}=–5V, Ta=25°C)

Item	Symbol	Test conditions	Test circuit Fig.	Min.	Typ.	Max.	Unit
rise time	tr	Pins used: PCK, Dn R_P=1kΩ			0.8		nsec
fall time	tf				1.4		nsec
rise time	tr	Pins used: SX, SY R_P=220Ω			0.7		nsec
fall time	tf				0.7		nsec
delay time	td	PCK-Dn		–5		+5	nsec

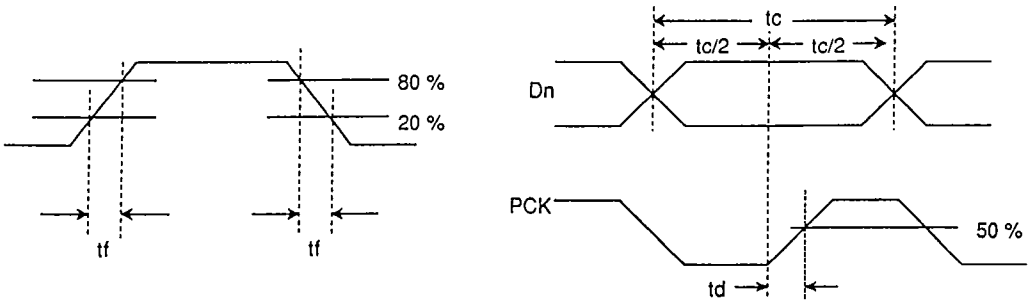


Fig. 8-1. Definition of tr, tf, tc, td

Equalizer

(V_{EE}=–5V, Ta=25°C)

Item	Symbol	Test conditions	Test circuit Fig.	Min.	Typ.	Max.	Unit
Equalizer input voltage	V_{AIN}	Pins used: AIX	Fig. 8-2			0.88	Vp-p
Input capaciance	C_{IN}	Pins used: AIX freq=100MHz					pF
Input resistance	R_{IN}	Pins used: AIX freq=100MHz					Ω

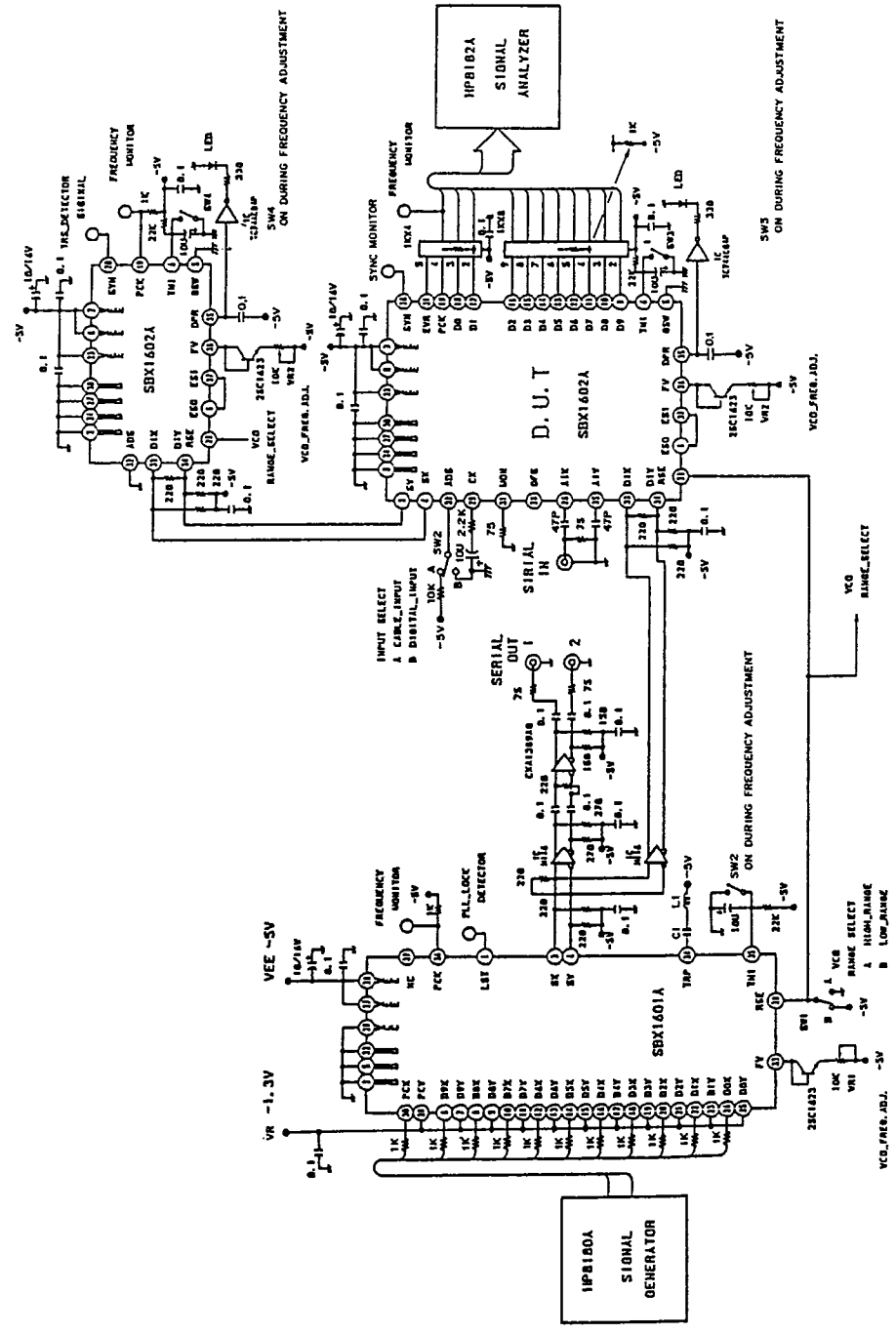


Fig. 8-2. Test circuit diagram

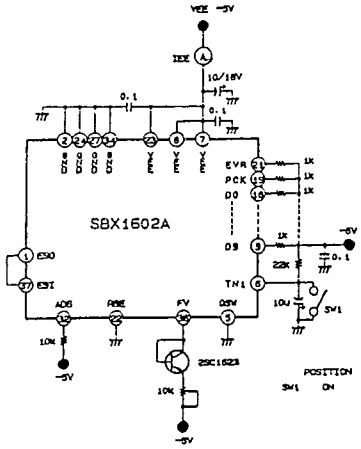


Fig. 8-3.

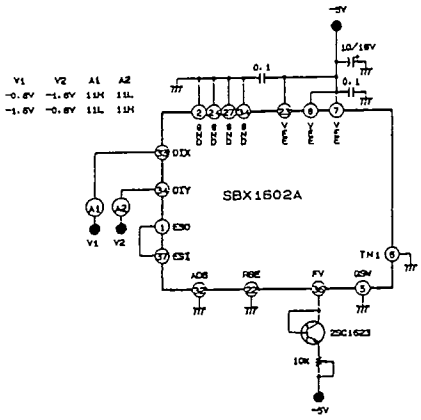


Fig. 8-4.

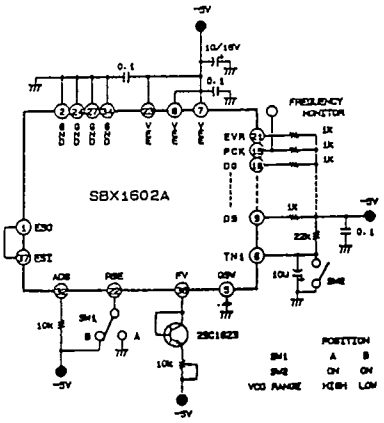


Fig. 8-5.

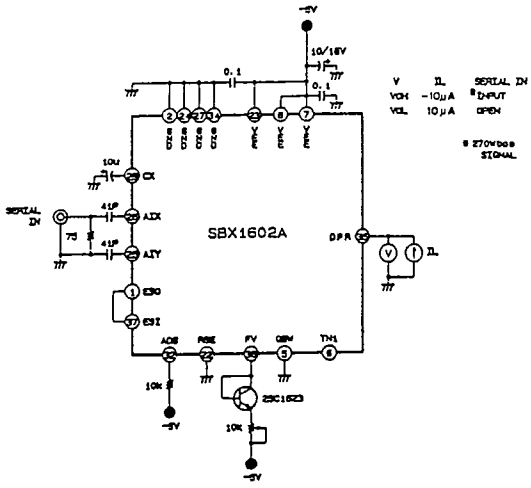


Fig. 8-6.

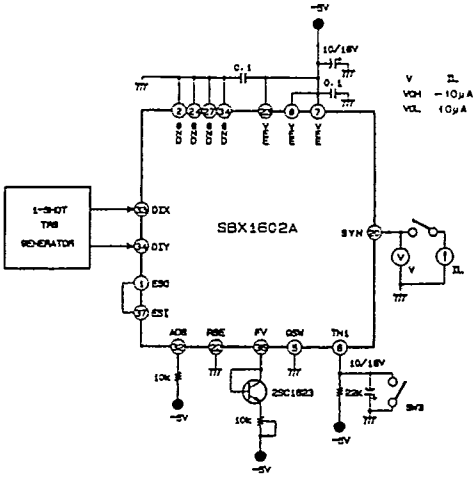


Fig. 8-7.

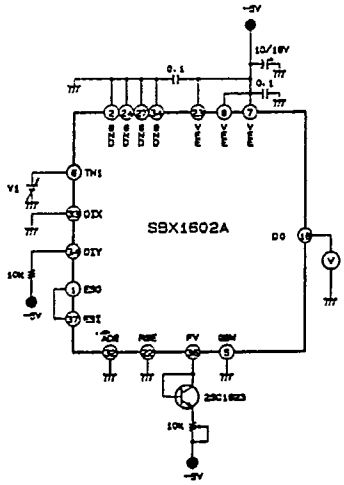


Fig. 8-8.

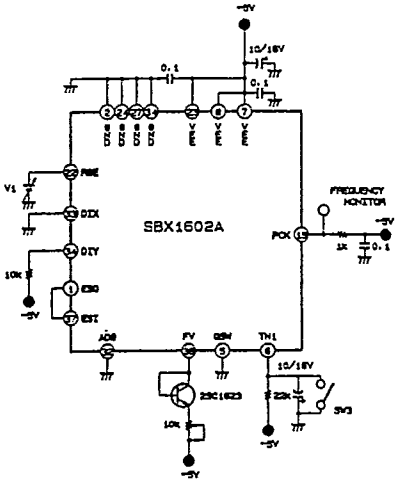


Fig. 8-9.

9. SBX1602A General

As is shown in the overall block diagram on Page 3, SBX1602A is composed of the following functions:

(1) Analog input as a primary input with automatic equalizer to meet the loss characteristics of coaxial cable

(2) Digital serial input as a secondary input to receive the encoded signal from short distances within the same printed circuit board or the same equipment

(3) Phase locked loop (PLL) variable oscillator

(4) Reclocked serial output

(5) Serial descrambler

(6) SYNC detector

(7) Deserializer

(8) Parallel output buffer amplifiers

(9) Three diagnostic signals: eye monitor, SYNC monitor and input data presence monitor.

A brief explanation of each function is given in the following sections.

9-1. Analog Input (Cable equalizer)

If the signal is applied to the analog input AIX (pin 26) high frequency loss due to the coaxial cable and low frequency loss caused by the DC cut for transmission are recovered by the cable equalizer and the quantized feedback respectively. The equalized serial signal is passed through a comparator (detector) to be regenerated.
Typical characteristics of the equalization are given in Section 11.

Fig. 9-1 (a) and (b) show two types of suggested input circuits. (a) is simple but slightly more susceptible with static or impulse noise than (b) while the reverse is true for (b).

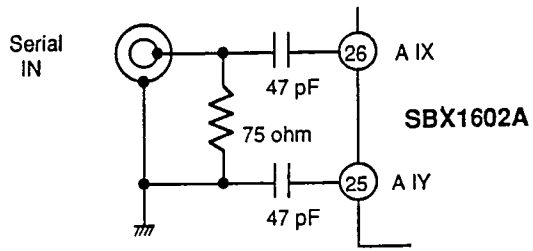


Fig. 9-1 (a). Equalizer input circuit with capacitor coupling

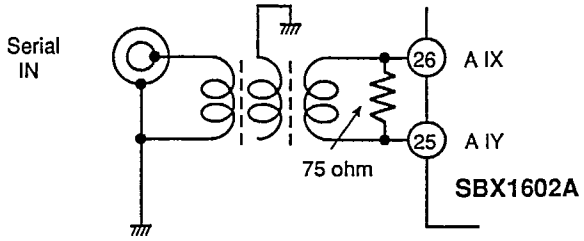


Fig. 9-1 (b). Equalizer input circuit with transformer coupling

In both input circuit configurations, a consideration is required in a practical design to obtain a sufficient return-loss (at least 15dB over a frequency range of 5MHz to the bit rate frequency used). To achieve this, it is effective to add a small inductance in series with the 75 Ω termination resistor. Fig. 9-2. shows an implementation example.

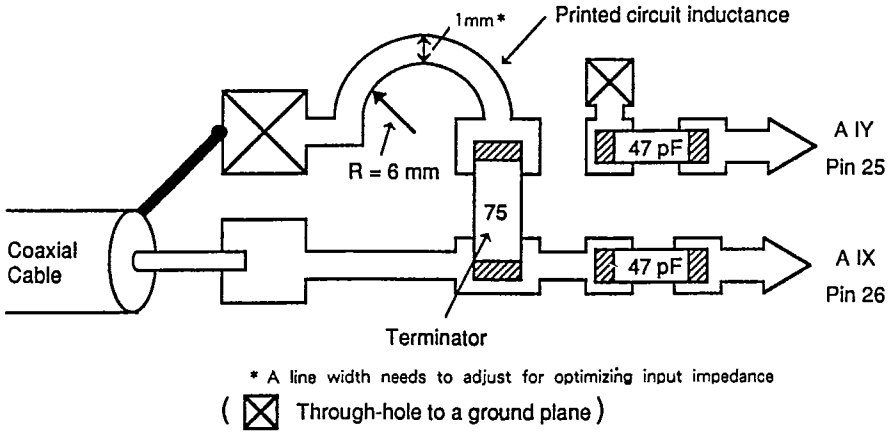


Fig. 9-2. An example of technique to improve the return-loss figure for the capacitor coupling input case.

9-2. Equalizer AGC time-constant

An external time-constant shown in Fig. 9-3. is required at CX node (pin 29) in order to obtain stable operation at all times.

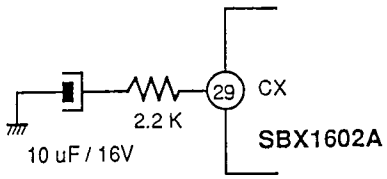


Fig. 9-3. AGC time-constant

9-3. Eye monitor output

It is possible to examine the eye-pattern at the decision point by connecting an oscilloscope as shown in Fig. 9-4.

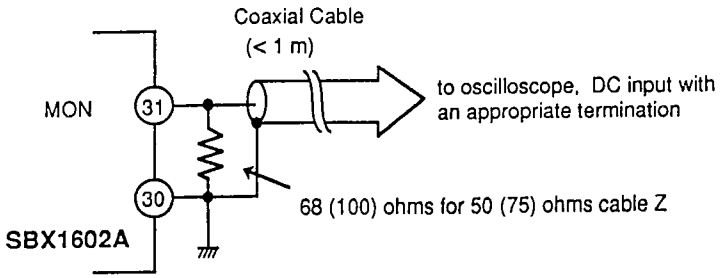


Fig. 9-4. Eye monitoring

9-4. Digital input

DIX (pin 33) and DIY (pin 34) comprise a differential direct input prepared for ECL interface purposes within the same board or the same equipment. With this input DC component shall be maintained and the logic shall be maintained at "0" whenever no signal or a meaningless signal appears at the input.

Also, while the analog input is in use, digital input must be kept "quiet" in order to avoid possible errors caused by cross-talk. This cross-talk problem naturally gets most severe when the analog input cable length is close to the limit of the transmission capability.

9-5. Input selection

Input signal selection (analog or digital) is made by ADS (pin 32). When ADS is kept at "L" or open (default), analog input is selected.

9-6. Phase locked loop (PLL)

The built-in PLL serves to generate the internal serial clock signal as well as to regenerate the serial data. A block diagram of the PLL employed is shown in Fig. 9-5.

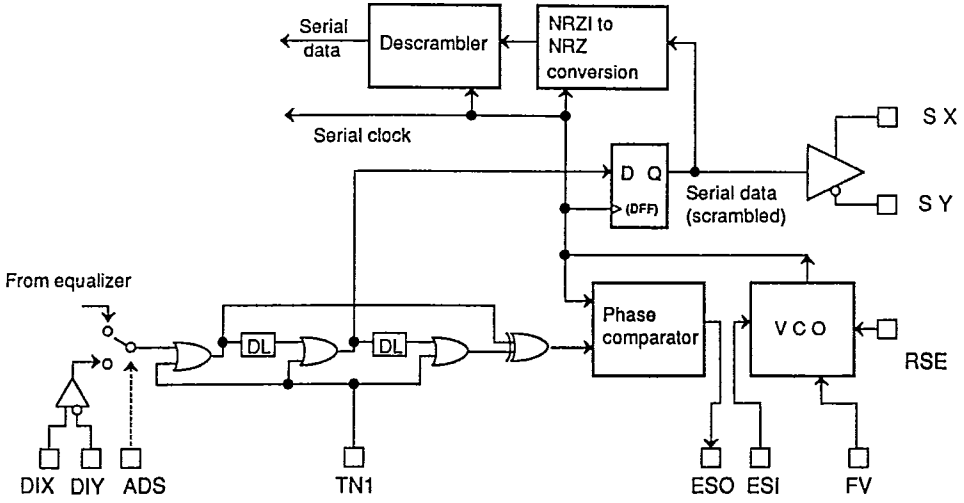


Fig. 9-5. Serial data input and PLL block

There are some nodes associated with the PLL. The function of each of nodes is given below:

In Fig. 9-5, ESO (pin 1) is an output of the phase comparator and ESI (pin 37) is an input of the VCO both of which are made available for product test purposes.

Since the VCO employed has a very high sensitivity, those two nodes must be connected with a shortest distance and a minimum area of conductor on the printed circuit board. Encircling those two nodes by a ground guardring is an efficient method to prevent errors caused by an "antenna effect".

FV (pin 36) is a node to control the free run frequency of the VCO.

RSE (pin 22) is a node to select the VCO free run frequency range. If the node is maintained at "logical H", a nominal bit rate from 140MHz to 270MHz is covered while "L" covers from 100MHz to 145MHz.

TN1 (pin 6) is provided to switch the PLL circuit into a test mode where the VCO frequency can be freely varied in terms of a control voltage given between FV and V_{EE} (–5V power supply). In practice, TN1 is also used to avoid a PLL mislock the transitional period when power is supplied. Fig. 9-6. shows such an arrangement.

9-7. VCO temperature characteristics

Although the VCO temperature characteristics are optimized for around 270MHz, a compensation in terms of an external diode as shown in Fig. 9-7. is recommended, particularly if the chip is used for the D2 PAL bit rate.

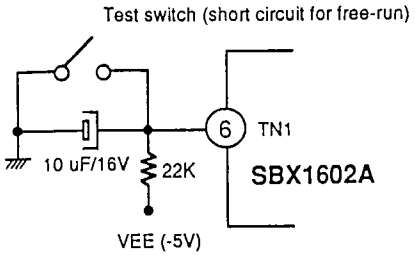


Fig. 9-6. Transient absorber time-constant

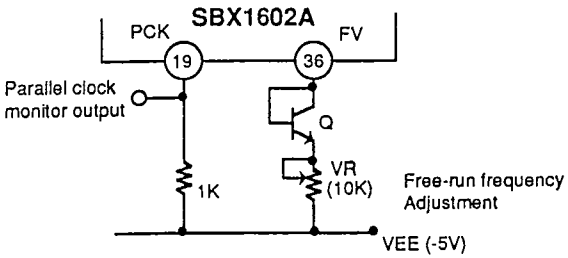


Fig. 9-7. Compensation on VCO temperature characteristics

9-8. NRZI to NRZ conversion

Following the data acquisition in the PLL block, the recovered NRZI data is converted to NRZ data according to the scheme shown in Fig. 9-8.

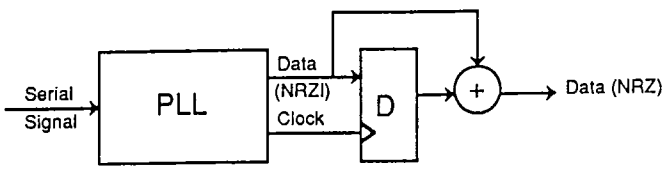


Fig. 9-8. NRZI to NRZ conversion

9-9. Descrambler

The output signal of the NRZI to NRZ converter is then descrambled by a multiplication of G (x)=X^9+X^4+1 as shown in Fig. 9-9 (a).

In a similar manner to that of the scrambler in SBX1601A, the actual descrambler employed is slightly different in order to take a fully pipe-lined structure as shown in Fig. 9-9 (b).

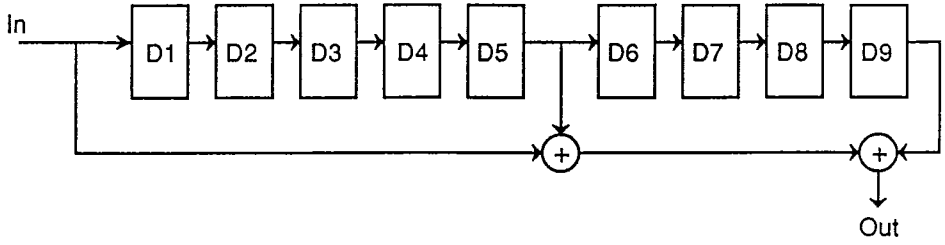


Fig. 9-9 (a). X^9+X^4+1 descrambler

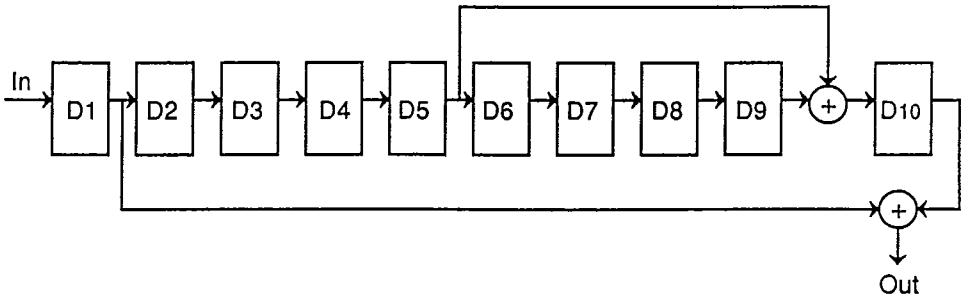


Fig. 9-9 (b). Actual X^9+X^4+1 descrambler

9-10. Serial to parallel conversion

Descrambled data is put into a 30 bits shift register to detect the SYNC word (TRS). When the content of the register gets 3FF, 000, 000 (Hex) or 1111111111, 0000000000, 0000000000 in an outgoing order, SYNC detection is made and the phase of an internal counter (1/10) is set such that each parallel bit can appear at the right place of the parallel output. The parallel data is taken from the last 10 bits of the shift register and passed through buffer amplifiers.

9-11. Parallel clock and data

The parallel clock and data logic level is nearly identical to that of ECL except that the suggested pull down resistors are 1kΩ . The same applies to EVR (pin 21) which is the reference potential of the parallel clock and data for line-drivers or for ECL/TTL translators. The rising edge of the parallel clock is located at the center of the parallel data window within a tolerance given.

9-12. Reclocked output

SBX1602A may be used as a repeater. The reclocked output, providing characteristics almost identical to the serial output of SBX1601A is available from SX (pin4) and SY (pin 3).

When the reclocked output is used, it is recommended not to use the parallel outputs simultaneously (data and clock) in order to avoid possible logic errors caused by an excessively high temperature which may result from additional power dissipation created by the reclocked output circuit under certain environmental conditions.

If, for the sake of a design convenience, both reclocked and parallel outputs are to be used, the ambient temperature has to be kept as low as possible or, at least, the airflow around SBX1602A must be carefully considered. In addition, it is recommended to put 220 Ω resistors on all parallel outputs including the clock as shown in Fig. 9-10. This reduces the magnitude of the spike current resulting from the parallel output circuits inside the chip and helps reduce the probability of logic errors at high temperature.

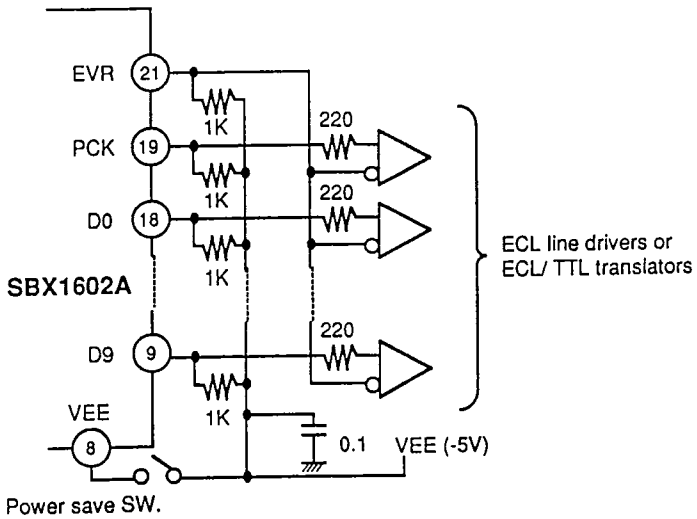


Fig. 9-10. A suggested parallel clock/data output circuit

9-13. Power saving in repeater mode

Since the parallel output is not always required for a reclocked repeater, the chip has been designed such that the unnecessary parallel logic circuit can be disabled by disconnecting pin 8, one of VEEs, from the power supply. With this arrangement the power dissipation is reducible to about 45 percent of that of the fully functional mode.

In practice, a test switch should be provided so that some parallel signals may be available during adjustment procedures as shown in Fig. 9-10.

10. Adjustments and Performance Checks

10-1. VCO free-run frequency adjustment

In order to assure a wide operational range despite changes of various parameters, the free-run frequency of the VCO shall be adjusted in the following manner:

(1) Keep the receiver, including the SBX1602A and associated circuits, switched on for at least 5 to 10 minutes in order to stabilize the thermal situation.

(2) Close the switch connected to TN1 in Fig. 9-6. to maintain TN1 at ground potential and confirm that the PLL of the chip is set for free-run by changing the value of VR in Fig. 9-7.

(3) Referring to Fig. 9-7, adjust the VR so that a frequency counter connected PCK can indicates,

f (bit rate frequency) ± 1%

at room temperature.

10-2. Data presence check

Prepare an oscilloscope input for DC, 1V/div, and check if the output of DPR (pin 35) gets high (closer to the ground potential) only when a signal is given at either (analog or digital) input. Since DPR output impedance is very high and only capable of switching CMOS input, a buffer amplifier or a CMOS gate circuit being connected between GND and V_{EE} must be added if it is used other than for monitoring purpose.

10-3. SYNC detection check

When a receiver using SBX1602A is properly implemented and adjusted, the health of the implementation can be checked simply by looking at SYN (pin 20) output while an encoded signal is present at the input.

SYN is an output of a flip-flop which toggles at each detection of TRS at the SYNC detector. Since the 4:2:2 signal contains two kinds of TRSs, SAV and EAV, when the output of SYN is observed by an oscilloscope it looks like either case A or case B as shown in Fig. 10-1. depending upon the initial condition of the Flip-Flop.

When bit errors are occurring somewhere in the transmission path, SYN output is affected and looks like as shown in case C.

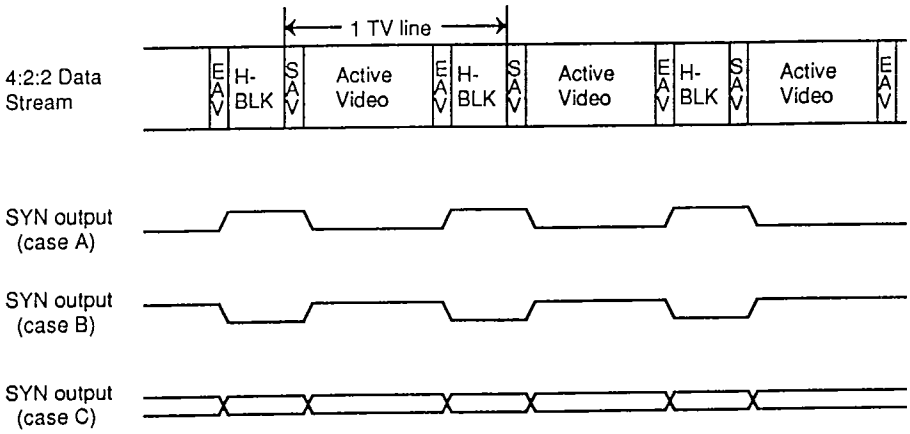


Fig. 10-1. SYNC output in 4:2:2 case (not to scale)

Fig. 10-2. illustrates the case for 4 fsc (D2 NTSC and PAL)

Differing from the 4:2:2 case, SYN output has an equal mark and space ratio due to the periodic occurrence (once per one TV line) of the TRS detection. However, tramsmission path bit errors will cause the SYN output to appear similar to the 4:2:2 case.

If SYN signal is used other than for monitoring purposes, buffering similar to that of DPR is required due to the high impedance nature of SYN output.

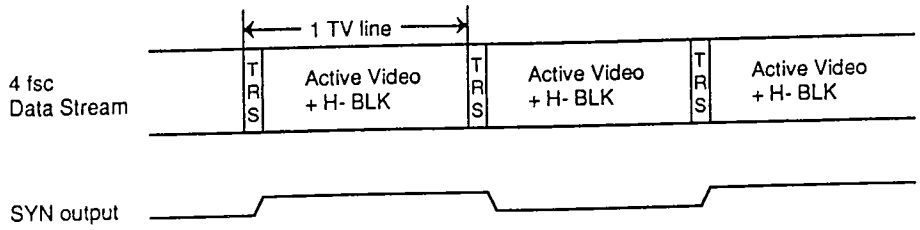


Fig. 10-2. SYNC output in 4 fsc case (not to scale)

10-4. Using particular codes to check overall performance

Although the scrambling method employed in the proposed SMPTE standard effectively randomizes the incoming data and puts out a signal with a nearly uniform spectrum, there still exist some combinations of codes that give somewhat unfriendly conditions to the transmission path in terms of low frequency component or of a long run without any transitions.

As shown in Fig. 10-3, it is known that if the code words 300, 198 (hex, 10 bit) are given alternately to the parallel input of the encodes, the largest amount of DC component (nearly one TV line period) can be produced at some place with a certain probability. (such a sequence is, however, destroyed when different data is input to the encoder.)

Even with such signals, error free reception is possible with the SBX1602A if a proper implementation is made (Refer to Section 12 for a recommended circuit).

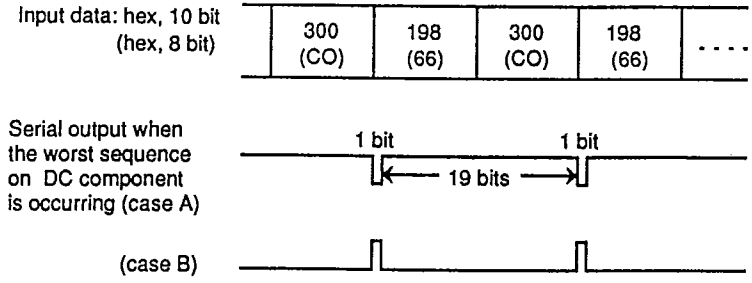


Fig. 10-3. Particular data words for checking equalization and AGC time-constant

Another particular combination of words, but with a different nature, is 200, 110 (hex, 10 bit) which can generate the sequence which is most vulnerable* to bit slip of nearly one TV line period. Fig. 10-4. illustrates such a situation. Similar to the previous case, the worst sequence stops upon an arrival of a data other than the alternating 200, 110 at the input of the encoder.

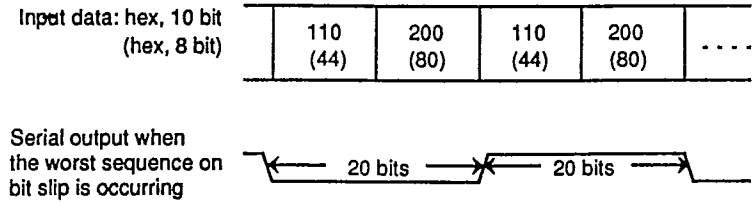


Fig. 10-4. Particular data words for checking PLL bit slip

* Strictly speaking the longest isolated run is 38 clocks for 4:2:2 and 43 clocks for 4 fsc NTSC and PAL. However, the above sequence generally shows the most critical situation for the bit slip problem.

Note: Actually there exists a family of such particular code as above described. They will, however, create an identical sequence in the serial domain since the difference amongst the family is merely which bit is regarded as the start bit of a word.

11. Characteristics of Key Parameters

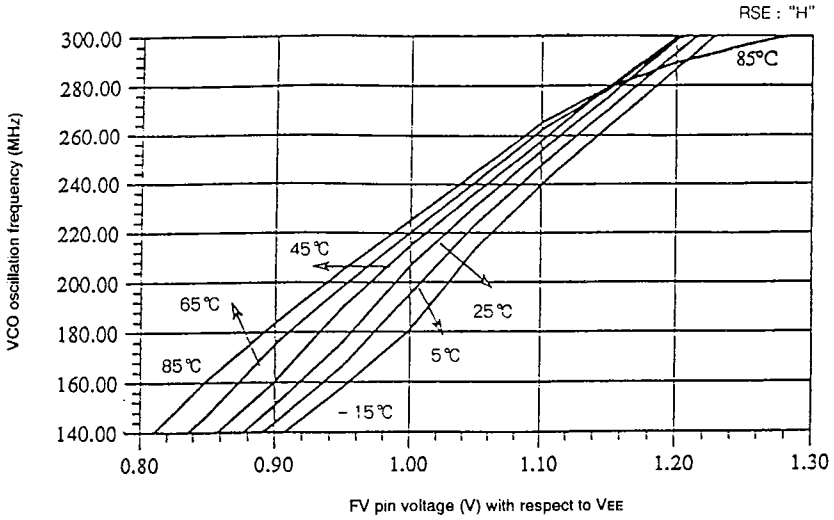


Fig. 11-1. VCO oscillation frequency vs. control voltage at high rate

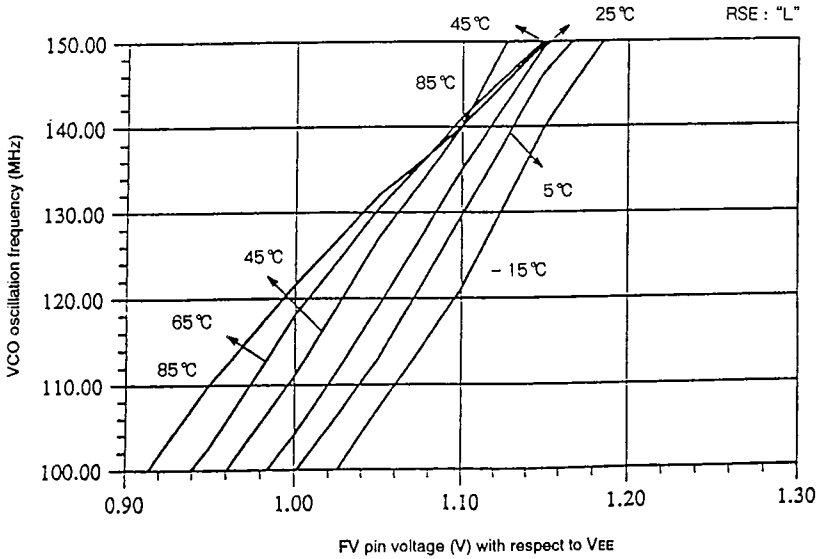


Fig. 11-2. VCO oscillation frequency vs. control voltage at low rate

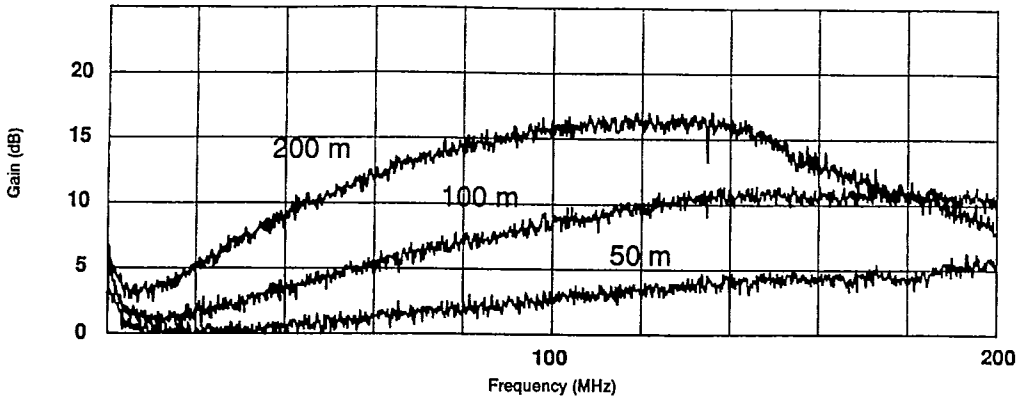
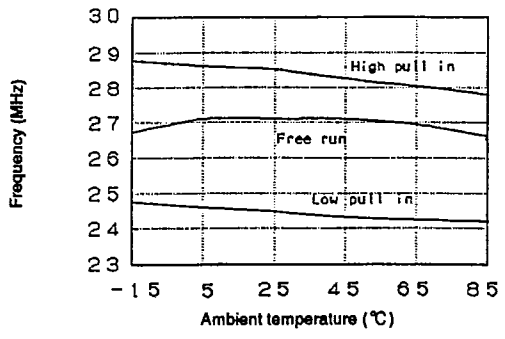
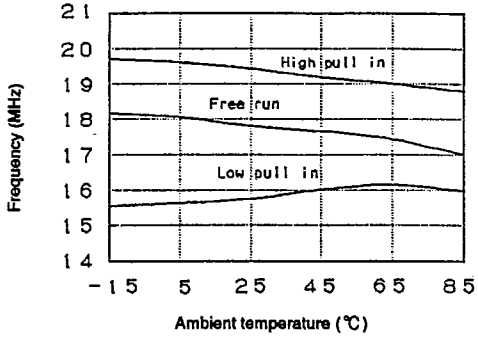


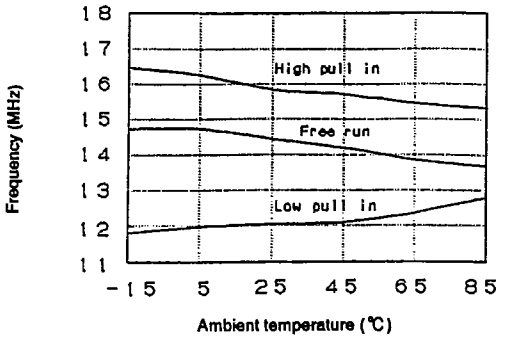
Fig.11-3. An example of equalizer characteristics using 5C-2V coaxial cable with respect to the gain for 0.5 meter



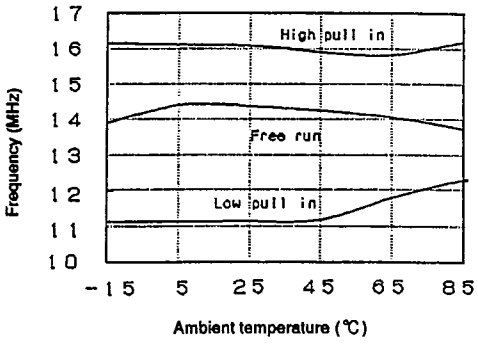
(a) at 270 Mb/sec (RSE="H")



(b) at 177 Mb/sec (RSE="H")



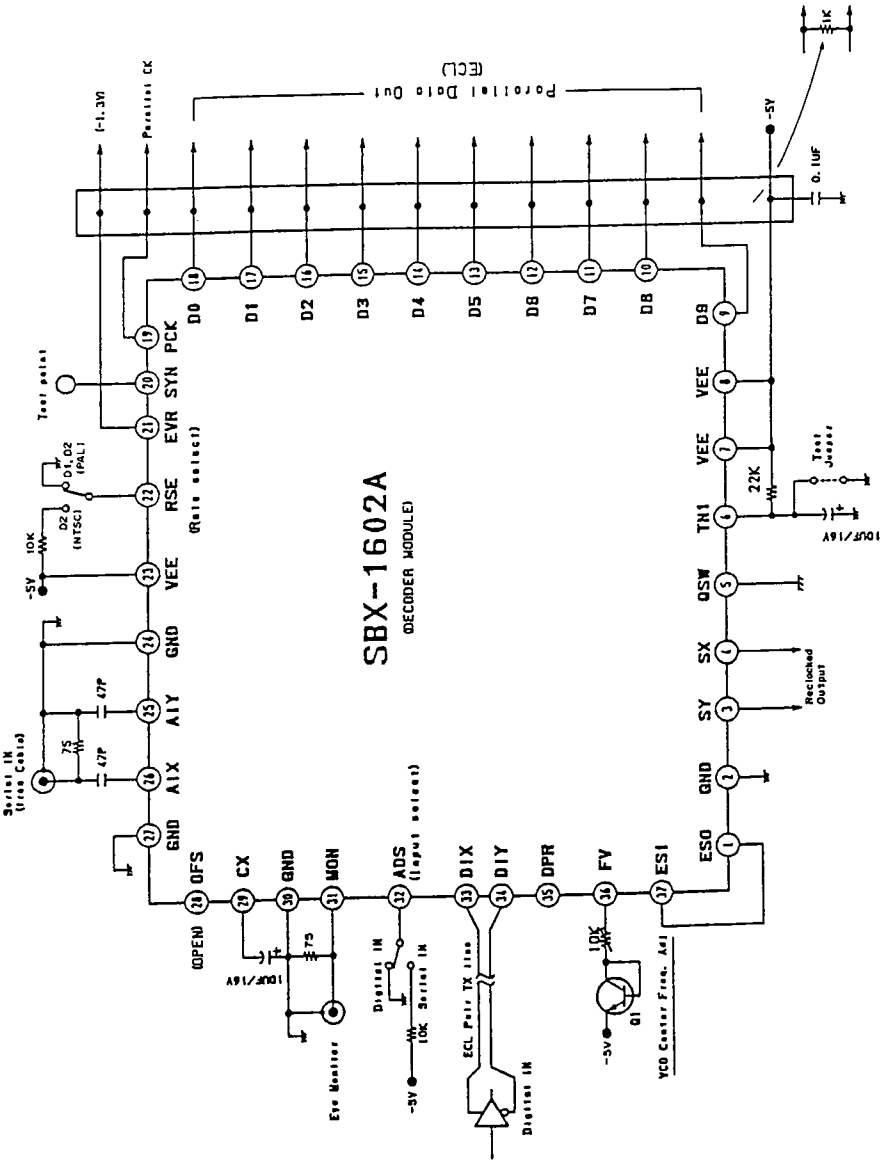
(c) at 143 Mb/sec (RSE="H")



(d) at 143 Mb/sec (RSE="L")

Fig. 11-4. Pull-in range and free-run characteristics of the PLL

12. Recommended Circuit for SBX-1602A



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

13. Markings

Markings and their meanings are as shown below.