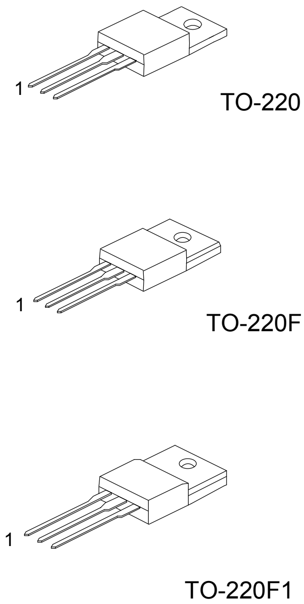
500V N-CHANNEL MOSFET



■ DESCRIPTION

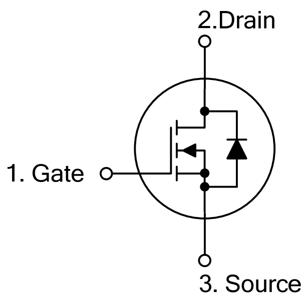
The UTC **13N50** is an N-Channel enhancement mode power MOSFET. The device adopts planar stripe and uses DMOS technology to minimize and provide lower on-state resistance and faster switching speed. It can also withstand high energy pulse under the avalanche and commutation mode conditions.

The UTC **13N50** is ideally suitable for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge topology.

■ FEATURES

* $R_{DS(ON)}$ =0.48Ω @V_{GS} = 10 V
* Ultra low gate charge (typical 43 nC)
* Low reverse transfer Capacitance (C_{RSS} = typical 20pF)
* Fast switching capability
* Avalanche energy tested
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
13N50L-TA3-T	13N50G-TA3-T	TO-220	G	D	S	Tube
13N50L-TF3-T	13N50G-TF3-T	TO-220F	G	D	S	Tube
13N50L- TF1-T	13N50G-TF1-T	TO-220F1	G	D	S	Tube

13N50L-TA3-T	
(1) Packing Type	(1) T: Tube
(2) Package Type	(2) TA3: TO-220, TF3: TO-220F, TF1:TO-220F1
(3) Lead Free	(3) L: Lead Free, G: Halogen Free

■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	±30	V
Continuous Drain Current		I_D	13	A
Pulsed Drain Current (Note 2)		I_{DM}	52	A
Avalanche Current (Note 2)		I_{AR}	13	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	810	mJ
Repetitive Avalanche Energy (Note 2)		E_{AR}	17	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation (T_C=25°C)	TO-220	P_D	168	W
	TO-220F		48	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating : Pulse width limited by maximum junction temperature
3. L = 9.3mA, I_{AS} = 13A, V_{DD} = 50V, R_G= 25Ω ,Starting T_J = 25°C
4. I_{SD}≤13.A, di/dt ≤200A/μs, V_{DD}≤ BV_{DSS}, Starting T_J= 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	°C/W
	TO-220F		62.5	°C/W
Junction to Case	TO-220	θ_{JC}	0.74	°C/W
	TO-220F		2.58	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500			V
Drain-Source Leakage Current	I_{DSS}	V_{DS} = 500V, V_{GS} = 0V			1	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 30V, V_{DS} = 0V			100	nA
		V_{GS} = -30V, V_{DS} = 0V			-100	nA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	I_D = 250μA Referenced to 25°C		0.5		V/°C
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 6.5A		0.33	0.43	Ω
Forward Transconductance	g_{FS}	V_{DS}=50V, I_D=6.25A (Note 1)		10		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz		1800	2300	pF
Output Capacitance	C_{OSS}			245	320	pF
Reverse Transfer Capacitance	C_{RSS}			25	35	pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} =250V, I_D =13A R_G =25Ω (Note 1,2)		40	90	nS
Turn-On Rise Time	t_R			140	290	nS
Turn-Off Delay Time	$t_{D(OFF)}$			100	210	nS
Turn-Off Fall Time	t_F			85	180	nS
Total Gate Charge	Q_G	V_{DS}=400V, I_D=13A, V_{GS}=10 V (Note 1, 2)		45	60	nC
Gate-Source Charge	Q_{GS}			11		nC
Gate-Drain Charge	Q_{GD}			22		nC

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = 13 A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				13	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				52	A
Reverse Recovery Time	t_{RR}	V_{GS} = 0V, I_S = 13A,		290		nS
Reverse Recovery Charge	Q_{RR}	dI_F / dt = 100A/μs (Note 1)		2.6		μC

Notes: 1. Pulse Test : Pulse width≤300μs, Duty cycle≤2%

2. Essentially independent of operating ambient temperature

■ TEST CIRCUITS AND WAVEFORMS

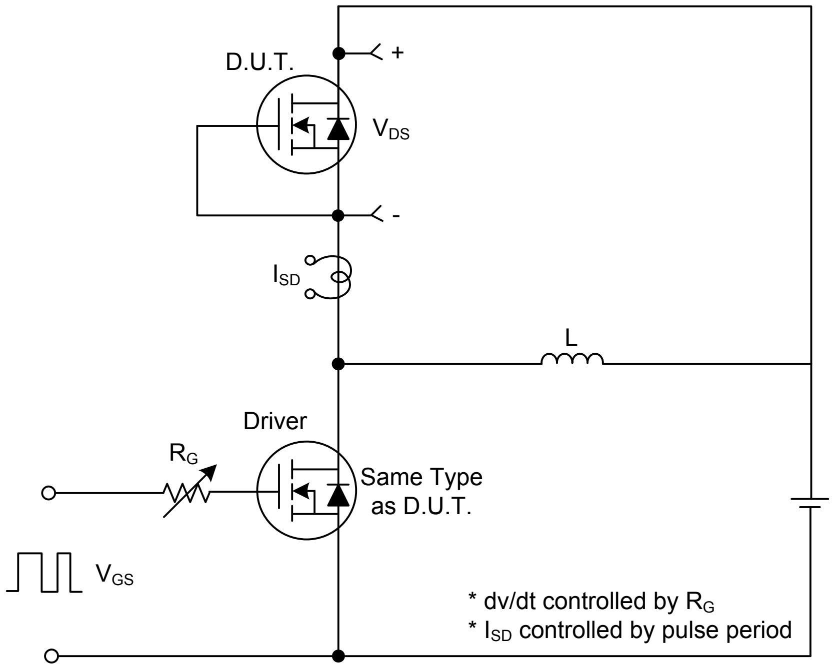


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

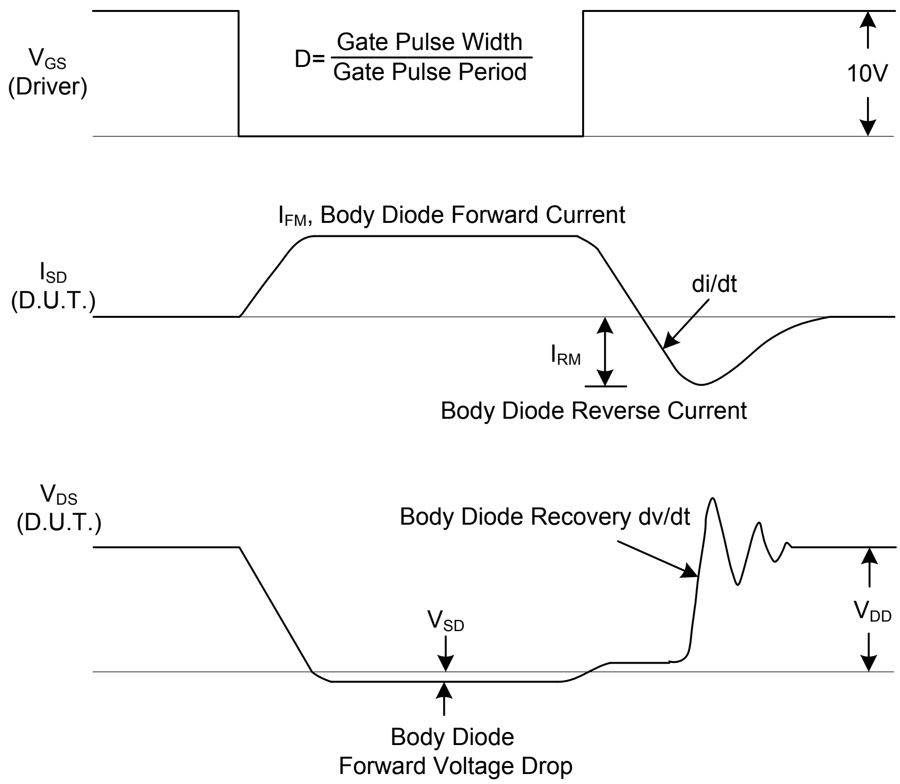


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

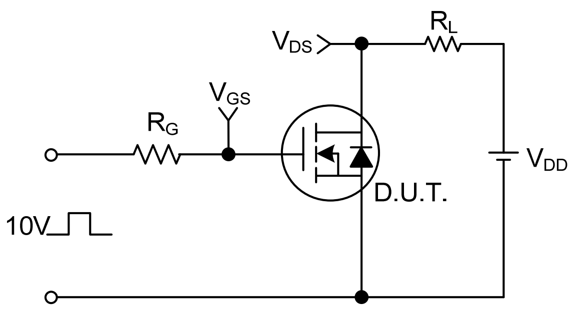


Fig. 2A Switching Test Circuit

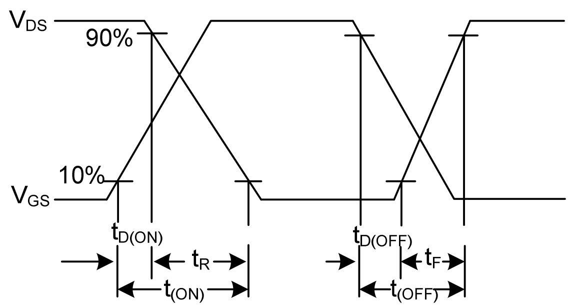


Fig.2B Switching Waveforms

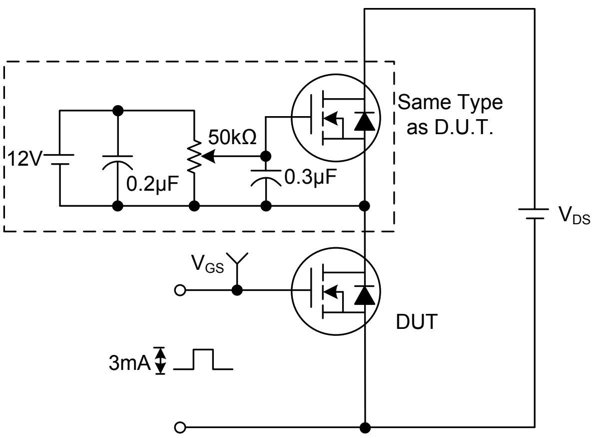


Fig. 3A Gate Charge Test Circuit

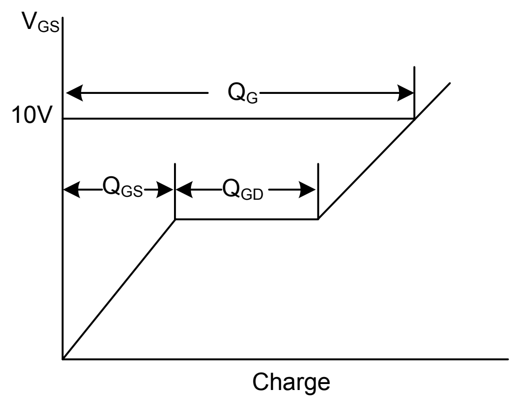


Fig. 3B Gate Charge Waveform

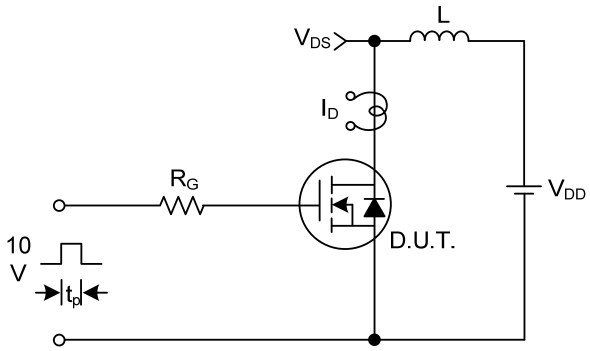


Fig. 4A Unclamped Inductive Switching Test Circuit

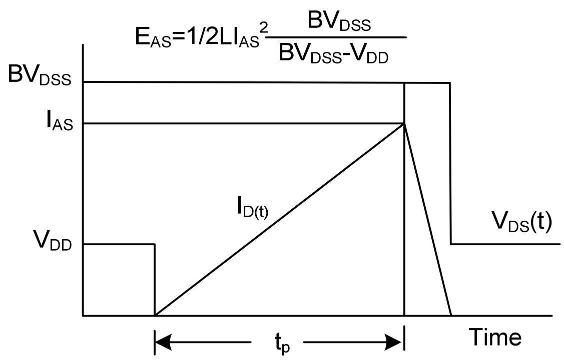


Fig. 4B Unclamped Inductive Switching Waveforms