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PART NO : GG1206N8SKN1T
FOR MESSRS : _____

CONTENTS

Accepted by : _____

Proposed by : _____
Date : 10,25,2002

RECORD OF REVISION

DATE	PAGE	SUMMARY

3. GENERAL SPECIFICATIONS AND MECHANICAL DATA

3.1 GENERAL SPECIFICATIONS

PLEASE REFER TO:

”CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS (SP-10-000)”.

3.2 THIS INDIVIDUAL SPECIFICATION IS PRIOR TO GENERAL SPECIFICATIONS.

3.3 MECHANICAL DATA

(1) NUMBER OF DOTS ---------- 128W× 64H DOTS

(2) MODULE SIZE ---------- 71.0W× 59.3H× 2.0D (MAX.) mm

(3) VEWING AREA ---------- 67.0W× 37.0H mm

(4)DISPLAY AREA ---------- 64.41W× 30.69Hmm

(5) DOT SIZE ---------- 0.45W× 0.45H mm

(6) DOT PITCH ---------- 0.48W× 0.48H mm

(7) VIEWING DIRECTION ---------- 6 O’CLOCK

(8) LCD COLOR ---------- STN, GRAY, TRANSFLECTIVE

4. ABSOLUTE MAXIMUM RATINGS

4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT	COMMENT
POWER SUPPLY FOR LOGIC	VDD-VSS	2.4	6.0	V	
INPUT VOLTAGE	VI	VSS	VDD	V	
STATIC ELECTRICITY	———	——	100	V	NOTE (1)

NOTE (1) : TEST METHOD AND CONDITIONS AFTER CHARGING UP 200PF CAPACITOR BY STATED VOLTAGE, THE CAPACITOR IS CONNECTED WITH INTERFACE PINS OF THE MODULE.

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RAINGS

ITEM	OPERATING		STORAGE		COMMENT
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	0℃	50℃	-20℃	60℃	NOTE (2)
HUMIDITY	NOTE (3)		NOTE (3)		WITHOUT CONDENSATION
VIBRATION	——	4.9 m/s^2 (0.5G)	——	19.6 m/s^2 (2G)	10~300HZ XYZ DIRECTIONS 1 Hr. EACH
SHOCK	——	29.4 m/s^2 (3G)	——	49.0 m/s^2 (5G)	10 ms XYZ DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE (2) : Ta AT -20℃ : 48HR MAX.
Ta AT 60℃ : 168HR MAX.

NOTE (3) : Ta ≦ 40℃ : 90% RH MAX.
Ta ＞ 40℃ : ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF 90%RH AT 40℃. (50% RH AT 50℃)

5. ELECTRICAL AND OPTICAL CHARACTERISTICS

5.1 ELECRICAL CHARACTERISTICS

Ta = 25℃ VDD = 2.4V~6.0V

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
LOGIC CIRCUIT POWER SUPPLY VOLTAGE	VDD-VSS	———	2.4	------	6.0	V
INPUT VOLTAGE	VOH	NOTE (1)	0.7*VDD	——	VDD	V
INPUT VOLTAGE	VOL	NOTE (1)	GND	——	0.3*VDD	V
LOGIC CIRCUIT POWER SUPPLY CURRENT	IDD	VDD-VSS =5.0V	——	1.0	3.0	mA
RECOMMENDED LCD DRIVING VOLTAGE (NOTE 1)	VDD - VO DUTY = 1/64 § = 10°	Ta = 0℃	——	-------	——	V
		Ta = 25℃	——	(8.8)	——	V
		Ta = 50℃	——	------	——	V

NOTE (1): CS1, CS2, R/W, D/I, DB0~DB7, E, RST

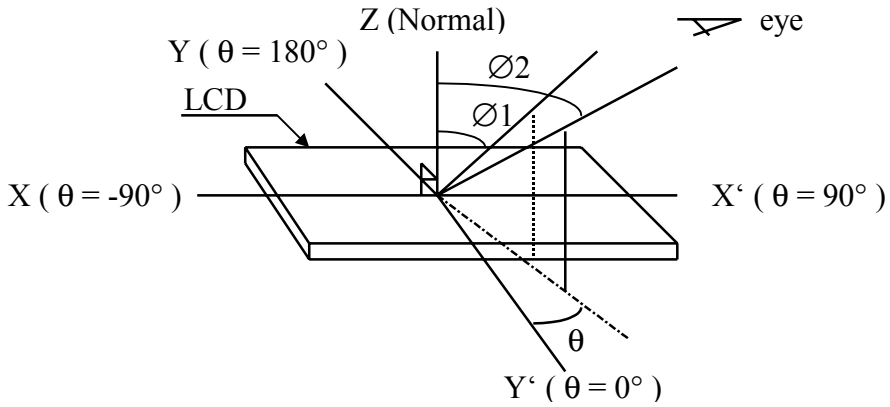
NOTE (2): RECOMMENDED LCD DRIVING VOLTAGE MAY FLUCTUATE ABOUT ± 0.5V BY EACH MODULE.

5.2 OPTICAL CHARACTERISTICS

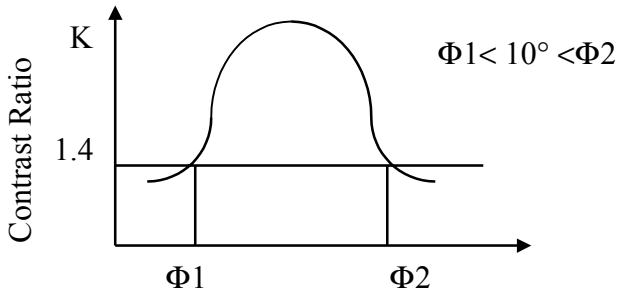
Ta = 25°C VDD = 2.4V~6.0V

I T E M	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
VIEWING AREA	Φ2-Φ1	K≧ 1.4	20	——	——	deg.
CONTRAST RATIO	K	Φ = 10° θ = 0°	——	4	——	——
RESPONSE TIME	tr(rise)	Φ = 10° θ = 0°	——	250	350	ms
	tf(fall)	Φ = 10° θ = 0°	——	300	400	ms

NOTE (1): DEFINITION OF θ AND Φ



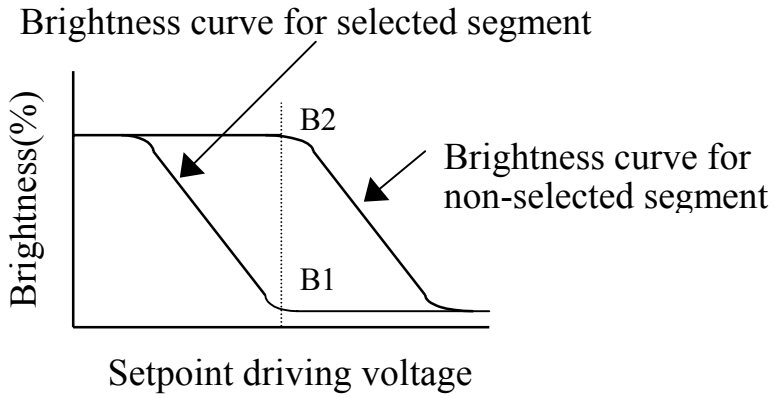
NOTE (2): DEFINITION OF VIEWING ANGLE Φ1 AND Φ2



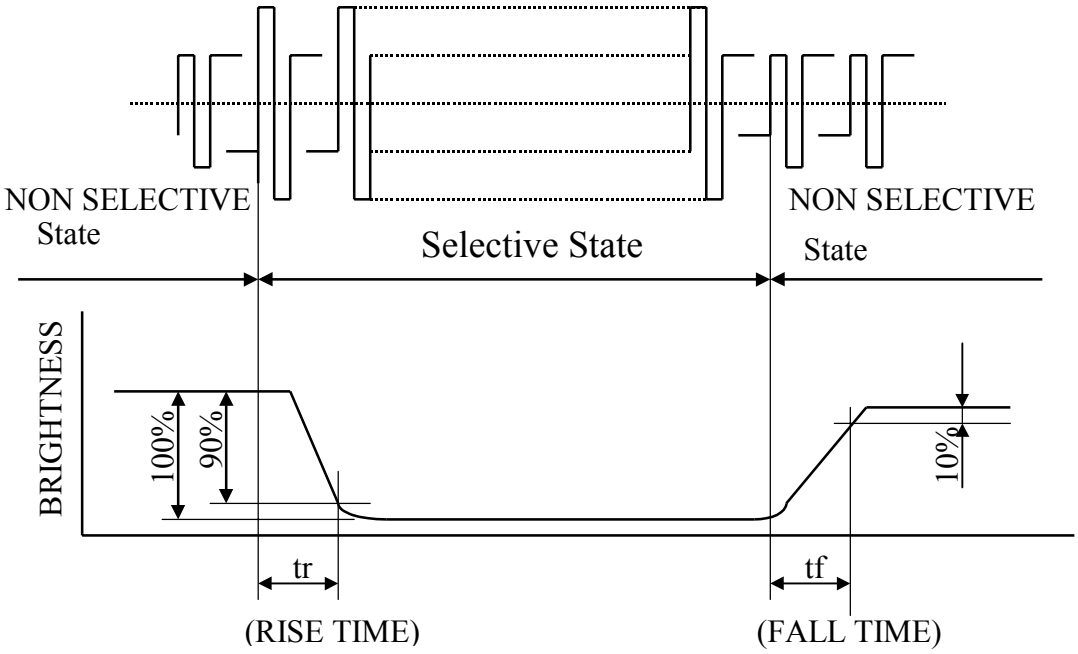
Viewing Angle

NOTE (3): DEFINITION OF CONTRAST"K"

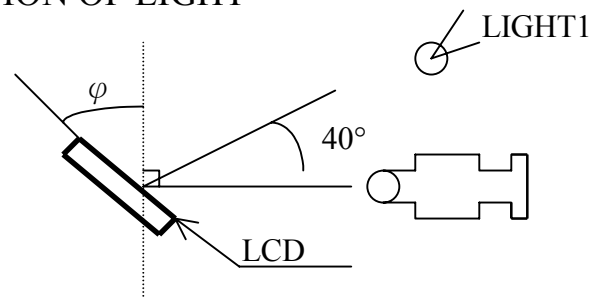
$$K = \frac{\text{Brightness of non-selected segment (B2)}}{\text{Brightness of selected segment (B1)}}$$



NOTE (4): DEFINITION OF OPTICAL RESPONSE

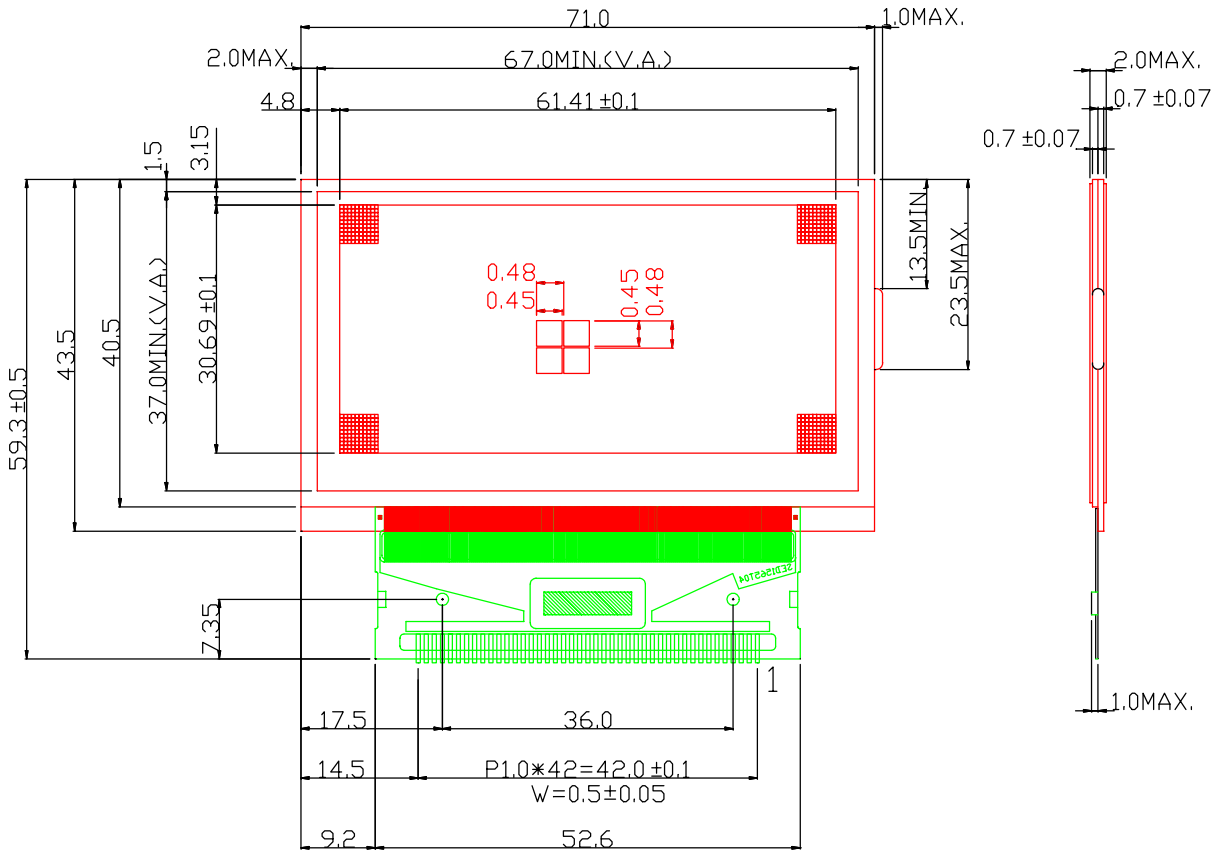


NOTE (5): POSITION OF LIGHT



VIEWING ANGLE

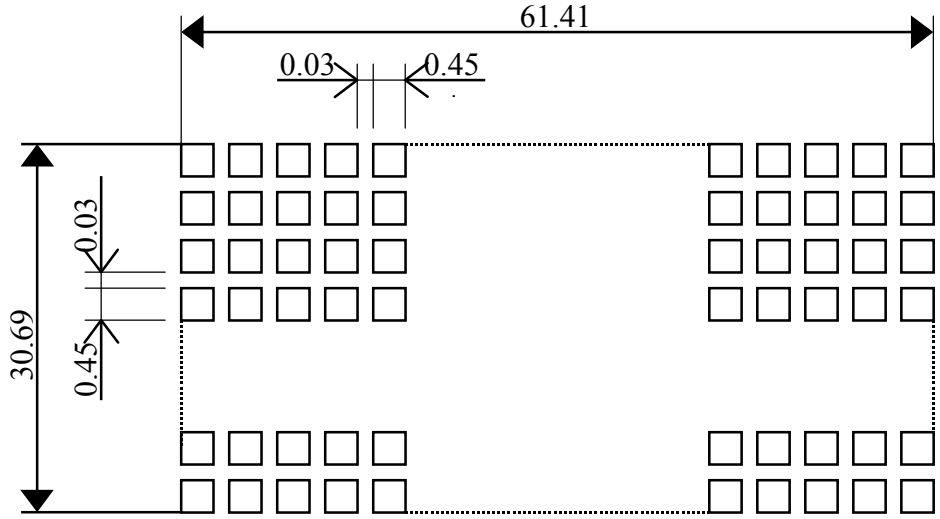
6. OUTLINE DIMENSION



PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SYMBOL	N.C	FR	CL	DOF	CS1	CS2	RES	A0	R/W	E	D0	D1	D2	D3	D4	D5
PIN	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
SYMBOL	D6	D7	VDD	VSS	VSS2	VOUT	CAP3-	CAP1+	CAP1-	CAP2-	CAP2+	VRS	VDD	V1	V2	V3
PIN	33	34	35	36	37	38	39	40	41	42	43					
SYMBOL	V4	V5	VR	VDD	M/S	CLS	C86	P/S	HPM	IRS	NC					

NO SPECIFIED TOLERANCE: ±0.3
NUIT : mm
SCALE : NTS

NOTE (1): DETAIL DRAWING OF MATRIX PATTERN



INTERFACE CONNECTOR PIN

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>COM0
to
COM31</td><td>O</td><td>These are te liquid crystal common drive output.
<table>
<tr><td>Part No.</td><td>COM</td><td></td><td>Part NO.</td><td></td></tr>
<tr><td>SED1565*</td><td>COM0~COM63</td><td></td><td>SED1565*</td><td>64</td></tr>
<tr><td>SED1566*</td><td>COM0~COM47</td><td></td><td>SED1566*</td><td>48</td></tr>
<tr><td>SED1567*</td><td>COM0~COM31</td><td></td><td>SED1567*</td><td>32</td></tr>
</table>
Through a combination of the contents of the scan data and with the FR signal, a single level is selected from VDD,V1,V4,and V5
<table>
<tr><td>Scan Data</td><td>FR</td><td>Output Voltage</td></tr>
<tr><td>H</td><td>H</td><td>V5</td></tr>
<tr><td>H</td><td>L</td><td>VDD</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td>Power Save</td><td>----------</td><td>VDD</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>These ae the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.
When in master/slave mode , the same signal is output by both master and slave.</td></tr>
</table>

PIN NAME	I/O	FOUNCTION
VDD	POWER SUPPLY	Shared with the MPU power supply terminal Vcc
VSS	POWER SUPPLY	This is a 0V terminal connected to the system GND.
VSS2	POWER SUPPLY	This is the refernce power supply for the step-up voltage circuit for the liquid crystal drive.
VRS	POWER SUPPLY	This is the externally-input VREG power supply for the LCD power supply voltage regulator . These are only enabled for the models with theVREG external input option.
V1,V2 V3,V4 V5	POWER SUPPLY	This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or throgh changing the impedance using an op.amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. VDD(=V0)≥V1≥V2≥V3≥V4≥V5 Master operation :When the power supply turns ON , the internal power supply circuits produce the V1 to V4 voltage shown below. The voltage settings are selected using the LCD bias set command.
CAP1+	O	DC/DC voltage converter.Connect a capacitor between this terminal and the CAP1- terminal.
CAP1-	O	DC/DC voltage converter.Connect a capacitor between this terminal and the CAP1+ terminal.
CAP2+	O	DC/DC voltage converter.Connect a capacitor between this terminal and the CAP2- terminal.
CAP2-	O	DC/DC voltage converter.Connect a capacitor between this terminal and the CAP2+ terminal.
CAP3-	O	DC/DC voltage converter.Connect a capacitor between this terminal and the CAP1+ terminal.
VOUT	O	DC/DC voltage converter.Connect a capacitor between this terminal and Vss
VR	I	Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider . These are only enabled when the V5 voltage regulator internal resistors are not usde(IRS="L"). these cannot be used when the v5 voltage regulator internal resistors are used (IRS="H').
D7 to D0 (SI) (SCL)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit ot 16 bit standard MPU data bus. When the serial interface is selected (P/S="L"),then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance . When the chip select is inactive, D0 to D7 are set to high impedance.
A0	I	This is connect to the least significant bit of the normal MPU address bus,and it determines whether the data bits are data or a command. A0="H':Indicates that D0 to D7 are display data. A0="L":Idicates that D0 to D7 are control data.
/RES	I	When /RES is set to "L"the settings are initialized. The reset operation is performed by the /RES signal level.
/CS1,CS2	I	This is the chip select signal. When /CS1 ="L"and CS2="H",then the chip select becomes active, and data/command I/O is enable.
/RD,(E)	I	. When connected to an 8080 MPU ,this is active LOW. This pin is connected to the /RD signal of the 8080 MPU ,and the SED 1565 series data bus is in an output status when this signal is "L". . When connected to a 6800 Series MPU ,this is active HIGH . This is the 6800 Series MPU enable clock input termined.
/WR,(R/W)	I	. When connected to an 8080 MPU ,this is active LOW . This terminal connects to the 8080 MPU /WR signal .The signals on the data bus are latched at the rising edge of the /WR signal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. When R/W="H":Read. When R/W="L":Write.
C86	I	This is the MPUinterface switch terminal. C86="H":6800 Series MPU interface. C86="L":8080 MPU interface
P/S	I	This is the paralle data input/serial data input switch terminal. P/S="H":Parallel data input. P/S="L":Serial data input. The following applies depending on the P/S status:

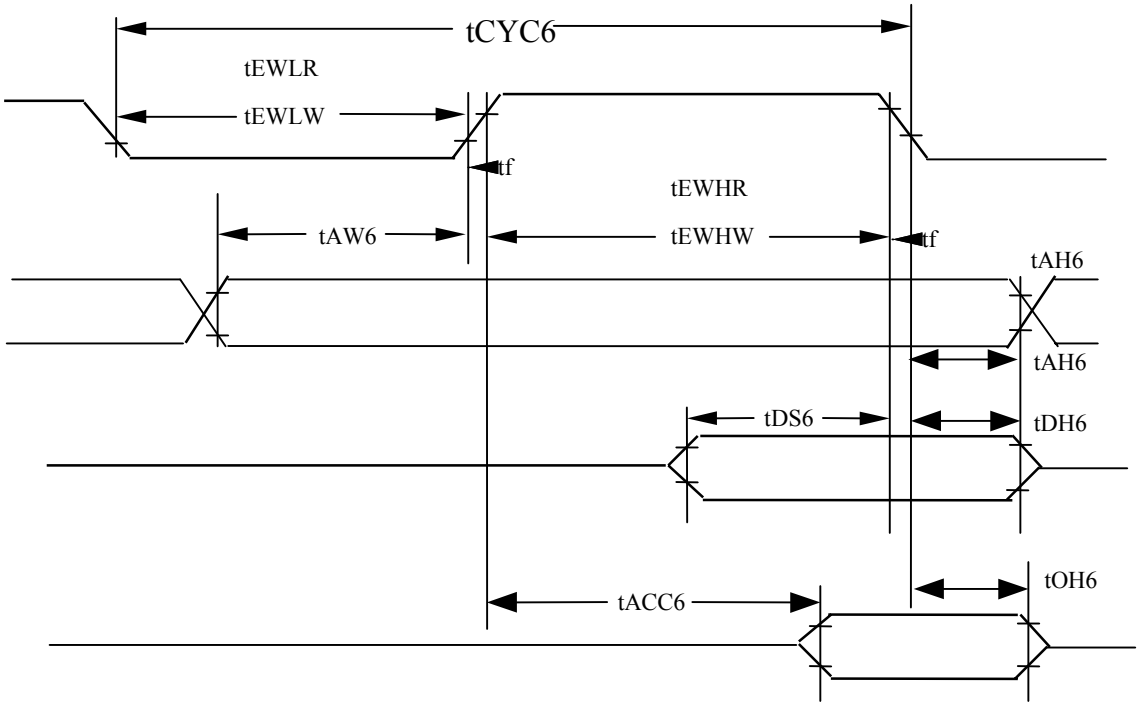
P/S	Data/Command	Data	Read/Write	Serial Clock
"H"	A0	D0 to D7	/RD,/WR	
"L"	A0	SI(D7)	Write only	SCL(D6)

When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H","L" or Open ./RD(E)and /WR(R/W)are fixed to either "H"or "L". With serial data input, RAM display data reading is not supported.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>CLS</td><td>I</td><td>Terminal to select whether or enable or disable the displa clock internal oscillator circuit.
CLS=“H”:Internal oscillator circuit is enabled
CLS=“L”:Internal oscillator circuit is disabled(requires external input)
When CLS=“L”,input the displayclock through the CL terminal.</td></tr>
<tr><td>M/S</td><td>I</td><td>This terminalselects the master/slave operation for the SED1565 Series chips. Master operation outputs the timing signals that are required for the LCD display , while slave operation inputs the timing signals required for the liquid crystal display ,synchronizing the liquid crystal display system.
M/S=“H”:Master operation M/S=“L”:Slave operation
The following is true depending on the M/S and CLS status:
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>DOF</th></tr>
<tr><td>“H”</td><td>“H”</td><td>Enable</td><td>Enable</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td></td><td>“L”</td><td>Disable</td><td>Enable</td><td>Iput</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>“L”</td><td>“H”</td><td>Disable</td><td>Disable</td><td>Iput</td><td>Iput</td><td>Output</td><td>Iput</td></tr>
<tr><td></td><td>“L”</td><td>Disable</td><td>Disable</td><td>Iput</td><td>Iput</td><td>Output</td><td>Iput</td></tr>
</table></td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the M/S and CLS status.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>“H”</td><td>“H”</td><td>Output</td></tr>
<tr><td></td><td>“L”</td><td>Input</td></tr>
<tr><td>“L”</td><td>“H”</td><td>Input</td></tr>
<tr><td></td><td>“L”</td><td>Input</td></tr>
</table>When the SED 1565 Series chips is used in master/slave mode,the various CL terminal must e connected.</td></tr>
<tr><td>FR</td><td>I/O</td><td>This is the liauid crystal alternating current signal I/O terminal.
M/S =“H”: Output M/S=“L”:Input
When the SED1565 Series chip is used in master/slave mode,the various FR terminals must be connected.</td></tr>
<tr><td>/DOF</td><td>I/O</td><td>This is the liquid crystal display blanking control terminal.
M/S=“H”:Output M/S=“L”:Input
When the SED1565 SERies chip used in master/slave mode ,the various /DOF terminal must be connected.</td></tr>
<tr><td>FRS</td><td>O</td><td>This is the output terminal for the static drive.
This is terminal is only enabled when the static indicator display is ON when in master operation mode,andis used in conjunction with the FR terminal.</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V5 voltage level adjustment.
IRS=“H”:Use the internal resistors
IRS=“L”:Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave opertion mode is selected.</td></tr>
<tr><td>/HPM</td><td>I</td><td>This is the power cotrol terminal for the power supply circuit for liquid crystal drive.
/HPM=“H”: Normal mode
/HPM=“L”:High power mode
This pin is enabled only when the master opertion mode is selected.
It is fixed to either “H” or “L” when the slave opertion mode is selected.</td></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>These are the liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal , a singale level is selected from VDD,V2,V3,and V5.
<table>
<tr><th>RAM DATA</th><th>FR</th><th colspan="2">Output Voltage</th></tr>
<tr><td></td><td></td><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>H</td><td>H</td><td>VDD</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>V5</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>VDD</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>V5</td></tr>
<tr><td>Power save</td><td>-----</td><td colspan="2">VDD</td></tr>
</table></td></tr>
</table>

Vss=-5.0V± 10%,Ta=-30~85℃

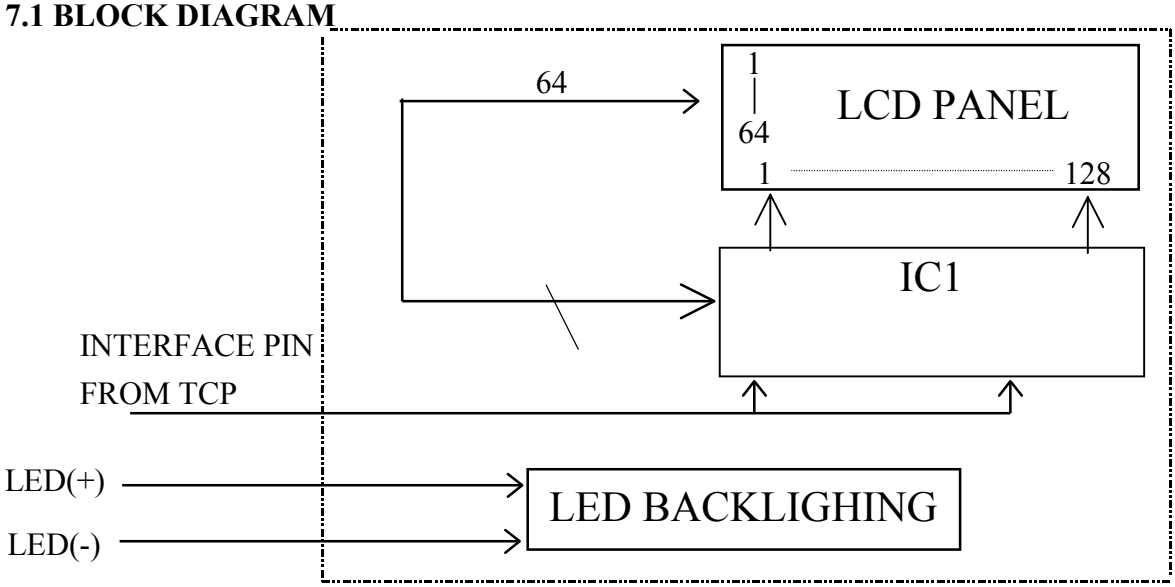
Item		Sgnal	Symbol	Conditions	Min.	Max.	Unit
System cycle time			tCYC6		200		ns
Address setup time		(A0)	tAW6		10		ns
address hold time		R/$\overline{W}$	tAH6		10		ns
Data setup time		D0-D7	tDS6		20		ns
Data hold time			tDH6		10		ns
Output disable time			tOH6	CL=100Pf	10	50	ns
Access time			tACC5			70	ns
Enable H pulse width	READ	E	tEWHR		77		ns
	WRITE		tEWHW		22		ns
Enable L pulse width	READ	E	tEWLR		117		ns
	WRITE		tEWLW		172		ns
Input signal change time			tr,tf			15	ns



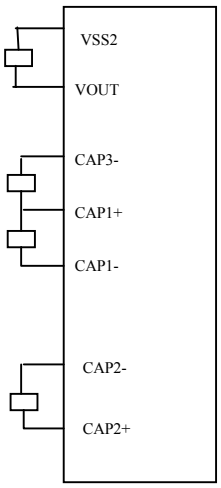
7. BLOCK DIAGRAM AND POWER SUPPLY

+

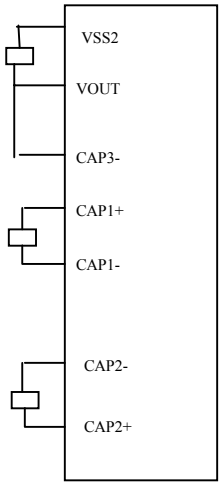
7.1 BLOCK DIAGRAM



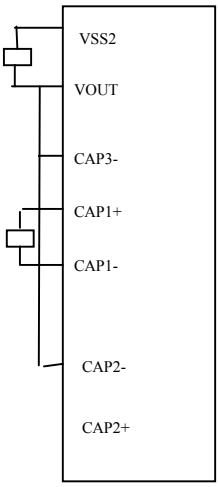
7.2 POWER SUPPLY FOR LCM



VDD=0V VSS2= -3V
VOUT=4*VSS2= -12V
4*STEP-UP VOLTAGE RELATIONSHIPS



VDD=0V VSS2= -3V
VOUT=3*VSS2= -9.0V
4*STEP-UP VOLTAGE RELATIONSHIPS



VDD=0V VSS2= -5V
VOUT=2*VSS2= -10
4*STEP-UP VOLTAGE RELATIONSHIPS

8. FUNCTION OF EACH BLOCK

● Selecting the interfaec type

With the SED1565 Serieschips,data transfers are done through an 8-bit bi-directional data bus (D7 to D0)or through a serial data input(SI). Through selecting the P/S terminal polarity to the "H" or "L" it is possible to select either parallel data input or serial data input as shown in Table1.

P/S	$\overline{CS1}$	$\overline{CS2}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5-D0
H:Parallel Input	$\overline{CS1}$	$\overline{CS2}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5-D0
L:Serial Input	CS1	$\overline{CS2}$	A0	----	----	----	SI	SCL	(Hz)

The Parallel interface

When the parallel interface has been selected (P/S="H"), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (as shown in Table 2) by selecting the C86 terminal to either "H" or to "L".

C86	MPU type	$\overline{CS1}$	$\overline{CS2}$	A0	$\overline{RD}$	$\overline{WR}$	D7 TO D0
HIGH	6800-SERIES	$\overline{CS1}$	$\overline{CS2}$	A0	E	R/$\overline{W}$	D7 TO D0
LOW	8080-SERIES	$\overline{CS1}$	$\overline{CS2}$	A0	$\overline{RD}$	$\overline{WR}$	D7 TO D0

Moreover, data bus signals are recognized by a combination of A0,RD(E),WR(R/W)signals,as shown in table3.

shared	6800 series	8080 Series		FUNTION
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	1	1	0	write control data (command)

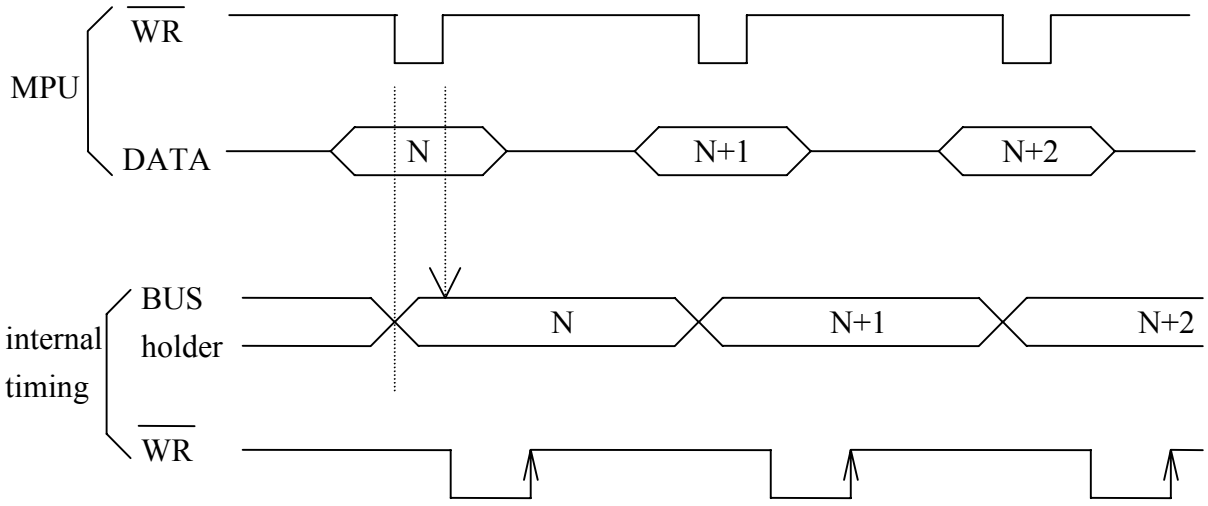
The Chip select

The SED1565 Series chips have two chip select terminals:CS1 and CS2. THE MPU interface is enabled only when CS1="L" and cs2="H" when the chip select is inactive,D0 to D7 enter a high impedance state, and the A0,RD,and WR inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

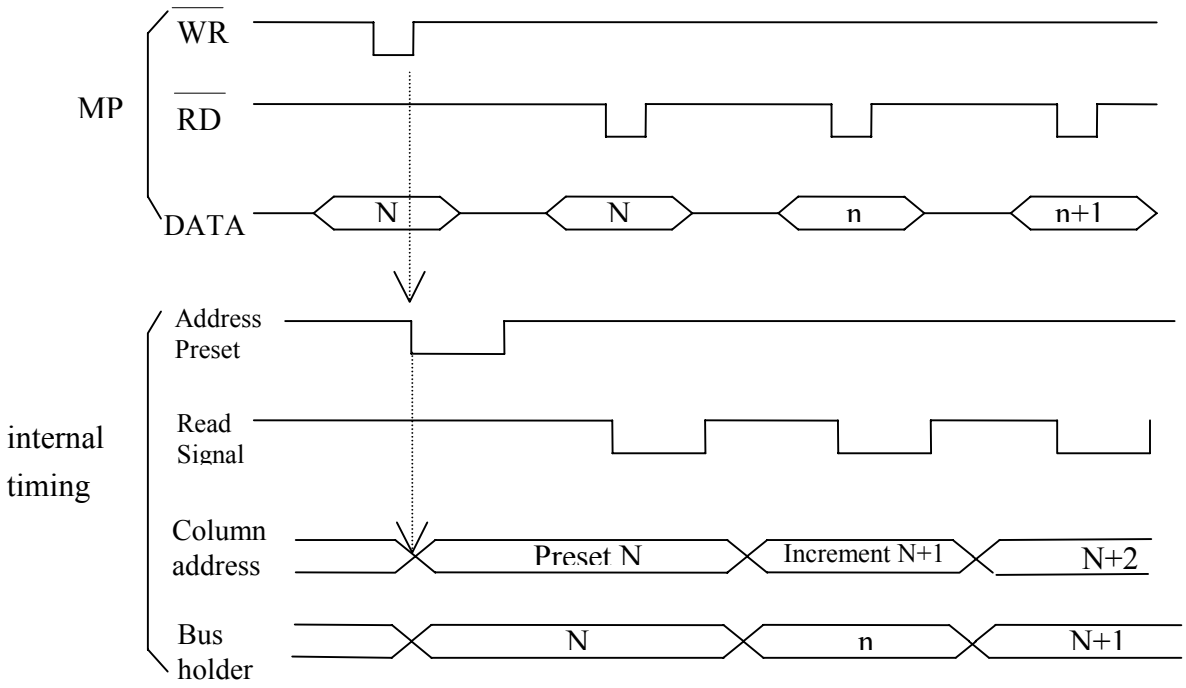
The Busy Flag

When the busy flag is "I" it indicates that the SED1565 Series chip is running internal processes,and at this time no command aside from a status read will be received . If the cycle time (t_{cyc}) is maintained, it is not necessary to check for this flag before each command.This makes vast improvements in MPU processing capabilities possible.

Write timing



Read timing



Address Set #n | Dummy Read | Data Read #n

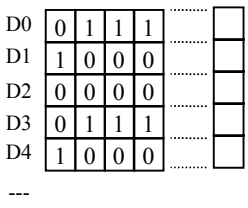
*There are constraints on the display data RAM read sequence. When an address set has been performed and is immediately follower by a read command,one must be cautious because the data that is output is not from the specified address; the data from the specified address is output the second time that the data is read.Consequently,one dummy read cycle is required after an has been set or after a write cycle.

Display Data RAM

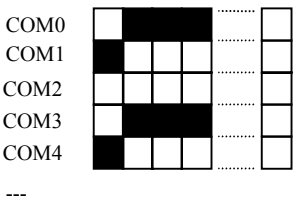
Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65(8 page*8bit+1)*132 it structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3,the D7 to D0 display data from the MPU corresponds to the liguid crystal display common direction, there are few constraints at the time of display data transfer when multiple SED1565 series chips are used, thus and display structures can be created easily and with a high degree of freedom.

Moreover, reading form and writing to the display RAM from the MPU side is performed through the I/O buffer,which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is assessed asynchronously during liquid crystal display , it will not cause adverse effects on the display(such as flickering).



Display data RAM



Liquid crystal Display

Display Data RAM

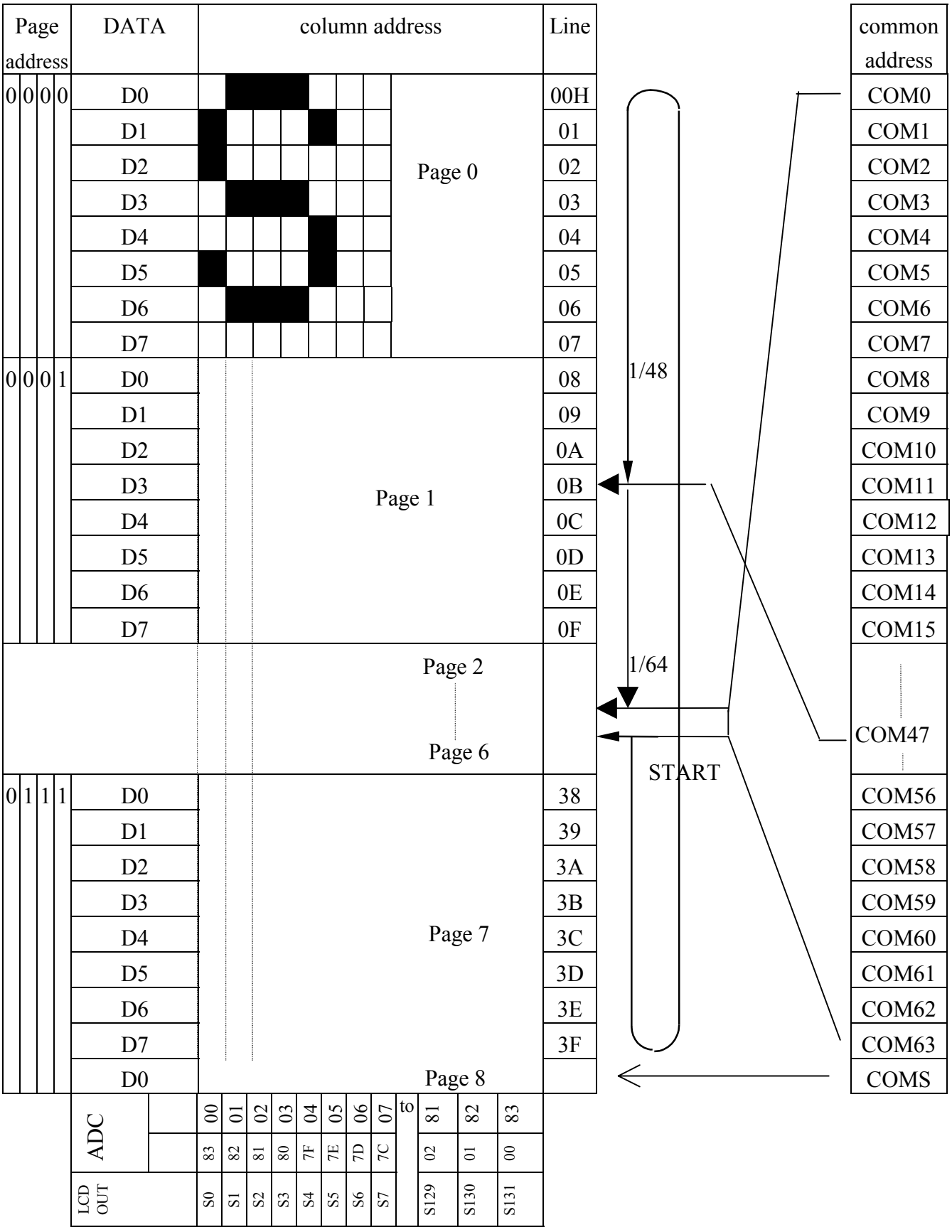


Figure 4

COMMANDS

The SED1565 Series chips identify the data bus signals by a combination of A0,$\overline{RD}$(E),$\overline{WR}$(R/$\overline{W}$)signals. Command interpretation and execution does not depend on the extemal clock,but rather is performed through intermal timing only, and thus the processing is fast enough that normally a buy check is not required.In the 8080 MPU interface, commands are launched by inputting a low pulse to the $\overline{RD}$ terminal for reading, and inputting a low pulse to the $\overline{WR}$ terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the R/$\overline{W}$ terminal and placed in a write mode when a "L" signal is input to the R/$\overline{W}$ terminal and then the command is launched by inputting a high pulse to the E terminal.Consequently,the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanations of commands and the display commands the status read and display data read $\overline{RD}$(E)becomes"1(H)".In the explanations below the commands are explained using the 8080 Series MPU interface as the example.

When the serial interface is selected, the data is input in sequence starting with D7.

<Explanation of Commands>

Display ON / OFF

This command turns the display ON andOFF

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	DISPLAY ON
										0	DISPLAY OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. for further details see the explanation of this function in "The Line Address Circuit".

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

Page Address Set

This command specifies the page address of the display data RAM shown in Figure 4. See the explanation of this function in "The Page Address Circuit" for details.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
							↓	↓	↓	↓	↓
							0	1	1	1	7
							1	0	0	0	8

Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits)when it is set(fundamentally ,set continuously).Each time the display data RAM is accessed, the column automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. See the funtion explanation in "The Column Address Circuit,"for details.

	A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
High bits							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
															↓					↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

Status Read

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY =1,it indicaltes that either processing is occurring internally or a reset condition is in process.While the chip does not accept commands until BUSY=0,if the cycle time can be satisfied,there is no need to check for BUSY conditions.
ADC	This showns the relationship between the column address and the segment driver. 0:Reverse (column address 131-n↔SEG n) 1:Normal (column address n↔SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF:indicates the display ON/OFF state. 0:Display ON 1:Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initializtion either because of a (RES)signal or because of a reset command. 0:Operating state 1:Reset in progress

Display Data Write

This command writes 8-bit data to the specified display data RAM address.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Display Data Read

This command reads 8-bit data from the specified display data RAM address. One dummy read required immediately after the column address has been set.SEE the function explanation in “Display Data RAM”for the explanation of accessing the internal registers.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

ADC Select(Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. See the explanation of the function in "Column Address Circuit" for details.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Rotate right(normal)
										1	Rotate left(reverse)

Display Normal/Reverse

This command can reverse the lit and unit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data"H" LCD ON voltage(normal)
										1	RAM Data "L" LCD ON voltage (reverse)

Display All Point ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM.The contents of the display data RAM are maintained when this is done.This command takes priority over the display normal/reverse command.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode,excuting the display all points ON command will place the display in power save mode. For details,see the (20)Power Save section.

LCD Bias Set

This command selects the voltage bais ratio required for the liquid crystal display.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	select status
0	1	0	1	0	1	0	0	0	1	0	1/9 bias
										1	1/7 bias

Read/Modify/Write

This command is used paired with the "END" command. Once this command has been input,the display data read command does not change the column address,but only the display data write command increments(+1)the column address. This mode is maintained unit the END command is input .When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered.This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

*Even in read/modify/write mode, other commands aside from display data read/write commands can also be used. However,the column address set command cannot be used.

*The sequence for cursor display

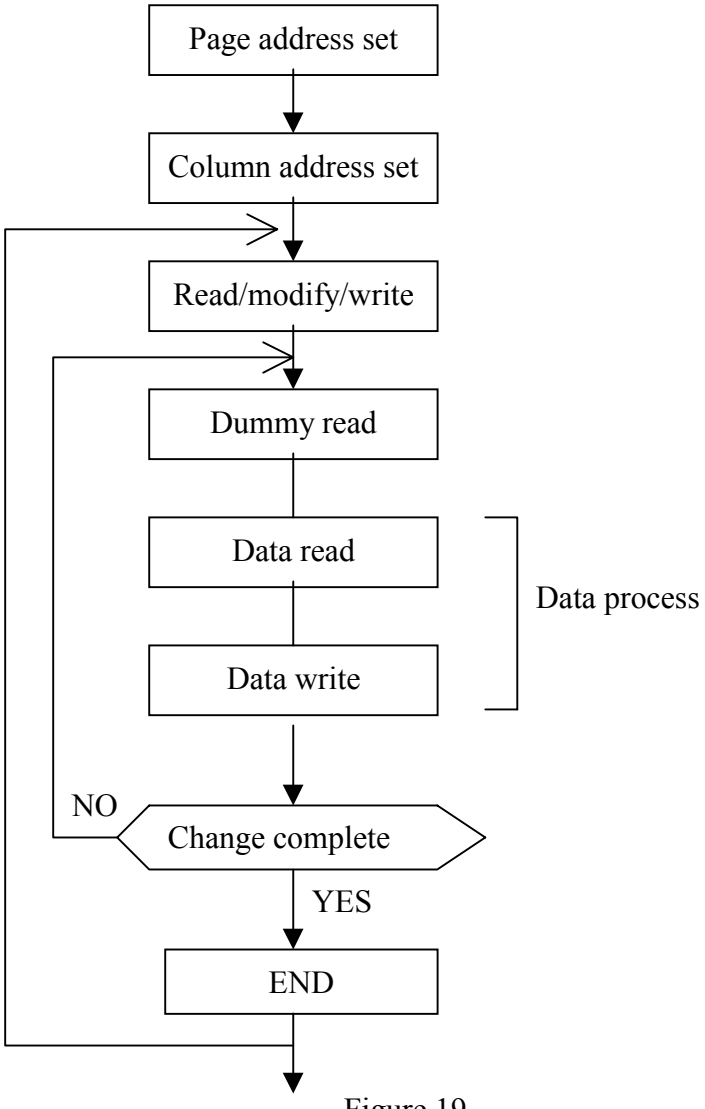
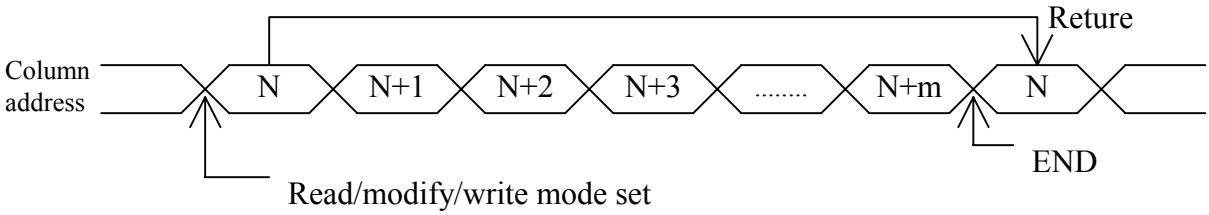


Figure 19

END

This command releases the read/modify/write mode,and returns the column addres to the address it was when the mode was entered.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



Reset

This command initializes the display start line,the column address ,the page address, the common output mode,the V5 voltgae regulator internal resistor ratio,the electronic volume,and the static indicator are reset,and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in “Reset” for details.

The initialization when the power supply is applied must be done through applying a reset signal to the $\overline{RES}$ terminal.

The reset operation is performed after the reset command is entered.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

The initializtion when the power supply is applied must be done through applying a reset signal to the $\overline{RES}$ terminal.

The reset command must not be used instead.

Command Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the funtion explanation “Command Output Mode Selet Circuit.”

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	1	1	0	0	0	*	*	*	Normal COM→COM63
							1				Reverse COM63→COM

*Disabled bit

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in “The Power Supply Circuit,” for details

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Set-up circuit:OFF
								1			Set-up circuit:ON
									0		Voltage regulator circuit:OFF
									1		Voltage regulator circuit:ON
										0	Voltage follower circuit:OFF
										1	Voltage follower circuit:ON

[Translator's Note:the abbreviations explained within these parentheses for V and V/F have been written out in the English translation and are therefore no longer necessary.]

V5 Voltage Regulator Internal Resister Ratio Set

This command sets the V5 voltage regulator internal resistor ratio. For details,see the function explanation is "The Power Supply Circuits."

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
									0	1	
									1	0	
									↓		↓
									1	0	
									1	1	Large

The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal driver voltage V5 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and electronic volume register set command, and both commands must be issued one after the other.

The Electronic Volume Mode Set

When this command is input , the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V5 assumes one of the 64 voltage levels.

When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	|V5|
0	1	0	*	*	0	0	0	0	0	1	Small
0	1	0	*	*	0	0	0	0	1	0	↓
0	1	0	*	*	0	0	0	0	1	1	↓
0	1	0					↓				↓
0	1	0	*	*	1	1	1	1	1	0	↓
0	1	0	*	*	1	1	1	1	1	1	Large

*Inactive bit

When the electronic volume function is not used this to (1,0,0,0,0,0)

* The Electronic Volume Register Set Sequence

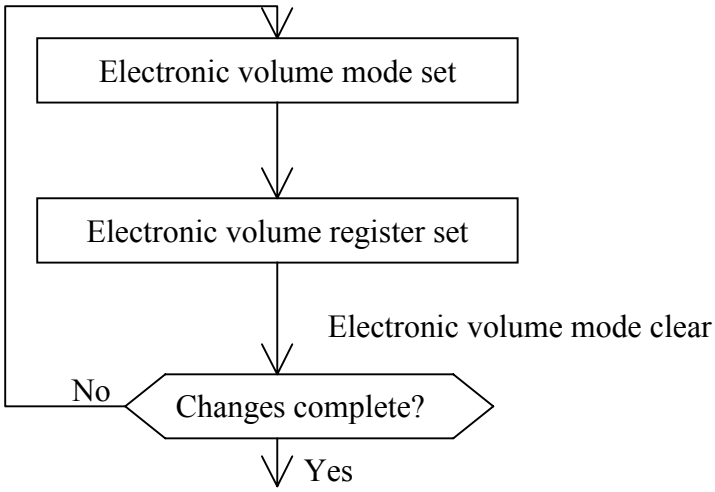


Figure 21

Static Indicator(Double Byte Command)

This command controls the static drive system indicator display.The staric indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal.A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other.(The static indicator OFF command is a single byte command.)

*Static Indicator ON/OFF

When the static indicator ON command is entered,the static indicator register set command is enable. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E(RD)	R/W(WR)	D7	D6	D5	D4	D3	D2	D1	D0	Static indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

*Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into blinking mode.

A0	E(RD)	R/W(WR)	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display Sets
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON(blinking at approximately one second intervals
									1	0	ON(blinking at approximately 0.5 second intervals
									1	1	ON (constantly on)

*Disabled bit

*Static Indicator Register Set Sequence

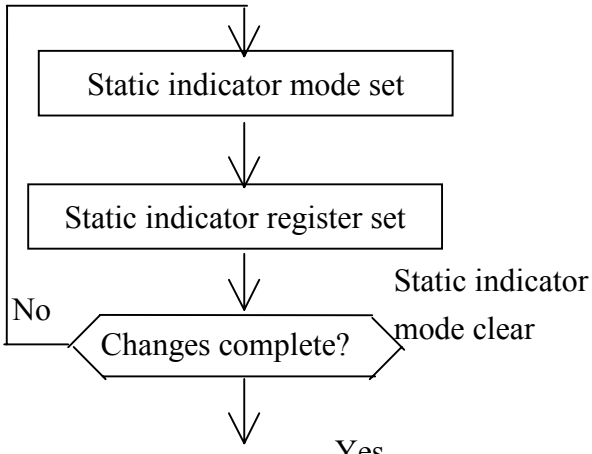


Figure 22

Power Save (Compound command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.

The power saver mode has two different modes:the sleep mode and the standby mode.When the indicator is OFF, it is the sleep mode that is entered.When the static indicator is ON ,it is the standby mode that is entered.

In the sleep mode and in the standby mode,the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.

The power saver mode is cleared by the display all points OFF command.

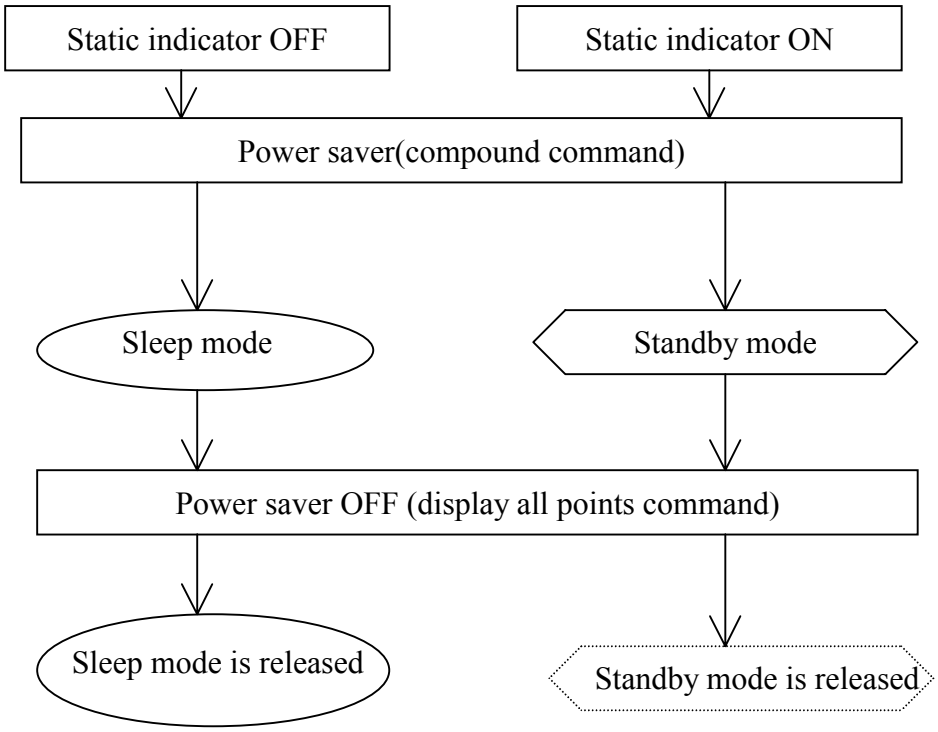


Figure 23

* Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU,the consumption current is reduced to a value near the static current.The internal modes during sleep mode are as follows:

①The oscillator circuit and the LCD power supply circuit are halted.

②All liquid crystal drive circuits are halted, and the segment in common drive outputs output a V_{DD} level.

*Standby mode

The duty LCD display system opertions are halted and only the static drive system for the indicator continues to operte, providing the minmun required consumption current for the static driver.The internal modes are in the following states during standby mode.

① The LCD power supply circuits are halted. The oscillator circuit continues to operate.

② The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a VDD level.The static drive system does not operate.

When a reset command is performed while in standby mode, the system enters sleep mode.

When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started.For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a citcuit be added in order to cut the electrical current floeing through the resistive voltage divider circuit when the power saver mode is in effect.The SED1565 series chips have a liquid crtstal display blanking control terminal $\overline{DOF}$.This terminal enters an “L”state when the power saver mode is launched. Using the output of $\overline{DOF}$, it is possible to stop the function of an external power supply circuit.

NOP

Non-OPeration Command

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for IC chip testing.Please do not use it.If the test command is used by accident,it can be cleared by applying a “L” signal to the $\overline{RES}$ input by the reset command or by using an NOP.

A0	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*Inactive bit

Note:The SED 1565 Series chips maintain their operating modes unit something happens to change them.Consequently,excessive external noise,etc.,can change the internal modes of the SED 1565 Series chip.Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip.Moreover,it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Table 16 Table of SED 1565 Series Commands

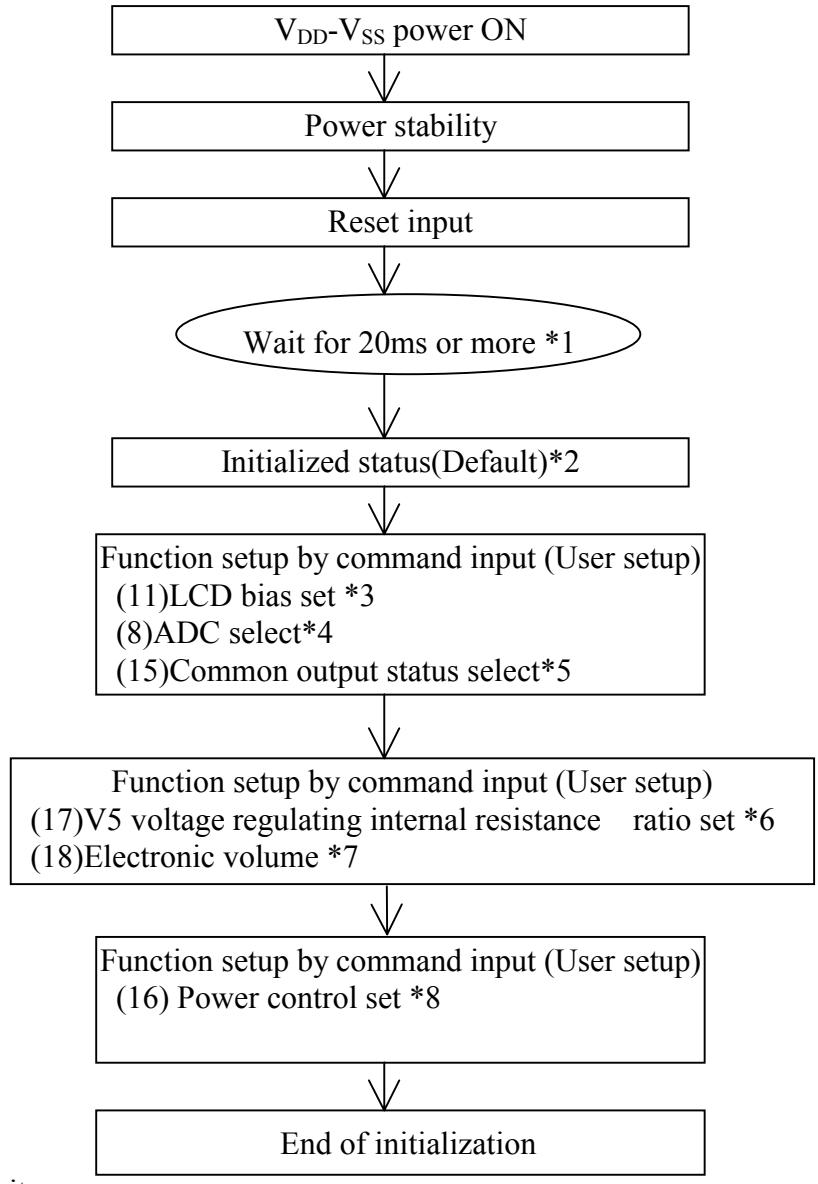
Command	Command Code											Function
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1)Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0:OFF ,1:ON
(2)Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3)Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4)Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address
(5)status read	0	0	1	Status				0	0	0	0	Reads the status data
(6)Display data write	1	1	0	Write data								Write to the display RAM
(7)Display data read	1	0	1	Read data								Reads from the display RAM
(8)ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0:normal, 1:reverse
(9)Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/reverse 0:normal, 1:reverse
(10)Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0:normal display 1:all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio SED 1565 0:1/9 , 1:1/7
(12)Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write:+1 At read:0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15)Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0:normal direction 1:reverse direction
(16)Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17)V5 voltage internal resister ratio set	0	1	0	0	0	1	0	0	Resister ratio			Select internal resister ratio (Rb/Ra)mode
(18)Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	
Electronic volume register set	0	1	0	*	*	Electronic volume value						Set the v5 output voltage electronic volume register
(19)Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0:OFF , 1:ON
Static indicator register set	1	0	1	*	*	*	*	*	*	mode		Set the flashing mode
(20)Power saver												Display OFF and display all points ON compound command
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22)Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

(Note)*:disable data

COMMAND DESCRIPTION

Instruction Setup:Refernce

(1)Initializtion



Notes: Reference items

*1:Stability timing of internal oscillator circuit

*2:Function Description;Reset citcuit

*3:Command Description;(11)LCD bias set

*4:Command Description;(8)ADC select

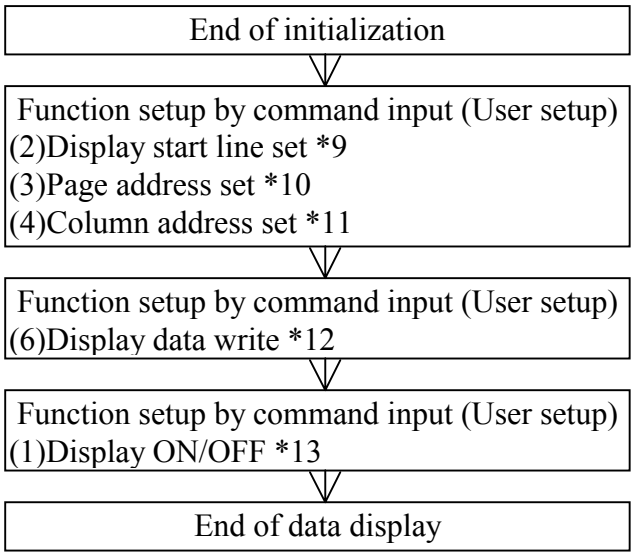
*5:Command Description;(15)Common output status select

*6:Function Description;Power supply circuit;and Command Description;(17)V5 voltage regulating internal resistance ratio set.

*7:Function Description;Power circuit;and Command Description; (18)Electronic volume

*8:Function Description;Power supply circuit;and Command Description;(16)Power control set

(2)Data Display



Notes:Reference items

*9:Command Description;(2)Display start line set

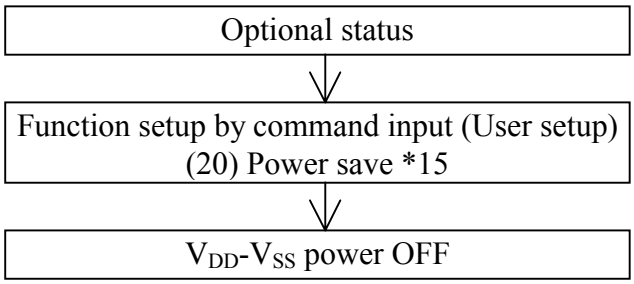
*10:Command Description;(3)Page address set

*11:Command Description;(4)Column address set

*12:Command Description;(6)Display data write

*13:Command Description;(1)Display ON/OFF

(3) Power OFF *14



Notes:Reference items

*14 After turning OFF the internal power supply, turn OFF the power supply of this IC.(Function Description - Power Supply Circuit)

When the power of this IC is turned OFF with the internal power suuply is held in the ON status,since the status where the voltage is supplies,even though an only little, to the internal LCD drive circuit is still continued,it is feared to ill affect the display quality of the LCD panel. To avoid this , be sure to observe the power OFF sequence strictly.

*15 Command Description;(20)Power save