NT5SV16M4DT
NT5SV8M8DT
NT5SV4M16DT

64Mb Synchronous DRAM

Features

- High Performance:

		-6K		-7K		-7	Units
f_{CK}	Clock Frequency	166	133	143	133	143	MHz
t_{CK}	Clock Cycle	6	7.5	7	7.5	7	ns
CL	CAS Latency	CL=3	CL=2	CL=3	CL=2	CL=3	CKs
t_{AC}	Clock Access Time[1]	---	—	---	—	—	ns
t_{AC}	Clock Access Time[2]	5.4	5.4	5.4	5.4	5.4	ns

1. Terminated load. See AC Characteristics on page 16.
2. Unterminated load. See AC Characteristics on page 16.

- Single Pulsed $\overline{RAS}$ Interface
- Fully Synchronous to Positive Clock Edge
- Four Banks controlled by BS0/BS1 (Bank Select)
- Programmable CAS Latency: 2, 3
- Programmable Burst Length: 1, 2, 4, 8, Full page
- Programmable Wrap: Sequential or Interleave
- Multiple Burst Read with Single Write Option
- Automatic and Controlled Precharge Command
- Data Mask for Read/Write control (x4, x8)
- Dual Data Mask for byte control (x16)
- Auto Refresh (CBR) and Self Refresh
- Suspend Mode and Power Down Mode
- Standard Power operation
- 4096 refresh cycles/64ms
- Random Column Address every CK (1-N Rule)
- Single 3.3V ± 0.3V Power Supply
- LVTTL compatible
- Package: 54-pin 400 mil TSOP-Type II

Description

The NT5SV16M4DT, NT5SV8M8DT, and NT5SV4M16DT are four-bank Synchronous DRAMs organized as 4Mbit x 4 I/O x 4 Bank, 2Mbit x 8 I/O x 4 Bank, and 1Mbit x 16 I/O x 4 Bank, respectively. These synchronous devices achieve high-speed data transfer rates of up to 200MHz by employing a pipeline chip architecture that synchronizes the output data to a system clock. The chip is fabricated with NTC's advanced 64Mbit single transistor CMOS DRAM process technology.

The device is designed to comply with all JEDEC standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, and data input/output (I/O or DQ) circuits are synchronized with the positive edge of an externally supplied clock.

$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{CS}$ are pulsed signals which are examined at the positive edge of each externally applied clock (CK). Internal chip operating modes are defined by combinations of these signals and a command decoder initiates the necessary timings for each operation. A fourteen bit address bus accepts address data in the conventional $\overline{RAS}$/$\overline{CAS}$ multiplexing style. Twelve row addresses (A0-A11) and two bank select addresses (BS0, BS1) are strobed with $\overline{RAS}$. Eleven column addresses (A0-A9) plus bank select addresses and A10 are strobed with $\overline{CAS}$. Column address A9 is dropped on the x8 device, and column addresses A8 and A9 are dropped on the x16 device.

Prior to any access operation, the $\overline{CAS}$ latency, burst length, and burst sequence must be programmed into the device by address inputs A0-A11, BS0, BS1 during a mode register set cycle. In addition, it is possible to program a multiple burst sequence with single write cycle for write through cache operation.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 200MHz is possible depending on burst length, $\overline{CAS}$ latency, and speed grade of the device. Simultaneous operation of both decks of a stacked device is allowed, depending on the operation being done. Auto Refresh (CBR) and Self Refresh operation are supported.

Pin Assignments for Planar Components (Top View)

V_{DD}	V_{DD}	V_{DD}	1	54	V_{SS}	V_{SS}	V_{SS}
DQ0	DQ0	NC	2	53	NC	DQ7	DQ15
V_{DDQ}	V_{DDQ}	V_{DDQ}	3	52	V_{SSQ}	V_{SSQ}	V_{SSQ}
DQ1	NC	NC	4	51	NC	NC	DQ14
DQ2	DQ1	DQ0	5	50	DQ3	DQ6	DQ13
V_{SSQ}	V_{SSQ}	V_{SSQ}	6	49	V_{DDQ}	V_{DDQ}	V_{DDQ}
DQ3	NC	NC	7	48	NC	NC	DQ12
DQ4	DQ2	NC	8	47	NC	DQ5	DQ11
V_{DDQ}	V_{DDQ}	V_{DDQ}	9	46	V_{SSQ}	V_{SSQ}	V_{SSQ}
DQ5	NC	NC	10	45	NC	NC	DQ10
DQ6	DQ3	DQ1	11	44	DQ2	DQ4	DQ9
V_{SSQ}	V_{SSQ}	V_{SSQ}	12	43	V_{DDQ}	V_{DDQ}	V_{DDQ}
DQ7	NC	NC	13	42	NC	NC	DQ8
V_{DD}	V_{DD}	V_{DD}	14	41	V_{SS}	V_{SS}	V_{SS}
LDQM	NC	NC	15	40	NC	NC	NC
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	16	39	DQM	DQM	UDQM
$\overline{CAS}$	$\overline{CAS}$	$\overline{CAS}$	17	38	CK	CK	CK
$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	18	37	CKE	CKE	CKE
$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	19	36	NC	NC	NC
BS0	BS0	BS0	20	35	A11	A11	A11
BS1	BS1	BS1	21	34	A9	A9	A9
A10/AP	A10/AP	A10/AP	22	33	A8	A8	A8
A0	A0	A0	23	32	A7	A7	A7
A1	A1	A1	24	31	A6	A6	A6
A2	A2	A2	25	30	A5	A5	A5
A3	A3	A3	26	29	A4	A4	A4
V_{DD}	V_{DD}	V_{DD}	27	28	V_{SS}	V_{SS}	V_{SS}

54-pin Plastic TSOP(II) 400 mil

4Mbit x 4 I/O x 4 Bank

NT5SV16M4DT

2Mbit x 8 I/O x 4 Bank

NT5SV8M8DT

1Mbit x 16 I/O x 4 Bank

NT5SV4M16DT

Pin Description

CK	Clock Input	DQ0-DQ15	Data Input/Output
CKE	Clock Enable	DQM, LDQM, UDQM	Data Mask
$\overline{CS}$	Chip Select	V_{DD}	Power (+3.3V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	V_{DDQ}	Power for DQs (+3.3V)
$\overline{WE}$	Write Enable	V_{SSQ}	Ground for DQs
BS1, BS0	Bank Select	NC	No Connection
A0 - A11	Address Inputs	—	—

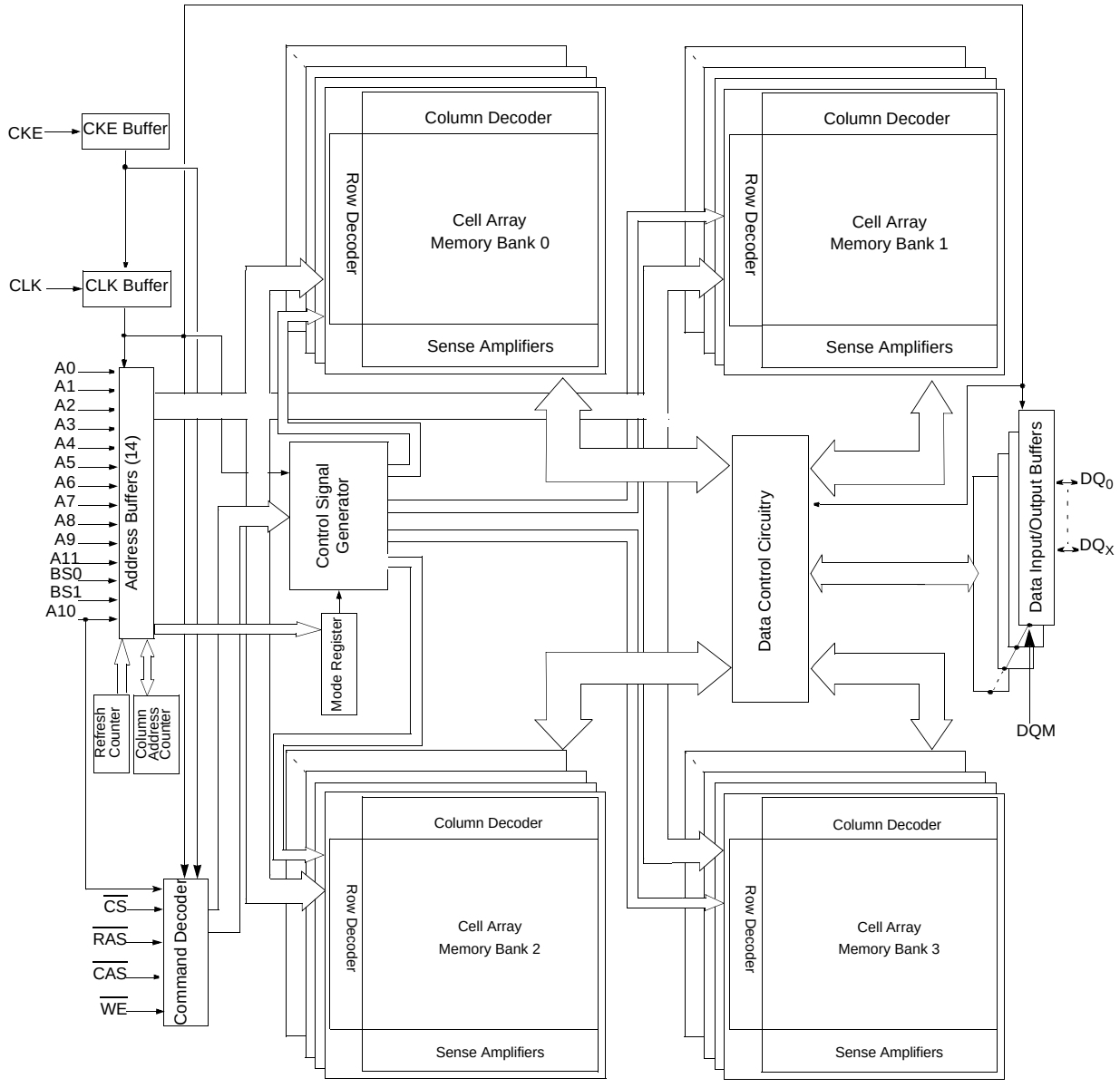
Input/Output Functional Description

Symbol	Type	Polarity	Function
CLK	Input	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Active High	Activates the CLK signal when high and deactivates the CLK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BS0, BS1	Input	—	Selects which bank is to be active.
A0 - A11	Input	—	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. A10 is used to invoke auto-precharge operation at the end of the burst read or write cycle. If A10 is high, auto-precharge is selected and BS0, BS1 defines the bank to be precharged. If A10 is low, auto-precharge is disabled. During a Precharge command cycle, A10 is used in conjunction with BS0, BS1 to control which bank(s) to precharge. If A10 is high, all banks will be precharged regardless of the state of BS. If A10 is low, then BS0 and BS1 are used to define which bank to precharge.
DQ0 - DQ15	Input-Output	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQM LDQM UDQM	Input	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In x16 products, LDQM and UDQM control the lower and upper byte I/O buffers, respectively. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. DQM low turns the output buffers on and DQM high turns them off. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
V_{DD}, V_{SS}	Supply	—	Power and ground for the input buffers and the core logic.
V_{DDQ} V_{SSQ}	Supply	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.

Ordering Information

Organization	Part Number	Speed Grade			Power Supply	Package
		Clock Frequency@CAS Latency		Note		
16M x 4	NT5SV16M4DT-6K	166MHz@CL3	133MHz@CL2	PC133 , PC100	3.3 V	400mil 54-PIN TSOP II
	NT5SV16M4DT-7K	143MHz@CL3	133MHz@CL2			
	NT5SV16M4DT-7	143MHz@CL3	100MHz@CL2			
8M x 8	NT5SV8M8DT-6K	166MHz@CL3	133MHz@CL2			
	NT5SV8M8DT-7K	143MHz@CL3	133MHz@CL2			
	NT5SV8M8DT-7	143MHz@CL3	100MHz@CL2			
4M x 16	NT5SV4M16DT-6K	166MHz@CL3	133MHz@CL2			
	NT5SV4M16DT-7K	143MHz@CL3	133MHz@CL2			
	NT5SV4M16DT-7	143MHz@CL3	100MHz@CL2			

Block Diagram

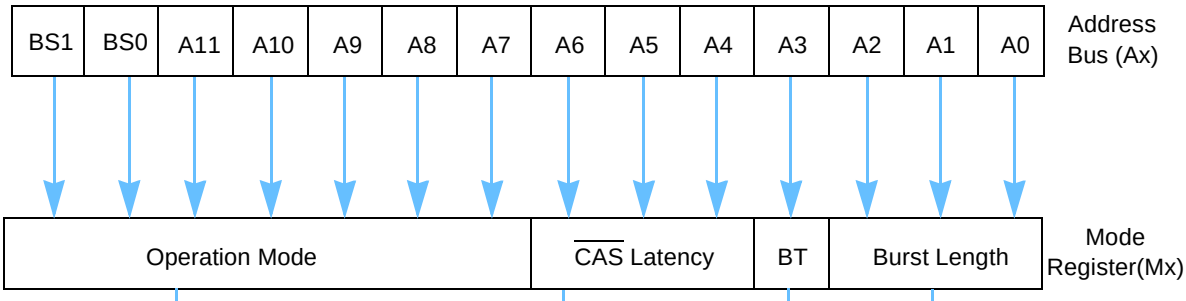


Cell Array, per bank, for 4Mb x 4 DQ: 4096 Row x 1024 Col x 4 DQ (DQ0-DQ3).

Cell Array, per bank, for 2Mb x 8 DQ: 4096 Row x 512 Col x 8 DQ (DQ0-DQ7).

Cell Array, per bank, for 1Mb x 16 DQ: 4096 Row x 256 Col x 16 DQ (DQ0-DQ15).

Mode Register Operation (Address Input For Mode Set)



Burst Type

M3	Type
0	Sequential
1	Interleave

Operation Mode

M13	M12	M11	M10	M9	M8	M7	Mode
0	0	0	0	0	0	0	Normal
0	0	0	0	1	0	0	Multiple Burst with Single Write

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

CAS Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). There are three parameters that define how the burst mode will operate. These parameters include burst sequence, burst length, and operation mode. The burst sequence and burst length are programmable, and are determined by address bits A0 - A3 during the Mode Register Set command. Operation mode is also programmable and is set by address bits A7 - A11, BS0, and BS1.

The burst type is used to define the order in which the burst data will be delivered or stored to the SDRAM. Two types of burst sequences are supported, sequential and interleaved. See the table below.

The burst length controls the number of bits that will be output after a Read Command, or the number of bits to be input after a Write Command. The burst length can be programmed to have values of 1, 2, 4, 8 or full page(actual page length is dependent on organization: x4, x8, or x16).Full page burst operation is only posible using the sequential burst type.

Burst operation mode can be normal operation or multiple burst with single write operation. Normal operation implies that the device will perform burst operations on both read and write cycles until the desired burst length is satisfied. Multiple burst with single write operation was added to support Write Through Cache operation. Here, the programmed burst length only applies to read cycles. All write cycles are single write operations when this mode is selected.

Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
2	x x 0	0, 1	0, 1
	x x 1	1, 0	1, 0
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
Full Page(Note)	n n n	Cn, Cn+1, Cn+2, ...	Not Supported

Note: Page length is a function of I/O organization and column addressing.

x4 organization (CA0-CA9); Page Length = 1024 bits

x8 organization (CA0-CA8); Page Length = 512 bits

x16 organization (CA0-CA7); Page Length = 256 bits

Command Truth Table (See note 1)

Function	Device State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BS0, BS1	A10	A11, A11, A9-A0	Notes
		Previous Cycle	Current Cycle									
Mode Register Set	Idle	H	X	L	L	L	L	X	OP Code			
Auto (CBR) Refresh	Idle	H	H	L	L	L	H	X	X	X	X	
Entry Self Refresh	Idle	H	L	L	L	L	H	X	X	X	X	
Exit Self Refresh	Idle (Self-Refresh)	L	H	H	X	X	X	X	X	X	X	
				L	H	H	H					
Single Bank Precharge	See Current State Table	H	X	L	L	H	L	X	BS	L	X	2
Precharge all Banks	See Current State Table	H	X	L	L	H	L	X	X	H	X	
Bank Activate	Idle	H	X	L	L	H	H	X	BS	Row Address		2
Write	Active	H	X	L	H	L	L	X	BS	L	Column	2
Write with Auto-Precharge	Active	H	X	L	H	L	L	X	BS	H	Column	2
Read	Active	H	X	L	H	L	H	X	BS	L	Column	2
Read with Auto-Precharge	Active	H	X	L	H	L	H	X	BS	H	Column	2
Burst Termination	Active	H	X	L	H	H	L	X	X	X	X	3,8
No Operation	Any	H	X	L	H	H	H	X	X	X	X	
Device Deselect	Any	H	X	H	X	X	X	X	X	X	X	
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X	4
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X	
Data Write/Output Enable	Active	H	X	X	X	X	X	L	X	X	X	5
Data Mask/Output Disable	Active	H	X	X	X	X	X	H	X	X	X	
Power Down Mode Entry	Idle/Active	H	L	H	X	X	X	X	X	X	X	6, 7
				L	H	H	H					
Power Down Mode Exit	Any (Power Down)	L	H	H	X	X	X	X	X	X	X	6, 7
				L	H	H	H					

1. All of the SDRAM operations are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and DQM at the positive rising edge of the clock.Operation of both decks of a stacked device at the same time is allowed, depending on the operation being performed on the other deck. Refer to the Current State Truth Table.
2. Bank Select (BS0, BS1): BS0, BS1 = 0,0 selects bank 0; BS0, BS1 = 1,0 selects bank 1; BS0, BS1 = 0,1 selects bank 2; BS0, BS1 = 1,1 selects bank 3.
3. During a Burst Write cycle there is a zero clock delay; for a Burst Read cycle the delay is equal to the $\overline{CAS}$ latency.
4. During normal access mode, CKE is held high and CK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two-clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).
6. All banks must be precharged before entering the Power Down Mode. (If this command is issued during a burst operation, the device state will be Clock Suspend Mode.) The Power Down Mode does not perform any refresh operations; therefore the device can't remain in this mode longer than the Refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.
7. A No Operation or Device Deselect Command is required on the next clock edge following CKE going high.
8. Device state is full page burst operation. Use of this command to terminate other burst length operations is illegal.

Clock Enable (CKE) Truth Table

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS0, BS1	A11 - A0		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down mode exit, all banks idle	2
	L	H	L	X	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				3
	H	H	L	L	H	X				3
	H	H	L	L	L	H	X	X	CBR Refresh	
	H	H	L	L	L	L	OP Code		Mode Register Set	4
	H	L	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				3
	H	L	L	L	H	X				3
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L	OP Code		Mode Register Set	
	L	X	X	X	X	X	X	X	Power Down	4
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to operations in the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	5
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

1. For the given Current State CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE (t_{CES}) must be satisfied. When exiting power down mode, a NOP command (or Device Deselect Command) is required on the first rising clock after CKE goes high (see page 26).
3. The address inputs depend on the command that is issued. See the Idle State section of the Current State Truth Table for more information.
4. The Precharge Power Down Mode, the Self Refresh Mode, and the Mode Register Set can only be entered from the all banks idle state.
5. Must be a legal command as defined in the Current State Truth Table.

Current State Truth Table (Part 1 of 3)(See note 1)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS0,BS1	A11 - A0	Description		
Idle	L	L	L	L	OP Code		Mode Register Set	Set the Mode Register	2
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	2, 3
	L	L	H	L	BS	X	Precharge	No Operation	
	L	L	H	H	BS	Row Address	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BS	Column	Write w/o Precharge	ILLEGAL	4
	L	H	L	H	BS	Column	Read w/o Precharge	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	5
Row Active	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Precharge	6
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Start Write; Determine if Auto Precharge	7, 8
	L	H	L	H	BS	Column	Read	Start Read; Determine if Auto Precharge	7, 8
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Terminate Burst; Start the Write cycle	8, 9
	L	H	L	H	BS	Column	Read	Terminate Burst; Start a new Read cycle	8, 9
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Terminate Burst; Start a new Write cycle	8, 9
	L	H	L	H	BS	Column	Read	Terminate Burst; Start the Read cycle	8, 9
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. All Banks must be idle; otherwise, it is an illegal action.
3. If CKE is active (high) the SDRAM will start the Auto (CBR) Refresh operation, if CKE is inactive (low) than the Self Refresh mode is entered.
4. The Current State refers to only one of the banks. If BS selects this bank then the action is illegal. If BS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered; otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

Current State Truth Table (Part 2 of 3)(See note 1)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS0,BS1	A11 - A0	Description		
Read with Auto Pre-charge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Precharging	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	No Operation; Bank(s) idle after t_{RP}	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{RP}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RP}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{RP}	
Row Activating	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4, 10
	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation; Row Active after t_{RCD}	
	L	H	H	H	X	X	No Operation	No Operation; Row Active after t_{RCD}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row Active after t_{RCD}	

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. All Banks must be idle; otherwise, it is an illegal action.
3. If CKE is active (high) the SDRAM will start the Auto (CBR) Refresh operation, if CKE is inactive (low) than the Self Refresh mode is entered.
4. The Current State refers to only one of the banks. If BS selects this bank then the action is illegal. If BS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered; otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

Current State Truth Table (Part 3 of 3)(See note 1)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS0,BS1	A11 - A0	Description		
Write Recovering	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Start Write; Determine if Auto Precharge	9
	L	H	L	H	BS	Column	Read	Start Read; Determine if Auto Precharge	9
	L	H	H	L	X	X	Burst Termination	No Operation; Row Active after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Row Active after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row Active after t_{DPL}	
Write Recovering with Auto Pre-charge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4, 9
	L	H	L	H	BS	Column	Read	ILLEGAL	4, 9
	L	H	H	L	X	X	Burst Termination	No Operation; Precharge after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Precharge after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Precharge after t_{DPL}	
Refreshing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; Idle after t_{RC}	
	L	H	H	H	X	X	No Operation	No Operation; Idle after t_{RC}	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after t_{RC}	
Mode Register Accessing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after two clock cycles	

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. All Banks must be idle; otherwise, it is an illegal action.
3. If CKE is active (high) the SDRAM will start the Auto (CBR) Refresh operation, if CKE is inactive (low) than the Self Refresh mode is entered.
4. The Current State refers to only one of the banks. If BS selects this bank then the action is illegal. If BS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered; otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Power Supply Voltage	-0.3 to +4.6	V	1
V_{DDQ}	Power Supply Voltage for Output	-0.3 to +4.6	V	1
V_{IN}	Input Voltage	-0.3 to V_{DD}+0.3	V	1
V_{OUT}	Output Voltage	-0.3 to V_{DD}+0.3	V	1
T_A	Operating Temperature (ambient)	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0°C to 70°C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V_{DDQ}	Supply Voltage for Output	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3	V	1, 2
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1, 3

1. All voltages referenced to V_{SS} and V_{SSQ}.
2. V_{IH} (max) = V_{DD} + 1.2V for pulse width ≤ 5ns.
3. V_{IL} (min) = V_{SS} - 1.2V for pulse width ≤ 5ns.

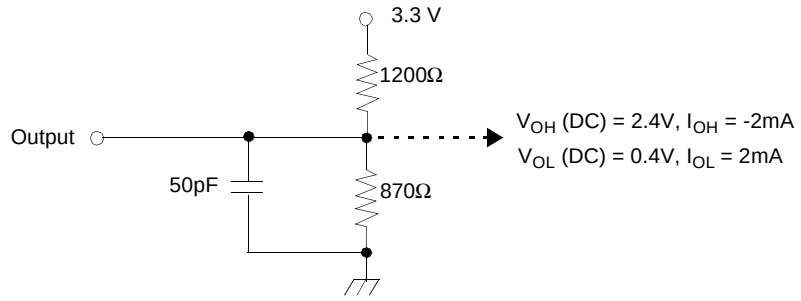
Capacitance (T_A = 25°C, f = 1MHz, V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Min.	Typ	Max.	Units
C_I	Input Capacitance (A0-A11, BS0, BS1, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, DQM)	2.5	3.0	3.8	pF
	Input Capacitance (CK)	2.5	2.8	3.5	pF
C_O	Output Capacitance (DQ0 - DQ15)	4.0	4.5	6.5	pF

DC Electrical Characteristics (T_A = 0 to +70°C, V_{DD} = 3.3V ±0.3V)

Symbol	Parameter	Min.	Max.	Units
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ V_{DD}), All Other Pins Not Under Test = 0V	-1	+1	µA
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ V_{DDQ})	-1	+1	µA
V_{OH}	Output Level (LVTTL) Output "H" Level Voltage (I_{OUT} = -2.0mA)	2.4	—	V
V_{OL}	Output Level (LVTTL) Output "L" Level Voltage (I_{OUT} = +2.0mA)	—	0.4	V

DC Output Load Circuit



Operating, Standby, and Refresh Currents (T_A = 0 to +70°C, V_{DD} = 3.3V ±0.3V)

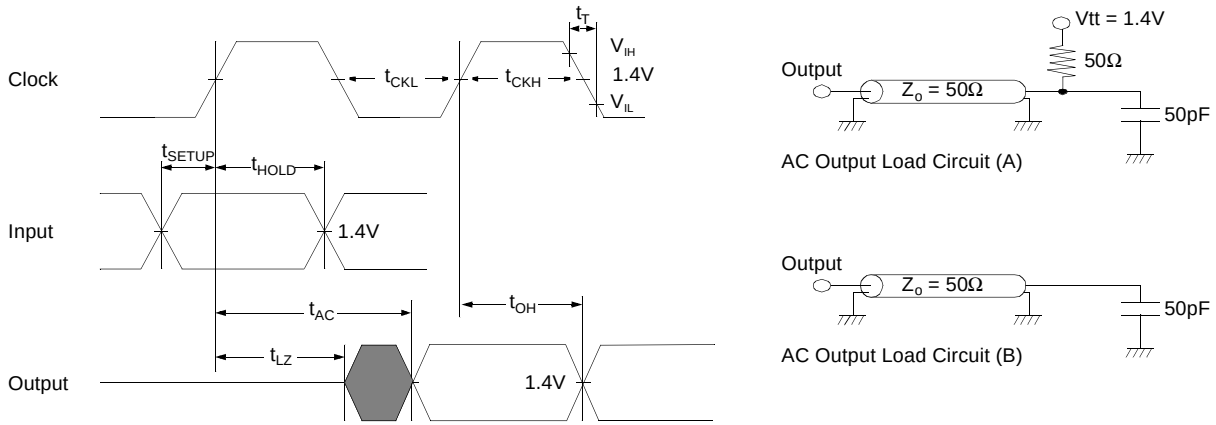
Parameter	Symbol	Test Condition	-6K (6ns)	-7K (7ns)	-7 (7ns)	Units	Notes
Operating Current	I_{CC1}	1 bank operation $t_{RC} = t_{RC}(min)$, t_{CK} = min Active-Precharge command cycling without burst operation	60	55		mA	1, 2, 3
Precharge Standby Current in Power Down Mode	I_{CC2P}	$\overline{CKE} \le V_{IL}(max)$, t_{CK} = min, $\overline{CS} = V_{IH}(min)$	1			mA	1
	I_{CC2PS}	$\overline{CKE} \le V_{IL}(max)$, t_{CK} = Infinity, $\overline{CS} = V_{IH}(min)$	1			mA	1
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	$\overline{CKE} \ge V_{IH}(min)$, t_{CK} = min, $\overline{CS} = V_{IH}$ (min)	10			mA	1, 5
	I_{CC2NS}	CKE ≥ V_{IH}(min), t_{CK} = Infinity,	5			mA	1, 7
No Operating Current (Active state: 4 bank)	I_{CC3N}	$\overline{CKE} \ge V_{IH}(min)$, t_{CK} = min, $\overline{CS} = V_{IH}$ (min)	30			mA	1, 5
	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CK} = min,	9			mA	1, 6
Operating Current (Burst Mode)	I_{CC4}	t_{CK} = min, Read/ Write command cycling, Multiple banks active, gapless data, BL = 4	75	70		mA	1, 3, 4
Auto (CBR) Refresh Current	I_{CC5}	t_{CK} = min, $t_{RC} = t_{RC}(min)$ CBR command cycling	120	110		mA	1
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	1			mA	1

1. Currents given are valid for a single device. The total current for a stacked device depends on the operation being performed on the other deck.
2. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed up to three times during t_{RC}(min).
3. The specified values are obtained with the output open.
4. Input signals are changed once during t_{CK}(min).
5. Input signals are changed once during three clock cycles.
6. Active Standby Current will be higher if Clock Suspend is entered during a burst read cycle (add 1mA per DQ).
7. Input signals are stable.

AC Characteristics (T_A = 0 to +70°C, V_{DD} = 3.3V ± 0.3V)

1. An initial pause of 200µs, with DQM and CKE held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of two Auto (CBR) Refresh cycles before or after the Mode Register Set operation.
2. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH})
3. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. Load Circuit A: AC timing tests have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.40V crossover point
5. Load Circuit A: AC measurements assume t_T = 1.0ns.
6. Load Circuit B: AC timing tests have V_{IL} = 0.8 V and V_{IH} = 2.0 V with the timing referenced to the 1.40V crossover point
7. Load Circuit B: AC measurements assume t_T = 1.2ns.

AC Characteristics Diagrams



Clock and Clock Enable Parameters

Symbol	Parameter	-6K		-7K		-7		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CK3}	Clock Cycle Time, $\overline{CAS}$ Latency = 3	6	1000	7	1000	7	1000	ns	
t_{CK2}	Clock Cycle Time, $\overline{CAS}$ Latency = 2	7.5	1000	7.5	1000	10	1000	ns	
$t_{AC3\ (A)}$	Clock Access Time, $\overline{CAS}$ Latency = 3	—	—	—	—	—	—	ns	1
$t_{AC2\ (A)}$	Clock Access Time, $\overline{CAS}$ Latency = 2	—	—	—	—	—	—	ns	1
$t_{AC3\ (B)}$	Clock Access Time, $\overline{CAS}$ Latency = 3	—	5.4	—	5.4	—	5.4	ns	2
$t_{AC2\ (B)}$	Clock Access Time, $\overline{CAS}$ Latency = 2	—	5.4	—	5.4	—	6	ns	2
t_{CKH}	Clock High Pulse Width	2.5	—	2.5	—	3	—	ns	
t_{CKL}	Clock Low Pulse Width	2.5	—	2.5	—	3	—	ns	
t_{CES}	Clock Enable Set-up Time	1.5	—	1.5	—	2	—	ns	
t_{CEH}	Clock Enable Hold Time	0.8	—	0.8	—	1	—	ns	
t_{SB}	Power down mode Entry Time	0	6	0	7	0	7.5	ns	
t_T	Transition Time (Rise and Fall)	0.5	10	0.5	10	0.5	10	ns	

1. Access time is measured at 1.4V. See AC Characteristics: notes 1, 2, 3, 4, 5 and load circuit A.
2. Access time is measured at 1.4V. See AC Characteristics: notes 1, 2, 3, 6, 7 and load circuit B.

Common Parameters

Symbol	Parameter	-6K		-7K		-7		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CS}	Command Setup Time	1.5	—	1.5	—	1.5	—	ns	
t_{CH}	Command Hold Time	0.8	—	0.8	—	0.8	—	ns	
t_{AS}	Address and Bank Select Set-up Time	1.5	—	1.5	—	1.5	—	ns	
t_{AH}	Address and Bank Select Hold Time	0.8	—	0.8	—	0.8	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	15	—	15	—	20	—	ns	1
t_{RC}	Bank Cycle Time	48	—	52	—	63	—	ns	1
t_{RAS}	Active Command Period	36	100K	37	100K	42	100K	ns	1
t_{RP}	Precharge Time	15	—	15	—	20	—	ns	1
t_{RRD}	Bank to Bank Delay Time	12	—	14	—	14	—	ns	1

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Mode Register Set Cycle

Symbol	Parameter	-6K		-7K		-7		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RSC}	Mode Register Set Cycle Time	12	—	14	—	14	—	ns

Read Cycle

Symbol	Parameter	-6K		-7K		-7		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{OH}	Data Out Hold Time		—	—	—	—	—	ns	1
		3	—	3	—	3	—	ns	2, 4
t_{LZ}	Data Out to Low Impedance Time		—	0	—	0	—	ns	
t_{HZ3}	Data Out to High Impedance Time	2.7	5.4	2.7	5.4	2.7	5.4	ns	3
t_{HZ2}	Data Out to High Impedance Time	2.7	5.4	2.7	5.4	3	6	ns	3
t_{DQZ}	DQM Data Out Disable Latency	2	—	2	—	2	—	CK	

1. AC Output Load Circuit A.
2. AC Output Load Circuit B.
3. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.
4. Data Out Hold Time with no load must meet 1.8ns (-5K, -7K, -75B).

Refresh Cycle

Symbol	Parameter	-6K		-7K		-7		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Refresh Period	—	64	—	64	—	64	ms	1
t_{SREX}	Self Refresh Exit Time	10	—	10	—	10	—	ns	

1. 4096 auto refresh cycles.

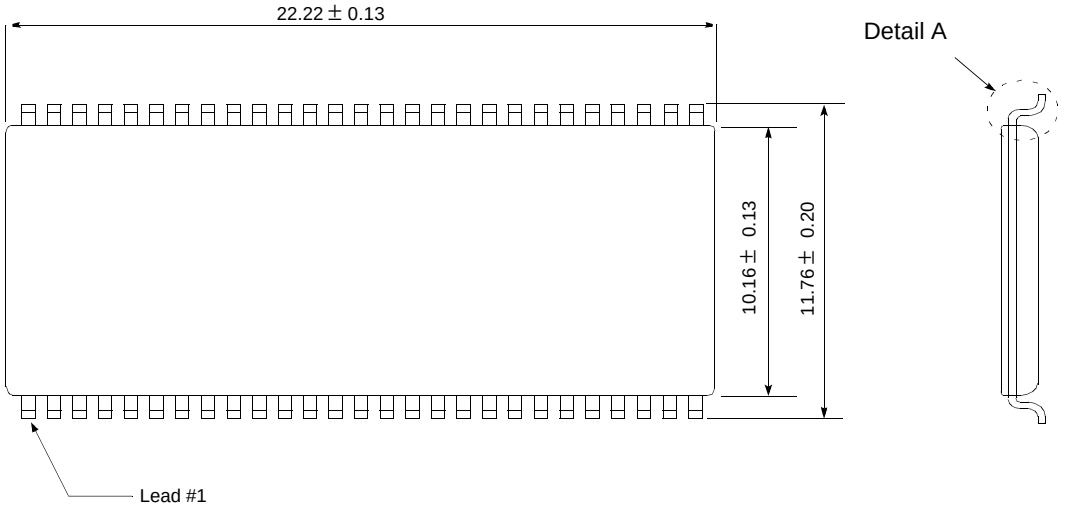
Write Cycle

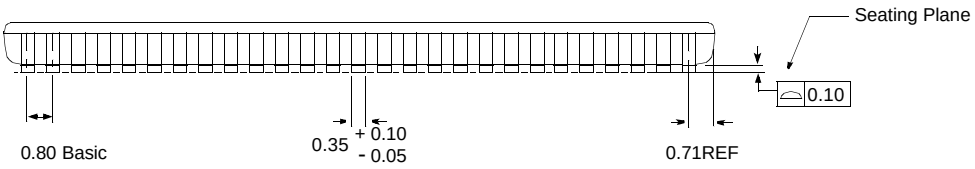
Symbol	Parameter	-6K		-7K		-7		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{DS}	Data In Set-up Time	1.5	—	1.5	—	1.5	—	ns
t_{DH}	Data In Hold Time	0.8	—	0.8	—	0.8	—	ns
t_{DPL}	Data input to Precharge	12	—	14	—	14	—	ns
t_{WR}	Write Recovery Time	12	—	14	—	14	—	ns
t_{DAL3}	Data In to Active Delay CAS Latency = 3	5	—	5	—	5	—	CK
t_{DAL2}	Data In to Active Delay CAS Latency = 2	4	—	4	—	4	—	CK
t_{DQW}	DQM Write Mask Latency	0	—	0	—		—	CK

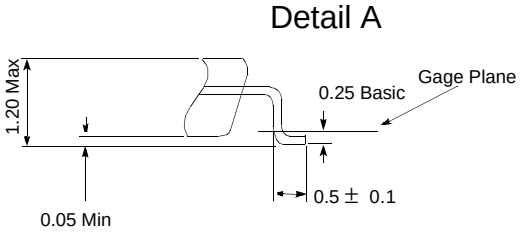
Clock Frequency and Latency

Symbol	Parameter	-6K		-7K		-7		Units
f_{CK}	Clock Frequency	166	133	143	133	143	100	MHz
t_{CK}	Clock Cycle Time	6	7.5	7	7.5	7	10	ns
t_{AA}	$\overline{CAS}$ Latency	3	2	3	2	3	2	CK
t_{RP}	Precharge Time	3	2	3	2	3	2	CK
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	3	2	3	2	3	2	CK
t_{RC}	Bank Cycle Time	9	7	9	7	9	7	CK
t_{RAS}	Minimum Bank Active Time	6	5	6	5	6	5	CK
t_{DPL}	Data In to Precharge	2	2	2	2	2	2	CK
t_{DAL}	Data In to Active/Refresh	5	4	5	4	5	4	CK
t_{RRD}	Bank to Bank Delay Time	2	2	2	2	2	2	CK
t_{WL}	Write Latency	0	0	0	0	0	0	CK
t_{DQW}	DQM Write Mask Latency	0	0	0	0	0	0	CK
t_{DQZ}	DQM Data Disable Latency	2	2	2	2	2	2	CK
t_{CSL}	Clock Suspend Latency	1	1	1	1	1	1	CK

Package Dimensions (400mil; 54 lead; Thin Small Outline Package)







Revision Log

Rev	Contents of Modification
05/01	Preliminary
09/01	Changed to Revision 1.0
	Removed -75B speed grade
	Added -7 speed grade.
	Removed Icc6 low power product grade.
10/01	Changed to Revision 1.1
	Changed tOH from 2.7ns to 3ns for all speed sort.