Engineering Specification

15.0 inches SXGA+ Color TFT/LCD Module
Model Name:ITSX93C

Document Control Number : OEM93C-04

Note:Specification is subject to change without notice. Consequently it is better to contact to IBM before proceeding with the design of your product incorporating this module.

Display Business Unit
International Business Machines Corporation

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ii Record of Revision

Date	Document Revision	Page	Summary
March 26,1999	OEM93C-01 (Preliminary)	All	First Edition for customer. Based on Initial Internal Spec. as of March 8,1999 Based on Mechanical Drawing as of Draft March 3,1999. Updated information as of March 23. Lamp cable length:75.5 mm
April 13,1999	OEM93C-02 (Preliminary)	7, 10 27	To update P/N for connector.
July 9,1999	OEM93C-03	4 6 8 9 11 16 18 19 20 21 23 25, 26	To add an explanation for UL. To update White Luminance, Optical Rise Time/Fall Time, and Power consumption. To correct Absolute Maximum Rating For Shock. To update Optical Charastaristics. To correct Signal Name of Pin #15. To update LVDS Macro AC characteristics. To update White Luminance and CFL Ignition Voltage. To add a refference data. To update Timing Characteristics. To update Timing Definition. To update Power consumption. To update DWGs. Lamp cable length:95 mm Based on Internal Spec. as of June 22,1999. Based on Mechanical Drawing as of July 5,1999.
August 27,1999	OEM93C-04	25 , 26	To update DWGs for EMI solution. Based on Mechanical Drawing as of August 18,1999.

1.0 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge.
   Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.11, IEC60950 or UL1950), or be applied exemption conditions of flammability requirements (4.4.3.3, IEC60950 or UL1950) in an end product.
13) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

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2.0 General Description

This specification applies to the 15.0 inches- Color TFT/LCD Module 'ITSX93C'.
This module is designed for a display unit of notebook style personal computer.
The screen format and electrical interface are intended to support the SXGA+(1400(H) x 1050(V)) screen.
Support color is native 262K colors(RGB 6-bit data driver).
All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.
This module does not contain an inverter card for backlight.

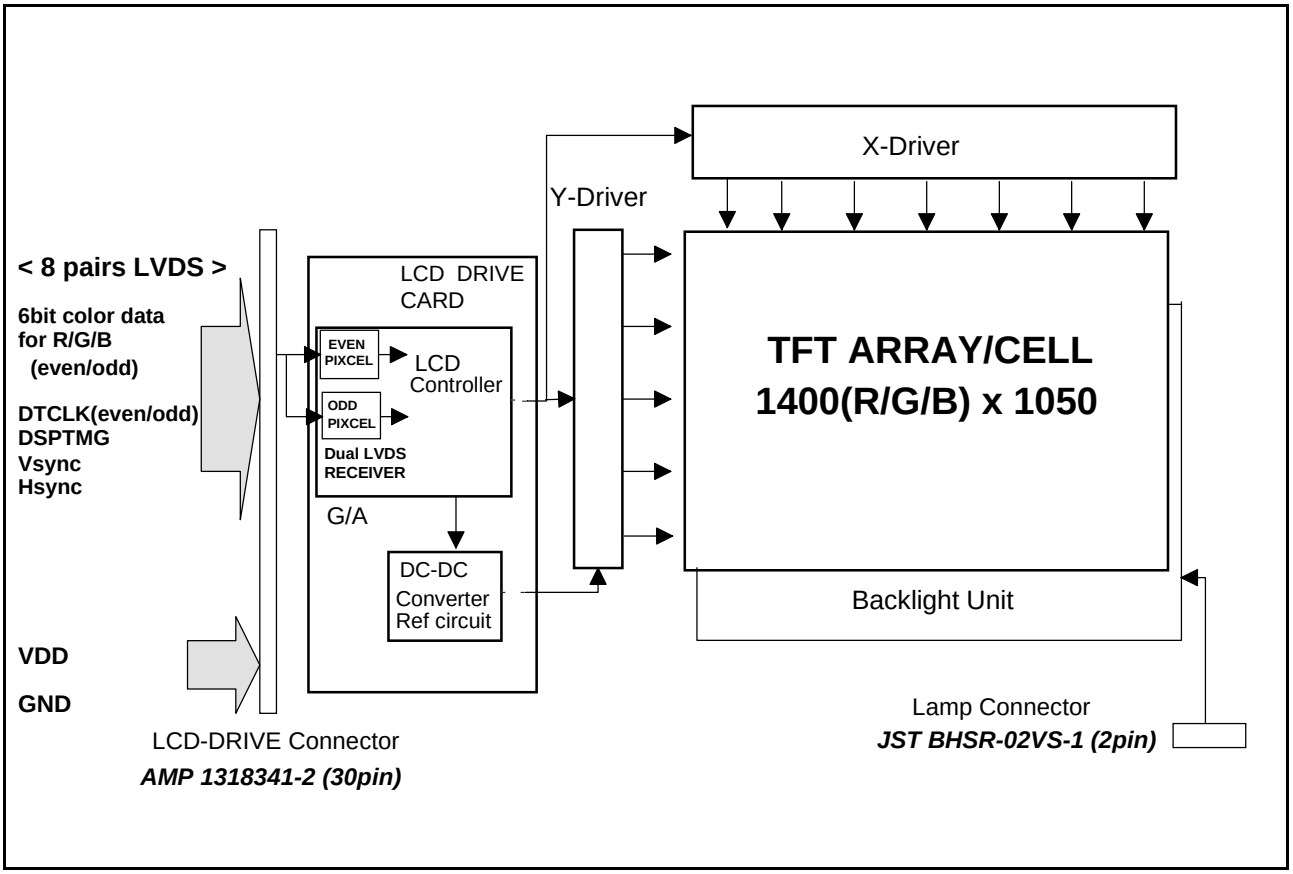
2.1 Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	381(15.0")
Pixels H x V	1400(x3) x 1050
Active Area [mm]	304.5(H) x 228.4(V)
Pixel Pitch [mm]	0.2175(per one triad) x 0.2175
Pixel Arrangement	R,G,B Vertical Stripe
Weight [grams]	740Typ.
Physical Size [mm]	318.5(W) x 241.5(H) x 7.5(D) typ.
Display Mode	Normally White
Support Color	Native 262K colors(RGB 6-bit data driver)
White Luminance [cd/m^2] Design Point 1:(ICFL=3.9mA) Design Point 2:(ICFL=6.5mA)	 90 Typ(center) 85 Typ(5 points average) 150 Typ(center)140 Typ(5 points average)
Contrast Ratio	200 : 1 Typ.
Optical Rise Time/Fall Time [msec]	30Typ.,50 Max.
Nominal Input Voltage VDD [Volt]	+3.3 Typ.
Power Consumption [Watt](VDD Line)	2.0 Typ.,2.8MAX.
Lamp Power Consumption [Watt] (VCFL Line) Design Point 1:(ICFL=3.9mA) Design Point 2:(ICFL=6.5mA)	 2.6Typ.,(W/o inverter loss) 4.0Typ.,(W/o inverter loss)
Typical Power Consumption [Watt] (VDD Line + VCFL Line) Design Point 1:(ICFL=3.9mA) Design Point 2:(ICFL=6.5mA)	 4.6Typ.5.4MAX,(W/o inverter loss) 6.0Typ.6.8MAX,(W/o inverter loss)
Electrical Interface	8 pairs LVDS(Even/Odd R/G/B Data(6bit), 3sync signals, Clock)
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of this 15.0 inches Color TFT/LCD Module. The first LVDS port transmits even pixels while the second LVDS port transmits odd pixels.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	V	
Input Signal Voltage	VIN	-0.3	VDD+0.3	V	
CFL Ignition Voltage	Vs	-	+1,600	Vrms	Note 2
CFL Current	ICFL	-	+7	mAms	
CFL Peak Inrush Current	ICFLP	-	20	mA	
Operating Temperature	TOP	0	+50	℃	Note 1
Operating Relative Humidity	HOP	8	95	%RH	Note 1
Storage Temperature	TST	-20	+60	℃	Note 1
Storage Relative Humidity	HST	5	95	%RH	Note 1
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle wave

Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.
Note 2 : Duration : 50msec Max. Ta=0 ℃

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25**°C condition**:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≥10 (Left) Vertical (Upper) K≥10 (Lower)	40 40 15 30	- - - -
Contrast ratio		200	-
Response Time (ms)	Rising	30	50Max
	Falling	30	50Max
Color Chromaticity (CIE)	Red x	0.577	+-0.040
	Red y	0.338	+-0.030
	Green x	0.310	+-0.030
	Green y	0.563	+-0.030
	Blue x	0.158	+-0.030
	Blue y	0.157	+-0.040
	White x	0.310	+-0.030
	White y	0.346	+-0.030
White Luminance (cd/㎡) ICFL 6.5 mA		150Typ.(TBD) Center 140Typ.(TBD) 5 points average	-

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	AMP
Type / Part Number	1318341-2
Mating Receptacle Manufacture	AMP
Mating Receptacle/Part Number	1318335-2

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Interface Signal Connector

Pin #	Signal Name	Pin #	Signal Name
1	VDD	16	ReCLKIN+
2	VDD	17	GND
3	VDD	18	RoIN0-
4	GND	19	RoIN0+
5	GND	20	GND
6	ReIN0-	21	RoIN1-
7	ReIN0+	22	RoIN1+
8	GND	23	GND
9	ReIN1-	24	RoIN2-
10	ReIN1+	25	RoIN2+
11	GND	26	GND
12	ReIN2-	27	RoCLKIN-
13	ReIN2+	28	RoCLKIN+
14	GND	29	GND
15	ReCLKIN-	30	Reserved

Note: 'Reserved' pins are not allowed to connect any other line.
Voltage levels of all input signals are LVDS compatible (except VDD). Refer to 5.4 " Interface Signal Electrical Characteristics", for voltage levels of all input signals.

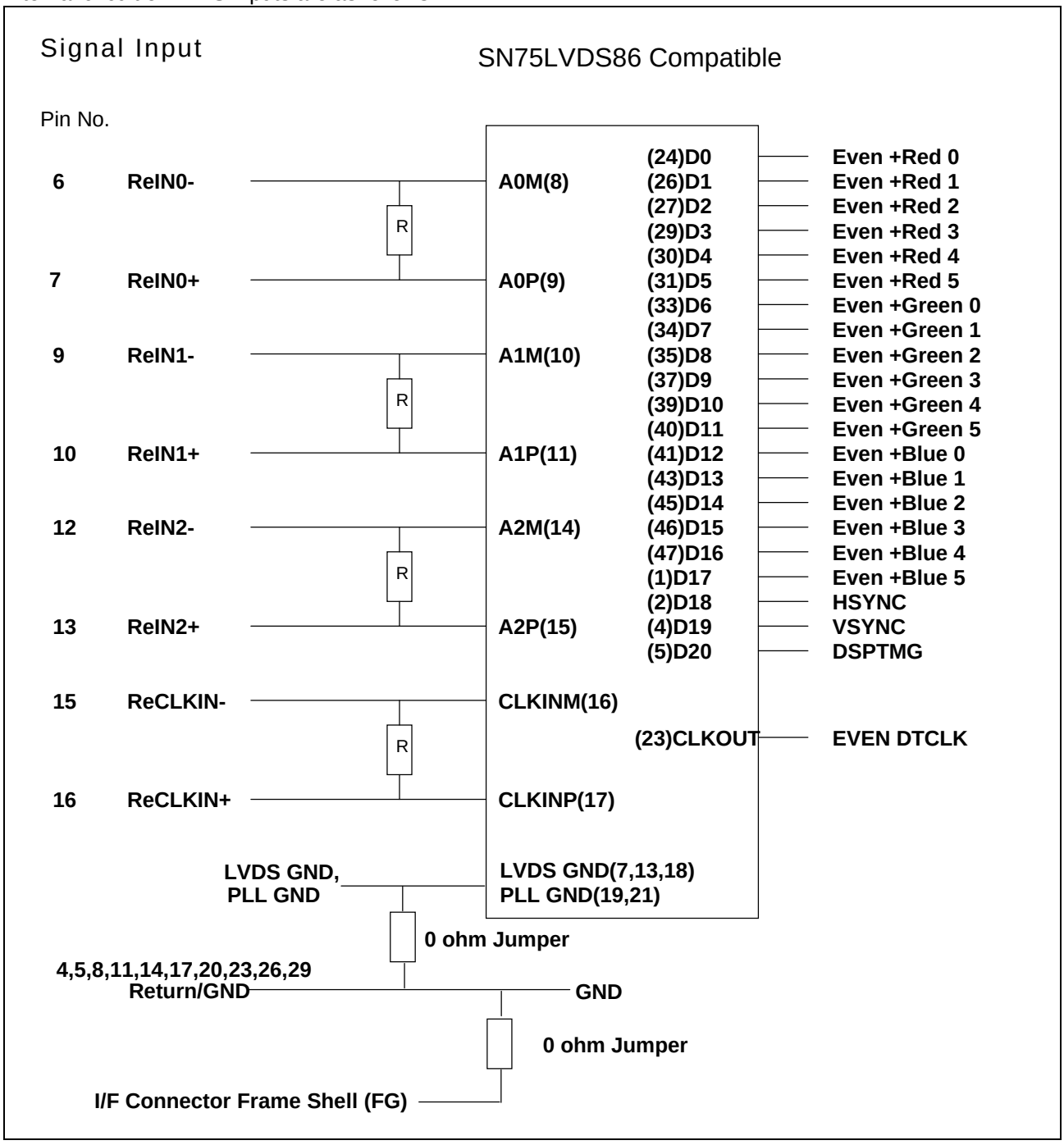
5.3 Interface Signal Description

The module uses a pair of LVDS receiver SN75LVDS86(Texas Instruments) compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84/85 or compatible.

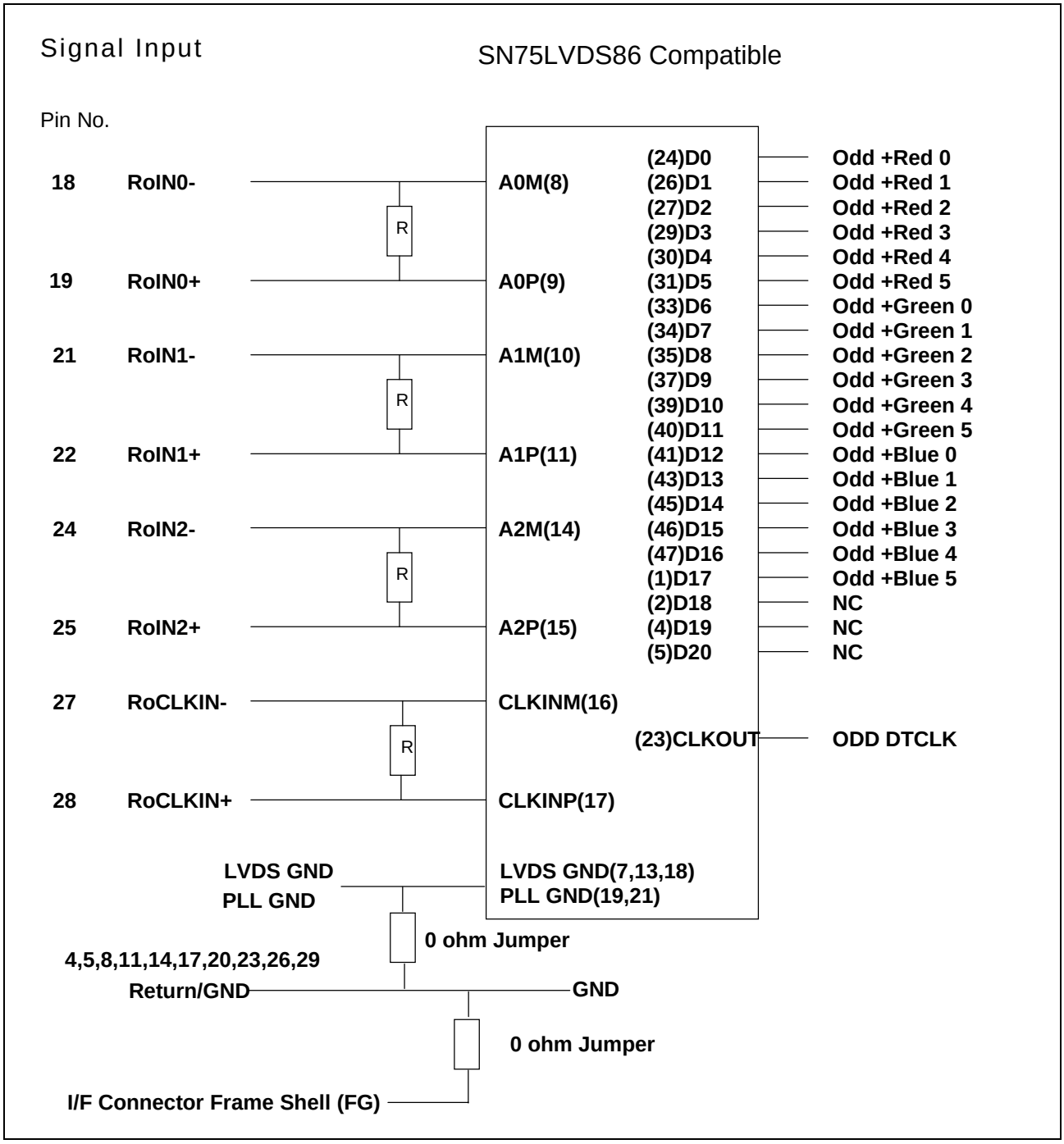
PIN #	SIGNAL NAME	Description
1	VDD	VDD (+3.3V)
2	VDD	VDD (+3.3V)
3	VDD	VDD (+3.3V)
4	GND	Ground
5	GND	Ground
6	ReIN0-	Negative LVDS differential data input (Even R0-R5, G0)
7	ReIN0+	Positive LVDS differential data input (Even R0-R5, G0)
8	GND	Ground
9	ReIN1-	Negative LVDS differential data input (Even G1-G5, B0-B1)
10	ReIN1+	Positive LVDS differential data input (Even G1-G5, B0-B1)
11	GND	Ground
12	ReIN2-	Negative LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
13	ReIN2+	Positive LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
14	GND	Ground
15	ReCLKIN-	Negative LVDS differential clock input (Even)
16	ReCLKIN+	Positive LVDS differential clock input (Even)
17	GND	Ground
18	RoIN0-	Negative LVDS differential data input (Odd R0-R5, G0)
19	RoIN0+	Positive LVDS differential data input (Odd R0-R5, G0)
20	GND	Ground
21	RoIN1-	Negative LVDS differential data input (Odd G1-G5, B0-B1)
22	RoIN1+	Positive LVDS differential data input (Odd G1-G5, B0-B1)
23	GND	Ground
24	RoIN2-	Negative LVDS differential data input (Odd B2-B5)
25	RoIN2+	Positive LVDS differential data input (Odd B2-B5)
26	GND	Ground
27	ReCLKIN-	Negative LVDS differential clock input (Odd)
28	RoCLKIN+	Positive LVDS differential clock input (Odd)
29	GND	Ground
30	Reserved	Reserved

Note:'Reserved' pin is not allowed to connect any other line.
Output signals from any system shall be Hi-Z state when VDD is off.
Input signals of odd and even clock shall be the same timing.

Internal circuit of LVDS inputs are as follows.



The module uses a 100ohm resistor between positive and negative data lines of each receiver input.



The module uses a 100ohm resistor between positive and negative lines of each receiver input.

SIGNAL NAME	Description (ITSX93)
+RED 5 +RED 4 +RED 3 +RED 2 +RED 1 +RED 0 (EVEN/ODD)	RED Data 5 (MSB) RED Data 4 RED Data 3 RED Data 2 RED Data 1 RED Data 0 (LSB) Red-pixel Data: Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0 (EVEN/ODD)	GREEN Data 5 (MSB) GREEN Data 4 GREEN Data 3 GREEN Data 2 GREEN Data 1 GREEN Data 0 (LSB) Green-pixel Data: Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0 (EVEN/ODD)	BLUE Data 5 (MSB) BLUE Data 4 BLUE Data 3 BLUE Data 2 BLUE Data 1 BLUE Data 0 (LSB) Blue-pixel Data: Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK (EVEN/ODD)	Data Clock: The typical frequency is 54MHz. The signal is used to strobe the pixel +data and the +DSPTMG
+DSPTMG	Display Timing: When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync: This signal is synchronized with -DTCLK. Both active high/low signals are acceptable.
HSYNC	Horizontal Sync: This signal is synchronized with -DTCLK. Both active high/low signals are acceptable.
VDD	+3.3V Power Supply
GND	Ground

Note: Output signals from any system shall be Hi-Z state when VDD is off.

5.4 Interface Signal Electrical Characteristics

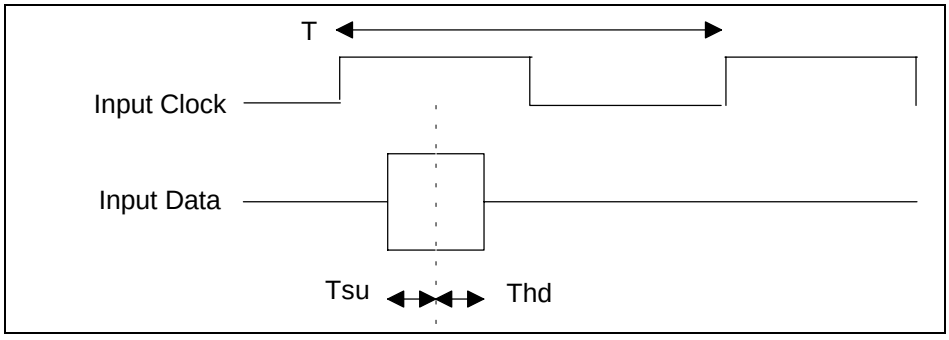
Input signals shall be low or Hi-Z state when VDD is off.
It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	unit
Vth	Defferential Input High Voltage (Vcom=+1.2V)		100	mV
Vtl	Differential Input High Voltage (Vcm=+1.2V)	-100		mV

LVDS Macro AC characteristics are as follows:

	Value	Unit
Clock Frequency (T)	54 Typ.	MHz
Data Setup Time (Tsu)	800 Min	ps
Data Hold Time (Thd)	800 Min	ps

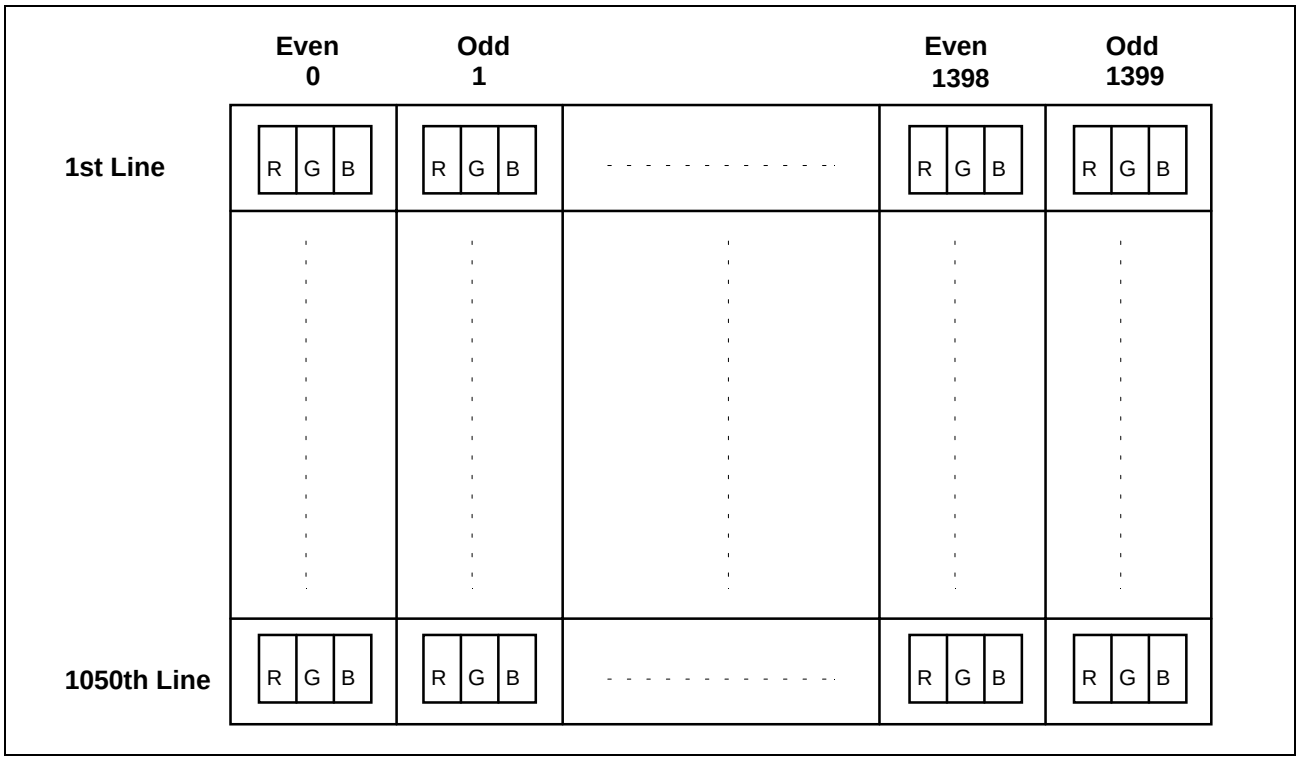


5.5 Signal for Lamp Connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image. Even and odd pair of RGB data are sampled at a time.



7.0 Parameter guide line for CFL Inverter

PARAMETER	MIN	DP-1	DP-2	MAX	UNITS	CONDITION
White Luminance (Center) (5 Points average)	- -	90 85	150 140	- -	cd/m²	(Ta=25℃)
CFL current(ICFL)	3.0	3.9	6.5	7.0	mArms	(Ta=25℃)
CFL Frequency(FCFL)	40	50	50	60	KHz	(Ta=25℃) **Note 1**
CFL Ignition Voltage(Vs)	1,450	-	-	-	Vrms	(Ta= 0℃) **Note 3**
CFL Voltage (Reference)(VCFL)	-	675	610	-	Vrms	(Ta=25℃) **Note 2**
CFL Power consumption(PCFL)	-	2.6	4	-	W	(Ta=25℃) **Note 2**

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 2: Calculated value for reference (ICFL x VCFL = PCFL).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,450 voltage. Lamp units need 1,450 voltage minimum for ignition.

Note 4: DP-1 and DP-2 are IBM recommended Design Points.

*1 All of characteristics listed are measured under the condition using the IBM Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

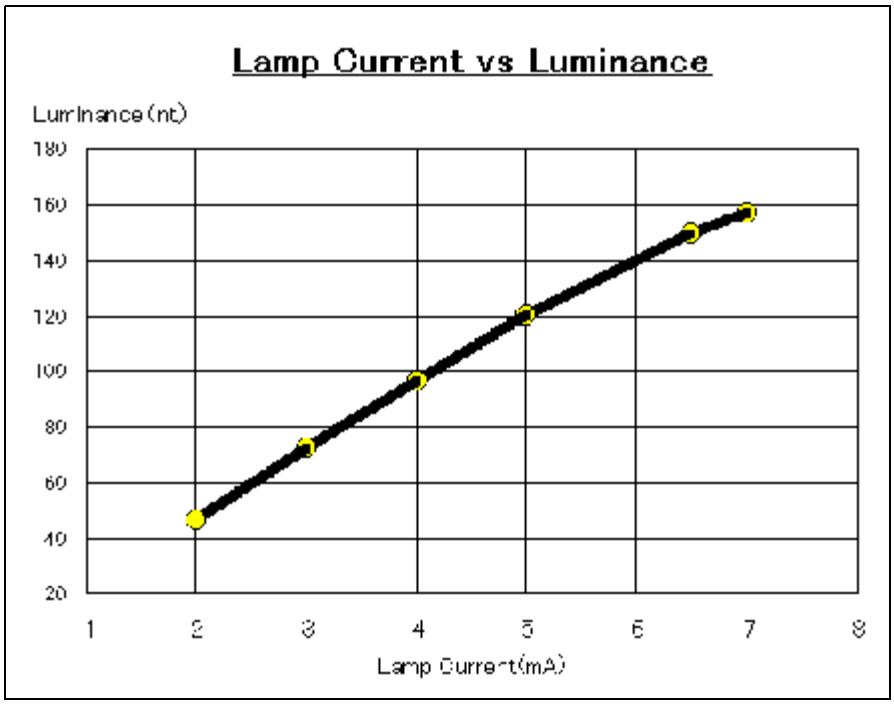
*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

The following chart is CFL current versus the luminance for your reference.



8.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86(Texas Instruments) or equivalent.

8.1 Timing Characteristics

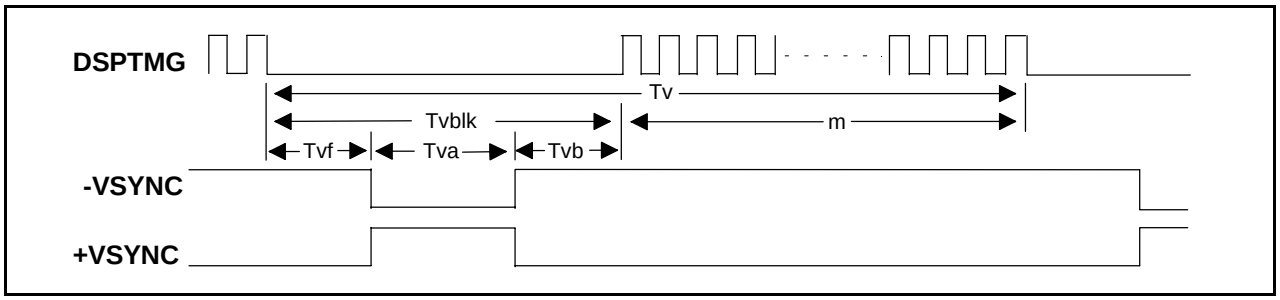
Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Freqency	Fdck		54	60	[MHz]
		Tck	17.5	18.5		[ns]
+V-Sync	Frame Rate	Fv	(56.25)	60	(61)	[Hz]
		Tv	16.39	16.67	17.78	[ms]
		Nv	1059	1066	2047	[lines]
	V-Active Level	Tva	15.78	46.7		[us]
		Nva	1	3		[lines]
	V-Back Porch	Nvb	7	12	63	[lines]
	V-Front Porch	Nvf	1	1		[lines]
+DSPTMG	V-Line	m		1050		[lines]
+H-Sync	Scan Rate	Fh		63.98	69.51	[kHz]
		Th		15.63		[usec]
		Nh	820	844	1023	[Tck]
	H-Active Level	Tha		1.037		[usec]
		Tha	10	56		[Tck]
	H-Back Porch	Thb	8	64		[Tck]
	H-Front Porch	Thf	8	24		[Tck]
+DSPTMG	Display	Thd		12.96		[usec]
+DATA	Data Even/Odd	n		1400		[dots]

Note:
1. Tha+Thb should be less than 1024.
2. Both positive Hsync and positive Vsync polarity is recommended.

8.2 Timing Definition

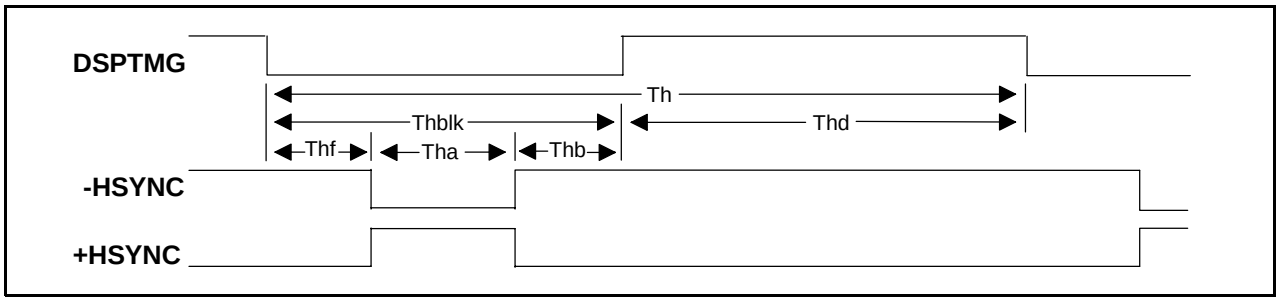
Vertical Timing

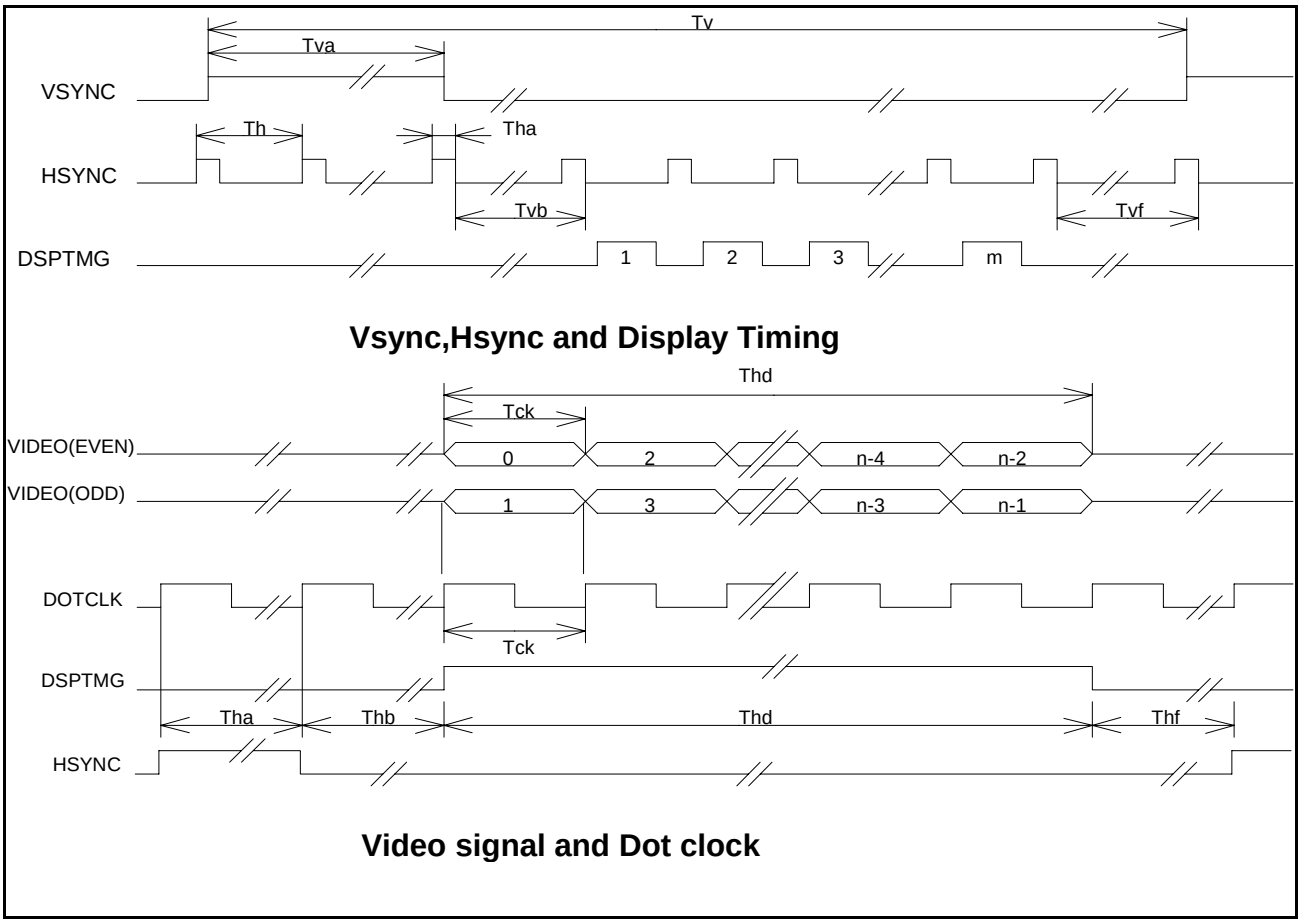
Support mode	Tvblk Vertical Blanking	m Active Field	Tvf VSYNC Front Porch	Tv,Nv Frame Time	Tva VSYNC Width	Tvb VSYNC Back Porch
1400 x 1050 at 60Hz (H line rate : 15.63 us)	0.250 ms (16 lines)	16.411 ms (1050 lines)	0.016 ms (1 line)	16.661 ms (1066 lines)	0.047 ms (3 lines)	0.188 ms (12 lines)



Horizontal Timing

Support mode	Thblk Horizontal Blanking	Thd Active Field	Thf HSYNC Front Porch	Th,Nh H Line Time	Tha HSYNC Width	Thb HSYNC Back Porch
1400 x 1050 Dotclock : 108.000 MHz (54.000MHz x2)	2.667 us (288 dots)	12.963 us (1400 dots)	0.444 us (48 dots)	15.630 us (1688 dots)	1.037 us (112 dots)	1.185 us (128 dots)





Vsync,Hsync and Display Timing

Video signal and Dot clock

9.0 Power Consumption

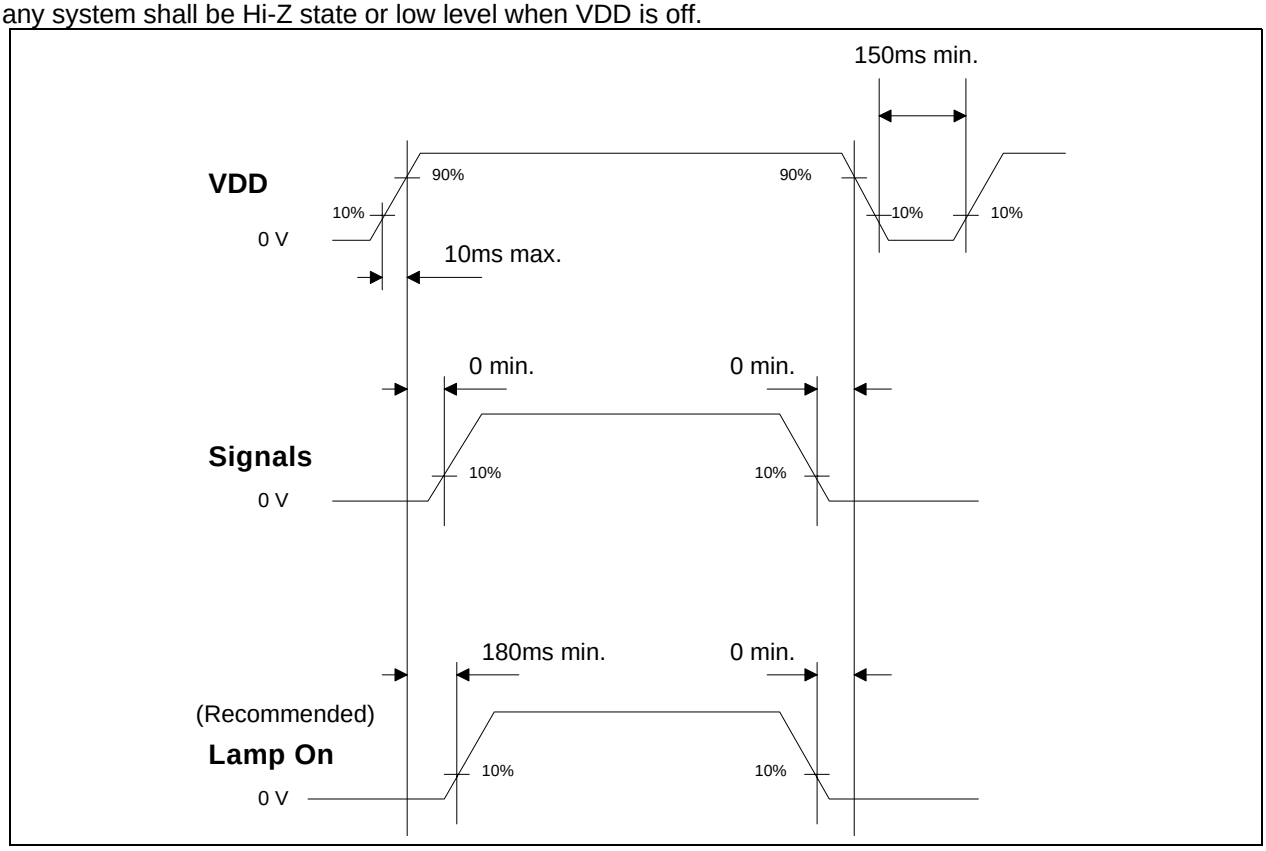
Input power specifications are as follows;

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3	3.3	3.6	V	Load Capacitance 30uF
PDD	VDD Power Max			2.8	W	MAX Pattern **VDD=3.6V**
PDD	VDD Power		2		W	All Black Pattern **VDD=3.3V**
IDD Max	IDD Current Max			85	mA	MAX Pattern **VDD=3.0V**
IDD	IDD Current		600		mA	All Black Pattern **VDD=3.3V**
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

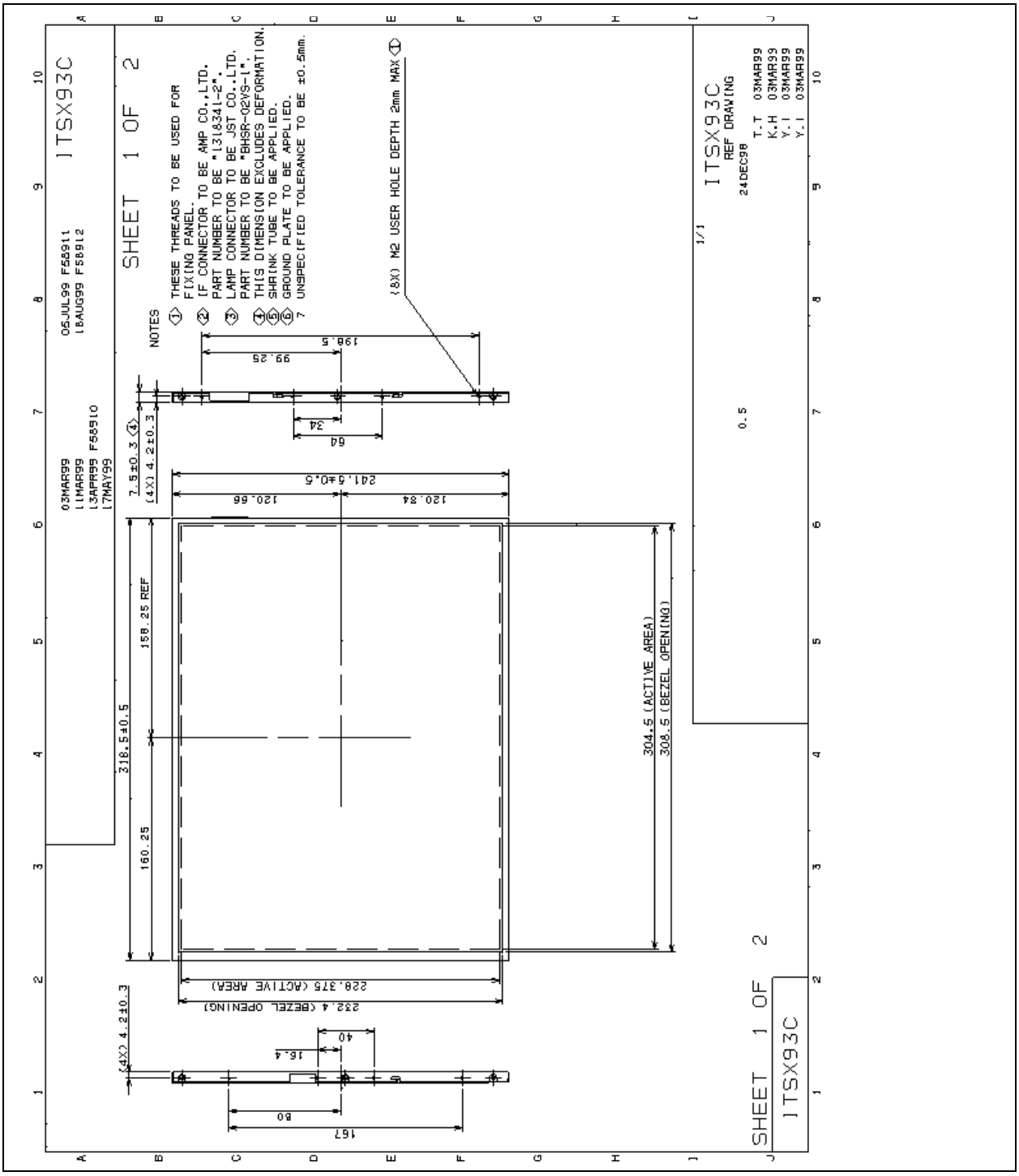
Note: Max Pattern:2 dot Vertical sub-pixel stripe.

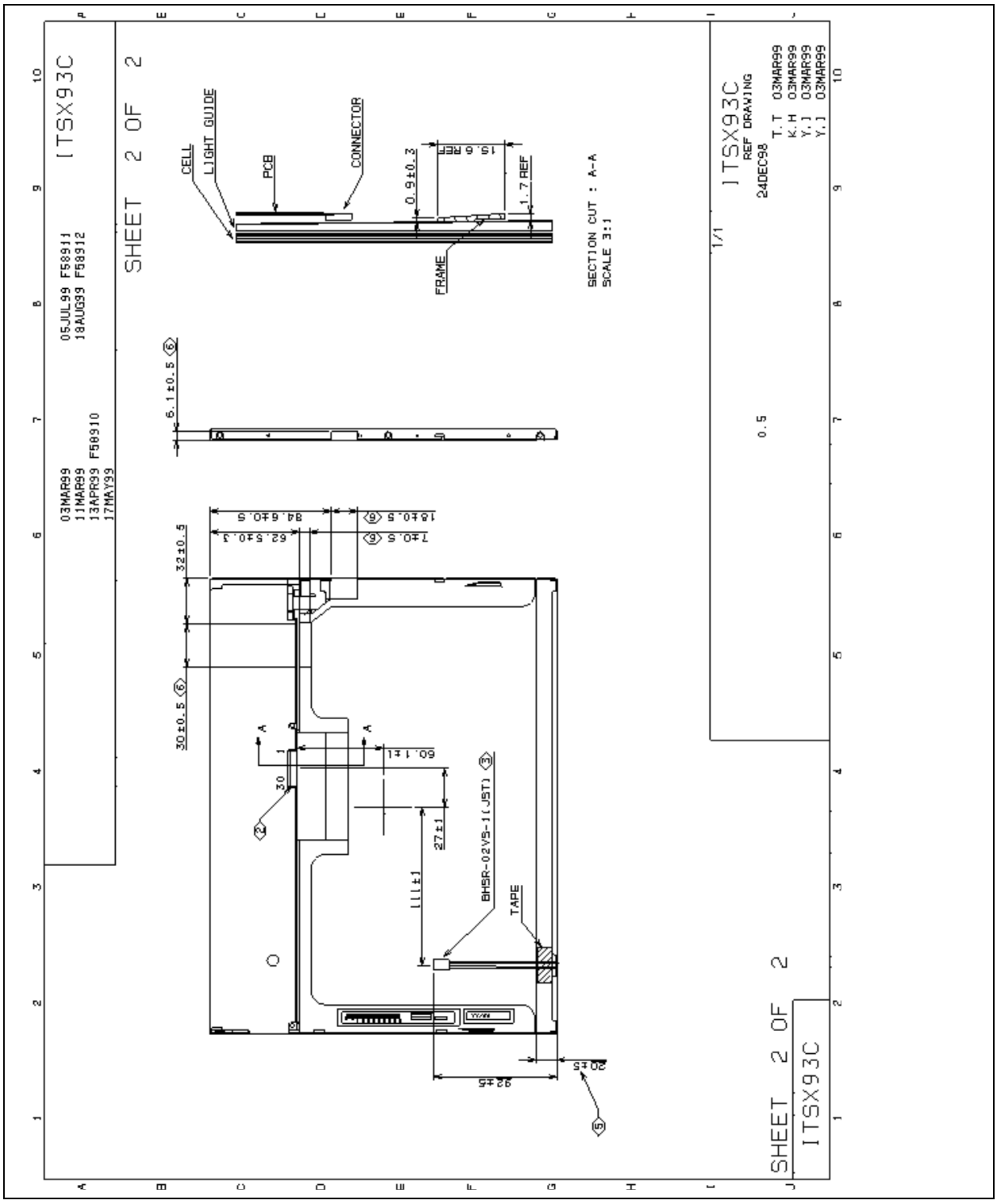
10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics





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