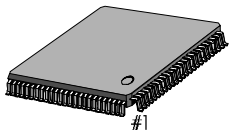
INTRODUCTION

S5L9291X is a signal processing LSI for the CD. Digital processing functions (EFM demodulation, error correction), spindle motor servo processing, compression for anti-rolling and anti-shock, expandable memory control functions (4M, 16M, 64M EDO/Fast Page DRAM and 16M, 32M, 64M, 128M, 256M SDRAM), 10-band EQ (Equalizer) Filter, CD-Text and 1-bit DAC for the CD-MP3 Interface are installed in S5L9291X.

100-TQFP-1414



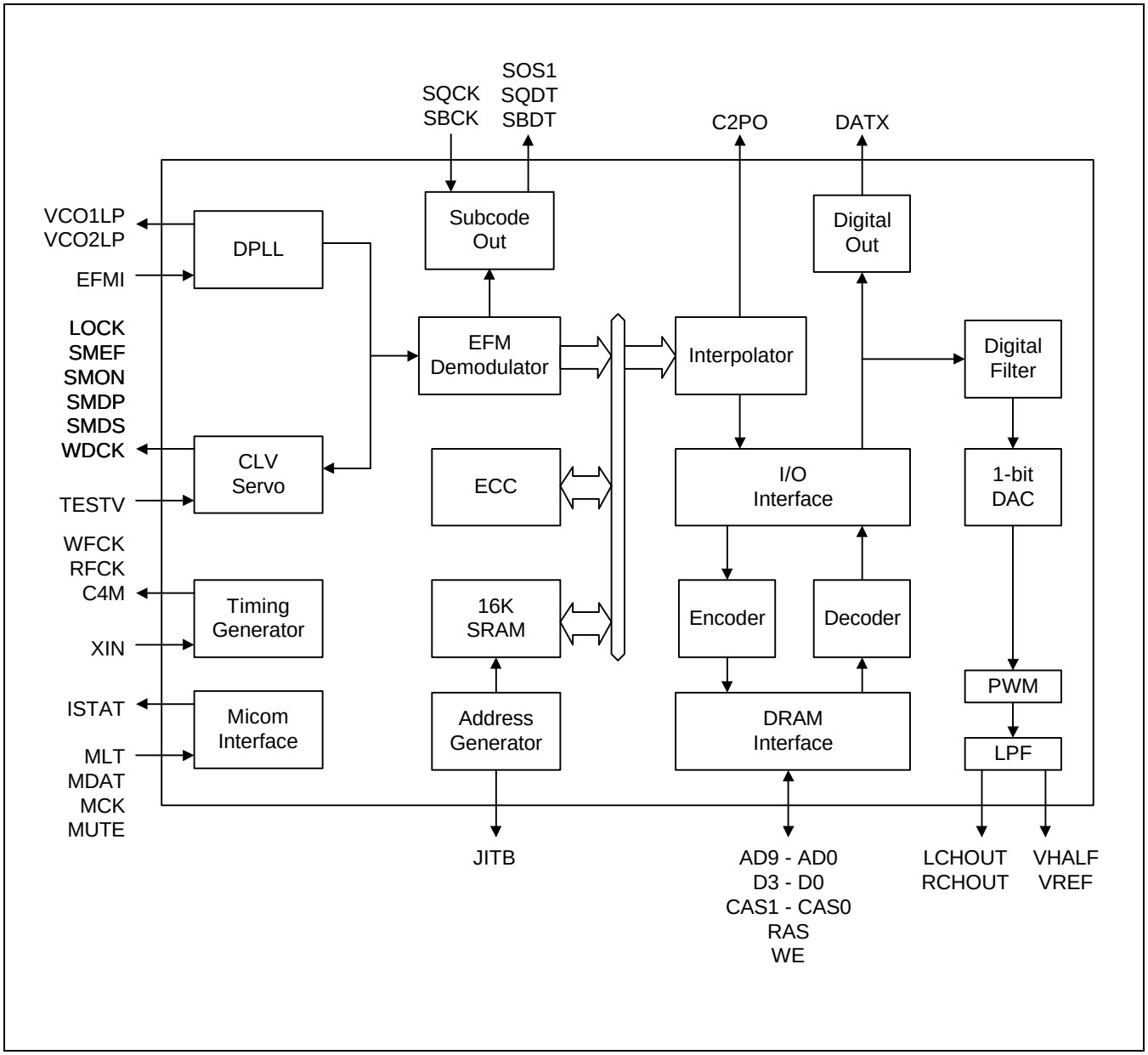
FEATURES

- Signal processing part
  - EFM data demodulation
  - Frame sync detection, protection, insertion
  - Sub code data processing (Q data CRC check, Q data register installed)
  - Error correction (C1: 2 error correction, C2: 4 erasure correction)
  - Installed 16K SRAM for De-interleave
  - Interpolation
  - Digital audio interface
  - CLV/pseudo-CAV servo control
  - Wide capture range digital PLL (± 50%)
  - CD-Text
  - Variable speed CLV Control (×1 to ×2)
  - CD MP3 Interface
- Digital filter, DAC part
  - 4 times over sampling digital filter
  - Digital de-emphasis
  - 10 Band EQ function
  - Sigma-delta stereo DAC installed
  - Audio L.P.F installed
- Memory control part
  - 4/5/6 bit compression and expandable control
  - Full bit control
  - 4M/16M/64M, ×4, ×8, ×16 EDO/FastPage DRAM Support
  - 16M/64M/128M/256M, 32M(16M 2EA), ×8, ×16 SDRAM Support

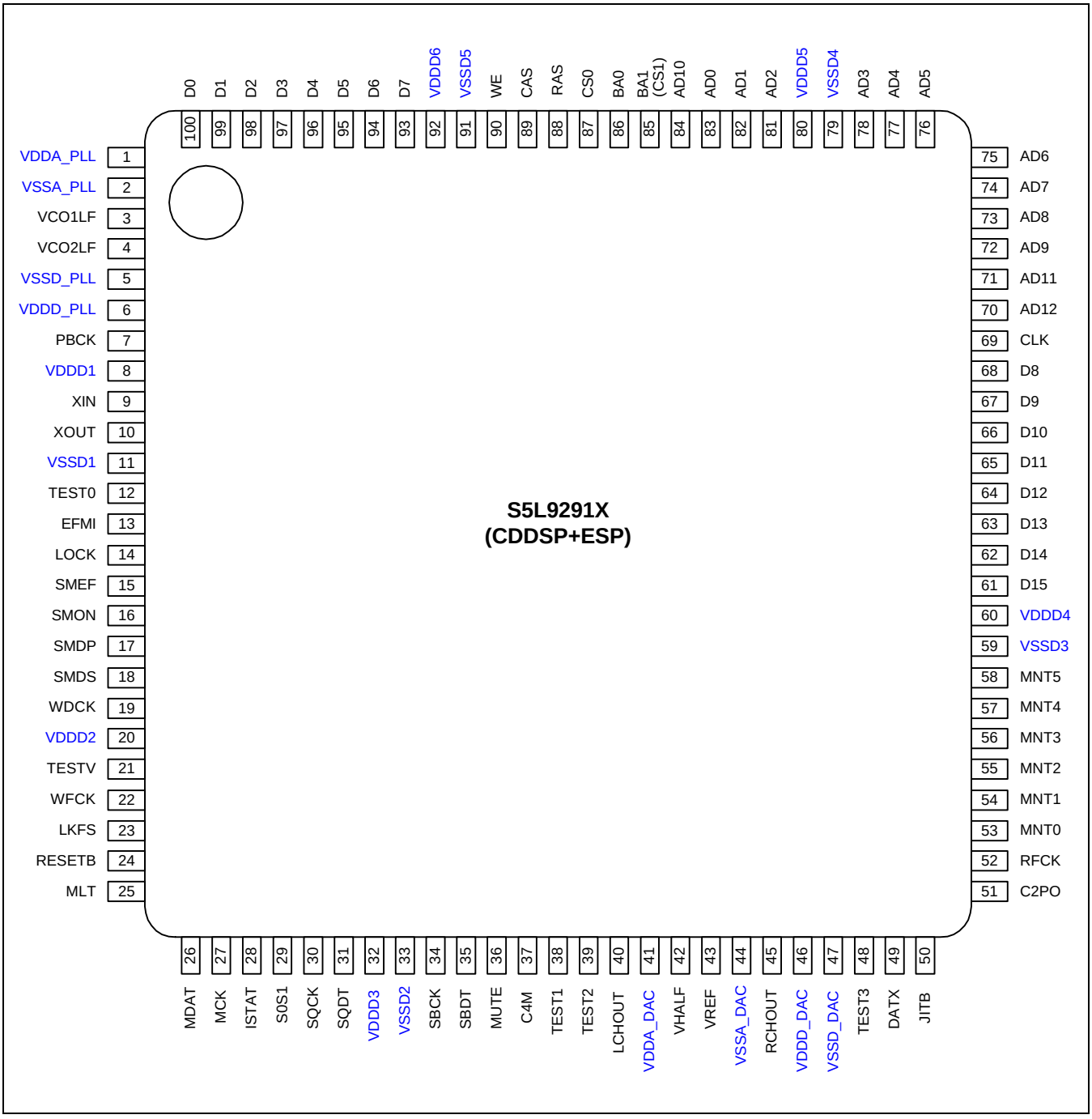
ORDERING INFORMATION

Device	Package	Supply Voltage	Operating Temperature
S5L9291X01-T0R0	100-TQFP-1414	2.7 to 3.3V	-20 to +75°C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	VDDA_PLL	-	Analog power for DPLL
2	VSSA_PLL	-	Analog ground for DPLL
3	VCO1LF	O	Pump out for VCO1
4	VCO2LF	O	Pump out for VCO2
5	VSSD_PLL	-	Digital ground separated bulk bias for DPLL
6	VDDD_PLL	-	Digital power separated bulk bias for DPLL
7	PBCK	O	VCO1/2 clock output (4.3218MHz)
8	VDDD1	-	Digital power
9	XIN	I	X'tal oscillator input (16.9344MHz)
10	XOUT	O	X'tal oscillator output
11	VSSD1	-	Digital ground
12	TEST0	I	Test input
13	EFMI	I	EFM signal input
14	LOCK	O	CLV servo locking status output
15	SMEF	O	LPF time constant control of the spindle servo error signal
16	SMON	O	ON/off control signal for spindle servo
17	SMDP	O	Phase control output for spindle motor drive
18	SMDS	O	Speed control output for spindle motor drive
19	WDCK	O	Word clock output (×1: 88.2kHz, ×2: 176.4kHz)
20	VDDD2	-	Digital power
21	TESTV	I	Various test input
22	WFCK	O	Write base clock output
23	LKFS	O	The lock status output of frame sync
24	RESETB	I	System reset at "L"
25	MLT	I	Latch signal input from micom
26	MDAT	I	Serial data input from micom
27	MCK	I	Serial data receiving clock input from micom
28	ISTAT	O	The internal status output to micom (3-state output)
29	S0S1	I/O	Subcode sync signal (S0+S1) output
30	SQCK	I	Subcode-Q data transferring bit clock input
31	SQDT	O	Subcode-Q data serial output
32	VDDD3	-	Digital Power
33	VSSD2	-	Digital Ground

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
34	SBCK	I	Subcode data transferring bit clock
35	SBDT	I/O	Subcode data serial output
36	MUTE	I	System mute at "H"
37	C4M	O	4.2336MHz clock output
38	TEST1	I	Test Input
39	TEST2	I	Test Input
40	LCHOUT	O	Left-Channel audio output through DAC
41	VDDA_DAC	-	Analog Power for DAC
42	VHALF	O	Reference Voltage output for bypass
43	VREF	O	Reference Voltage output for bypass
44	VSSA_DAC	-	Analog Ground for DAC
45	RCHOUT	O	Right-Channel audio output through DAC
46	VDDD_DAC	-	Digital Power for DAC
47	VSSD_DAC	-	Digital Ground for DAC
48	TEST3	I	Test Input
49	DATX	O	Digital audio data output
50	JITB	I/O	Internal SRAM jitter margin status output
51	C2PO	O	C2 pointer Output
52	RFCK	I/O	Read base clock output
53	MNT0	I/O	Monitoring signal output
54	MNT1	I/O	Monitoring signal output
55	MNT2	I/O	Monitoring signal output
56	MNT3	I/O	Monitoring signal output
57	MNT4	I/O	Monitoring signal output
58	MNT5	I/O	Monitoring signal output
59	VSSD3	-	Digital Ground
60	VDDD4	-	Digital Power
61	D15	I/O	DRAM data Input/Output 15 (3-State Output)
62	D14	I/O	DRAM data input/output 14 (3-State Output)
63	D13	I/O	DRAM data input/output 13 (3-State Output)
64	D12	I/O	DRAM data input/output 12 (3-State Output)
65	D11	I/O	DRAM data input/output 11 (3-State Output)
66	D10	I/O	DRAM data input/output 10 (3-State Output)
67	D9	I/O	DRAM data input/output 9 (3-State Output)

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
68	D8	I/O	DRAM data input/output 8 (3-State Output)
69	CLK	O	SDRAM Clock(4MHz) (3-State Output
70	AD12	O	DRAM address output 12 (3-state output)
71	AD11	O	DRAM address output 11 (3-state output)
72	AD9	O	DRAM address output 9 (3-state output)
73	AD8	O	DRAM address output 8 (3-state output)
74	AD7	O	DRAM address output 7 (3-state output)
75	AD6	O	DRAM address output 6 (3-state output)
76	AD5	O	DRAM address output 5 (3-state output)
77	AD4	O	DRAM address output 4 (3-state output)
78	AD3	O	DRAM address output 3 (3-state output)
79	VSSD4	-	Digital Ground
80	VDDD5	-	Digital Power
81	AD2	O	DRAM address output 2 (3-state output)
82	AD1	O	DRAM address output 1 (3-state output)
83	AD0	O	DRAM address output 0 (3-state output)
84	AD10	O	DRAM address output 10 (3-state output)
85	BA1(CS1)	O	Bank Address 1 / DRAM Chip Select 1 (3-State Output)
86	BA0	O	Bank Address 0 (3-State Output)
87	CS0	O	DRAM Chip Select 0 (3-State Output)
88	RAS	O	DRAM Row Address Selection output (active Low) (3-State Output)
89	CAS	O	DRAM Column Address Selection output 0 (active Low) (3-State Output)
90	WE	O	DRAM Write Enable output (active Low) (3-State Output)
91	VSSD5	-	Digital Ground
92	VDDD6	-	Digital Power
93	D7	I/O	DRAM data Input/Output 7 (3-State Output)
94	D6	I/O	DRAM data Input/Output 6 (3-State Output)
95	D5	I/O	DRAM data Input/Output 5 (3-State Output)
96	D4	I/O	DRAM data Input/Output 4 (3-State Output)
97	D3	I/O	DRAM data Input/Output 3 (3-State Output)
98	D2	I/O	DRAM data Input/Output 2 (3-State Output)
99	D1	I/O	DRAM data Input/Output 1 (3-State Output)
100	D0	I/O	DRAM data Input/Output 0 (3-State Output)

MAXIMUM ABSOLUTE RATINGS

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3 to 3.8	V
Input supply voltage	V_I	-0.3 to V_{DD} + 0.3	V
Operating temperature	T_{OPR}	-20 to 75	°C
Storage temperature	T_{STG}	-40 to 125	°C

ELECTRICAL CHARACTERISTICS

OPERATING CONDITION

Item	Symbol	Operating Range	Unit
Power supply voltage	V_{DD}	2.7 to 3.3	V
Operating temp.	T_{OPR}	-20 to 75	°C

DC CHARACTERISTIC

(V_{DD} = 3.0V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	Condition	Design Values			Unit	Comment
			Min	Typ	Max		
'H' input voltage1	V_{IH}		$0.8V_{DD}$	-	-	V	(Note 1)
'L' input voltage1	V_{IL}		-	-	$0.2V_{DD}$	V	
'H' output voltage1	$V_{OH(1)}$	I_{OH} = -1mA	2.4	-	-	V	(Note 2)
'L' output voltage1	$V_{OL(1)}$	I_{OL} = 1mA	-	-	0.4	V	
'H' output voltage2	$V_{OH(2)}$	I_{OH} = -1mA	2.4	-	-	V	(Note 3)
'L' output voltage2	$V_{OL(2)}$	I_{OL} = 1mA	-	-	0.4	V	
'H' output voltage3	$V_{OH(3)}$	I_{OH} = -1mA	2.4	-	-	V	(Note 4)
'L' output voltage3	$V_{OL(3)}$	I_{OL} = 1mA	-	-	0.4	V	
Input leak current1	I_{LKG1}	V_I = 0-V_{DD}	-10	-	10	uA	(Note 5)
Input leak current2	I_{LKG2}	V_I = 0-V_{DD}	-10	-	10	uA	(Note 6)
Three state output leak current	$I_{O(LKG)}$	V_O = 0-V_{DD}	-10	-	10	uA	(Note 7)

NOTES:

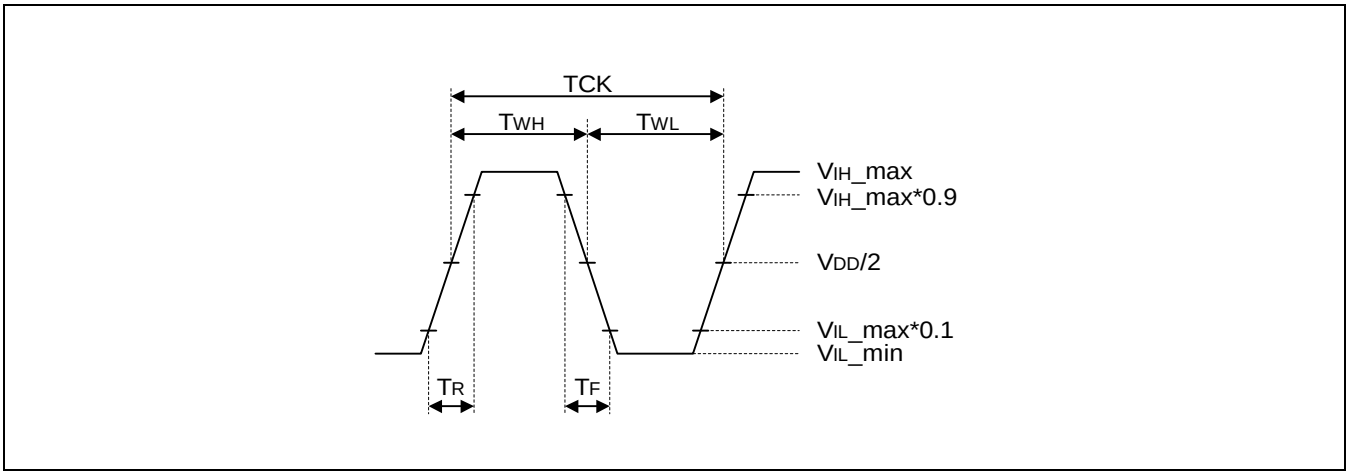
1. Related pins: All input, bi-direction terminal (input mode)
2. Related pins: All output terminal
3. Related pins: All bi-direction terminal (output mode)
4. Related pins: All tri-state output terminal
5. Related pins: All input terminal (excluding XIN)
6. Related pins: XIN
7. Related pins: SMEF, SMDP, SMDS, ISTAT

AC CHARACTERISTIC

When Pulse is Applied to X_{IN}

(Ta = 25°C, V_{DD} = 3.0V, V_{SS} = 0V)

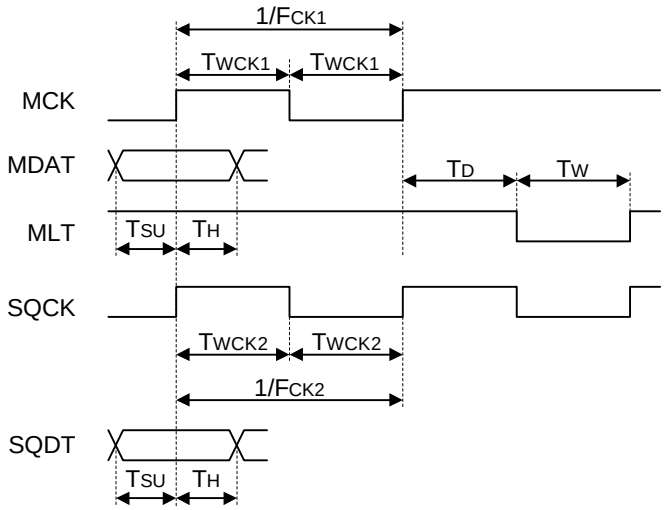
Item	Symbol	Min	Typ	Max	Unit
'H' level pulse width	T_{WH}	13	-	-	ns
'L' level pulse width	T_{WL}	13	-	-	ns
Pulse frequency	T_{CK}	26	-	-	ns
Input 'H' level	V_{IH}	V_{DD}-1.0	-	-	V
Input 'L' level	V_{IL}	-	-	0.8	V
Rising & falling time	T_R,T_F	-	-	10	ns



MCK, MDAT, MLT, SQCK

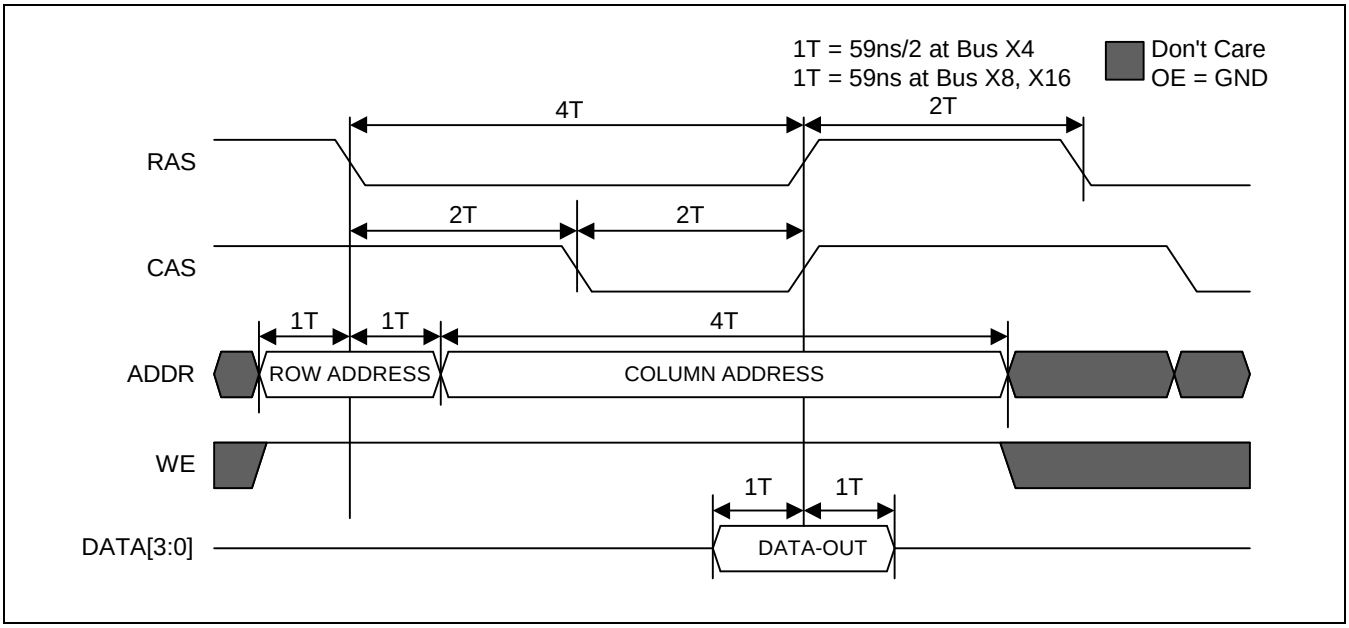
(Ta = 25°C, V_{DD} = 3.0V, V_{SS} = 0V)

Item	Symbol	Max	Typ	Min	Unit
Clock frequency	F_{CK1}	1	-	-	MHz
Clock pule width	T_{WCK1}	-	-	500	ns
Setup time	T_{SU}	-	-	300	ns
Hold time	T_H	-	-	300	Ns
Delay time	T_D	-	-	300	Ns
Latch pulse width	T_W	-	-	1000	ns
SQCK frequency	F_{CK2}	1	-	-	MHz
SQCK pulse width	T_{WCK2}	-	-	500	ns

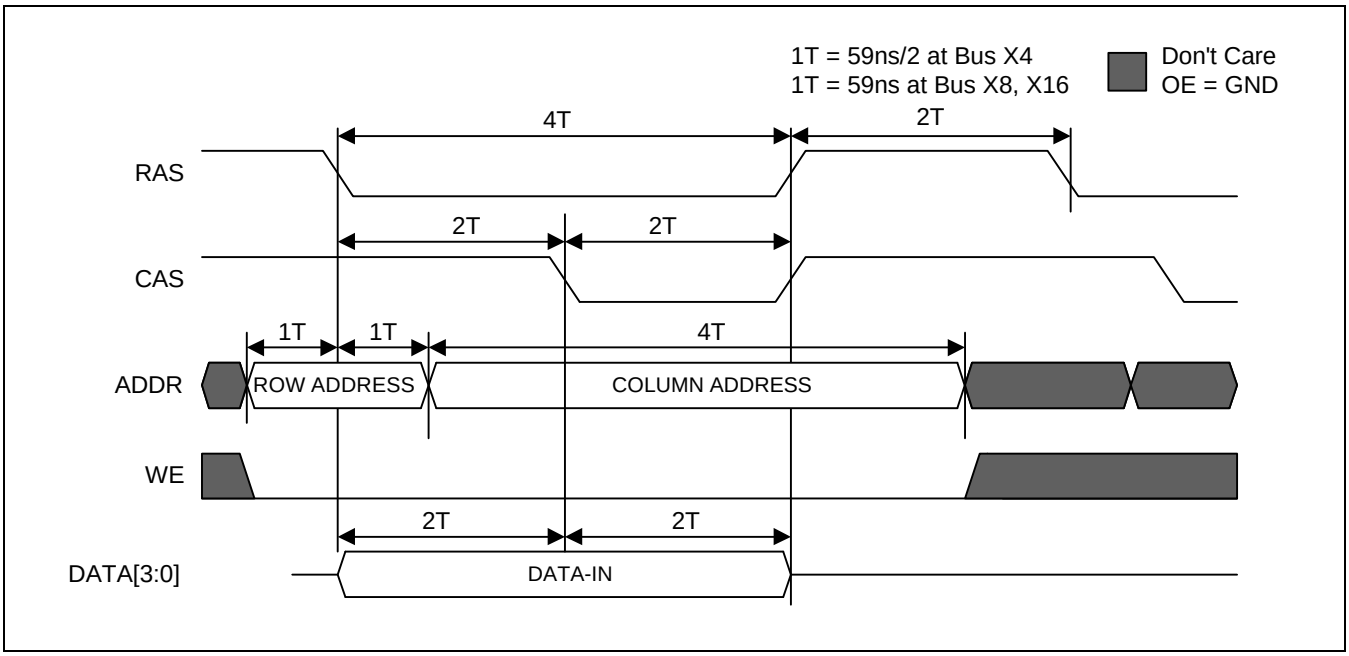


EDO-DRAM, FAST-PAGE DRAM INTERFACE TIMING

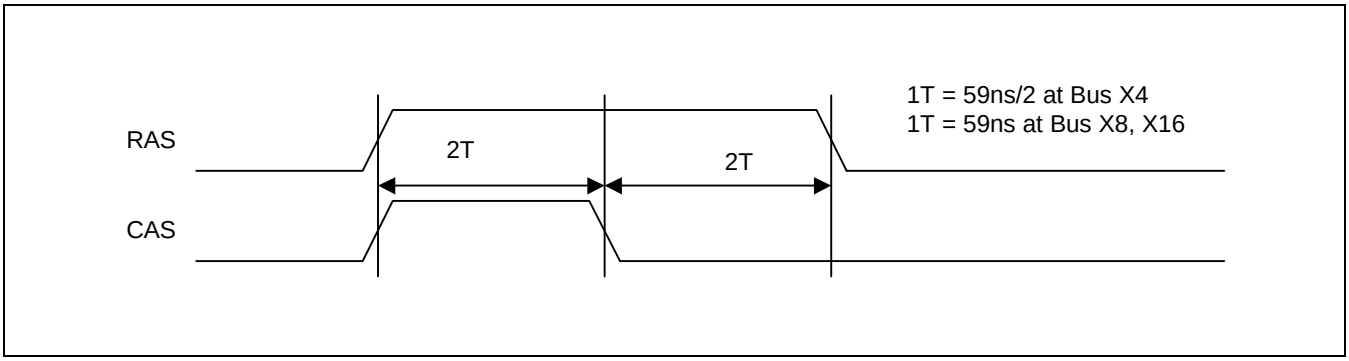
Read Cycle



Write Cycle

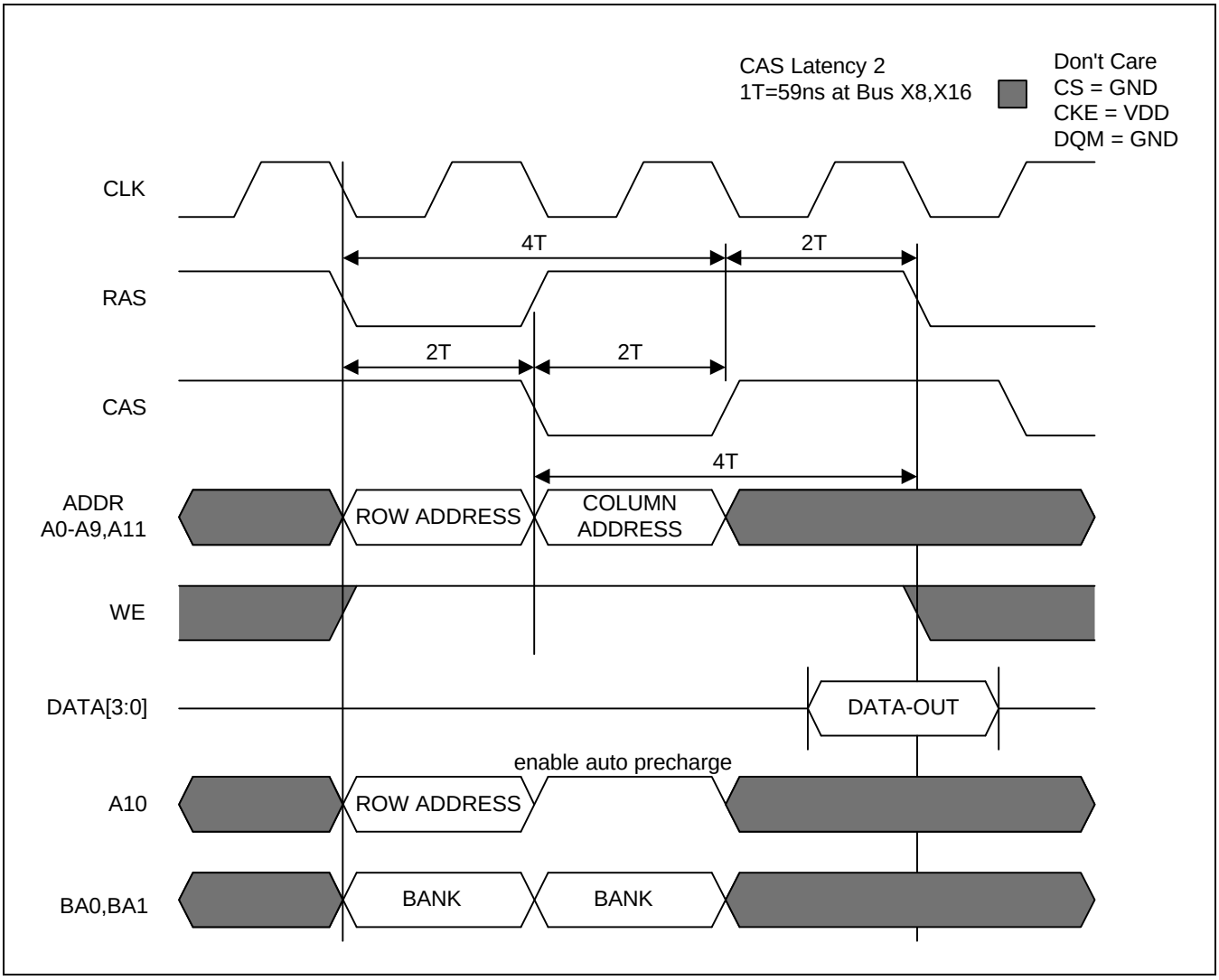


CAS-BEFORE-RAS Refresh Cycle

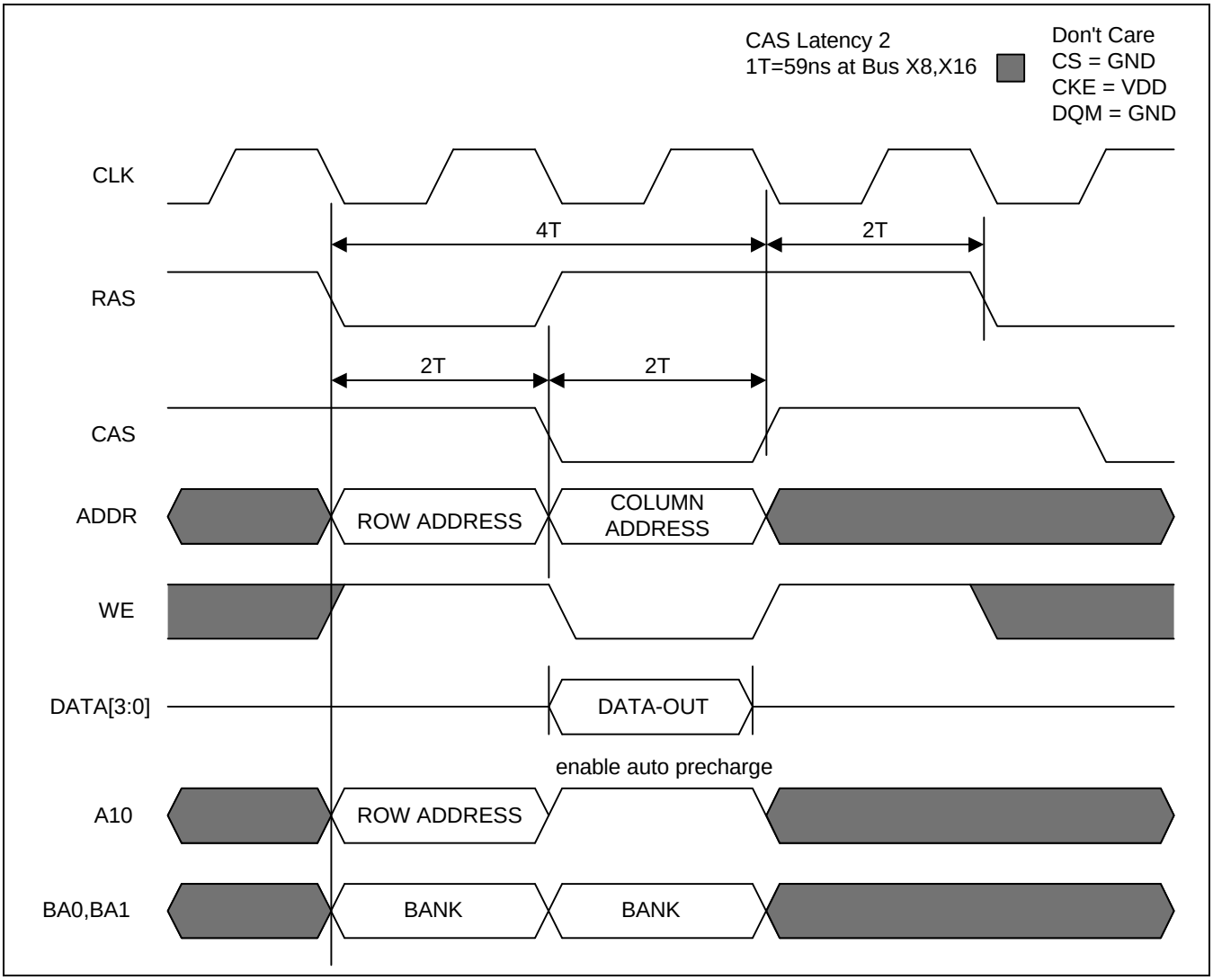


SDRAM INTERFACE TIMING

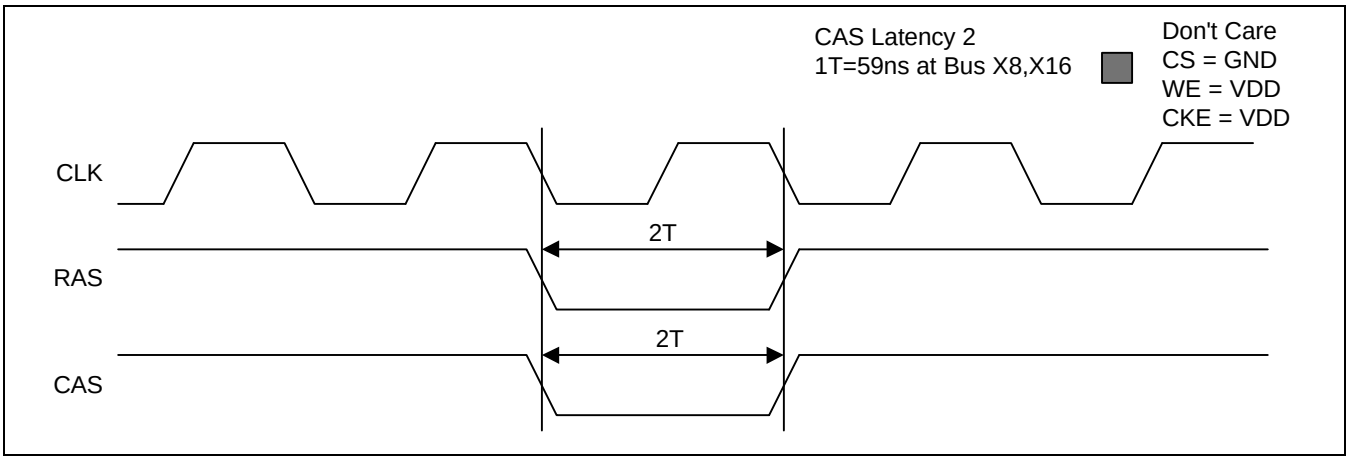
READ (with auto precharge) Cycle



Write (with auto precharge) Cycle



Auto Refresh Cycle

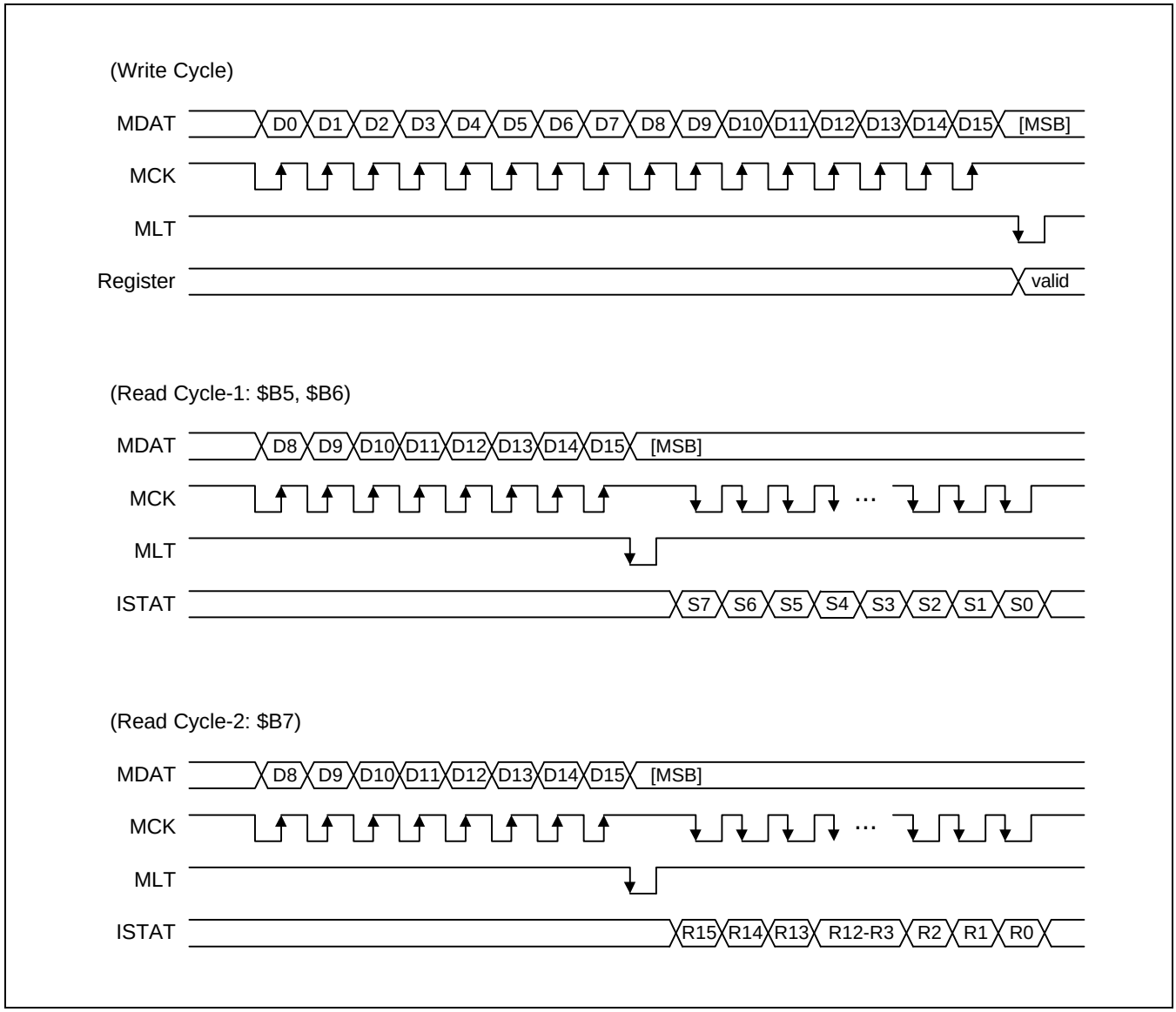


DESCRIPTION OF OPERATION

MICOM INTERFACE

Each command is executed when data and command is input as LSB first according to timing shown in the figure below through MDAT, MCK, and MLT inputs and ISTAT output.

- Read/Write mode support
- Address: 8-bit
- Data: 8-bit (writing), 8/16-bit (reading)



DSP Command

Command	Address	Data								ISTAT
		D7	D6	D5	D4	D3	D2	D1	D0	Terminal
DAC ATTN control	01011101 ($5D)	M5	M4	M3	M2	M1	MO	SOFT ATTN	C MD DIRECT	Hi-Z
DPLL control 1	10001000 ($88)	WIDE	INC3T	PHASE GAIN	DLF gain	ACC 3t	CO1T	CO2T	RETREF	Hi-Z
DPLL control 2	10001001 ($89)	REF98[1:0]		REF[1:0]		MAXTGAIN[1:0]		CAPRANGE[1:0]		Hi-Z
DPLL control 3	10001010 ($8A)	DIVS1[1:0]		DIVP1[5:0]						Hi-Z
DPLL control 4	10001011 ($8B)	DIVS2[1:0]		DIVP2[5:0]						Hi-Z
DPLL control 5	10001100 ($8C)	DIVM2[7:0]								Hi-Z
DPLL control 6	10001101 ($8D)	C MD SPLIT	PHASE ONLY	MRANGE[1:0]		FSREG	PLL TEST	PLL PWRDN1	PLL PWRDN2	Hi-Z
Function control	10010000 ($90)	CDROM	FDEEM	DEEM	ERA OFF	C1PNT	C1PNT SW	-	JITM	Hi-Z
Audio control	10010001 ($91)	MUTE	ZCMT	ZDENL	ATTN	DAC MUTE	V FLAG	DATX MUTE	DATX OEN	S0S1
Frame sync control	10010010 ($92)	FSEL[1:0]		WSEL[1:0]		FSMD[1:0]		SCS[1:0]		LKFS
Mode control 1	10010011 ($93)	CDDSP PWDN	ESP PWDN	EQ PWDN	DAC PWDNB	ECLV	ECLV PD	NCLV	CRCQ	Hi-Z
Mode control 2	10010100 ($94)	MSCK SW	DACCK SW	CLVCK SW	DATCK SW	RFCK SW	C4M SW	JTFRV2	JTFRV1	Hi-Z
CD Text	10010101 ($95)	GEQ SW	GEQ2 SW	-	-	-	-	TEXT ON	TEXT OUT	Hi-Z
CLV gain control	10011000 ($98)	OVSPL	WBN	WPN	LOCK HIGH	OVSPL MS	WB	WP	GAIN	Hi-Z
CLV mode control	10011001 ($99)	UN LOCK	[1:0]	CLV IDLE	PCEN	CM[3:0]				/(PW≥64)
CLV control 1	10011010 ($9A)	STRIO	SMM	PME	SME	PCKSEL[1:0]		PGAIN[1:0]		Hi-Z
CLV control 2	10011011 ($9B)	LC	PML	SML[1:0]		POS	SGAIN[2:0]			Hi-Z
CLV control 3	10011100 ($9C)	POFFSET[7:0]								Hi-Z
CLV control 4	10011101 ($9D)	SPLUS	SDD	PHASEDIV[1:0]		SMOFFSET[3:0]				Hi-Z
CLV control 5	10011110 ($9E)	SOFFSET[7:0]								Hi-Z

DSP Command (Continued)

Command	Address	Data								ISTAT
		D7	D6	D5	D4	D3	D2	D1	D0	Terminal
CLV Control 6	10011111 ($9F)	-	-	-	-	-	-	-	CLV DFCT	Hi-Z
10Band EQ. Filter Gain Level(31Hz)	10100000 ($A0)	-	-	-	EQGB0[4:0]					Hi-Z
10Band EQ. Filter Gain Level(62Hz)	10100001 ($A1)	-	-	-	EQGB1[4:0]					Hi-Z
10Band EQ. Filter Gain Level(125Hz)	10100010 ($A2)	-	-	-	EQGB2[4:0]					Hi-Z
10Band EQ. Filter Gain Level(250Hz)	10100011 ($A3)	-	-	-	EQGB3[4:0]					Hi-Z
10Band EQ. Filter Gain Level(500Hz)	10100100 ($A4)	-	-	-	EQGB4[4:0]					Hi-Z
10Band EQ. Filter Gain Level(1kHz)	10100101 ($A5)	-	-	-	EQGB5[4:0]					Hi-Z
10Band EQ. Filter Gain Level(2kHz)	10100110 ($A6)	-	-	-	EQGB6[4:0]					Hi-Z
10Band EQ. Filter Gain Level(4kHz)	10100111 ($A7)	-	-	-	EQGB7[4:0]					Hi-Z
10Band EQ. Filter Gain Level(8kHz)	10101000 ($A8)	-	-	-	EQGB8[4:0]					Hi-Z
10Band EQ. Filter Gain Level(16kHz)	10101001 ($A9)	-	-	-	EQGB9[4:0]					Hi-Z
10EQ Volume Gain Control	10101010 ($AA)	EQRST	EQON	VOLON	EQVG[4:0]					Hi-Z
DATX & 1-bit DAC Control	10101110 A3→($AE)	-	-	-	-	SC[1:0]		SF[1:0]		Hi-Z
Output Port Control 1	10101111 A9 →($AF)	-	TALK[2:0]			MNT HIZ	-	RFCK OEN	SBDT DUMB	Hi-Z
Play Mode Control	11110000 ($F0)	DS1	DS0	-	-	PLAY SW	DFCK	PLAY1	PLAY0	Hi-Z

ESP Write Command

Command	Address	Data								ISTAT
		D7	D6	D5	D4	D3	D2	D1	D0	Terminal
MS control	10110000 ($B0)	MSWREN	MSWACL	MSRDEN	MSRACL	MSDCN2	MSDCN1	WAQV	MSON	Hi-Z
Data control 1	10110001 ($B1)	DRAM SEL [1:0]		YFLGS	YFCKP	CMP12	DC	COMP [1:0]		Hi-Z
Data control 2	10110010 ($B2)	BBW (0)	WFF (0)	MCP (1)	ESP RESET	JITB OFF	SHOCK EN	SHOCK SW	CMD SHOCK	Hi-Z
Data control 3	10110011 ($B3)	SBCEN	-	-	SBC[4:0]					Hi-Z
Data control 4	1011_0100 ($B4)	DRAM CTRL	RAM TYPE	RAM BANK	RAM_BUS[1:0]		RAM_SIZE[2:0]			Hi-Z

ESP Read Command -I

Command	Address	Data							
		S7	S6	S5	S4	S3	S2	S1	S0
MS state 1	10110101 ($B5)	FLAG6		MSOVFL		DCOMP		MSWIH	MSRIH
MS state 2	10110110 ($B6)	MSEMP		OVFL		ENCOD		DECOD	

ESP Read Command - II

Command	Address	Data
		R[15:0]
MS data residual	10110111 ($B7)	AM[21:6]

MICOM DRAM Write Command

Command	Address	Data								ISTAT
		D1	D2	D3	D4	D5	D6	D7	D8	Terminal
DRAM Access 0	10111010 ($BA)	MWR	MRD	-	-	MAD[11:8]				Hi-Z
DRAM Access 1	10111011 ($BB)	MAD[7:0]								Hi-Z
DRAM Access 2	10111100 ($BC)	WRDATA[15:8]								Hi-Z
DRAM Access 3	10111101 ($BD)	WRDATA[7:0]								Hi-Z

MICOM DRAM READ COMMAND

Command	Address	Data							
		D1	D2	D3	D4	D5	D6	D7	D8
DRAM Access Read Data	10111111 ($BF)	RDDATA[15:0]							

$5D Command

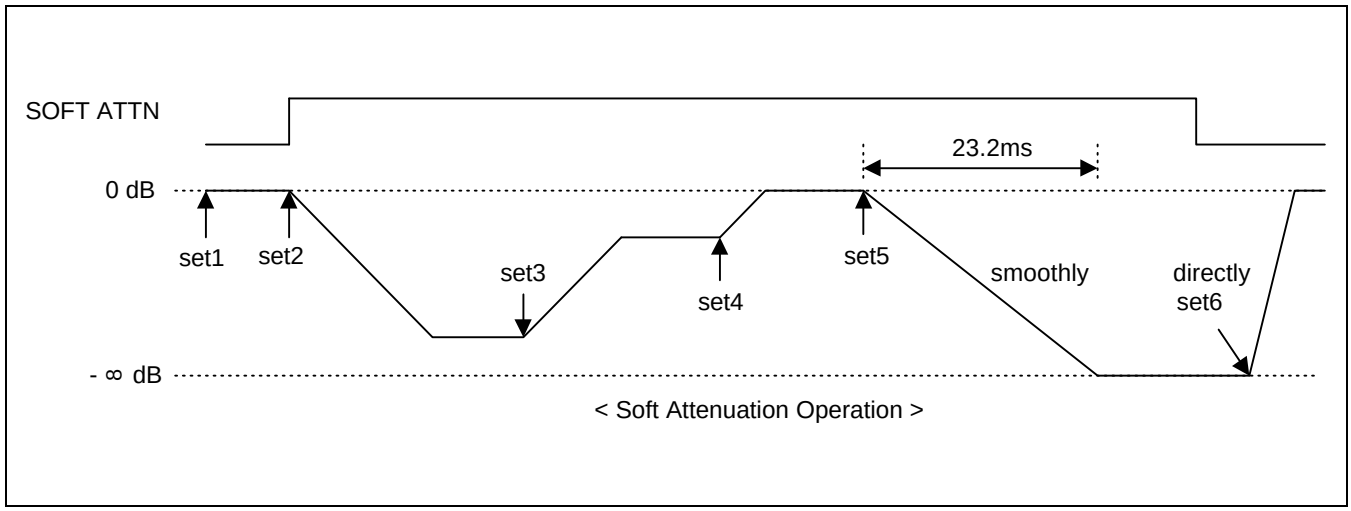
Digital attenuation level control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DAC ATTN control	01011101 ($5D)	M5	M4	M3	M2	M1	M0	SOFT ATTN	CMD DIRECT

MDAT MSB M5 M4 M3 M2 M1 M0 LSB	Attenuation Level (dB)	MDAT MSB M5 M4 M3 M2 M1 M0 LSB	Attenuation Level (dB)
0 0 0 0 0 0	0	1 0 0 0 0 0	-6.30
0 0 0 0 0 1	-0.28	1 0 0 0 0 1	-6.58
0 0 0 0 1 0	-0.42	1 0 0 0 1 0	-6.88
0 0 0 0 1 1	-0.56	1 0 0 0 1 1	-7.18
0 0 0 1 0 0	-0.71	1 0 0 1 0 0	-7.50
0 0 0 1 0 1	-0.86	1 0 0 1 0 1	-7.82
0 0 0 1 1 0	-1.01	1 0 0 1 1 0	-8.16
0 0 0 1 1 1	-1.16	1 0 0 1 1 1	-8.52
0 0 1 0 0 0	-1.32	1 0 1 0 0 0	-8.89
0 0 1 0 0 1	-1.48	1 0 1 0 0 1	-9.28
0 0 1 0 1 0	-1.64	1 0 1 0 1 0	-9.68
0 0 1 0 1 1	-1.80	1 0 1 0 1 1	-10.10
0 0 1 1 0 0	-1.97	1 0 1 1 0 0	-10.55
0 0 1 1 0 1	-2.14	1 0 1 1 0 1	-11.02
0 0 1 1 1 0	-2.32	1 0 1 1 1 0	-11.51
0 0 1 1 1 1	-2.50	1 0 1 1 1 1	-12.04
0 1 0 0 0 0	-2.68	1 1 0 0 0 0	-12.60
0 1 0 0 0 1	-2.87	1 1 0 0 0 1	-13.20
0 1 0 0 1 0	-3.06	1 1 0 0 1 0	-13.84
0 1 0 0 1 1	-3.25	1 1 0 0 1 1	-14.54
0 1 0 1 0 0	-3.45	1 1 0 1 0 0	-15.30
0 1 0 1 0 1	-3.66	1 1 0 1 0 1	-16.12
0 1 0 1 1 0	-3.87	1 1 0 1 1 0	-17.04
0 1 0 1 1 1	-4.08	1 1 0 1 1 1	-18.06
0 1 1 0 0 0	-4.30	1 1 1 0 0 0	-19.22
0 1 1 0 0 1	-4.53	1 1 1 0 0 1	-20.56
0 1 1 0 1 0	-4.76	1 1 1 0 1 0	-22.14
0 1 1 0 1 1	-5.00	1 1 1 0 1 1	-24.08
0 1 1 1 0 0	-5.24	1 1 1 1 0 0	-26.58
0 1 1 1 0 1	-5.49	1 1 1 1 0 1	-30.10
0 1 1 1 1 0	-5.75	1 1 1 1 1 0	-36.12
0 1 1 1 1 1	-6.02	1 1 1 1 1 1	-∞

SOFT ATTN

Enable soft attenuation.
The attenuation level is divided into 64 steps.



< Soft Attenuation Operation >

— CMD DIRECT (option)

L : Attenuate the 1-bit DAC using the soft attenuation block.

H : Apply direct attenuation level to the 1-bit DAC without using the soft attenuation block. This disables the soft attenuation.

$88 Command (Default Values D[7:0] = 0000 0000)

Digital PLL control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 1	10001000 ($88)	WIDE	INC3T	PHASE GAIN	DLF GAIN	ACC3t	CO1T	CO2T	RETREF

Bit	Name	DATA = 0	Data = 1	Comment
D7	WIDE	Normal	Wide	Wide mode Select
D6	INC3T	Normal	New	3T frequency error application
D5	PHASE_GAIN	1/2t	1t	Phase Adjust selection (option)
D4	DLF_GAIN	1/2^10	1/2^9	Digital Loop Filter Gain selection
D3	ACC3t	ignore ± 3t	accept ± 3t	ROM coefficient selection
D2	CO1T	Normal	1T correction	1T → 3T correction
D1	CO2T	Normal	2T correction	2T → 3T correction
D0	RETREF	± 1.1%	± 2.3%	reference when return to M1 = 98

$89 Command (Default Value D [7:0] = 1111 0000)

Digital PLL control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 2	10001001 ($89)	REF98[1:0]		REF[1:0]		MAXTGAIN[1:0]		CAPRANGE[1:0]	

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[7:6]	REF98[1:0]	± 1.7%	± 2.3%	± 3.4%	± 4.6%	Outward reference when M1 = 98
D[5:4]	REF[1:0]	± 1.7%	± 2.3%	± 3.4%	± 4.6%	Outward reference when M1≠ 98
D[3:2]	MAXTGAIN[1:0]	1	1/2	1/4	1/8	MAX T accumulation gain
D[1:0]	CAPRANGE[1:0]	50%	40%	30%	20%	Capture range selection

$8A Command (Default Values D [7:0] = 0101 0110)

Digital PLL control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 3	10001010 ($8A)	DIVS1[1:0]		DIVP1[5:0]					

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[7:6]	DIVS1[1:0]	1	1/2	1/4	1/8	PLL1 post scaler

Bits	Name	Data = 000000 - 111111	Comment
D[5:0]	DIVP1[5:0]	0 - 63	PLL1 pre divider

$8B Command (Default Value D [7:0] = 1001 0110)

Digital PLL control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 4	10001011 ($8B)	DIVS2[1:0]		DIVP2[5:0]					

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[7:6]	DIVS2[1:0]	1	1/2	1/4	1/8	PLL2 post scalar

Bits	Name	Data = 000000 - 111111	Comment
D[5:0]	DIVP2[5:0]	0 - 63	PLL2 pre divider

$8C Command (Default Values D [7:0] = 0101 0000)

Digital PLL Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 5	10001100 ($8C)	DIVM2[7:0]							

Bits	Name	Data = 00000000 - 11111111	Comment
D[7:0]	DIVM2[7:0]	0 - 255	PLL2 main divider

$8D Command (Default Values D [7:0] = 0000 0000)

Digital PLL control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 6	10001101 ($8D)	CMD SPLIT	PHASE ONLY	MRANGE[1:0]		FSREG	PLL TEST	PLL PWRDN1	PLL PWRDN2

CMD_SPLIT (option)

The digital PLL control micom command is automatically applied when the speed is changed($F0) or at Jitter Free2($94).
H : Each DPLL control Micom Commands ($8A, $8B, $8B) are applied using the Micom Interface terminals (MCK, MDAT, MLT).
L : DPLL control Micom Command ($8A, $8B, $8B) is applied automatically inside.

PHASE_ONLY (option)

Controls phase compensation status at DPLL.
H : Phase compensation
L : Phase compensation + Frequency compensation

MRANGE[1:0]

Controls the range of the PLL1 Main Divider M value range

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[5:4]	MRANGE[1:0]	50%	40%	30%	20%	Lock Range

FSREG

Verifies the Frame Sync status(|Thigh-Tlow| $\leq$ 1) at MAX T
H : Verify
L : Ignore

PLLTEST

PLL1 TEST mode
H : TEST (M1<=M2), L : Normal

PLL PWDN1

PLL1 Power Down mode
H : Power Down, L : Normal

PLL PWDN2

PLL2 Power Down mode
H : Power Down, L : Normal

$90 Command DSP Function Control (Default Values D [7:0] = 0000 0000)

DSP Function Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Function control	10010000 ($90)	CDROM	FDEEM	DEEM	ERA OFF	C1PNT	C1PNT SW	-	JITM

CDROM
H: CDROM mode (Interpolation off)
L: CDP mode (Interpolation on)

FDEEM, DEEM
De-Emphasis Automatic control and compulsion control select

FDEEM	DEEM	De-emphasis on/off	Comment
0	0	Off	-
0	1	On/Off	Automatic operate to detect emphasis signal of subcode information
1	0	Off	-
1	1	On	Operate without regard to emphasis signal of subcode information

ERA_OFF:
H: Erasure correction off
L: Erasure correction on

C1PNT :
C1 2 Error correction C1 pointer set/reset control
H: C1PNT = reset L: C1PNT = set

C1PNT_SW:
C1PNT set/reset command input method control
H: TESTV terminal use
L: Micom command use

C1PNT (option)
Mute SRAM Address copy permission (Write base count copy from read base counter)
H: Accept
L: Reject

$91 Command (Default Values D [7:0] = 1000 1000)

Control of each function related to audio data

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Audio control	10010001 ($91)	MUTE	ZCMT	ZDENL	ATTN	DAC MUTE	VFALG	DATX MUTE	DATX OEN

MUTE
DSP Mute Enable Signal
H : DSP MUTE On L : DSP MUTE Off

ZCMT
DSP Zero Cross Mute Enable Signal (Valid when MUTE On)
H : DSP Zero Cross Mute On, L : DSP Zero Cross Mute Off

ZDENL
Zero Detection Mute Disable
H : Disable L : Enable

ATTN
DSP Attenuation Control
H : DSP Attenuation On L : DSP Attenuation Off

DAC MUTE
Sets 1-bit DAC Block input data to 'L'.
H : DAC MUTE On, L : DAC MUTE Off

VFALG
DATX Block Input V-bit Control
H : Set to 'L' L : C2PO

DATX_MUTE
Sets Digital Audio Interface Block Input Data to 'L'.
H : DATX MUTE On L : DATX MUTE Off

DATX_OEN
DATX Output function enable.
H : Enable L : Disable

$92 Command (Default Values D [7:0] = 0000 0000)

Control of functions related to frame sync

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Frame sync control	10010010 ($92)	FSEL[1:0]		WSEL[1:0]		FSMD[1:0]		SCS[1:0]	

FSEL[1:0]: Control of cycle for frame sync protection and insertion

FSEL[1:0]	Control Cycle (Frame)
00	2
01	4
10	8
11	13

WSEL[1:0]: Control of window size related to frame sync protection

WSEL[1:0]	Window Size(t)
00	± 3
01	± 7
10	± 13
11	± 26

FSMD: [1:0] Frame sync detection method control

FSMD [1:0]	Detection Method	Comment
00	Pattern	11t – 11t
01	Compensation	11t – 11t, 10 – 12t, 12t – 10t
10	Cycle 1	10t – 11t, 11t – 12t, 11t – 11t, 11t – 10t, 12t – 11t
11	Cycle 2	cycle 1, 10t – 12t, 12t – 10t

SCS[1:0]

Subcode Sync S0S1 Select

SCS[1:0]	S0S1 (PAD or ESP)	SQOK Sync (to Subcode)
00	S0 or S1	S0 or S1
01	Windowed S0 or S1	S0 or S1
10	Windowed S0 and S1	S0 and S1
11	Windowed S0 and S1	Windowed S0 and S1

$93 Command (Default Values D [7:0] = 0010 0001)

Control of modes of functions in DSP

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Mode control 1	10010011 ($93)	CDDSP PWDN	ESP PWRDN	EQ PWDN	DAC PWDNB	ECLV	ECLV PD	NCLV	CRCQ

CDDSP_PWDN
CDDSP Function Power Down
H : Power Down, L : Power Down Off

ESP_PWDN
ESP function Power Down
H : Power Down On, L : Power Down Off

EQ_PWDN
EQ(Equalizer) Function Power Down
H : Power Down, L : Power Down Off

DAC_PWDNB
1-bit DAC Function Power Down
H : Power Down Off, L : Power Down

ECLV
Emergency CLV Servo, Overflow prevention
H : Repeat output of H, Hi-Z, and L at a regular cycle through the SMDP terminal
L : normal operation

ECLV_PD
SMDP output cycle control at ECLV
H: Bottom Hold cycle (Refer to $98)
L : Peak Hold cycle (Refer to $98)

NCLV
H : CLV phase servo driven by frame sync
L : CLV phase servo driven by base counter

CRCQ
L : SQDT without SQOK
H : SQDT with SQOK (If S0S1 is 'H', SQDT = SQOK)

$94 Command (Default Values D [7:0] = 0000 0000)

Control of function modes in DSP

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Mode control 2	10010100 ($94)	MSCK SW	DACCK, SW	CLVCK SW	DATCK SW	RFCK SW	C4M SW	JTFRV2	JTFRV1

Bit	Value	1-Bit DAC Master Clock
{D7,D6}	1x	Input to RFCK terminal for external clock source $A9 D1(RFCK_OEN) is always "L".
	01	VCO2(PLL Block Clock)
	00	X'tal

Bit	Name	Data = 0	Data = 1	Comment
D5	CLVCK_SW	X'tal	VCO2	Fixed X'tal or variable X'tal conversion
D4	DATCK_SW	X'tal	VCO2	Fixed X'tal or variable X'tal conversion
D3	RFCK_SW	X'tal/VCO	X'tal	Use RFCK clock in CLV servo processing according to jitter free mode
D2	C4M_SW	X'tal	VCO2	Fixed X'tal or variable X'tal conversion
D1	JTFRV2	X'tal	VCO2	Use the variable VCO2 clock in data processing according to VCO1
D0	JTFRV1	X'tal	VCO1	Use VCO1 clock in data processing

$95 Command (Default Values D[7:0] = 0000 0000)

Control of CD Text mode

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CD TEXT	10010101 ($95)	GEQ SW	GEQ2 SW	-	-	-	-	TEXT ON	TEXT OUT

GEQ_SW,GEQ2_SW

Bit	Value	GEQ Master Clock	
		DACCK_SW == 0	DACCK_SW == 1
{D7,D6}	00	XI*2/3(11MHz)	VCO2*2/3
	10	XI(16.9344MHz)	
	X1	Input to RFCK terminal for external clock source $A9 D1(RFCK_OEN) is always "L"	

GEQ Power Optimization Command

Value		CDDSP	External Audio Source(Ex:MP3)		
Sampling Frequency		44.1kHz	32kHz	44.1kHz	48kHz
$94	{D7,D6}	00	10	00	10
$95	{D7,D6}	00	01	00	10

TEXTON

CD Text Function On/Off Signal.
H : CD Text Function Enable,
L : CD Text Function Disable

TEXTOUT

CD TEXT Information Output Control On/Off Signal
H : SQDT with signal CD-Text information transmission Enable,
L : Disable

$98 Command (Default Values D [7:0] = 0000 0111)

Control cycle and gain control in CLV speed mode

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV gain control	10011000 ($98)	OVSPL	WBN	WPN	LOCK HIGH	OVSPL MS	WB	WP	GAIN

OVSPL (option)
Over sampling of CLV output (SMDP, SMDS) cycle by 7.35kHz * 4 and output.
H : Over-sampling Enable L : Over-sampling Disable

WBN (option)
CLV speed mode Bottom Hold cycle control
H : RFCK/64 L : determined by WB

WPN (option)
CLV speed mode Peak Hold cycle control
H : RFCK/8 L : determined by WP

LOCK_HIGH
LOCK PAD as 'H' while Command is input.
H : LOCK High L : Normal Lock

OVSPL_MS (option)
Over-sampling Enable SMDS Output Mode Select
H : PWM (H, L) L : Tri-State (H, Hi-Z, L)

WB
CLV speed mode Bottom Hold Cycle Control
H : RFCK/16 L : RFCK/32

WP
CLV speed mode Peak Hold Cycle Control
H : RFCK/2 L : RFCK/4

{WPN,WP}	Control Cycle	{WBN,WB}	Control Cycle
00	RFCK/4	00	RFCK/32
01	RFCK/2	01	RFCK/16
10	RFCK/8	10	RFCK/64
11	1RFCK/8	11	RFCK/64

GAIN
CLV speed mode SMDS Output GAIN Control
H : 0dB L : -12dB

$99 Command (Default Values D [7:0] = 0000 0000)

CLV mode control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV mode control	10011001 ($99)	UNLOCK [1:0]		CLV IDLE	PCEN	CM[3:0]			

UNLOCK[1:0]
unlock cycle control

UNLOCK[1:0]	Function
00	If LKFS can remain at 'L' for 128 frames, the LOCK is 'L'.
01	If LKFS can remain at 'L' for 96 frames, the LOCK is 'L'.
10	If LKFS can remain at 'L' for 192 frames, the LOCK is 'L'.
11	If LKFS can remain at 'L' for 224 frames, the LOCK is 'L'.

CLV_IDLE
Use to place CLV servo control in idle mode. (Set POS ($9B) to 'H')
H : Output a specific error ($9E, SOFFSET[7:0])to the SMDS terminal, IDLE mode.
L : Normal Mode

PCEN
Phase Error Masking status determination when setting the dead zone.
H : SMDP Phase Error Masking Enable. (When WFCK frequency Error has entered the Dead Zone)
L : SMDP Phase Error Masking Disable.

CM[3:0]
CLV Servo Control Mode Setting

Mode	CM[3:0]	SMDP	SMDS	SMEF	SMON	Function
Forward (KICK)	1 0 0 0	H	Hi-Z	L	H	Spindle motor forward mode
Reverse (BRAKE)	1 0 1 0	L	Hi-Z	L	H	Spindle motor reverse mode
High speed (CLV-H)	1 1 0 0	Speed	Hi-Z	L	H	Rough servo mode at jump
Speed (CLV-S)	1 1 1 0	Speed	Hi-Z	L	H	Rough servo mode at start up
Phase (CLV-P)	1 1 1 1	Phase	Phase	Hi-Z	H	PLL servo mode
XPHSP (CLV-A)	0 1 1 0	Speed Phase	Hi-Z Phase	L Hi-Z	H	Normal play mode (When LOCK is 'H', CLV-P operation and when 'L', CLV-S operation)
VPHSP (CLV-A)	0 1 0 1	Speed Phase	Hi-Z Phase	L Hi-Z	H	Automatic servo mode (When LOCK is 'H' or GFS is 'H', operate in CLV-P, but others, operate in CLV-S')
Stop (STOP)	0 0 0 0	L	Hi-Z	L	L	Spindle motor stop mode

$9A Command (Default Values D [7:0] = 0000 0000)

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 1	10011010 ($9A)	STRIO	SMM	PME	SME	PCKSEL[1:0]		PGAIN[1:0]	

STRIO: Tri-state out enable in phase mode
H: Tri-state
L: PWM

SMM: SMDS mask limit manual setting enable
H: Manual setting
L: Auto setting

PME: SMDP mask enable
H: Mask enable
L: Mask disable

SME SMDS mask enable (dead zone enable)
H: Mask enable
L: Mask disable

PCKSEL[1:0]: MDP resolution clock selection

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[3:2]	PCKSEL [1:0]	CLK4M_ CLV/2	CLK4M_ CLV/4	CLK4M_ CLV/8	CLK4M_ CLV/16	MDP resolution clock selection

PGAIN: SMDP gain setting

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[1:0]	PGAIN[1:0]	1	1/2	1/4	1/8	MDP gain selection

$9B Command (Default Values [7:0] = 0000 0010)

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 2	10011011 ($9B)	LC	PML	SML[1:0]		POS	SGAIN[2:0]		

LC: Lock control
H : 1x → 2x or 2x → 1x then LOCK is forced to 0
L : Normal LOCK control

PML : SMDP mask limit
H : SMDP mask for SMDS error center value ± 50%
L : SMDP mask for SMDS error center value ± 25%

SML: MDS mask limit (dead zone area) at MDS error center value

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[5:4]	SML[1:0]	± 0%	± 6.25%	± 12.5%	± 25%	Dead zone selection

When it enters the dead zone around the data rate, the MDS error value is output as 0.

This minimizes the change in plus(+) and minus(-) frequently generated in the reference data rate and reduces the number of times required for motor control to reduce power consumption.
The phase control also turns off in this dead zone.

POS: MDP output selection
H: Gain controlled SMDP
L: Normal SMDP

SGAIN: SMDS gain setting

SGAIN[2:0]	Gain Value
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

$9C Command (Default Values D [7:0] = 0000 0000)

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 3	10011100 ($9C)	POFFSET[7:0]							

POFFSET[7]:SMDP offset sign
H: Minus (-)
L: Plus (+)

POFFSET[6:0]: SMDP offset absolute value

$9D Command (Default Values D [7:0] = 0000 0000)

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 4	10011101 ($9D)	SPLUS	SDD	PHASEDIV[1:0]		SMOFFSET[3:0]			

SPLUS: SMDS offset plus enable
H: Enable
L: Disable

SDD: SMDS speed down control disable
H: Speed down control disable
L: Speed down control enable

PHASEDIV[5:4]: Phase comparator period setting

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[5:4]	PHASEDIV [1:0]	RFCK/2	RFCK/4	RFCK/8	RFCK/16	Phase comparator period selection

SMOFFSET[3:0]:SMDS mask limit value
0000 - 1111

$9E Command (Default Values D [7:0] = 0000 0000)

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 5	10011110 ($9E)	SOFFSET[7:0]							

SOFFSET[7:0]:
SMDS offset
Output the final error which add the SOFFSET in SMDS error when SPLUS is "1"

$9F Command (Default Values D[7:0]:=0000 0000)

Control of function modes in DSP

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 6	10011111 ($9F)	-	-	-	-	-	-	-	CLV DFCT

CLV_DFCT
If EFM Pulse Width is greater than 64T, the signal is indicates DEFECT and SMDP and SMDS outputs are set to hi-z so, it (ED: what does "it" refer to?) does not control CLV.
H : Defect detection control , L : Normal control

$A0 Command (Default Values D[7:0]:=0000 0000)

10Band EQ. Filter Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10Band EQ. Filter Gain Control 1	10100000 ($A0)	-				Filter Gain Level(31Hz)			

[ED: cannot understand what these sentences are saying.]

$A1 Command (Default Values D[7:0]:=0000 0000)

10Band EQ. Filter Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10Band EQ. Filter Gain Control 2	10100001 ($A1)	-			Filter Gain Level(62Hz)				

[4:0] is the level of Gain which is multiplied by Band1.

$A2 Command (Default Values D[7:0]:=0000 0000)

10Band EQ. Filter Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10Band EQ. Filter Gain Control 3	10100010 ($A2)	-			Filter Gain Level(125Hz)				

[4:0] it is the level of Gain that multiplied by Band2.

$A3 Command (Default Values D[7:0]:=0000 0000)

10Band EQ. Filter Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10Band EQ. Filter Gain Control 4	10100011 ($A3)	-			Filter Gain Level(250Hz)				

[4:0] is the level of Gain which is multiplied by Band3.

$A4 Command (Default Values D[7:0]:=0000 0000)

10Band EQ. Filter Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10Band EQ. Filter Gain Control 5	10100100 ($A4)	-			Filter Gain Level(500Hz)				

[4:0] is the level of Gain which is multiplied by Band4.

$A5 Command (Default Values D[7:0]:=0000 0000)

10Band EQ. Filter Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10Band EQ. Filter Gain Control 6	10100101 ($A5)	-			Filter Gain Level(1KHz)				

[4:0] is the level of Gain which is multiplied by Band5.

$A6 Command (Default Values D[7:0]:=0000 0000)

10Band EQ. Filter Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10Band EQ. Filter Gain Control 7	10100110 ($A6)	-			Filter Gain Level (2kHz)				

[4:0] is the level of Gain which is multiplied by Band 6.

$A7 Command (Default Values D[7:0]:=0000 0000)

10Band EQ. Filter Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10Band EQ. Filter Gain Control 8	10100111 ($A7)	-			Filter Gain Level (4kHz)				

[4:0] is the level of Gain which is multiplied by Band 7.

$A8 Command (Default Values D[7:0]:=0000 0000)

10Band EQ. Filter Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10Band EQ. Filter Gain Control 9	10101000 ($A8)	-			Filter Gain Level (8kHz)				

[4:0] is the level of Gain which is multiplied by Band 8.

$A9 Command (Default Values D [7:0] = 0000 0000)

10Band EQ. Filter Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
10Band EQ. Filter Gain Control 10	10101001 ($A9)	-			Filter Gain Level (16kHz)				

[4:0] is the level of Gain which is multiplied by Band 9.

$AA Command (Default Values D[7:0] = 1000 0000)

Volume Gain Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Volume Gain Control	10101010 ($AA)	EQRST	EQON	VOLON	Volume Gain Control				

D[7] : band equalizer reset
L : reset enable
H : reset disable

D[6] : band equalizer on/off
H : on
L : off

D[5] : digital volume only mode on/off
H : on (no band equalization)
L : off

D[4:0] Volume Gain must be input from 0 to 31.The actual gain value is inside the IC, and the MICOM controls the volume level according to the proper input value.

$AE Command (Default Values D[7:0]:=0000 0000)

1-Bit DAC Mode Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
1-Bit DAC Control	10101110 ($AE)	-	-	-	-	SC[1:0]		SF[1:0]	

SF[1:0]

1-Bit DAC & DATX Sampling Frequency Control

In the Control Status Data, it controls the Sampling Rate(bit24 – bit27) from Digital Audio output signal(DATX)

SF[1:0]	Audio Sampling Frequency
00	44.1 kHz
01	48 kHz
11	32 kHz
Others	Reserved

SC[1:0]

Calibration Range Scale Control

Bits	Name	Data=00	Data=01	Data=10	Data=11	Comment
D[1:0]	SC[1:0]	X1	X2	X4	X0.5	Zero Detection Mute used Available

$AF Command (Default Values D[7:0] = 0000 0000)

Output Signal On/Off Control and Monitor Output Signal Selection

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Output Port Control 1	10101111 ($AF)	-	TALK[2:0]			MNT HIZ	-	RFCK OEN	SBDT DUMB

TALK[2:0]
Monitoring Terminal Output Selection

Bit Name	Output Description					
TALK[2:0]	MNT5	MNT4	MNT3	MNT2	MNT1	MNT0
000	0	0	0	0	0	0
001	FSYNC	EFMFLAG	ECFL3	ECFL2	ECFL1	ECFL0
010	FSYNC	FSDW	ULKFS	EMPH	SQOK	TIM2
011	DAC_SADT	DAC_LRCK	DAC_BCK	ESP_BCK	ESP_LRCK	ESP_SADT
100	Fchange	DIVN98	DIVNFAST	AT2T	EFMIN	EFMOUT
101	DIVN1[5]	DIVN1[4]	DIVN1[3]	DIVN1[2]	DIVN1[1]	DIVN1[0]
110	DAC_SADT	DAC_LRCK	DAC_BCK	DSP_BCK	DSP_LRCK	DSP_SADT
111	FLAG6	SHOCK STATUS	OVFL	EMPTY	DCOMP	MATCH

Signal Name	ESP Off(X1 – X2)	ESP On(X1 – X2)	Comment
DAC_LRCK, DAC_BCK, DAC_SADT	X1 – X2	X1	DSP Output, DAC Input
DSP_LRCK, DSP_BCK, DSP_SADT	X1 – X2	X1 – X2	DSP Output
ESP_LRCK, ESP_BCK, ESP_SADT	-	X1	ESP Output

MNT_HIZ
H : MNT[2:0] Hi-Z Output (Input mode)
L : MNT[2:0] Normal Output

RFCK_OEN
H : RFCK output, L : RFCK input

SBDT DUMB
H : Output Off, L : Output On

$B0 Command (Default Values D [7:0] = 0000 0000)

ESP memory system setting

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
MS control	10110000 ($B0)	MSWREN	MSWACL	MSRDEN	MSRACL	MSDCN2	MSDCN1	WAQV	MSON

MSWREN: Memory system write enable (ADPCM encoding on/off)
H: Write enable
L: Write disable

MSWACL: Memory system write address clear
H: Clear enable
L: Clear disable

MSRDEN: Memory system read enable (ADPCM decoding on/off)
H: Read enable
L: Read disable

MSRACL: Memory system read address clear
H: Clear enable
L: Clear disable

MSDCN2, MSDCN1: Memory system data compare/connection control

MSDCN2	MSDCN1	Mode
0	0	Connection operation disable
0	1	Direct connection
1	0	2-pair connection
1	1	3-pair connection

WAQV: Q data valid
H: Valid
L: Invalid

MSON: Memory system on/off (ESP on/off)
H: On
L: Off

$B1 Command (Default Values D [7:0] = 0000 0000)

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Data control 1	10110001 ($B1)	-		YFLGS	YFCKP	CMP12	-	COMP [1:0]	

YFLGS, YFCK

JITB Signal Input Conditional Control

YFLGS	YFCLK	Mode
0	0	RFCK input negative edge, JITB = 'L'
0	1	RFCK input positive edge, JITB = 'L'
1	0	JITB = 'L'
1	1	JITB = 'H'

CMP12:

12/16 bits comparison connection

H: 12-bit comparison connection

L: 16-bit comparison connection

COMP[1:0]

Encoded data comparison mode control

Comp [1:0]	Mode
0 0	4-bit comparison
0 1	5-bit comparison
1 0	6-bit comparison
1 1	Full bits comparison

$B2 Command (Default Values D[7:0] = 0000 0000)

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DATA Control 2	10110010 ($B2)	BBW	WFF	MCP	ESP RESET	JITB OFF	SHOCK EN	SHOCK SW	CMD SHOCK

BBW

BlkCk(S0S1) Blocking Signal From WAQV.
H : Blocking L : No Blocking .

WFF

WAQV Forced falling signal within a particular region.
H : No Forced Falling. L : Forced Falling.

MCP

Repeat Sound Mis-Connection Protect.
H : Protect. L : No Protect.

ESP RESET

ESP Block Reset while at 'H'.
H : All ESP Block Reset. L : Normal

JITB_OFF

JITB signal is not used for shock processing.
H : JITB signal not used. L : JITB signal used.

SHOCK_EN

Determines whether the external input shock sense signal (SBCK) and Micom Command SHOCK sense signal(CMD_SHOCK) should be used at shock processing
H : Use SHOCK sense signal (Use SBCK lead when using external signal)
L : Not use SHOCK sense signal.

SHOCK_SW

Determines whether to use the SHOCK sense signal should be used as an external lead or as an internal Micom command.
H : Use as external lead(SBCK)
L : Use as internal Micom Command(CMD_SHOCK)

CMD_SHOCK

Internal SHOCK sense signal
H : SHOCK generation L : SHOCK not generated

$B3 Command (Default Values D[7:0] = 0000 0000)

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DATA Control 3	10110011 ($B3)	SBC EN	-	-	SBC[4:0]				

SBC EN: SQOK Bad Count Setting Enable
BlkCk(S0S1) Blocking Signal From WAQV.
H : Enable
L : Not Enable.

SBC: SQOK Bad Count Setting Value := SBC * 2 → Shock

$B4 Command (Default Values D[7:0] = 1000 0000)

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DATA Control 4	10110100 ($B4)	DRAM CTRL	RAM TYPE	RAM BANK	RAM_BUS[1:0]		RAM_SIZE[2:0]		

DRAMCTRL
DRAM CTRL On/Off Control
H : DRAM CTRL On
L : DRAM CTRL Off

RAM[6:0]

RAM_TYPE	RAM_BANK	RAM_BUS[1:0]	RAM_SIZE[2:0]
0 : EDO DRAM	0 : 2 Bank ©ç	00 : x4 ©è	000 : 4M ©è
1 : SDRAM	1 : 4 Bank ©ç	01 : x8	001 : 16M
		10 : x16	010 : 32M(16M 2EA) ©ç
		11 : X16(Reserved)	011 : 64M
			100 : 128M
			101 : 128M(64M 2EA)
			110 : 256M
			111 : 256M(128M 2EA)

1) SDRAM Only, 2) EDO DRAM Only
- 2 Bank in the SDRAM is consist in only 16M and 64M.

$B5 Command (Default Values D [7:0] = 0000 0000)

Command	Address	Data								
		S7	S6	S5	S4	S3	S2	S1	S0	M7-M0
MS state 1	10110101 ($B5)	FLAG6		MSOVFL		DCOMP		MSWIH	MSRIH	-

FLAG6: JITB signal, Reset after $B5H status read.
H: Jitter margin overflow

MSOVFL: Memory system overflow pulse, reset after $B5H status read.
H: Write overflow

DCOMP: Data compare/connection operation
H: Compare/connection operating now

MSWIH: Encoding sequence stop due to internal states
H: Encoding stop

MSRIH: Decoding sequence stop due to internal states, reset after $B5H status read.
H: Decoding stop

$B6 Command (Default Values D [7:0] = 0000 0000)

Command	Address	Data								
		S7	S6	S5	S4	S3	S2	S1	S0	M7-M0
MS state 2	10110110 ($B6)	MSEMP		OVFL		ENCOD		DECOD		-

MSEMP: Valid data empty state
H: Invalid (when RA exceed VWA)
L: Valid

OVFL: Write overflow state
H: Memory full

ENCOD: Encoding sequence operating state
H: Encoding now

DECOD: Decoding sequence operating state
H: Decoding now

$B7 Command

Memory system valid data residual

Command	Address	Data
MS data residual	10110111($B7)	R[15:0]

R[15:0] := Valid Data Accumulated VWA-RA
Anti-shock memory valid data residual

Bit	Function		
	X4	X8	X16
R15	64M Bits	128M Bits	
R14	32M Bits	64M Bits	128M Bits
R13	16M Bits	32M Bits	64M Bits
R12	8M Bits	16M Bits	32M Bits
R11	4M Bits	8M Bits	16M Bits
R10	2M Bits	4M Bits	8M Bits
R9	1M Bits	2M Bits	4M Bits
R8	512K Bits	1M Bits	2M Bits
R7	256K Bits	512K Bits	1M Bits
R6	128K Bits	256K Bits	512K Bits
R5	64K Bits	128K Bits	256K Bits
R4	32K Bits	64K Bits	128K Bits
R3	16K Bits	32K Bits	64K Bits
R2	8K Bits	16K Bits	32K Bits
R1	4K Bits	8K Bits	16K Bits
R0		4K Bits	8K Bits

$BA – $BD Command

Write Data From Micom To External DRAM

Command	Address	Data								ISTAT Terminal
		D7	D6	D5	D4	D3	D2	D1	D0	
DRAM Access 0	10111010 ($BA)	MWR	MRD	-	-	MAD(11:8)				Hi-Z
DRAM Access 1	10111011 ($BB)	MAD [7:0]								Hi-Z
DRAM Access 2	10111100 ($BC)	WRDATA [15:8]								Hi-Z
DRAM Access 3	10111101 ($BD)	WRDATA [7:0]								Hi-Z

MWR

Sign bit for writing the datum of WRDATA[15:0] to DRAM MAD[11:0] address
H : Write Enable
Reset after writing to DRAM

MRD

Storing in RDRDATA[15:0] after datum reading from DRAM MAD[11:0] address
H : Read Enable
Reset after writing to DRAM

MAD[11:0]

DRAM Read/Write Address

WRDATA[15:0]

DRAM Write Data

BF Command

Write Data From External DRAM to MICOM

Command	Address	Data
		D[15:0]
DRAM Access Read Data	1011_1111 ($BF)	RDDATA[15:0]

RDDATA[15:0]

DRAM Read Data

$F0 Command (Default Values D [7:0] = 0000 0000)

Data processing speed control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Play mode control	11110000 ($F0)	DS1	DS0	-	-	PLAY SW	DFCK	PLAY[1:0]	

DS1, DS0

X1, X2 speed control

DS1	DS0	Mode
0	0	1X
1	1	2X

PLAY_SW

Normal Play Mode change by external TEST Pin or Micom Command
This function can be enabled only when TEST[3] Pin is 'L'.
L : TEST Pin control
H : Micom Command control

DFCK

1-bit DAC speed control
H : 2X, L : 1X

PLAY1, PLAY0

Normal Play Mode

Bit Name	TEST Pin	MODE	Comment
PLAY[1:0]	TEST[3:0]		
0 0	0 0 0 0	Normal 1	Serial Audio Data Interface impossible
0 1	0 0 0 1	Normal 2	Serial Audio Data Interface impossible, (3-Band EQ is OFF)
1 0	0 0 1 0	Normal 3	Serial Audio Data Interface possible (Audio Out Block Data Output)
1 1	0 0 1 1	Normal 4	Serial Audio Data Interface possible (ESP Block Data)

EFM DEMODULATION

EMF block is a circuit, which demodulates the EMF signal read from the disc, and is composed of the frame sync detection circuit and the control signal generator circuit.

EFM Demodulation

When the modulated 14 channel bit data is input, they are demodulated to 8 bit data. The demodulated data are classified into two types, the subcode data and audio data. The subcode data is input to the subcode processing block and the audio data is stored in the internal SRAM, after which it is corrected for error.

Frame Sync Detection/Protection/Insertion

Frame sync detection

The data is configured in the unit of frames, of which frame sync, subcode data, audio data, redundancy data are configured in one frame. The frame sync is detected because it is used as the reference signal to synchronize the data output from the frame sync for extracting correct data. (Related Command Register: $92, FSMD [1:0])

Frame sync protection/insertion

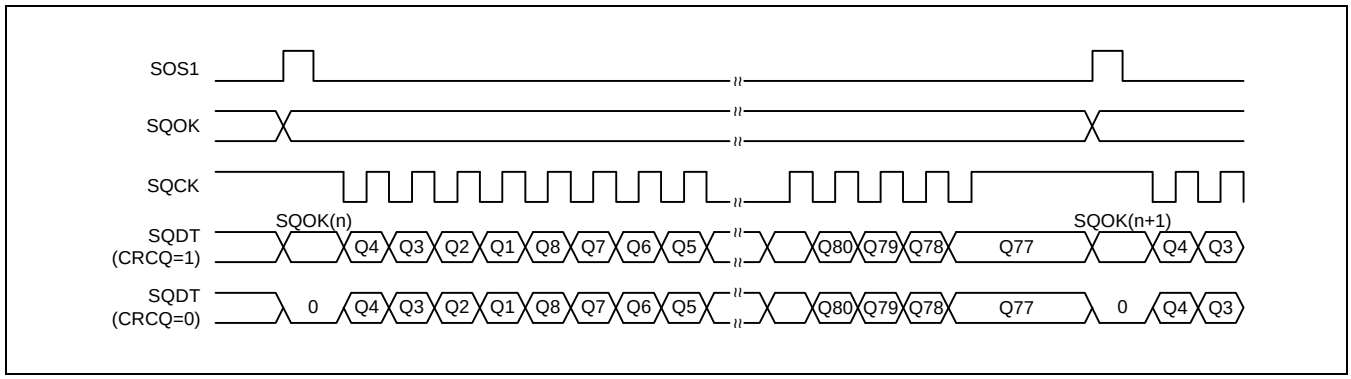
Frame sync may be detected in data besides that of frame sync or omitted due to effects from disc defects or jitters etc. In such cases, frame sync must be protected and inserted. A window must be made according to the $92 command register's WSEL[1:0] to protect frame sync. The data that enter this frame syn is the valid data and the frame sync that exits this window is ignored. If frame sync is not detected in the frame sync protection window, the frame sync made in the internal counter is inserted. If frame sync is inserted continuously to reach the number of frames specified by FSEL[1:0] of the $92 command register, the frame sync protection window is ignored as ULKFS becomes 'H' and the following frame sync detected is immediately accepted. If the frame sync is accepted, ULKFS signal becomes "L" to accept the frame sync detected in the window.

SUBCODE

The subcode sync signal SOS1 is detected in the subcode sync block. After SO is detected, S1 is detected after one frame passes. At this time, SO+S1 signal is output through the SOS1 terminal, and SOS1 signal is output through the SBDT terminal when the SOS1 signal is ‘ H’. Of the data input to the EFMI terminal, 14-bit subcode data is EFM demodulated, synchronized with the WFCK signal to become 8-bit (P, Q, R, S, T, U, V, W) subcode data and output as SBDT through the SBCK clock. Of the 8 subcode data, only Q data is selected and saved in 80 shift registers using the WFCK signal.

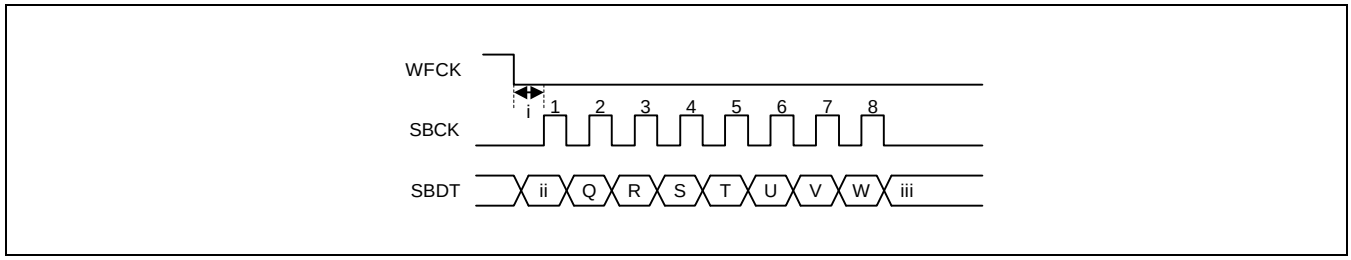
The CRC results of the stored data are synchronized to the S0S1 positive edge and output through the SQOK. If the CRC results are error, ‘L’ is output to the SQOK terminal and, if not, ‘H’ is output. If CRCQ’s $93 command register is ‘H’, CRC results are output through the SQDT terminal from the interval that SOS1 is ‘H’ to the negative edge of SQCK. The following illustrates the timing diagram of the subcode block.

SQCK, SQDT, S0S1 Timing Relationship



NOTE: If CRCQ of the subcode-Q data is ‘H’, SQOK signal is output through SQDT according to the SQCK signal and, if CRCQ is ‘L’, SQOK signal is not output through SQDT.

SBDT, SBCK Timing Relationship



i) SBCK is set to ‘L’ for approximately 10us after WFCK becomes negative edge.
ii) If SOS1 is ‘L’, subcode P is output but , if SOS1 is ‘H’, SOS1 is output.
iii) If more than 7 pulses are input to the SBCK terminal, subcode data P, Q, R, S, T, U, V, W data are output repeatedly.

(Notice)

Value of $B2 Address	BCK Pin
xxxx_x11x	External SHOCK perception signal (ATSC) with it is used
Value of Others	Both SBDT and SBCK are Used.

CD TEXT

If TextOn is 'L' at $95 Command Register, Subcode data are provided through SBCK and SBDT , but if 'H', SBCK and SBDT cannot be used.

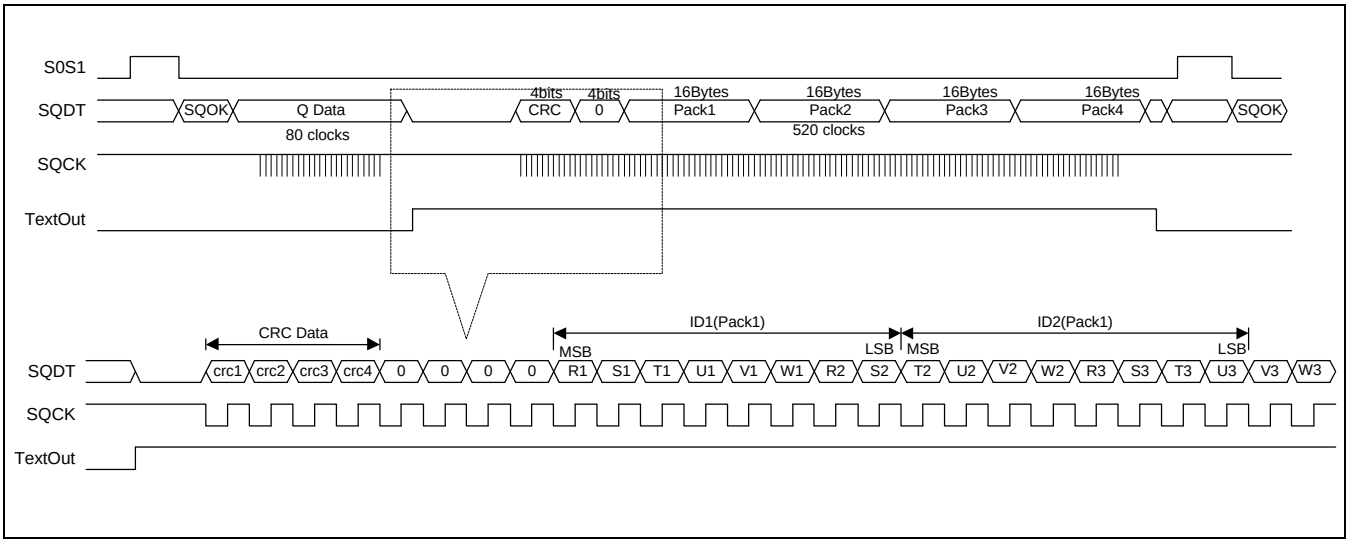
If TextOut is 'L' at $95 Command Resister, Q Datum is provided through SBCK,SQDT, but if 'L', text data, instead of Qdatum, are output.

Text data are output one bit at a time through the SQDT at the Falling Edge of SQCK.

First, CRC 4bit datum, in which each Pack(16bit) may have or not have an error, is output,

and then the real Text data are output from MSB to LSB. For example, if the first bit of CRC is 'H', it means that the first Pack has no error.

SQCK,SQDT,S0S1 Timing Relationship



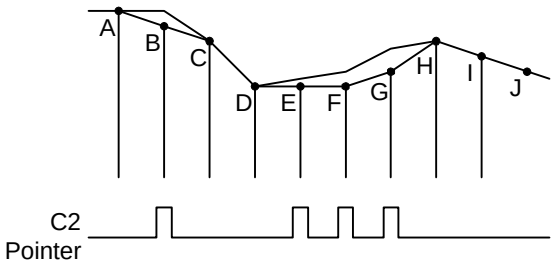
ECC (ERROR CORRECTION CODE)

If the data on the disc is damaged, the ECC (Error Correction Code) block is used to correct data. The CIRC (Cross Interleaved Reed-Solomon Code) is used to correct to 2 errors for C1 (32, 28) and 4 erasures for C2 (28, 24). For error correction, the data is processed in 1 symbol of 8-bit. Furthermore, the ECC block has the pointer function which generates the C1 pointer for C1 correction and C2 pointer for C2 correction. C1 and C2 pointers output flags for ECC processed data to indicate that the data has error. This flag signal is input to the interpolation block and used to process the error data. The error correction results can be monitored through MNT3-MNTO terminals. (Related Command Register: $A9, TALK[2:0])

Mode	MNT3	MNT2	MNT1	MNT0	Comment
	ECFL3	ECFL2	ECFL1	ECFL0	
C10 error	0	0	0	0	C1 flag = reset
C11 error	0	0	1	0	C1 flag = reset
C12 error	0	1	0	0	C1 flag = set/reset
C1 correction impossible	1	0	0	0	C1 flag = set
C20 error	0	0	0	1	C2 flag = reset
C21 error	0	0	1	1	C2 flag = reset
C22 error	0	1	0	1	C2 flag = reset
C23 error	0	1	1	1	C2 flag = reset
C24 error	1	0	0		C2 flag = reset
C2 correction impossible 1	1	0	1	1	C2 flag = set
C2 correction impossible 2	1	1	0	1	Copy C1 flag

INTERPOLATION

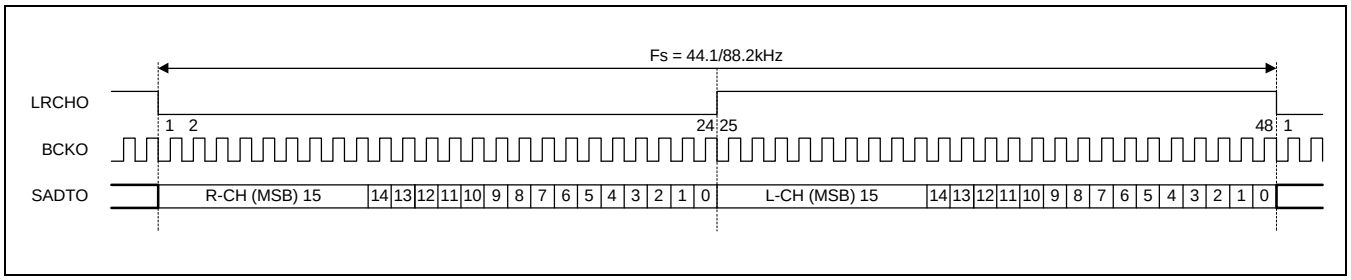
When a burst error is generated on the disc, there are cases when the data cannot be corrected even with the ECC process. The interpolator block uses the ECC'S C2 pointer to interpolate the data. The audio data is input for L/R-ch in 8-bit C2 point, lower data 8-bit, and upper data 8-bit order, respectively, to the data bus. If C2PO terminal is 'H' and there is only one error, the average value is interpolated, but, if there are 3 continuous errors, all values are hold interpolated. If LRCK is 'L' for one LRCK cycle, R-ch data is output, and, if 'H', L-ch is output. The timing clock in the interpolator block is shown below.



B: Average value interpolation
F = E = D: All value hold interpolation
G: Average value interpolation

SERIAL AUDIO DATA INTERFACE

Converts the 16-bit parallel data sent by the interpolation block to serial data. S5L9291X supports the following serial audio data format. The LRCK frequency for 1X is 44.1kHz and 2X is 88.3kHz.



MUTE & ATTENUATION

The mute signal can be accepted in two ways.

- When mute port (pin #: 44) is “H”
- When $91 command register’s D7 bit is “H”

The audio data is either muted or reduced based on the mute signal and ATTN signal of the $91 command register.

Zero Cross Mute

After ZCMT of the $91 command register is set to ‘H’, and the mute signal becomes ‘H’, and the audio data top 6-bit all are either ‘L’ or ‘H’, the audio data is muted.

Mute

When ZCMT of $91 command register is ‘L’ and the mute signal becomes ‘H’, the audio data is muted.

Attenuation

The signal is reduced by the ATTN of $91 command register and mute signals.

ATTN	MUTE	Degree of Attenuation [Db]
0	0	0
0	1	-∞
1	0	-12
1	1	-12

Digital Attenuation

By referencing command register $5D, $2^6 = 64$ attenuation levels can be controlled. When the reset signal becomes ‘L’, the attenuation level is initialized to 0Db.

$$\text{Gain} = 20 \times \log\frac{\text{Dattn}}{64}$$

Soft Mute

When the digital attenuation level is controlled from 0Db to -∞Db, the soft mute function can be configured.

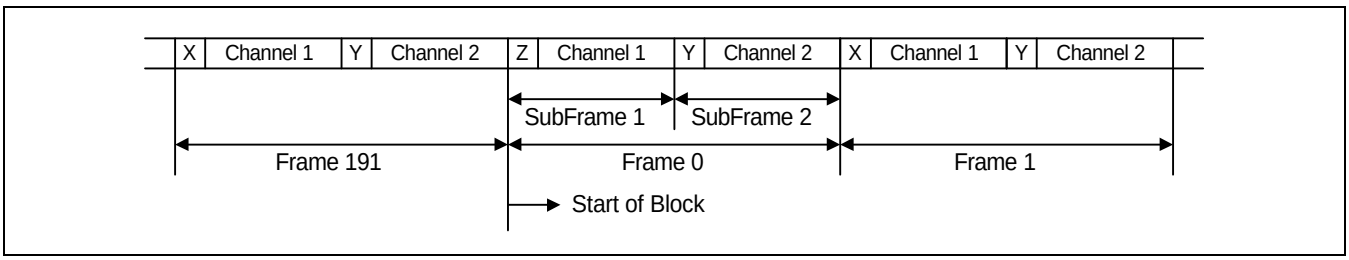
DAC Mute

When the $91 command register's DAC_MUTE is "H", only the DAC block is muted.

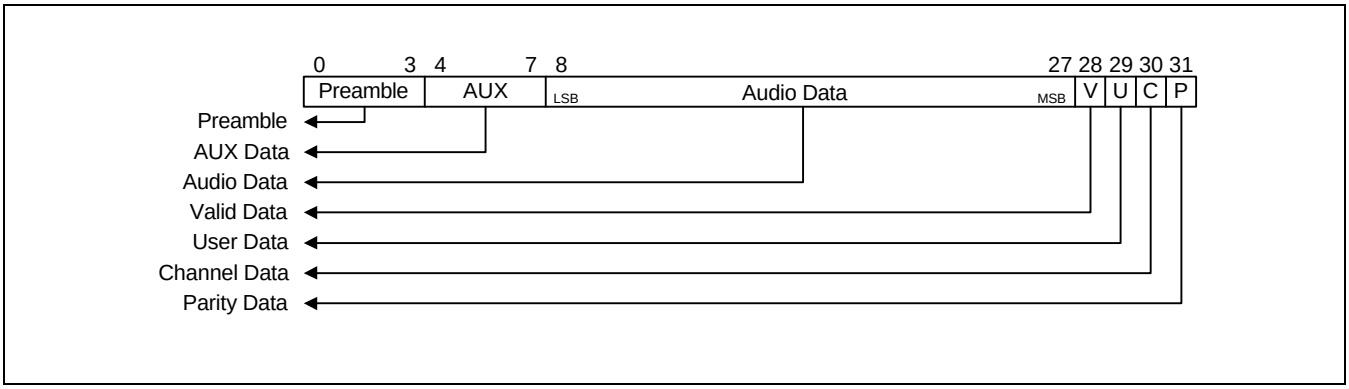
Digital Audio Out

This digital audio out block outputs 2-channel and 16-bit data to another digital set in serial format based on the digital audio interface format. The advantage of this interface method is that communication is possible with only one pin, that is, additions such as a separate clock are not required.

CD digital audio interface format

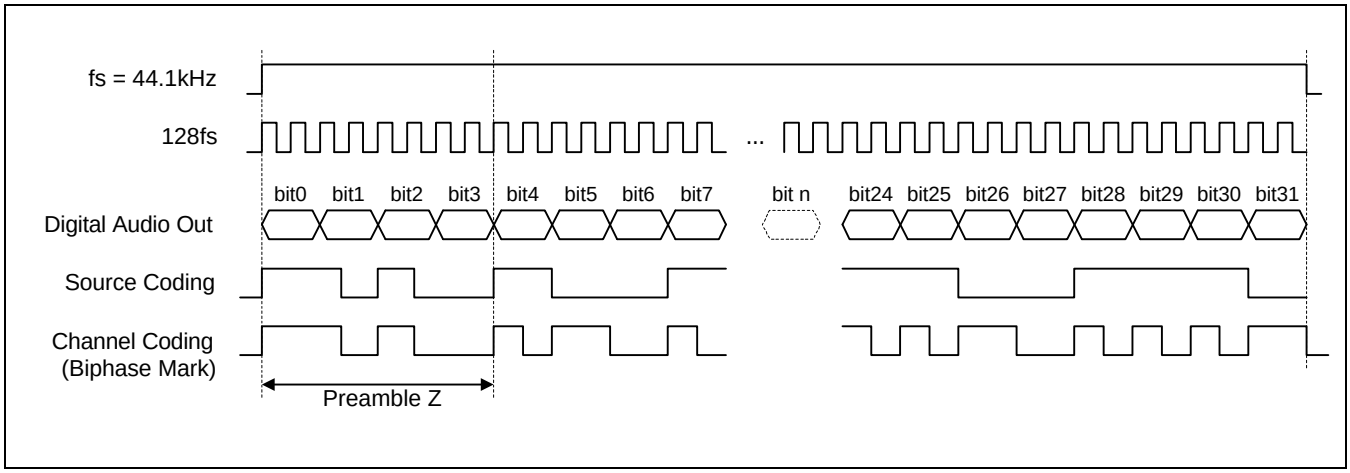


1) 1 block = 192 frame
2) 1 frame = 2 subframe
3) Frame 0, channel 1
   - Block sync preamble, Z included Ch.1 format
4) Frame 1, channel 1-frame 191, channel 1
   – Ch.1 sync preamble, X included Ch.1 format
5) Frame 0, channel 2-frame 191, channel 2
   – Ch.2 sync preamble, Y included Ch.2 format



Each subframe is composed of 32 time slots, and audio data is included in the subframe. Two subframes make one frame, which has both left and right stereo signal components; 192 frames make one block, which is in the control bit data unit.

Digital Audio Interface Timing Chart



SUBFRAME FORMAT

Preamble (4 bits):

The preamble has each subframe and block sync data. The preamble is not converted to biphase signal to maintain the inherent characteristic of the sync. On the other hand, it starts with the values opposite the phase 1 values of all the. The preamble requires three patterns, that is, a pattern to distinguish between and right and patterns that indicate start of the block. These patterns are shown.

Preceding State	0	1	
	Channel Coding		
“X”	11100010	00011101	Subframe 1
“Y”	11100100	00011011	Subframe 2
“Z”	11101000	00010111	Subframe 1 and block start

Preamble ‘X’ is the channel 1 sync; preamble ‘Y’ is the channel 2 sync; and preamble 3 is to show the start sync of the block. The reason that there are 2 sync patterns for preamble is that the value reverses according to the phase of the previous data.

AUX (4 bits):

Auxiliary data area.

Audio data (20 bits):

Although the audio data resolution for the CD transmitted to digital out is usually 16 bits, it can also be transmitted as 20 bits or 24 when AUX is to be included. This area is LSB first.

Validity bit (1 bit):

If the audio sample word can be converted to analog audio signal, the validity bit to ‘1’ and, if not, to ‘0’. For the CD, set it to ‘0’.

User data (1 bit):

This domain is used to transmit the subcode data for CD.

Control status data (1 bit):

Data is input for each subframe, and 192 subframes must be gathered to make one control data. This domain has both the consumer mode and professional mode, of which S5L9291X the consumer mode. The control status data for CD has the following meaning.

Parity data (1 bit):

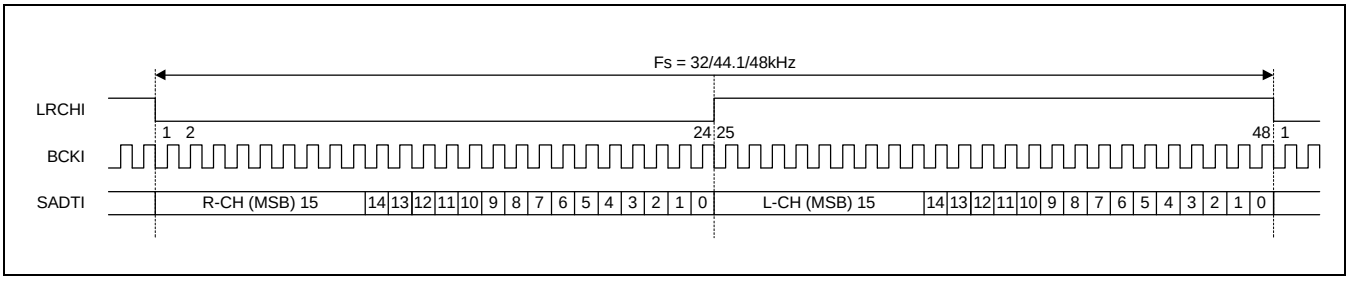
Use even parity

Bit	Control Status Data
0	0: Consumer use, 1: Professional use
1	0: Normal audio, 1: Non audio mode
2	0: Copy prohibit, 1: Copy permit
3	0: No pre-emphasis, 1: Pre-emphasis
4	Reserved = 0)
5	0: 2 channel, 1: 4 Channel
6 – 7	00: Mode 0, reserved
8 – 15	10000000: 2 channel CD player User bit channel = CD subcode V bit optional
16 – 19	Source number (= 0000)
20 – 23	Channel number (= 0000)
24 – 27	Sampling frequency: 44.1kHz = 0000
28 – 29	Clock accuracy 00: Normal accuracy 10: High accuracy 01: Variable speed
30 – 191	Don’t care (all zero)

SIGMA-DELTA STEREO DAC

As a digital-to-analog converter that uses the ∑ Δ modulation, the DAC installed in S5L9291X is composed of the digital attenuation, de-emphasis filter, FIR filter, SINC filter, digital sigma-delta modulator, analog post-filter, anti-Image filter etc. Normal input/output characteristics exist at 20kHz. It has SNR (Signal to Noise Ratio) above 90Db.

Timing Chart



32/44.1/48kHz Sampling Frequency (Fs) Support (External Master Clock Support)

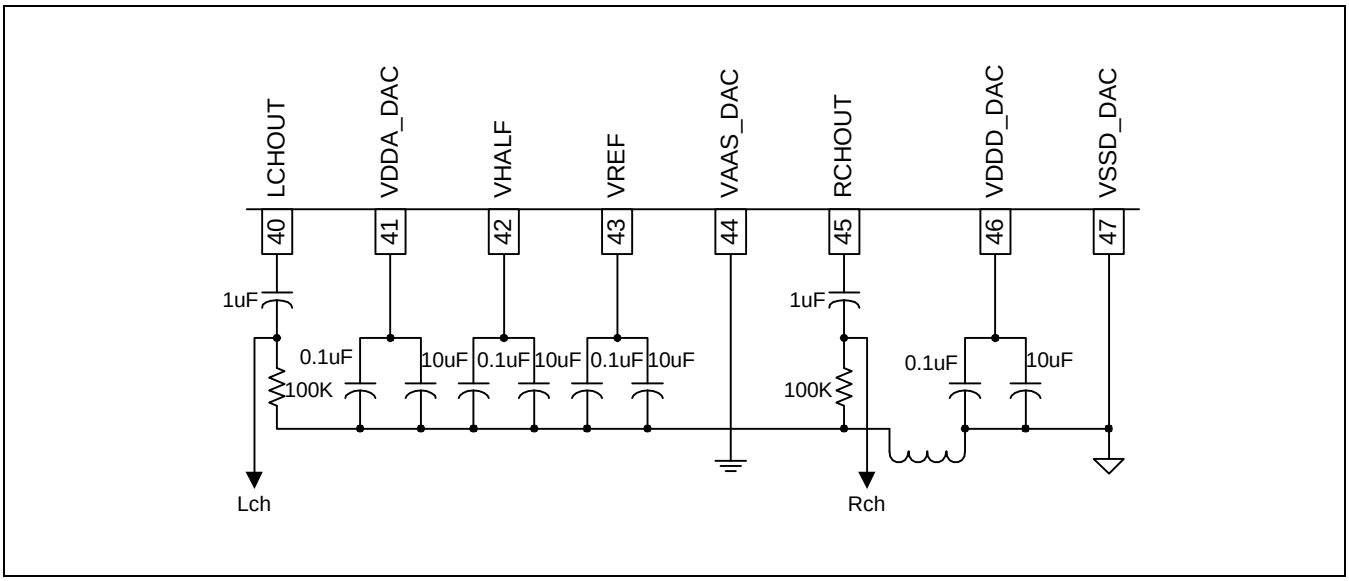
If the DAC master clock is applied to the RFCK terminal (PIN#: 53) in 384 × Fs cycle, it supports 3 sampling frequencies.

If the command register $94's MSCKSW is "H" and command register $A9's RFCK_OEN is "L", the external master clock can be applied to the RFCK terminal.

X1, X2 Speed Support

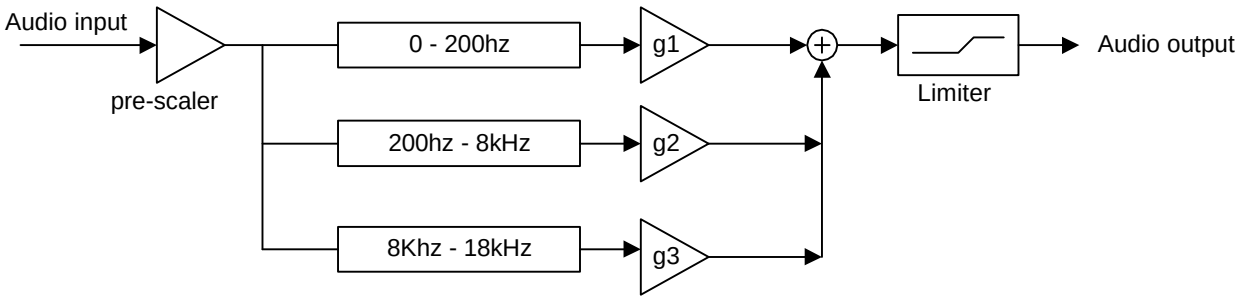
If the command register $93's DFCK is set to "H", the internal data input rate becomes 2*Fs and the speed becomes 2X.

APPLICATION CIRCUIT



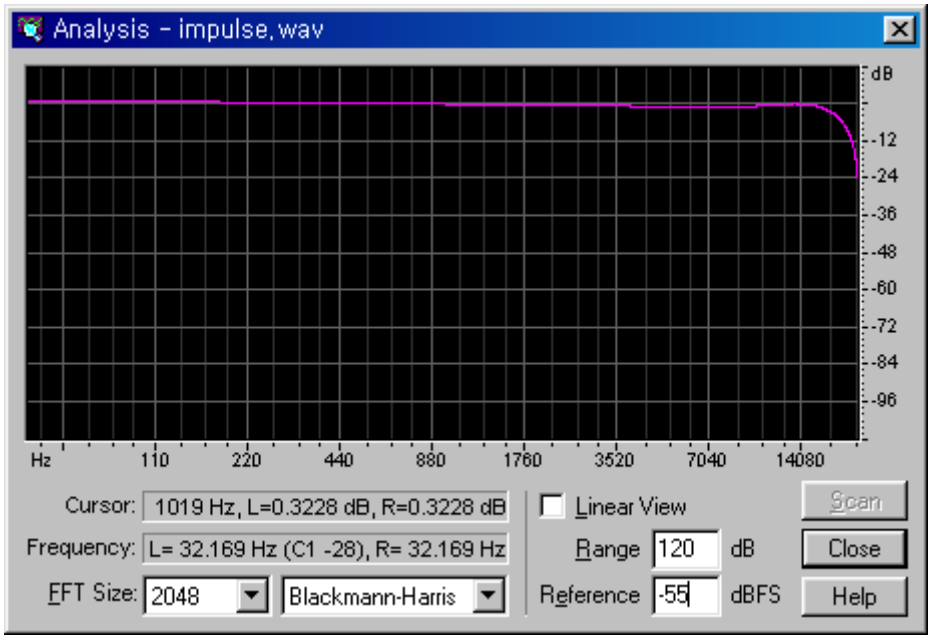
10-Band EQ. Filter

It has a Digital Filter inside the chip for equalizing the signal.
It is possible to control EQ Gain using Command Resister $A0 – $A2,A5 and three band EQ Digital Filter features are as follows.



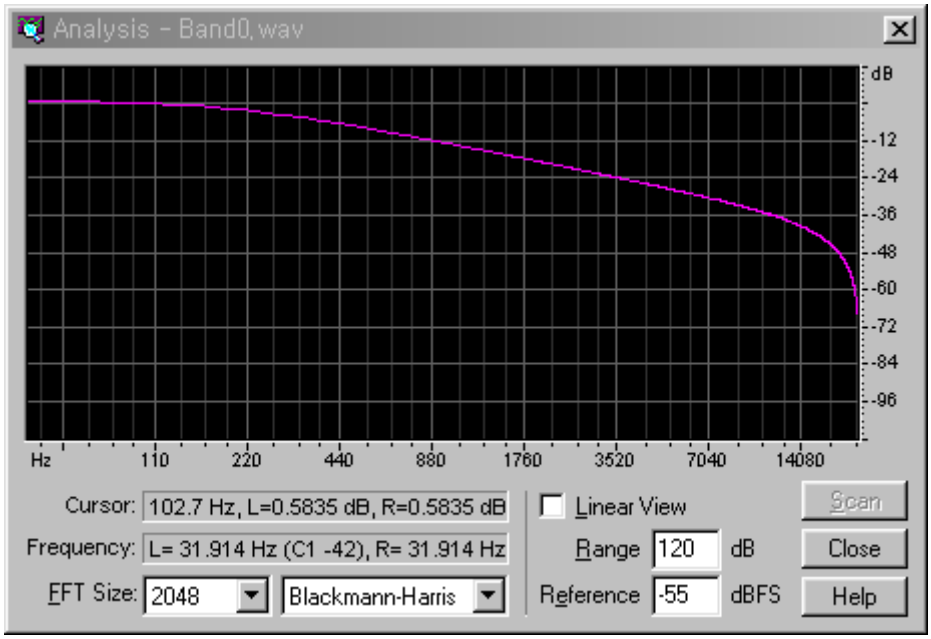
g1 : Bass gain, g2 : Mid gain, g3 : high gain
3Band EQ. Block Diagram

3Band EQ. Frequency Response

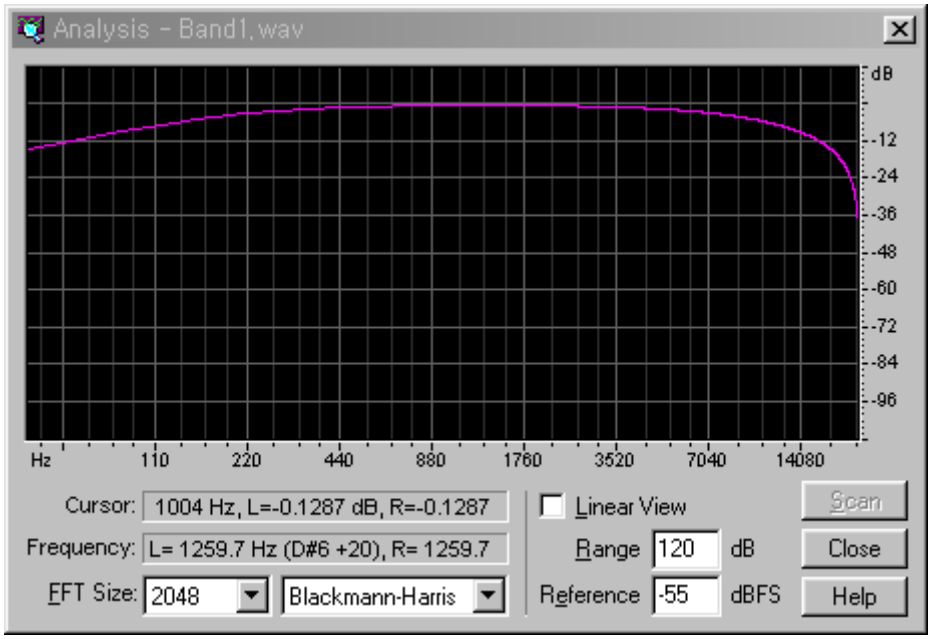


SAMSUNG ELECTRONICS

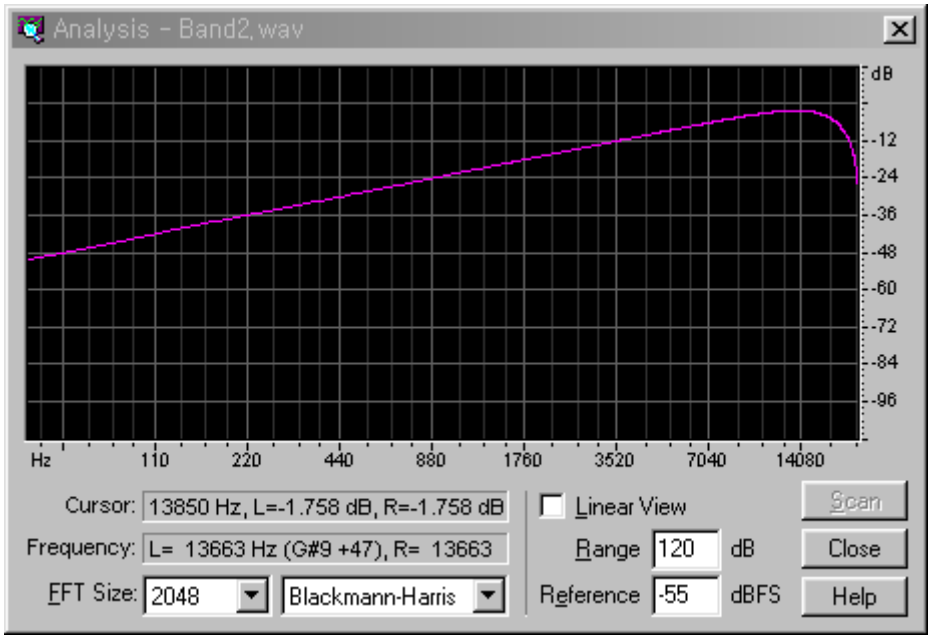
3Band EQ. Bass Frequency Response



3Band EQ. Mid. Band Frequency Response



3Band EQ. High Band Frequency Response



Micom Command flow

To drive the 3Band EQ., first the gains of each band must be set and the values must be converted to 16 (hex). Examples of this is as follows:

Pre Scale : 0Db, Bass : 10Db, Mid : -3Db, High : -3Db

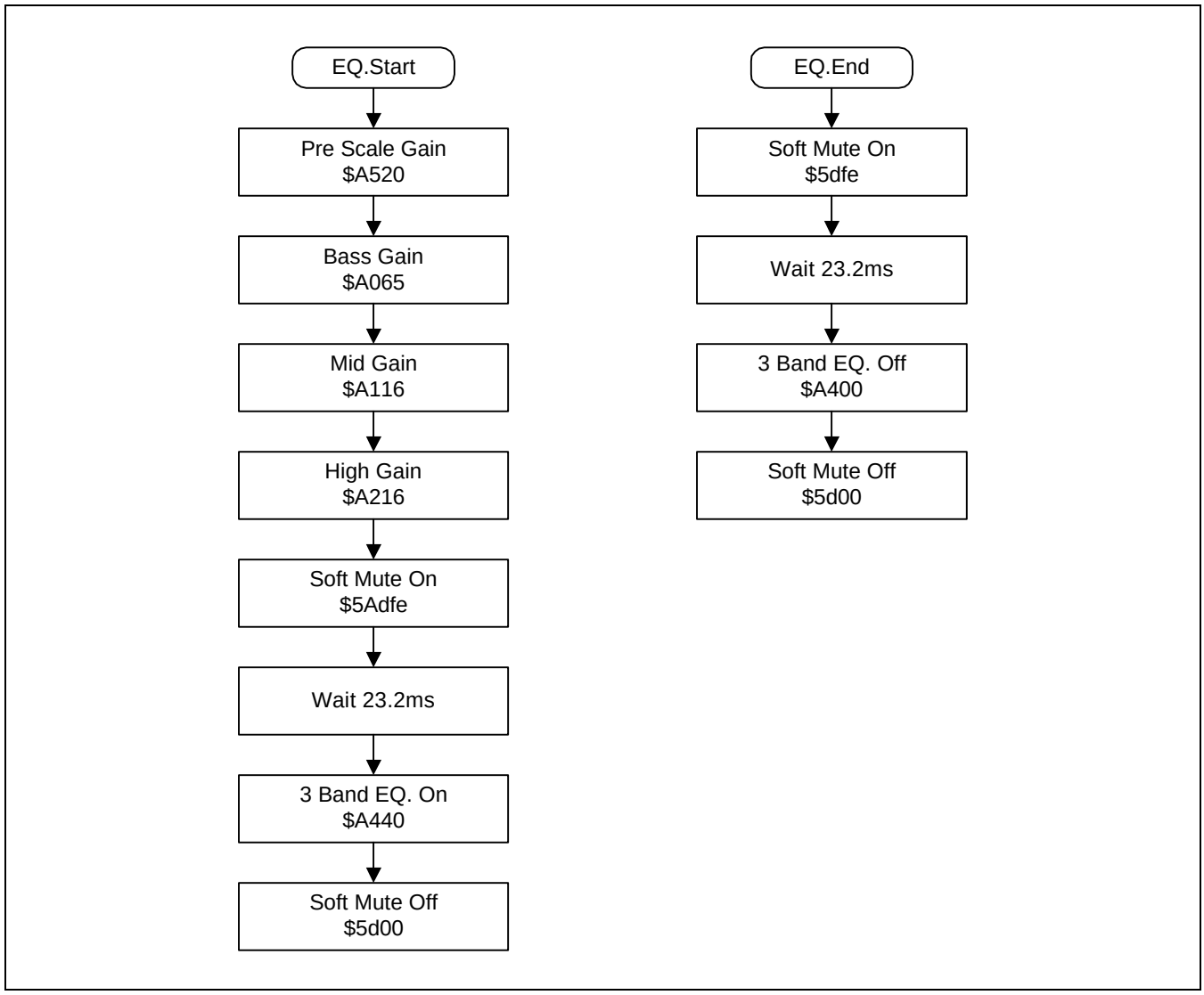
Pre Scale gain = $10^{(0/20)}$ = 1 (dec) = 001.00000 (bin) = 20 (hex)

Bass gain = $10^{(10/20)}$ = 3.162277 (dec) = 011.00101 (bin) = 65 (hex)

Mid gain = $10^{(-3/20)}$ = 0.707945 (dec) = 000.10110 (bin) = 16 (hex)

High gain = $10^{(-3/20)}$ = 0.707945 (dec) = 000.10110 (bin) = 16 (hex)

After calculating the pre-scale gain and different gains of each band, micom command is input in the order as shown in the flow chart below.



	Normal (Default)	+3Db	+6Db	+10Db	-3Db	-6Db	-10Db
Pre-Scale	$A520	$A52D	$A53F	$A565	$A516	$A510	$A50A
BASS	$A020	$A02D	$A03F	$A065	$A016	$A010	$A00A
MID	$A120	$A12D	$A13F	$A165	$A116	$A110	$A10A
HIGH	$A220	$A22D	$A23F	$A265	$A216	$A210	$A20A

DIGITAL CLV SERVO

This block controls the spindle motor speed by using RFCK and WFCK data to generate the control. Digital CLV Servo control related Command Registers are $93, $94, and $98 – $9E.

Forward (Kick) Mode

Mode ($99) that rotates the spindle motor in forward direction.

SMDP	SMDS	SMEF	SMON
H	Hi-Z	L	H

Reverse (Brake) Mode

Mode ($99) that rotates the spindle motor in the reverse direction.

SMDP	SMDS	SMEF	SMON
L	Hi-Z	L	H

Stop Mode

Mode ($99) that stops the spindle motor.

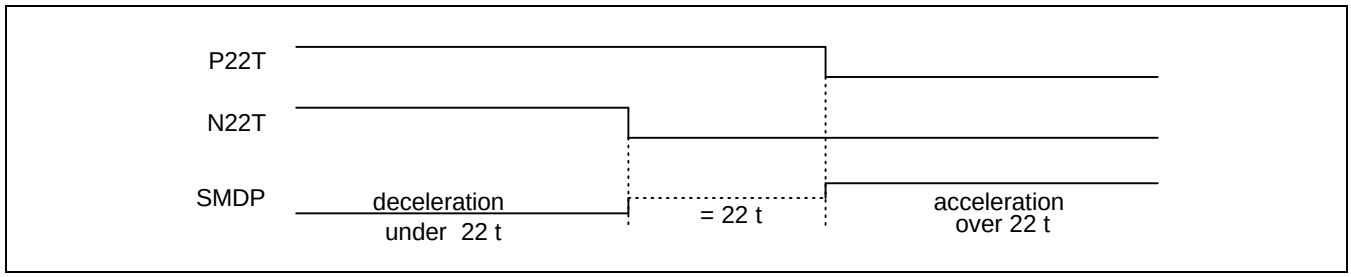
SMDP	SMDS	SMEF	SMON
L	Hi-Z	L	L

Speed (CLV-S) Mode ($99)

Controls the spindle motor during a track jump or if the EFM phase is unlocked.
Although the pulse width of the frame sync signal detected from the EFM signal is exactly 22T in PLCK cycle (T), it can be greater or less than 22T depending on the player status.
WB and WP of the command register $98 are used to control the frame sync detection cycle.

SMDP	SMDS	SMEF	SMON
L : deceleration H : acceleration Hi-Z : remain	Hi-Z	L	H

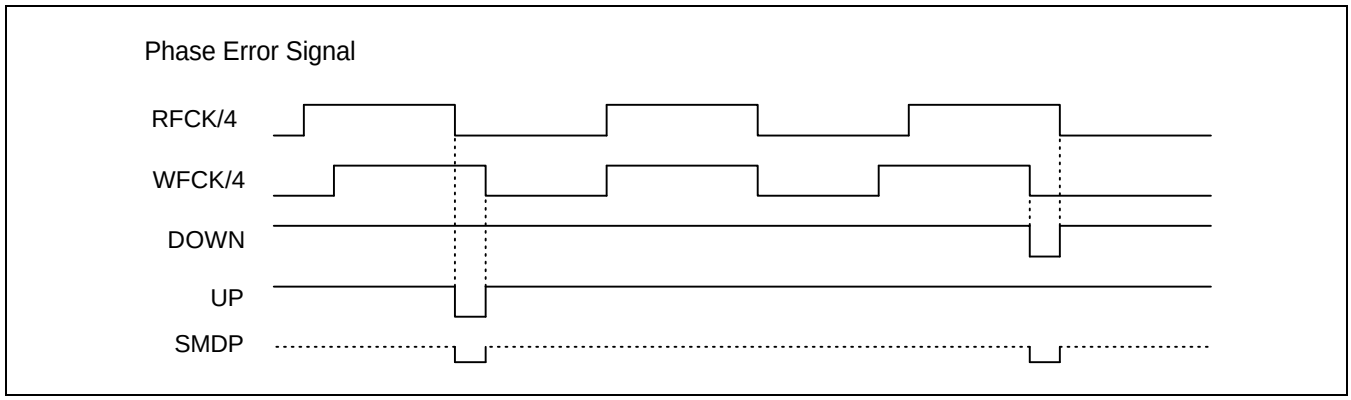
Detected Frame Sync Pulse Width	SMDP	Comment
≤ 21T = 22T ≥ 23T	L (deceleration) Hi-Z (remain) H (acceleration)	If the command Register $98's GAIN is 'L', the SMDP output is output after it has been attenuated by -12Db, but if 'H', it is output without being attenuated.



<SMDP output waveform in Speed (CLV-S) Mode>

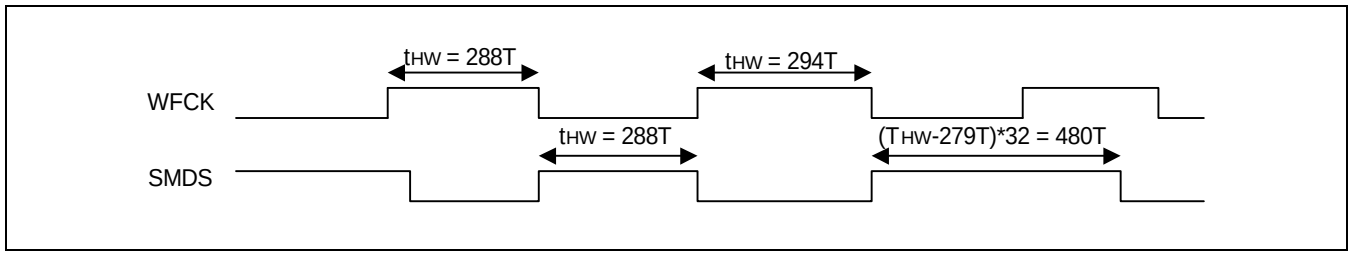
Phase (CLV-P) Mode (Command Register : $99)

As the EFM signal phase control mode, this mode precisely controls the spindle motor rotation speed.
Two methods of control are Phase control and Frequency control and the two signals produced, are sent to the SMDP and SMDS, respectively.
NCLV of the command register $93 can be used to change the reference clock, which is used in phase control.
The phase control signal is sent to SMDP and its waveform is shown below.



<SMDP output waveform in the Phase (CLV-P) Mode >

If the system clock and C4M cycles are T and WFCK's width, 'H', is Thw, SMDS outputs 'H' starting from WFCK's negative edge for (Thw - rise_mtval) × SGAIN and then falls to 'L'. Here, the rise_mtval and SGAIN values can be set through command register $9B.



< SMDS output waveform in Phase (CLV-P) Mode: SGAIN = 32, rise_mtval = 279 >

XPHSP (CLV-A) Mode (Command Register : $99)

In this normal operation mode, the speed mode and phase mode are change alternately by the lock signal. After the LKFS signal generated by the frame sync block is sampled in WFCK/16 cycles and is detected to be 'H', the phase mode executes and, if it is detected as 'L' eight consecutive times, the speed mode automatically executes.

High Speed (CLV-H) Mode (Command Register : $99)

In Jump mode, in which servo has to traverse about 20,00 track roughly, servo moves from inner track of disc to outer.
In that case, mirror signals about 20KHz are overlapped in EFM. So servo is to be unstable in Speed-mode, because false Mirror peak level , which is larger than Frame Sync, is detected.
In high Speed Mode, Peak Hold uses 8.4672MHz/256 cycle and Bottom hold uses RFCK/16 or RFCK/32 cycle, so it make possible to eliminate the Mirror signals and for servo to be stable

LOCK generation

If the LKFS signal remains at 'L' for the frame time, provided by Micom Command $99's UNLOCK[1:0], or for less, LOCK remains at 'H'. However, if it remains at 'L' for more than the given frame, the LOCK changes to 'L'. The time in LOCK is the same for 1X and 2X speed.

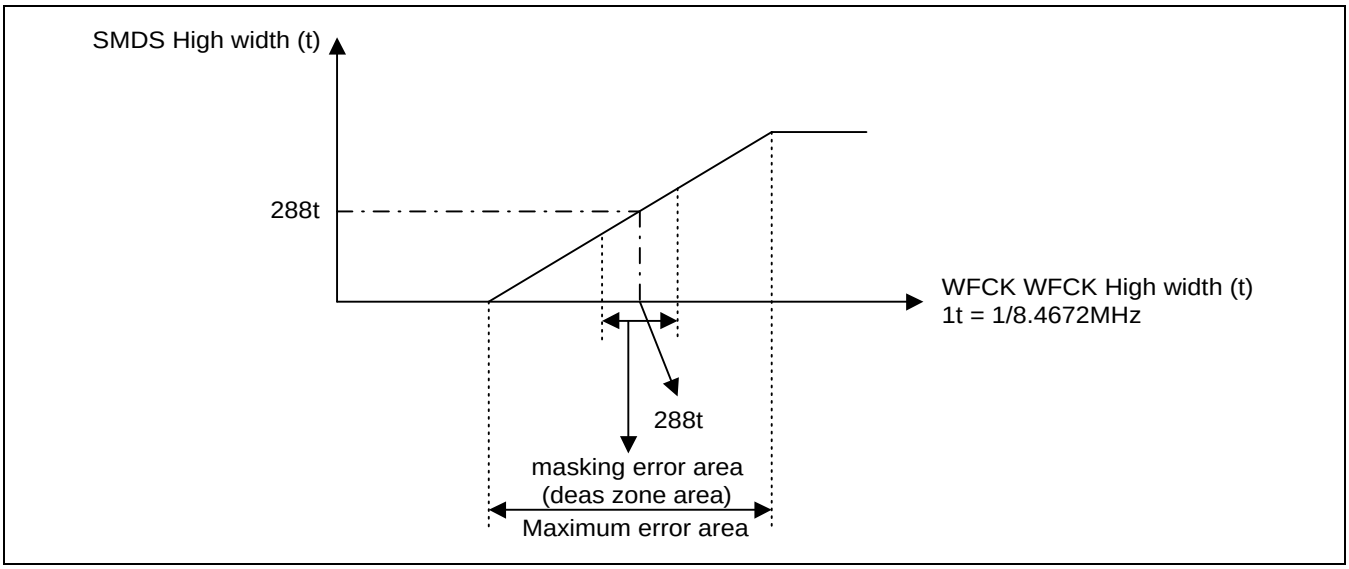
Additional Functions ($9B's POS must be set to = 'H')

1) SMDS masking
   This function prevents sensitive CLV servo response to small frequency error changes.
   If the SME of $9A is set to 'H', it operates in the SMDS masking mode (dead zone enable).
   The SML[1:0] masking range of $9B is set, and, if $9A's SMM bit is 'H', SML value becomes the absolute value of the masking range, set by 9D'h SMOFFSET[3:0], but if 'L', then the value is set to the one shown in the table below. If SMDS frequency error, that is, WFCK high width is within the masking range, the SMDS output is PWM of 50:50 or Hi-Z is output. (Determined by $9A's STRIO)
   If SMDS masking occurs, SMDP output is masked automatically and Hi-Z is output.

Command order : $9B(SML) → $9D(SMOFFSET) → $9A (SME, SMM)

SML[1:0]	masking error range (SML = 'L')
00	0 %
01	± 6.25 %
10	± 12.5 %
11	± 25 %

< SML[1:0] setting >



< Dead Zone Area >

SMDP masking

When the SMDS masking is enabled, the SMDP output is automatically masked in the dead zone area. There are two modes for masking only the SMDP without masking the SMDS.
In the first mode, if $9A's SME is set to 'L' and PME is set to 'H', the SMDP masking mode operates. At this time, if the phase error is greater than ± 50% or ± 25% of the WFCK frequency error (determined by $9B's PML), SMDP output is masked. That is, the output is Hi-Z.
This is to reduce the phase error effect at the state in which the frequency error is not sufficiently small. In the second mode, after setting SME and PME of $9A, PCEN of $99 can be used to set SMDP masking. In this case, if PCEN of $99 is set to 'H' and WFCK frequency error enters the dead zone area set by SML, the SMDP output is maked to Hi-Z.

Command order : $9B(PML) → $9A(PME), $9B(SML) → $99(PCEN)

CLV emergency mode (ECLV)

When there are events such as a focus drop, an unstable EFM is input and this in turn causes the spindle motor to overload. To prevent such an overload, the Micom notifies the CLV servo of such emergency conditions, and then CLV servo outputs H, Hi-Z and L repeatedly in regular intervals. This is all executed by the micom, which sets the ECLV of $93 to 'H' and changes the CLV mode to CLV-S mode. Then, SMDS outputs Hi-Z and SMDP outputs H, Hi-Z and L repeatedly in an interval determined by ECLV_PD of $93.

ECLV_PD	Comment
1	bottom hold pulse interval
0	peak hold pulse interval

Command order : $93(ECLV, ECLV_PD) → $99(CM3,CM2,CM1,CM0)

Defect response mode

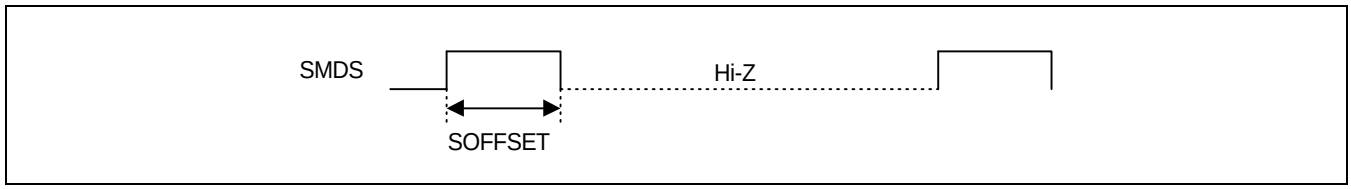
If the EFM enters as 'L' for a specific time due to a Scratch or defect, there is no PLL control, which fixes the PLCK to any frequency; this in turn fixes the WFCK and consequently the CLV servo output is fixed in the direction of acceleration or deceleration. In such a case, the final CLV speed can be reduced when normal EFM re-enters. If CLV_DFCT of $A2 is set to 'H', the CLV servo outputs, SMDP and SMDS, can be output as Hi-Z and 50:50, when EFM width is greater than 64t to prevent deceleration or acceleration.

Over sampling output

The SMDS output frequency is 7.35kHz at 1X speed and 14.7kHz at 2X speed. These are within the audio frequency range, so they be used as normal audio output noise source. Therefore, OVSPL of $98 can be set to 'H' and SMDS and SMDP frequencies can be over sampled by four times at 7.35KHz * 4 = 29.4kHz and output. If OVSPLMD of $98 is set to 'H', the SMDS becomes tri-state t output and, if set to 'L', SMDS become a PWM output.

CLV IDLE mode

This mode rotates the spindle motor at a fixed rate regardless of the EFM input.
To operate in the CLV IDLE mode, the $9E's SOFFSET[7:0] value, which represents the SMDS high width, must be set. Furthermore, if $99's CLV_IDLE is set to 'H', the SMDP output becomes Hi-Z, and SMDS outputs High for the duration of SOFFSET set value * 118ns in one cycle and outputs Hi-Z in the remaining intervals.



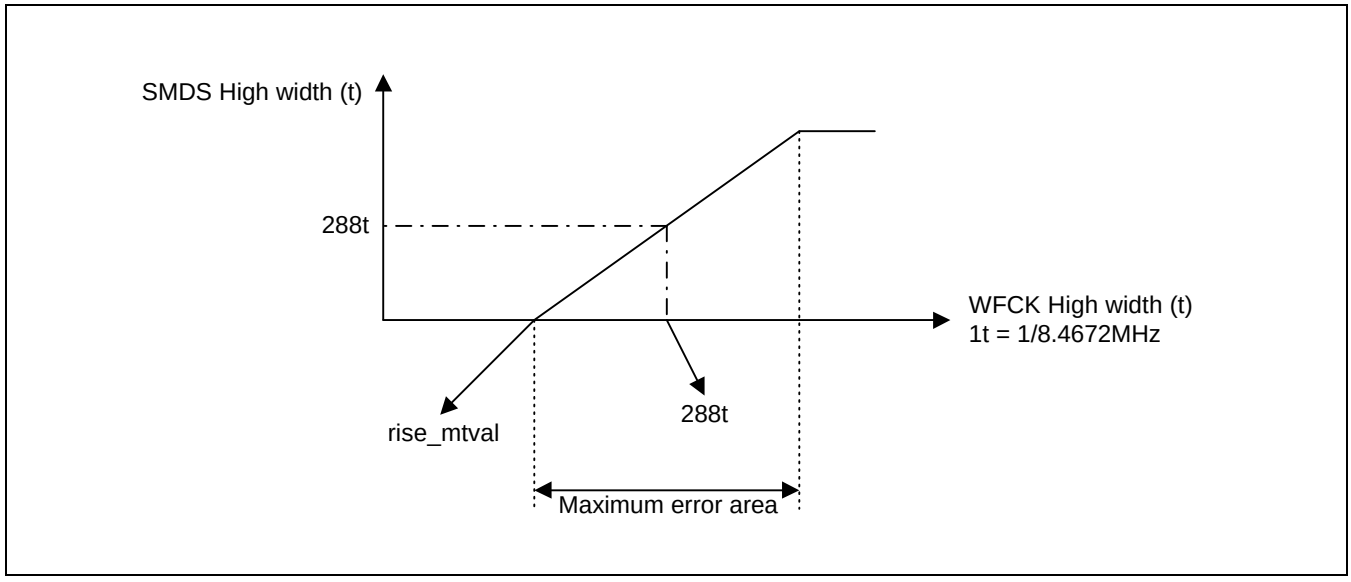
< SMDS output >

SMDS gain control

If the pickup or spindle motor is changed, the entire CLV loop transfer function changes and thus CLV gain must be controlled. The CLV servo is changed to PI controller type; we can assume that the frequency error output SMDS controls the P gain and the phase error output SMDP controls the I gain. SMDS gain can be set to 9B'h SGAIN[2:0] , where gain values of SGAIN are shown below. In terms of a graph, the gain is the slope.

SGAIN[2:0]	Gain Value	rise_mtval
000	1	0
001	2	144
010	4	216
011	8	252
100	16	270
101	32	279
110	64	283
111	128	285

< SMDS gain setting >



< SMDS gain vs SMDS output >

There is an additional feature which allows the addition of an offset to WFCK frequency error for output. If $9D's SPLUS is set to 'H' and $9E's SOFFSET[7:0] is set, the SOFFSET value is added to the frequency error, and the product of this value and the gain is output to SMDS.

SMDP gain control

The 9B'h POS must be set to 'H' for SMDP gain control. Furthermore, SMDP gain must be set to $9A's PGAIN[1:0]. The clock resolution, which measures WFCK and RFCK's phase error, must be set to $9A's PKSEL.

PGAIN[1:0]	Gain
00	1
01	1/2
10	1/4
11	2

<SMDP gain setting >

PKSEL[1:0]	frequency
00	clk4M/2
01	clk4M/4
10	clk4M/8
11	clk4M/16

< Phase error resolution clock setting >

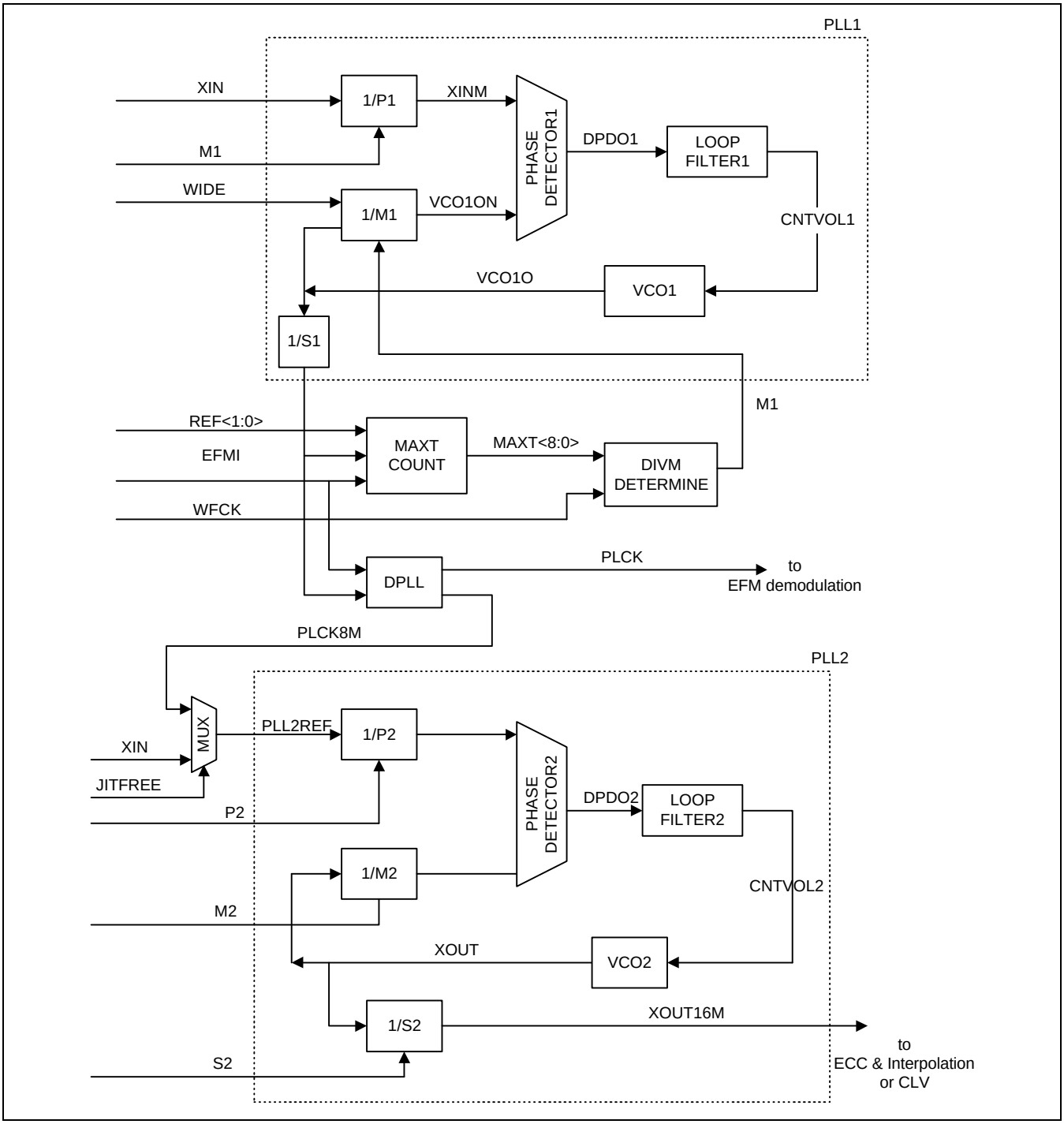
If POFFSET[7] is 'H', the value is subtracted and, if 'L', added. .

SMDS output Mode

If $9A's STRIO is set to 'H', the SMDS is output in tri-state (H, Hi-Z, L) states in phase mode.
If $9D's SDD is set to 'H', the SMDS outputs as Hi-Z in phase mode if the WFCK frequency error is a deceleration error. Even if SMDS is output as Hi-Z, this mode can reduce the power consumption by utilizing the principle of deceleration due to motor friction.

DIGITAL PLL

The existing Digital PLL (DPLL) is used to enter the wide capture range PLL mode, which allows the frequency of the frequency synthesizer, which supplies the DPLL clock, to follow the bit rate change of the EFM signal. Once in the wide capture range PLL mode, the jitter-free mode can be set to suppress the SRAM jitter that may be generated by the change in the input/output rate of the internal SRAM buffer. Furthermore, multi-speed CLV mode in 16 levels from 1X to 2X is possible.



< Block Diagram >

PLL1, a frequency synthesizer which supplies DPLL reference clock, uses the input (16.9344MHz) from the crystal to generate a clock of frequency that is a multiple of PLCK frequency. PLL2 is a frequency synthesizer which supports the entire speed range CLV or jitter-free mode. Therefore, PLL2 is set to the power down mode when it is not used in normal 1X and 2X mode or jitter free1 mode. In the entire speed range CLV mode, the output frequency of PLL2 the crystal input to be used as either the CLV mode reference clock and data operation(ECC, interpolation) reference clock; in the jitter free2 mode, the output together with the DPLL plck8M input is used as data operation reference clock. The entire speed range CLV mode and jitterfree2 mode cannot be set simultaneously. The equation of the output frequency from the frequency synthesizer is as follows. Divider value changes with mode.

$$Fout = Fin \times \frac{m}{p \times s}$$

Fin: input frequency, Fout: output frequency
p: pre-divider(=DIVP+2), m: main-divider(DIVM+8), s: post-scalor(2^{DIVS})

In the entire speed range CLV mode, once the values for DIVS1 and DIVP1 of 8A address are set according to speed, the remaining divider values are automatically set. Commands according to speed are as follows.

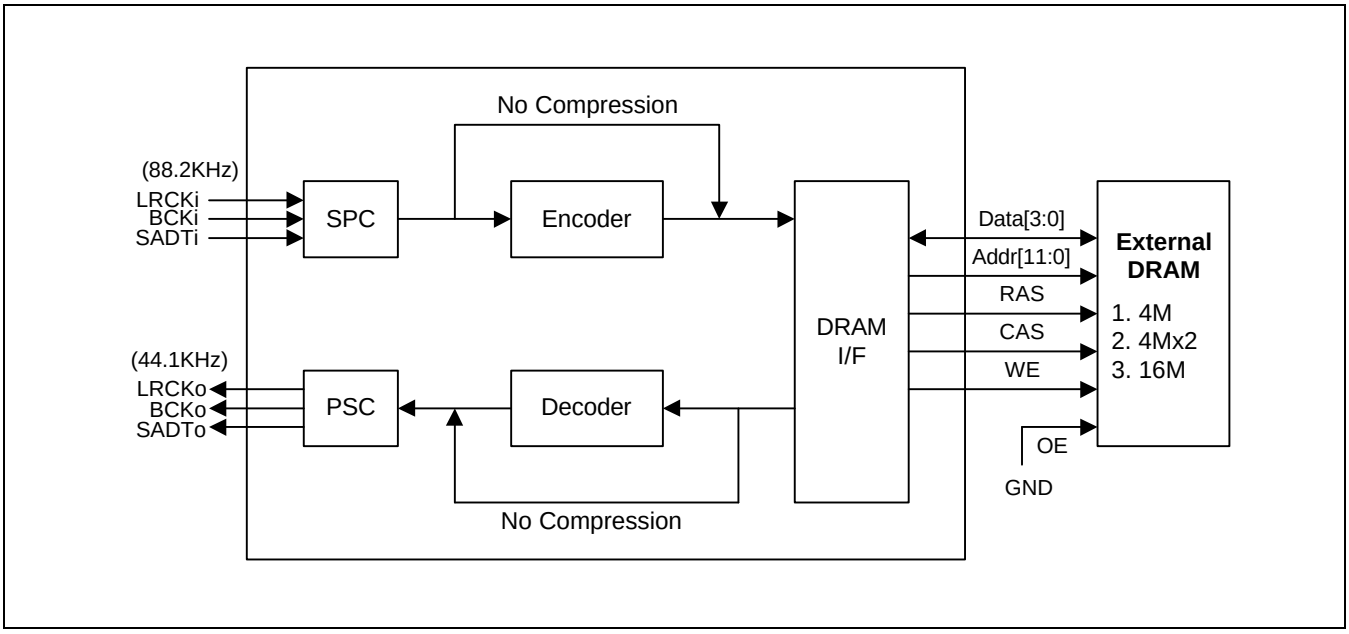
	Command	
speed	8A	F0
0.5	6E	00
…	…	
1	56	00
1.04	55	
1.09	54	
1.14	53	
1.2	52	
1.26	51	
1.33	50	
1.41	4F	
1.5	1E	F4
1.55	1D	
1.6	1C	
1.66	1B	
1.71	1A	
1.78	19	
1.85	18	
1.92	17	
2	16	
…	…	

ELECTRICAL SHOCK PROOF (ESP)

The ESP(Electrical Shock Proof) Block has the data compression/restoration functions, recovery decompression/restoration functions for anti-shock proofing of compact disc players and DRAM memory control function. The compression ratio is about 4/16bit, 5/16, and 6/16 and shock proof data storage memory sizes are 4M/4Mx2/16M DRAM.

FEATURE

1) 2-Channel Processing
2) Serial Data Input : 2's complement, 16-bit/MSB first
3) Anti-Shock Memory Controller
4) ARS(Anti-Rolling System) support : X1 — X4 Compression possible
5) Compression Method
   - 4-Bit Compression Mode 2.91s/Mbit
   - 5-Bit Compression Mode 2.34s/Mbit
   - 6-Bit Compression Mode 1.95s/Mbit
   - Full-Bit Non-Compression Mode 0.743s/Mbit
6) 3 Internal DRAM Configurations Selectable
   - 4M DRAM (1Mx4 bits)
   - 8M DRAM (1MX4 bits 2EA)
   - 16M DRAM (4MX4 bits)
7) Microcontroller Interface
   - Serial Command Write and Internal State Read-Out
   - Data Residual Quantity Detector : 16-Bit Output



< ESP Block Diagram >

Anti-Shock Operation

The shock-proof mode uses the data storage dram. If the Micom Command $B0's MSON = 'H', shock-proof operation executes.

Encode Sequence

In the encode sequence, the audio data from the CD data processor (CDP) is encoded through the ESP encoder and the compressed data is stored in the data storage DRAM.

Encode Sequence Internal Stop

If there is an data storage DRAM buffer overflow or shock(JITB=='L' or CMD_SHOCK=='H'), ESP is stopped internally regardless of the Micom Command $B0's MSWREN. The encoding starts when there is a match by Compare-Connect Sequence or a Direct-Connect Command input.

Decode Sequence

The ESP Decoder checks the system stability in the micom and the presence of the data which can be sent to the DRAM. If they both check out to be normal, the micom command $B0's MSRDEN is set to 'H' and decoding starts. Before the decoder starts, the mute/attenuation function for data output control is put on normal.

Data Compare-Connect Sequence

— Encoding stops when it detects a CDP system shock or DRAM overflow.

— Once the system shock stabilizes or the DRAM data is less than the amount specified in the MICOM PGM and the micom command $B0's MSDCN1(or = MSDCN2) = MSWREN = 'H', it executes the Data Compare-Connect Start Command.

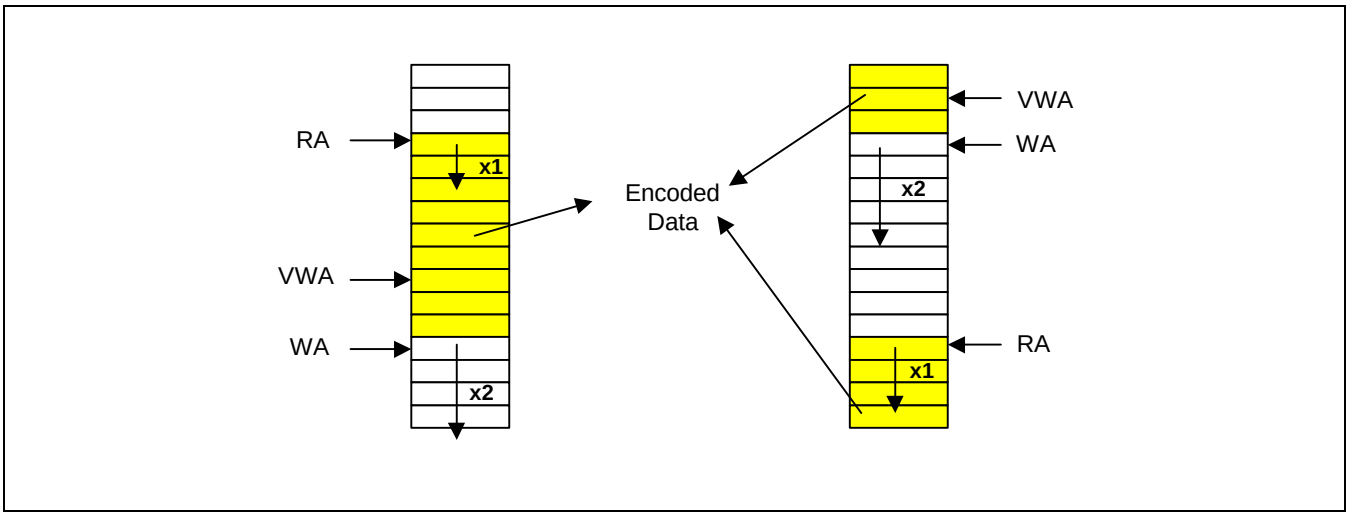
— If the data compare-connect matches normally or direct - connect command is input, the data compare - connect processing comes to an end and encoding begins. The audio data input at this time is directly connected to the last valid data.

DRAM Refresh Method

— The 16 cycle's RAS Only refresh begins at the MSON Rising Edge.

DRAM Address

1) To address the basically supported 4M/8M(4M+4M)/16M DRAM, the address register size is 22 bit and the DRAM is accessed in the form of a circular buffer.
2) RA : The data address read from the DRAM for decoding is stored. As long as it is not "empty", the read operation continues. "Empty" state occurs when RA and VWA becomes the same.
3) WA : The DRAM address to which the encoded data is stored. If compare-connect is operating or "Ovfl (Overflow)" condition exists, this also stops along with the encoding. When Compare-Connect Sequence begins, the data written after VWA becomes meaningless and writing must begin again starting from the address directed by VWA.
4) VWA : updated to the current WA value by the micom's WAQV.
5) As shown in the following figure < WA / RA Mapping> , RA becomes the address of the first data to be decoded and WA becomes the address value following the last encoded data. Therefore, as WA increases and the writing ends and it becomes the same value as RA, DRAM overflows and the encoding stops.



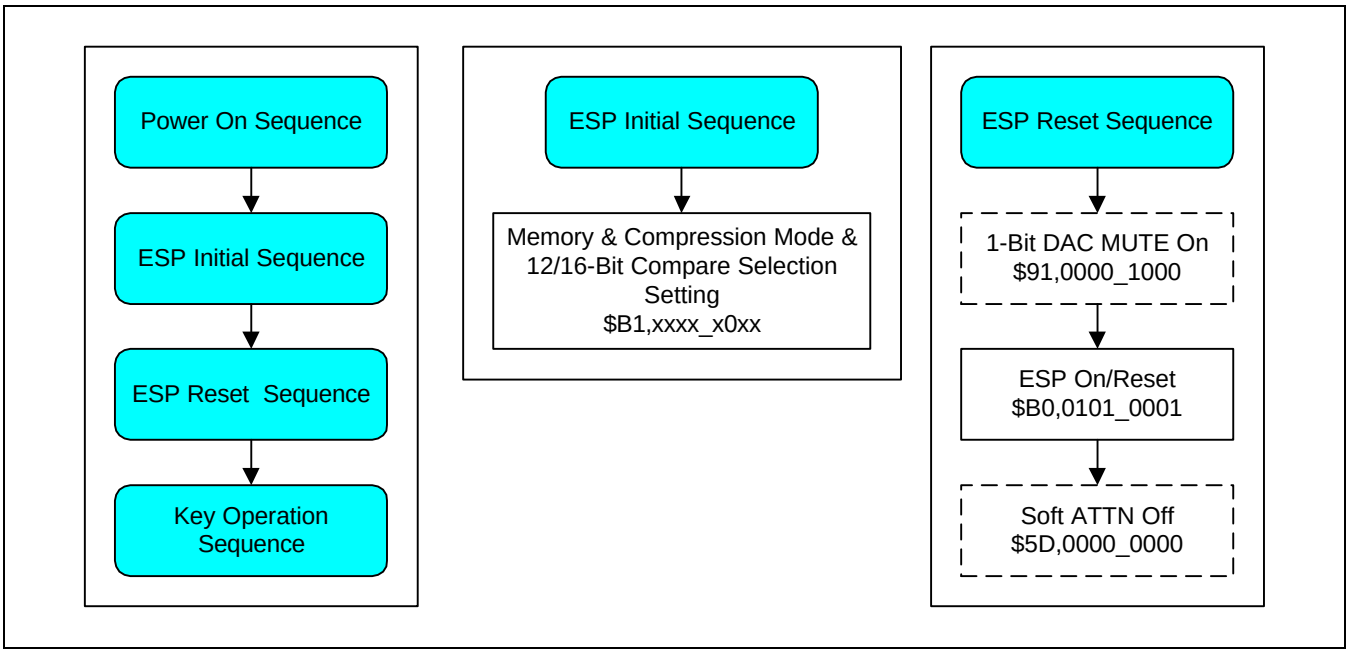
<RA/WA Mapping>

Valid Sample Save & VWA Update

1) In normal encoding (not Compare-Connect Sequence) when every S0S1 is the falling edge and WAQV command is 'H', the Valid Sample Data is updated to the present sample and present WA is updated to VWA. Because this means that WAQV is the previous block's subcode Q-CRC ok, the previous block's sample and WA are stored. VWA value increases for each SOS1.
2) WAQV signal can be generated by directly receiving it from CD DSP's SQOK or the MICOM can generate it.
3) If the VWA value is updated, the empty flag is recalculated.

Flowchart for the ESP MICOM Program

Power On Sequence

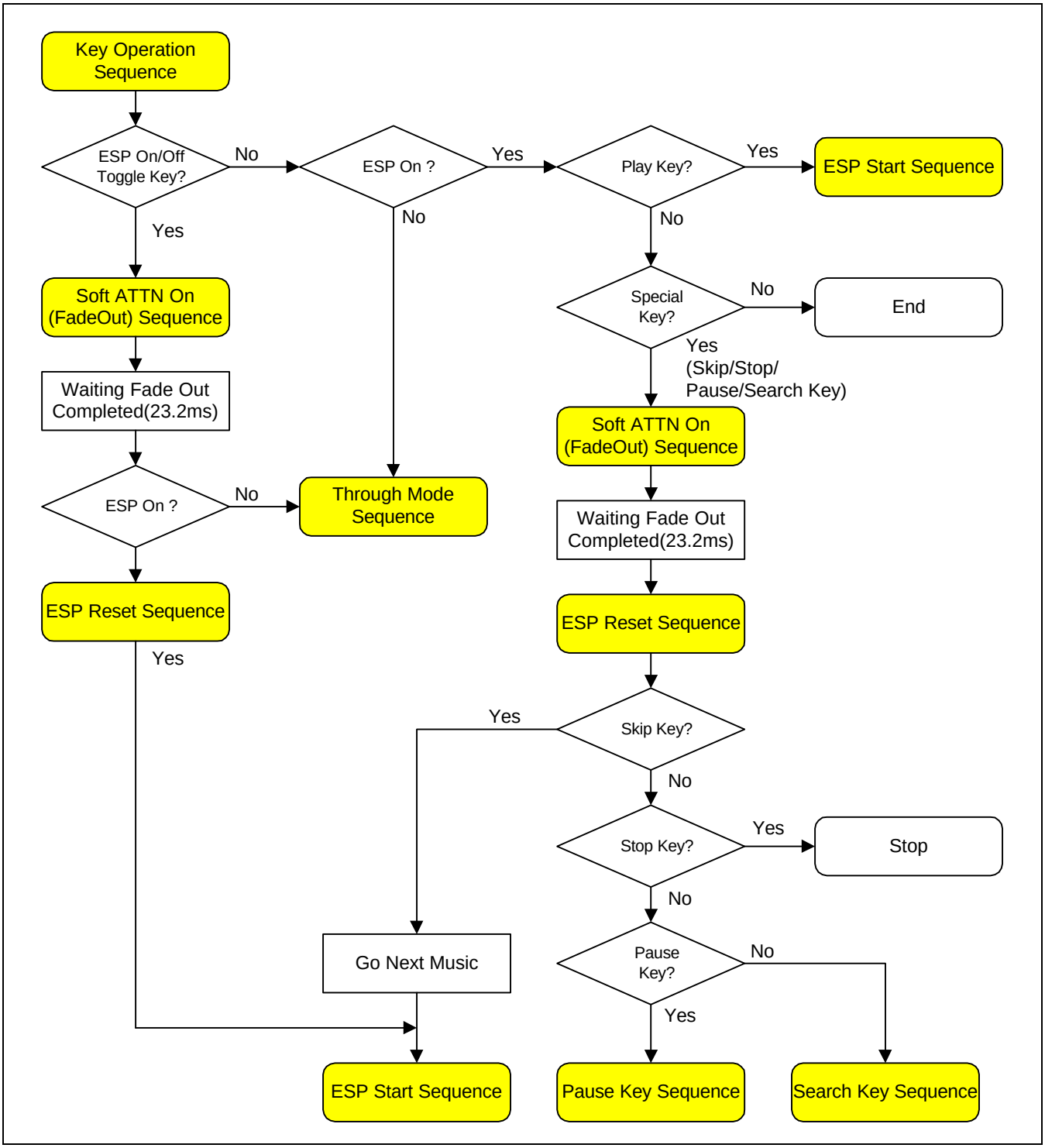


$B1 Address initial setting

	DRAM Selection		
	4M DRAM	$B1,00xx_xxxx	
	8M DRAM	$B1,01xx_xxxx	
	16M DRAM	$B1,1xxx_xxxx	
	FLAG6 Setting Selection		
	JITB in Falling Edge of RFCK	$B1,xx00_xxxx	
	JITB in Rising Edge of RFCL	$B1,xx01_xxxx	
	JITB L	$B1,xx10_xxxx	
	JITB H	$B1,xx11_xxxx	
	12/16-Bit Compare Selection		
	12-bit Compare	$B1,xxxx_1xxx	
	16-bit Compare	$B1,xxxx_0xxx	
	Compression Mode Selection		
	4-bit Mode	$B1,xxxx_xx00	
	5-bit Mode	$B1,xxxx_xx01	
	6-bit Mode	$B1,xxxx_xx10	
	Full-bit Mode	$B1,xxxx_xx11	

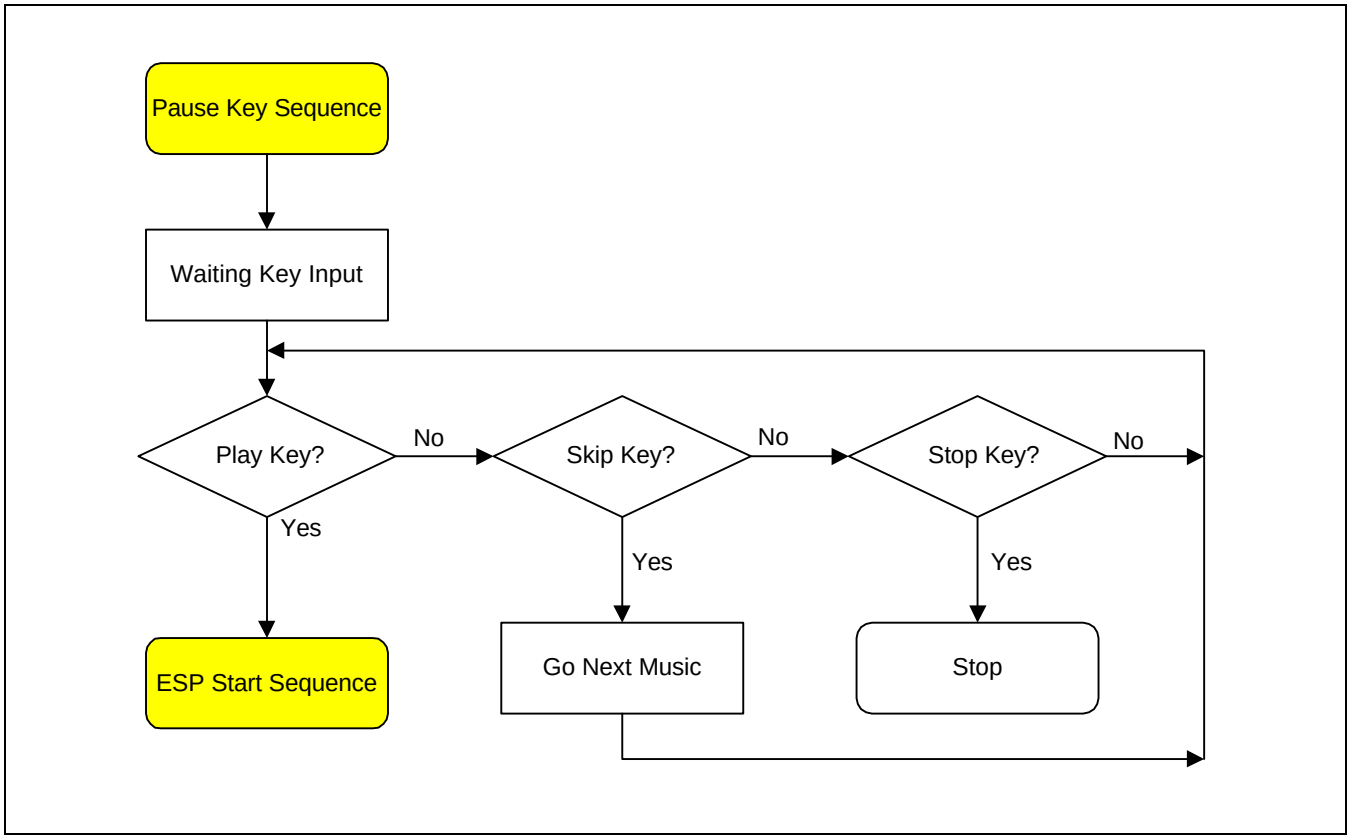
KEY OPERATION SEQUENCE

Key Operation

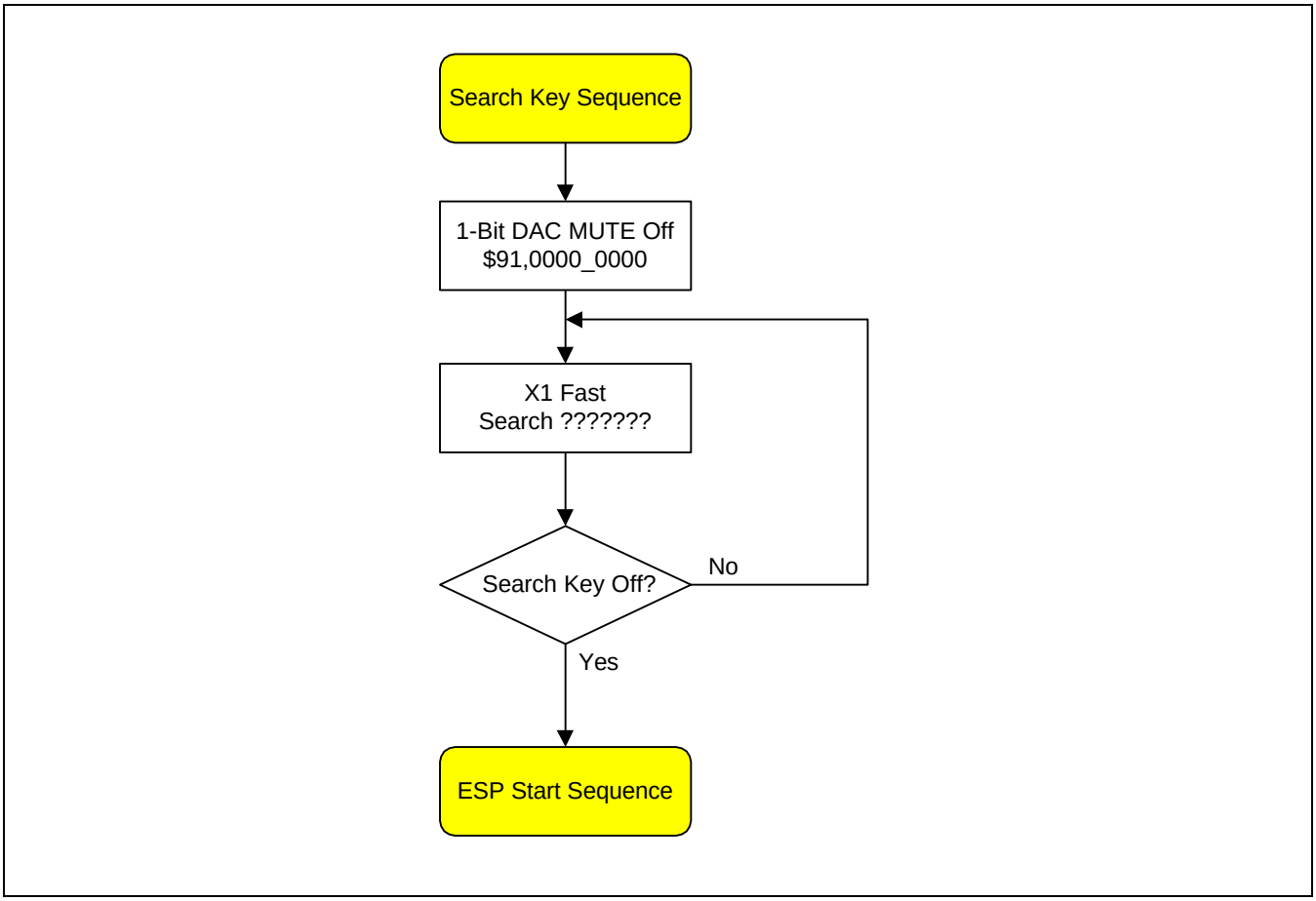


Through Mode sequence means a Normal 1x play.
In Pause Key Sequence , Play/Skip/Stop key must be entered one more time.

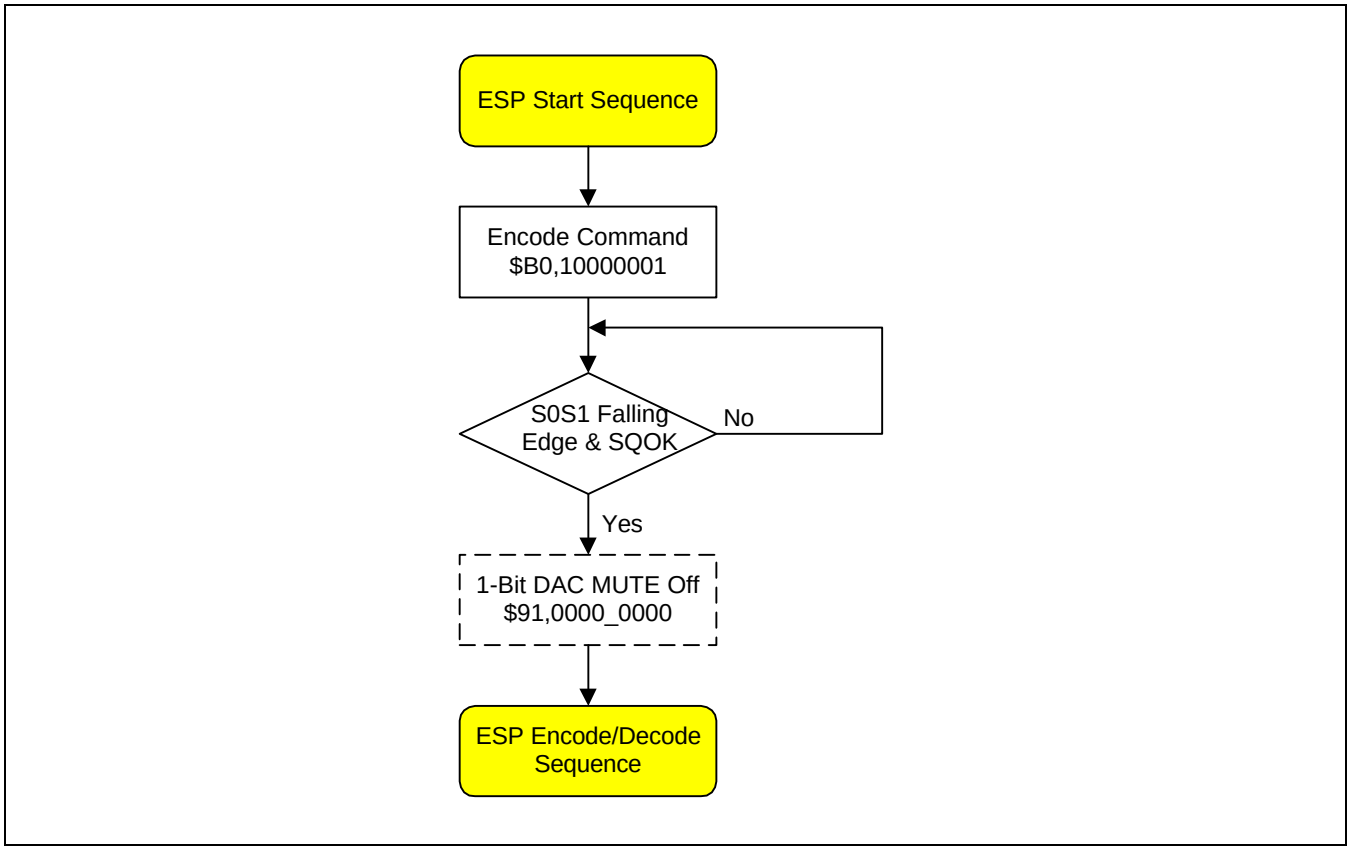
Pause Key Sequence



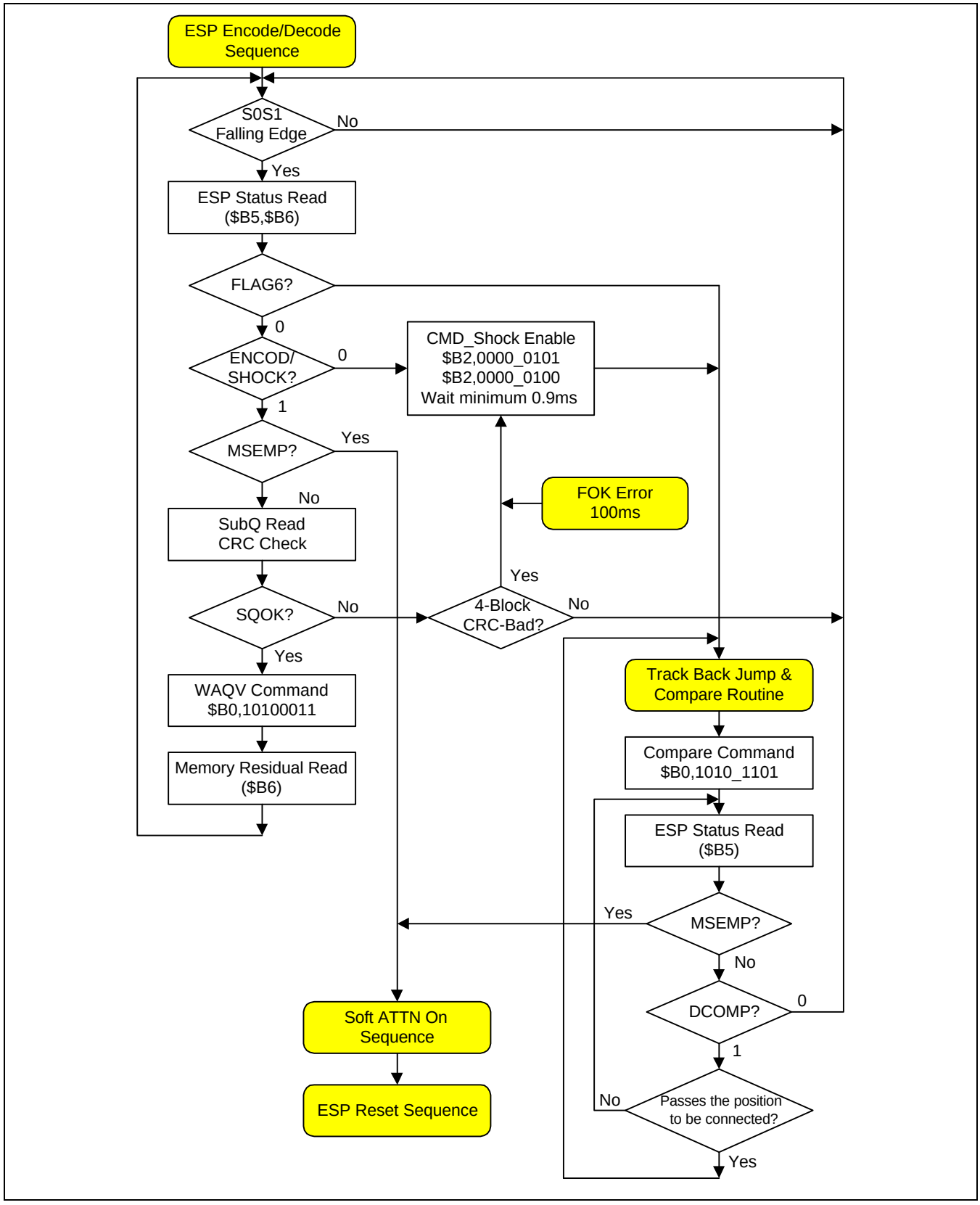
Search Key Sequence



ESP Start Sequence



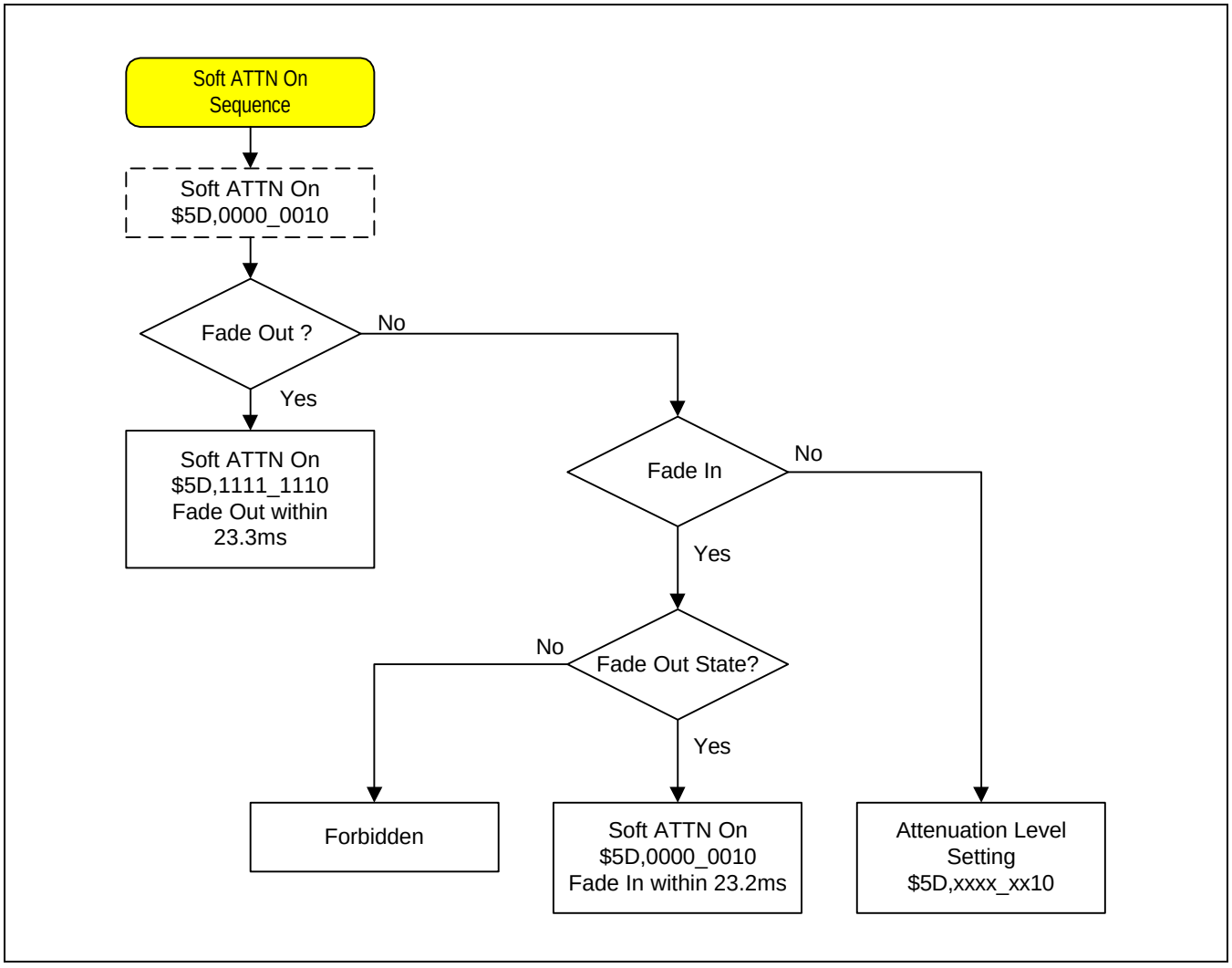
ESP Encode/Decode Sequence



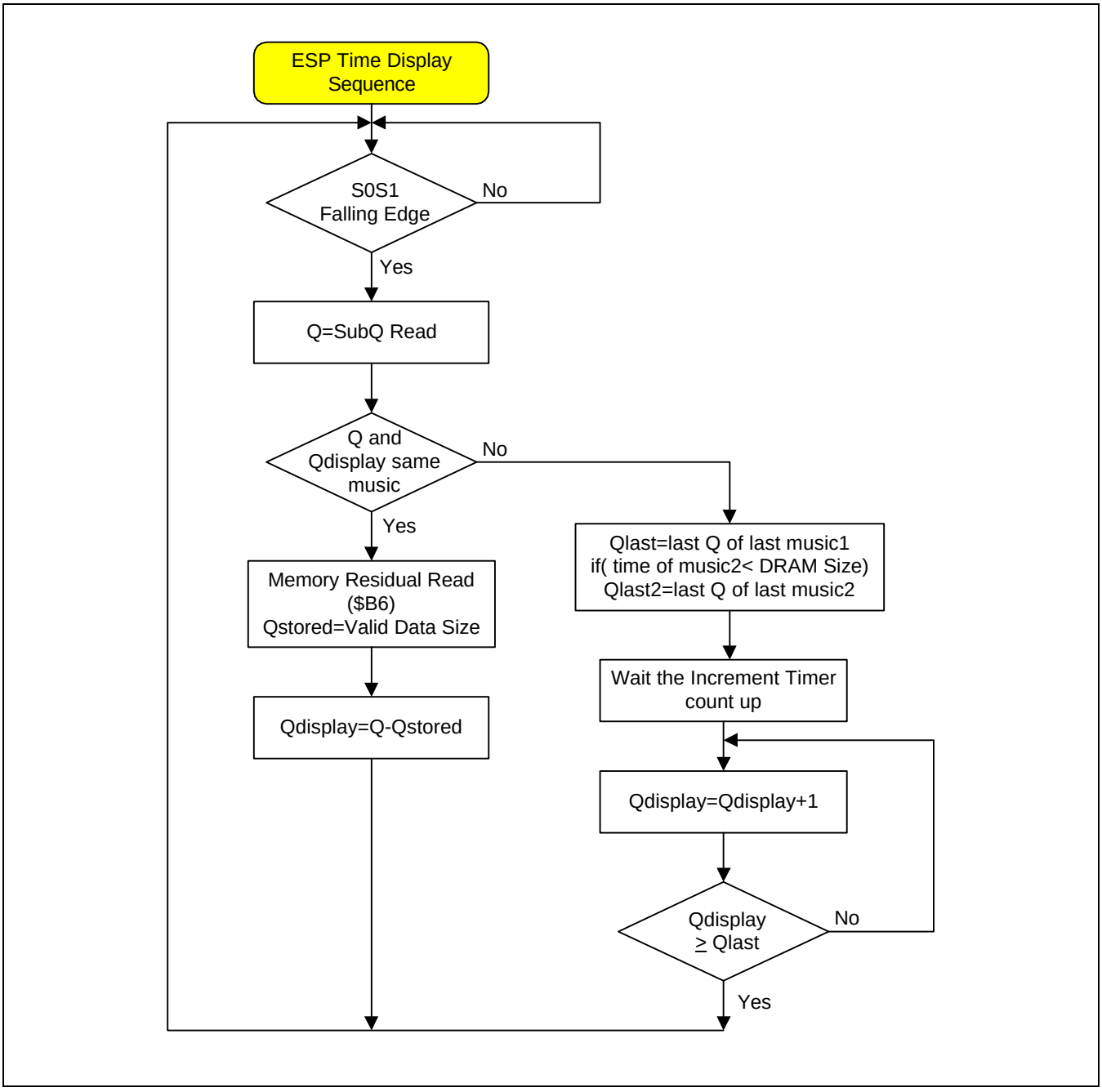
Soft ATTN On Sequence

In Soft Attn Command, Fade_in or Fade_out functions can be operated within 23.2ms
Fade Out :when $5D,1111_1110 Command is entered, Sound is fade out within 23.2ms
Fade In: When $5D,1111_1110 Command is entered, that is , from the start position of the music in Fade Out, when $5D 0000_0010 Command is entered, sound is fade in within 23.2ms.

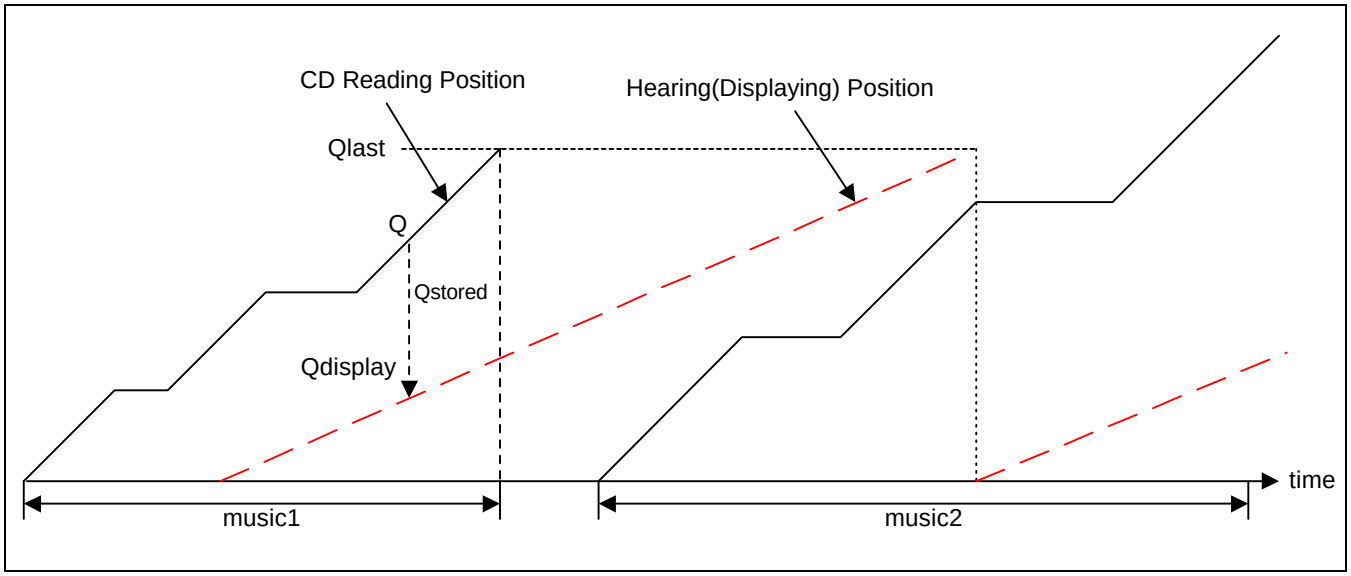
Soft ATTN On Sequence



ESP Time Display Sequence



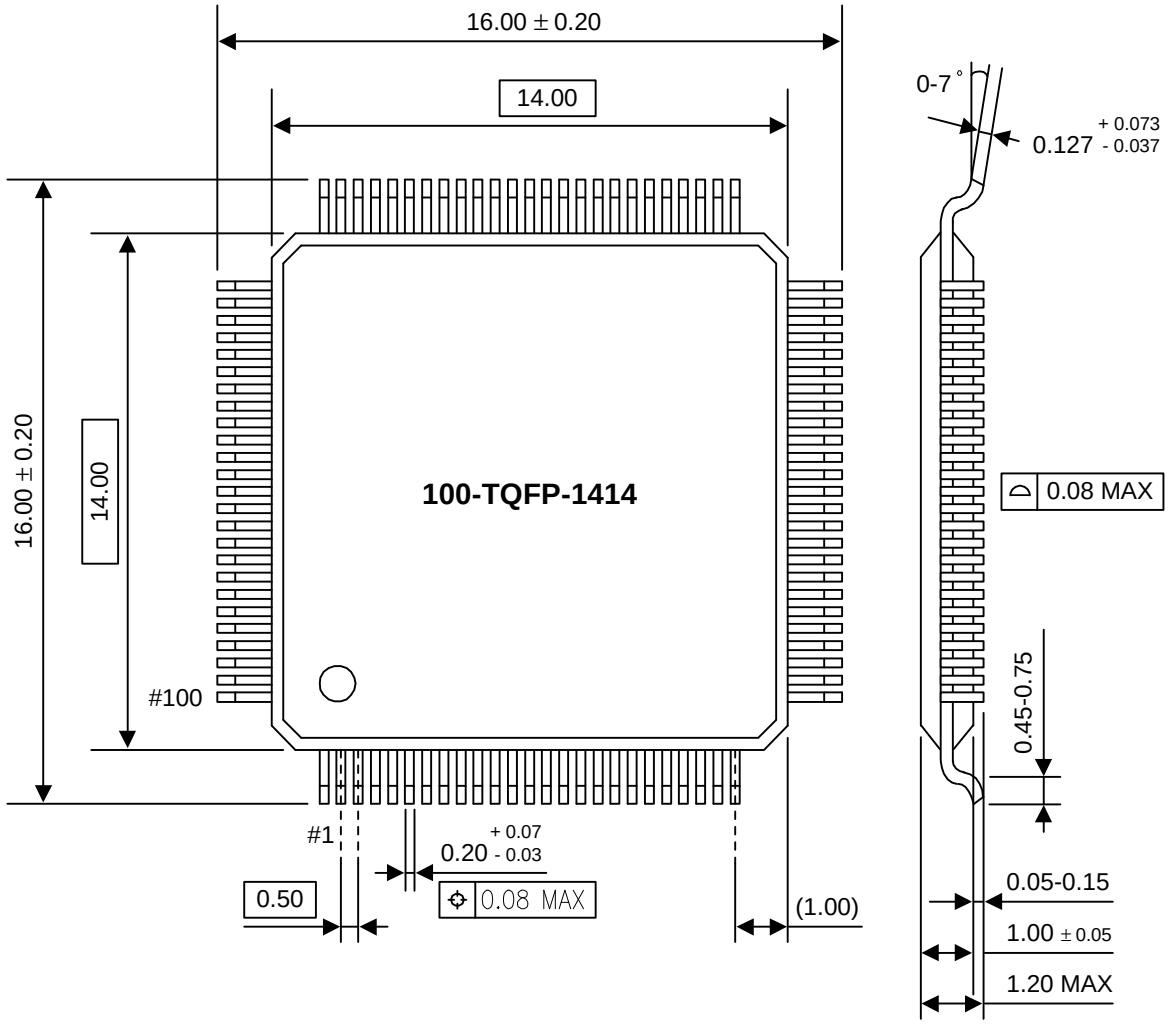
ESP Time Display Figure



ESP DATX Sequence

In Normal X1 speed mode, ESP ON, or external MP3 mode, for obtaining the DATX Output. $91,0000_0001 Command is used.

PACKAGE DIMENSION



NOTE: Dimensions are in millimeters.

NOTES