Digital DC/DC PMBus 12A Module

ZL9101M

The ZL9101M is a 12A variable output step-down PMBus-compliant digital power supply. Included in the module is a high performance digital PWM controller, power MOSFETs, an inductor, and all the passive components required for a complete DC/DC power solution. The ZL9101M operates over a wide input voltage range and supports an output voltage range of 0.6V to 4V, which can be set by external resistors or via PMBus. This high efficiency power module is capable of delivering 12A. Only bulk input and output capacitors are needed to finish the design. The output voltage can be precisely regulated to as low as 0.6V with ±1% output voltage regulation over line, load, and temperature variations.

The ZL9101M features internal compensation, internal soft-start, auto-recovery overcurrent protection, an enable option, and pre-biased output start-up capabilities.

The ZL9101M is packaged in a thermally enhanced, compact (15mmx15mm) and low profile (3.5mm) over-molded QFN package module suitable for automated assembly by standard surface mount equipment. The ZL9101M is Pb-free and RoHS compliant.

Features

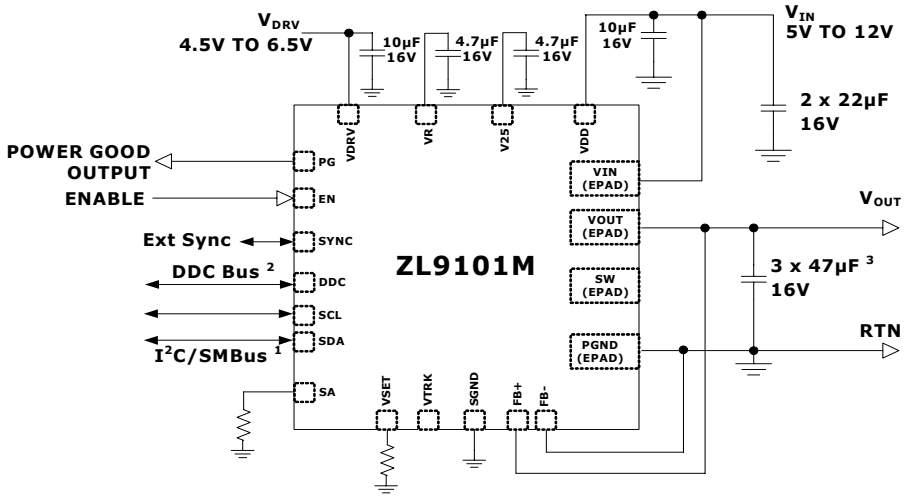
- Complete Digital Switch Mode Power Supply
- Fast Transient Response
- External Synchronization
- Tracking
- Current Sharing
- Programmable Soft-start Delay and Ramp
- Overcurrent/Undercurrent Protection
- PMBus Compliant

Applications

- Server, Telecom, and Datacom
- Industrial and Medical Equipment
- General Purpose Point of Load

Related Literature

- See AN2033, “Zilker Labs PMBus Command Set - DDC Products”
- See AN2034, “Configuring Current Sharing on the ZL2004 and ZL2006”



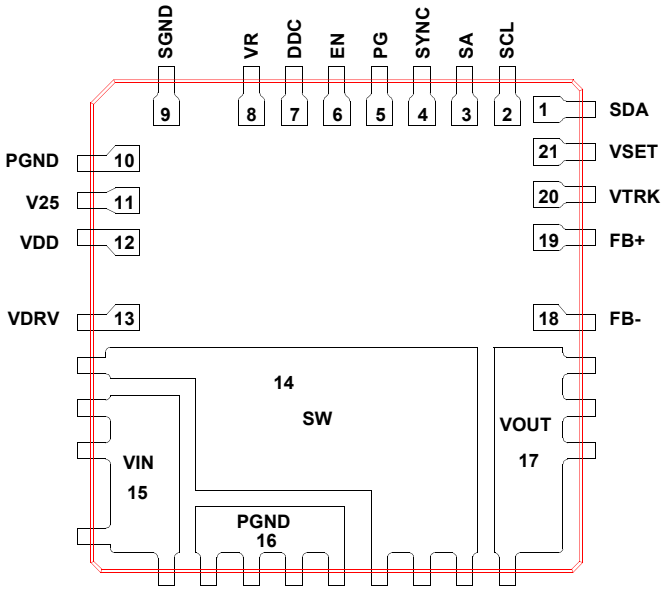
Notes:
1. The I²C/SMBus requires pull-up resistors. Please refer to the I²C/SMBus specifications for more details.
2. The DDC bus requires a pull-up resistor. The resistance will vary based on the capacitive loading of the bus (and on the number of devices connected). The 10kΩ default value, assuming a maximum of 100pF per device, provides the necessary 1µs pull-up rise time. Please refer to the Digital-DC Bus section for more details.
3. Additional capacitance may be required to meet specific transient response targets

FIGURE 1. 12A APPLICATION CIRCUIT

NOTE: Figure 1 represents a typical implementation of the ZL9101M. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.

Pin Configuration

ZL9101M
(21 LD QFN)
TOP VIEW



PIN	LABEL	TYPE	DESCRIPTION
1	SDA	I/O	Serial data.
2	SCL	I/O	Serial clock.
3	SA	I	Serial address select pin. Used to assign unique SMBus address to each module.
4	SYNC	I/O	Clock synchronization. Used for synchronization to external frequency reference.
5	PG	O	Power-good output.
6	EN	I	Enable input (factory setting active high). Pull-up to enable PWM switching and pull-down to disable PWM switching.
7	DDC	I/O	Digital-DC bus. (open drain) Interoperability between Zilker Labs modules.
8	VR	PWR	Internal 5V reference used to power internal drivers.
9	SGND	PWR	Signal ground. Connect to low impedance ground plane.
10	PGND	PWR	Power ground. Connect to low impedance ground plane.
11	V25	PWR	Internal 2.5V reference used to power internal circuitry.
12	VDD	PWR	Input supply voltage for controller.
13	VDRV	PWR	Power supply for internal FET drivers. Connect 10µF bypass capacitor to this pin.
14(epad)	SW	PWR	Drive train switch node
15(epad)	VIN	PWR	Power supply input FET voltage.
16(epad)	PGND	PWR	Power ground. Connect to low impedance ground plane.
17(epad)	VOUT	PWR	Power supply output voltage. Output voltage from PWM.
18	FB-	I	Output voltage feedback. Connect to load return of ground regulation point.
19	FB+	I	Output voltage feedback. Connect to output regulation point.
20	VTRK	I	Tracking sense input. Used to track an external voltage source.
21	VSET	I	Output voltage selection pin. Used to set V_{OUT} set point and V_{OUT} max.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ZL9101MIRZ	ZL9101M	-40 to +85	21 LD 15x15 QFN	L21.15x15

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil plastic packaged products employ special material sets, molding compounds and 100% matte tin plate plus anneal (e3) termination finish. These products do contain Pb but they are RoHS compliant by EU exemption 5 (Pb in glass of cathode ray tubes, electronic components and fluorescent tubes). These Intersil RoHS compliant products are compatible with both SnPb and Pb-free soldering operations. These Intersil RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ZL9101M. For more information on MSL please see techbrief TB363.

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Absolute Maximum Ratings (Note 4)

DC Supply Voltage for VDD Pin . . . . . -0.3V to 16V
Input Voltage for VIN Pin . . . . . -0.3V to 16V
MOSFET Drive Reference for VR Pin . . . . . -0.3V to 6.5V
2.5V Logic Reference for V25 Pin. . . . . -0.3V to 3V
MOSFET Driver Power for VDRV Pin . . . . . -0.3V to 7.5V
Logic I/O Voltage for DDC, EN,
FB+, FB-, PG, SA, SCL, SDA,SYNC, VSET Pins . . . . . -0.3V to 6V
ESD Rating
  Human Body Model (Tested per JESD22-A114F) 2000V
  Machine Model (Tested per JESD22-A115C) 200V
  Charged Device Model (Tested per JESD22-C110D) 1000V
Latch Up (Tested per JESD78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 7, 8)	11.5	2.2

Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Input Supply Voltage Range, V_{IN} . . . . . 5V to 14V
Input Supply For Controller, V_{DD} (Note 5) . . . . . 5V to 14V
Driver Supply Voltage, V_{DRV} . . . . . 4.5V to 6.5V
Output Voltage Range, V_{OUT} (Note 6). . . . . 0.54V to 4V
Output Current Range, $I_{OUT(DC)}$ . . . . . 0A to 15A
Operating Junction Temperature Range, T_J. . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Voltage measured with respect to SGND
5. V_{IN} supplies the power FETs. V_{DD} supplies the controller. V_{IN} can be tied to V_{DD}. For $V_{DD} \leq 5.5V$, V_{DD} should be tied to VR.
6. Includes ±10% margin limits.
7. θ_{JA} is simulated in free air with device mounted on a four-layer FR-4 test board (76.2 x 114.3 x 1.6mm) with 80%-coverage, 2-ounce Cu on top and bottom layers, plus two, buried, one-ounce Cu layers with coverage across the entire test board area. Multiple vias were used, with via diameter = 0.3mm on 1.2mm pitch.
8. For θ_{JC}, the “case” temperature is measured at the center of the package underside.

Electrical Specifications

V_{DD} = 12 V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	CONDITIONS	MIN (Note 9)	TYP (Note 10)	MAX (Note 9)	UNIT
INPUT AND SUPPLY CHARACTERISTICS					
Input Bias Supply Current, I_{DD}	f_{SW} = 615kHz, No load	–	20	**40**	mA
Input Bias Shutdown Current, I_{DDS}	EN = 0 V No I^2C/SMBus activity	–	9.5	**12**	mA
Input Supply Current, I_{VIN}	V_{IN} = 14V, I_{OUT} = 15A, V_{OUT} = 1.2V	–	1.5	**2**	A
Driver Supply Current, I_{VDRV}	Not switching	–	190	**220**	µA
VR Reference Output Voltage (Note 11)	V_{DD} > 6V, I_{VR} < 20mA	**4.5**	5.2	**5.7**	V
V25 Reference Output Voltage (Note 11)	V_R > 3V, I_{V25} < 20mA	**2.25**	2.5	**2.75**	V
OUTPUT CHARACTERISTICS					
Line Regulation Accuracy, $\Delta V_{OUT}/\Delta V_{IN}$ (Note 12)	V_{OUT} = 1.2V, I_{OUT} = 0A, V_{IN} = 5V to 14V	–	0.5	–	%
Load Regulation Accuracy, $\Delta V_{OUT}/\Delta I_{OUT}$ (Note 12)	I_{OUT} = 0A to 12A, V_{OUT} = 1.2V	–	0.5	–	%
Peak-to-peak Output Ripple Voltage, ΔV_{OUT} (Note 12)	I_{OUT} = 12A, V_{OUT} = 1.2V, C_{OUT} = 3000µF	–	6	–	mV
Soft-start Delay Duration Range (Notes 11, 13)	Set using I^2C/SMBus	**2**	–	**200**	ms
Soft-start Delay Duration Accuracy (Note 11)	Turn-on delay (precise mode) (Notes 13, 14)	–	±0.25	-	ms
	Turn-on delay (normal mode) (Note 15)	–	-0.25/+4	-	ms
	Turn-off delay (Note 15)	–	-0.25/+4	-	ms
Soft-start Ramp Duration Range (Note 11)	Set using I^2C	**0**	–	**200**	ms

Electrical Specifications V_{DD} = 12 V, T_A = -40 °C to +85 °C unless otherwise noted. Typical values are at T_A = 25 °C. **Boldface limits apply over the operating temperature range, -40 °C to +85 °C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 9)	TYP (Note 10)	MAX (Note 9)	UNIT
Soft-start Ramp Duration Accuracy (Note 11)		–	100	–	µs
DYNAMIC CHARACTERISTICS					
Voltage Change for Positive Load Step	ΔI_{OUT} = 6A, slew rate = 2.5A/µs, V_{OUT} = 1.2V, C_{OUT} = 3000µF	–	3	–	%
Voltage Change for Negative Load Step	ΔI_{OUT} = 6A, slew rate = 2.5A/µs, V_{OUT} = 1.2V, C_{OUT} = 3000µF	–	3	–	%
OSCILLATOR AND SWITCHING CHARACTERISTICS (Note 11)					
Switching Frequency Range		**590**	615	**630**	kHz
Maximum PWM Duty Cycle	Factory setting	**95**	–	–	%
Minimum SYNC Pulse Width		**150**	–	–	ns
Input clock Frequency Drift Tolerance	External clock source	**-13**	–	**13**	%
LOGIC INPUT/OUTPUT CHARACTERISTICS (Note 11)					
Logic Input Bias Current	EN, PG, SCL, SDA pins	**-10**	–	**10**	µA
Logic Input Low, V_{IL}		–	–	**0.8**	V
Logic Input High, V_{IH}		**2.0**	–	–	V
Logic Output Low, V_{OL}	I_{OL} ≤ 4mA (Note 17)	–	–	**0.4**	V
Logic Output High, V_{OH}	I_{OH} ≥ -2mA (Note 17)	**2.25**	–	–	V
FAULT PROTECTION CHARACTERISTICS (Note 11)					
UVLO Threshold Range	Configurable via I^2C/SMBus	**2.85**	–	**16**	V
UVLO Set-point Accuracy		**-150**	–	**150**	mV
UVLO Hysteresis	Factory setting	–	3	–	%
	Configurable via I^2C/SMBus	**0**	–	**100**	%
UVLO Delay		–	–	**2.5**	µs
Power Good V_{OUT} Threshold	Factory setting	–	90	–	% V_{OUT}
Power Good V_{OUT} Hysteresis	Factory setting	–	5	–	%
Power Good Delay (Note 16)	Configurable via I^2C/SMBus	**0**	–	**200**	ms
VSEN Undervoltage Threshold	Factory setting	–	85	–	% V_{OUT}
	Configurable via I^2C/SMBus	**0**	–	**110**	% V_{OUT}
VSEN Overvoltage Threshold	Factory setting	–	115	–	% V_{OUT}
	Configurable via I^2C/SMBus	**0**	–	**115**	% V_{OUT}
VSEN Undervoltage Hysteresis		–	5	–	% V_{OUT}
VSEN Undervoltage/Overvoltage Fault Response Time	Factory setting	–	16	–	µs
	Configurable via I^2C/SMBus	**5**	–	**60**	µs

Electrical Specifications

V_{DD} = 12 V, T_A = -40 °C to +85 °C unless otherwise noted. Typical values are at T_A = 25 °C. **Boldface limits apply over the operating temperature range, -40 °C to +85 °C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 9)	TYP (Note 10)	MAX (Note 9)	UNIT
Thermal Protection Threshold (Controller Junction Temperature)	Factory setting	–	125	–	°C
	Configurable via I^2C/SMBus	**-40**	–	**125**	°C
Thermal Protection Hysteresis		–	15	–	°C

NOTES:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
10. Parameters with TYP limits are not production tested unless otherwise specified.
11. Parameters are 100% tested for internal IC prior to module assembly.
12. V_{OUT} measured at the termination of the FB+ and FB- sense points.
13. The device requires a delay period following an enable signal and prior to ramping its output. Precise timing mode limits this delay period to approximately 2ms, where in normal mode it may vary up to 4ms.
14. Precise ramp timing mode is only valid when using the EN pin to enable the device rather than PMBus enable.
15. The devices may require up to a 4ms delay following the assertion of the enable signal (normal mode) or following the de-assertion of the enable signal.
16. Factory setting for Power Good delay is set to the same value as the soft-start ramp time.
17. Nominal capacitance of logic pins is 5pF.

Typical Performance Curves

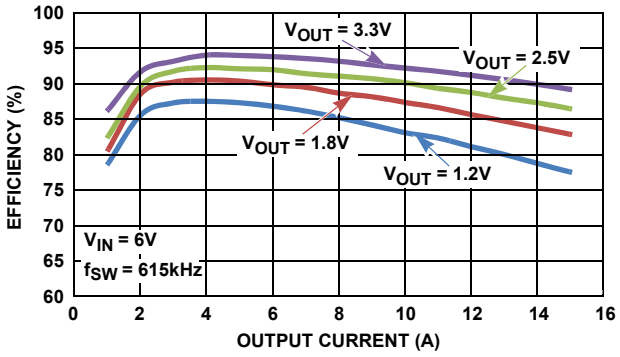


FIGURE 2. EFFICIENCY, V_{IN} = 6V

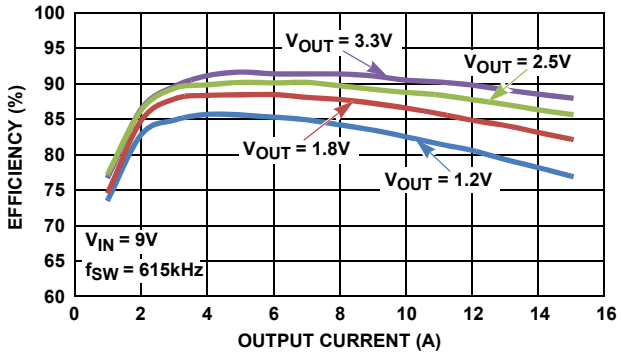


FIGURE 3. EFFICIENCY, V_{IN} = 9V

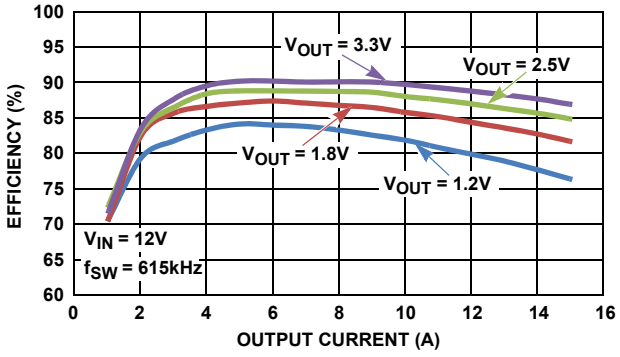


FIGURE 4. EFFICIENCY, V_{IN} = 12V

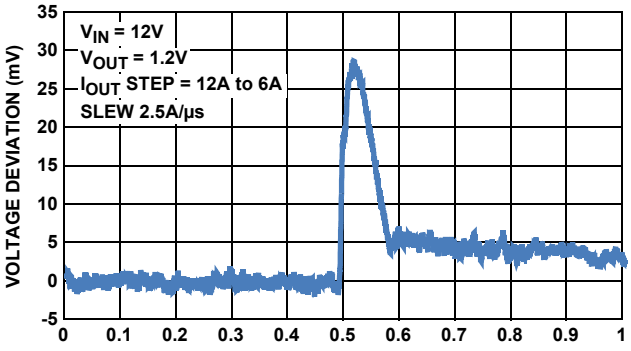


FIGURE 5. DYNAMIC RESPONSE, UNLOADING

Typical Performance Curves (Continued)

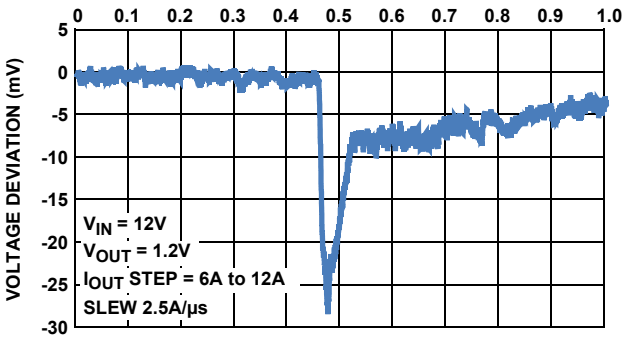


FIGURE 6. DYNAMIC RESPONSE, LOADING

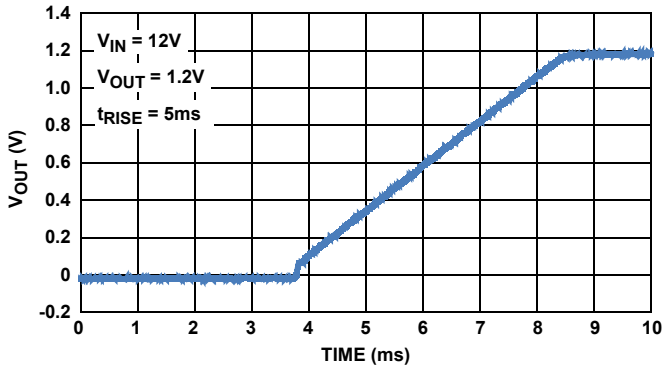


FIGURE 7. RAMP-UP

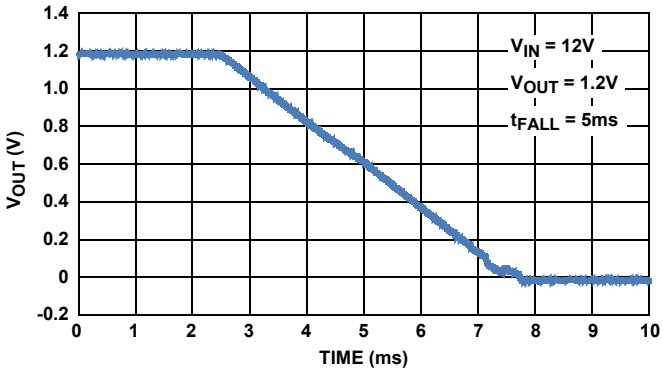


FIGURE 8. RAMP-DOWN

Derating Curves

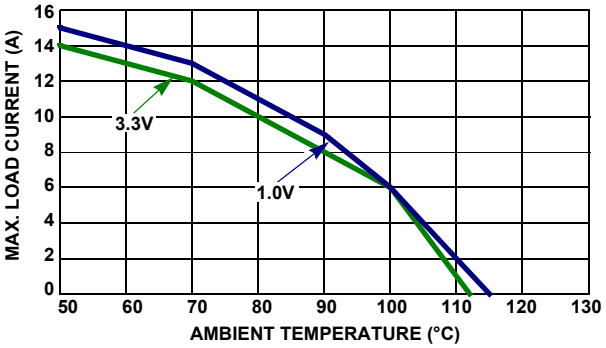


FIGURE 9A. DERATING CURVE, $5V_{IN}$

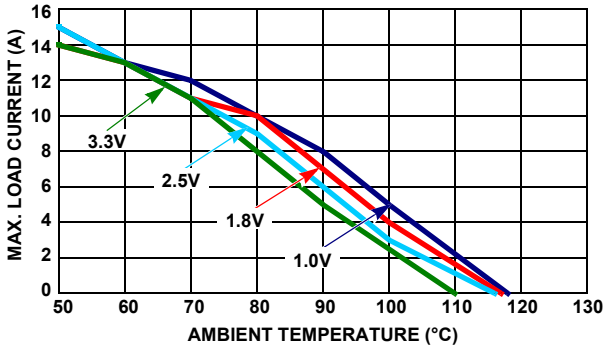


FIGURE 9B. DERATING CURVE, $12V_{IN}$

Functional Description

Output Voltage Selection

The output voltage may be set to a voltage between 0.6V and 4.0V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification.

The VSET pin is used to set the output voltage to levels as shown in Table 1. The R_{SET} resistor is placed between the VSET pin and SGND.

TABLE 1. OUTPUT VOLTAGE RESISTOR SETTINGS

V_{OUT} (V)	R_{SET} (kΩ)
0.60	10
0.65	11
0.70	12.1
0.75	13.3
0.80	14.7
0.85	16.2
0.90	17.8
0.95	19.6
1.00	21.5
1.05	23.7
1.10	26.1
1.15	28.7
1.20	31.6
1.25	34.8
1.30	38.3
1.40	42.2
1.50	46.4
1.60	51.1
1.70	56.2
1.80	61.9
1.90	68.1
2.00	75
2.10	82.5
2.20	90.9
2.30	100
2.50	110
2.80	121
3.00	133
3.30	147
4.00	162

The output voltage may also be set to any value between 0.6V and 4.0V using a PMBus command over the I^2C/SMBus interface. See Application Note AN2033 for details.

Soft-start Delay and Ramp Times

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ZL9101M gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay and ramp times are set to custom values via the I^2C/SMBus interface. When the delay time is set to 0ms, the device will begin its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output will ramp up as quickly as the output load capacitance and loop settings will allow. It is generally recommended to set the soft-start ramp to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current.

Power Good

The ZL9101M provides a Power Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within 10% of the target voltage. These limits and the polarity of the pin may be changed via the I^2C/SMBus interface. See Application Note AN2033 for details.

A PG delay period is defined as the time from when all conditions within the ZL9101M for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL9101M PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 10ms, the PG delay will be set to 10ms. The PG delay may be set independently of the soft-start ramp using the I^2C/SMBus as described in Application Note AN2033.

Switching Frequency and PLL

The ZL9101M incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source.

The internal switching frequency of the ZL9101M is 615kHz.

Loop Compensation

The ZL9101M operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. The module is internally compensated via the I^2C/SMBus interface. Please refer to Application Note AN2033 for further details.

Adaptive Diode Emulation

Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is available to single-phase devices only.

Note: the overall bandwidth of the device may be reduced when in diode emulation mode. It is recommended that diode emulation is disabled prior to applying significant load steps.

Input Undervoltage Lockout

The input undervoltage lockout (UVLO) prevents the ZL9101M from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 2.85V and 16V using the I^2C/SMBus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the module. The controller will continuously check for the presence of the fault condition. If the fault condition is no longer present, the ZL9101M will be re-enabled.

Please refer to Application Note AN2033 for details on how to configure the UVLO threshold or to select specific UVLO fault response options via the I^2C/SMBus interface.

Output Overvoltage Protection

The ZL9101M offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the FB+ pin) to a threshold set to 15% higher than the target output voltage (the default setting). If the FB+ voltage exceeds this threshold, the PG pin will de-assert and the controller can then respond in a number of ways as follows:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains ON until the device attempts a restart.

The default response from an overvoltage fault is to immediately shut down. The controller will continuously check for the presence of the fault condition, and when the fault condition no longer exists the device will be re-enabled.

For continuous overvoltage protection when operating from an external clock, the only allowed response is an immediate shutdown.

Please refer to Application Note AN2033 for details on how to select specific overvoltage fault response options via I^2C/SMBus.

Output Pre-Bias Protection

An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start up if a pre-bias condition exists at the output. The ZL9101M provides pre-bias protection by sampling the output voltage prior to initiating an output ramp.

If a pre-bias voltage lower than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output will take to ramp from the pre-bias voltage to the target voltage will vary depending on the pre-bias voltage but the total time elapsed from when the delay period expires and when the output reaches its target value will match the pre-configured ramp time. See Figure 10.

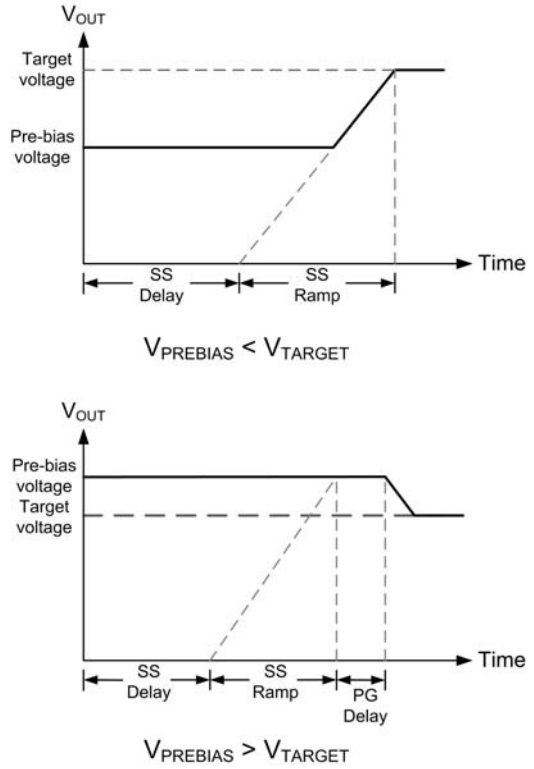


FIGURE 10. OUTPUT RESPONSES TO PRE-BIAS VOLTAGES

If a pre-bias voltage higher than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled with a PWM duty cycle that would ideally create the pre-bias voltage.

Once the pre-configured soft-start ramp period has expired, the PG pin will be asserted (assuming the pre-bias voltage is not higher than the overvoltage limit). The PWM will then adjust its

duty cycle to match the original target voltage and the output will ramp down to the preconfigured output voltage.

If a pre-bias voltage higher than the overvoltage limit exists, the device will not initiate a turn-on sequence and will declare an overvoltage fault condition to exist. In this case, the device will respond based on the output overvoltage fault response method that has been selected. See “Output Overvoltage Protection” on page 10 for response options due to an overvoltage condition.

Note that pre-bias protection is not offered for current sharing groups that also have tracking enabled.

Output Overcurrent Protection

The ZL9101M can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. The following overcurrent protection response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown of the controller. The controller will continuously check for the presence of the fault condition, and if the fault condition no longer exists the device will be re-enabled.

Please refer to Application Note AN2033 for details on how to select specific overcurrent fault response options via I^2C/SMBus.

Thermal Overload Protection

The ZL9101M includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The default temperature limit is set to +125°C in the factory, but the user may set the limit to a different value if desired. See Application Note AN2033 for details. Note that setting a higher thermal limit via the I^2C/SMBus interface may result in permanent damage to the controller. Once the module has been disabled due to an internal temperature fault, the user may select one of several fault response options as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

If the user has configured the module to restart, the controller will wait the preset delay period (if configured to do so) and will then check the module temperature. If the temperature has dropped below a threshold that is approximately +15 °C lower than the selected temperature fault limit, the controller will attempt to re-start. If the temperature still exceeds the fault limit the controller will wait the preset delay period and retry again.

The default response from a temperature fault is an immediate shutdown of the module. The controller will continuously check for the fault condition, and once the fault has cleared the ZL9101M will be re-enabled.

Please refer to Application Note AN2033 for details on how to select specific temperature fault response options via I^2C/SMBus.

I^2C/SMBus Communications

The ZL9101M provides an I^2C/SMBus digital interface that enables the user to configure all aspects of the module operation as well as monitor the input and output parameters. The ZL9101M can be used with any I^2C host device. In addition, the module is compatible with SMBus version 2.0. Pull-up resistors are required on the I^2C/SMBus as specified in the SMBus 2.0 specification. The ZL9101M accepts most standard PMBus commands. When controlling the device with PMBus commands, it is recommended that the enable pin is tied to SGND.

I^2C/SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between the SA pin and SGND. Table 2 lists the available module addresses.

TABLE 2. SMBus ADDRESS RESISTOR SELECTION

R_{SA0}	SMBus Address
10	0x19
11	0x1A
12.1	0x1B
13.3	0x1C
14.7	0x1D
16.2	0x1E
17.8	0x1F
19.6	0x20
21.5	0x21
23.7	0x22
26.1	0x23
28.7	0x24
31.6	0x25
34.8	0x26
38.3	0x27
42.2	0x28
46.4	0x29
51.1	0x2A
56.2	0x2B

TABLE 2. SMBus ADDRESS RESISTOR SELECTION (Continued)

R_{SA0}	SMBus Address
61.9	0x2C
68.1	0x2D
75	0x2E
82.5	0x2F
90.9	0x30
100	0x31

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Zilker Labs Digital-DC modules and devices. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading, and current sharing. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as follows:

$$\text{Rise Time} = R_{PU} * C_{LOAD} \approx 1\mu s \quad \text{(EQ. 1)}$$

where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor may be tied to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. As rules of thumb, each device connected to the DDC bus presents approximately 10pF of capacitive loading, and each inch of FR4 PCB trace introduces approximately 2pF. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the device monitoring point) given the pull-up voltage and the pull-down current capability of the ZL9101M (nominally 4mA).

Phase Spreading

When multiple point of load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

In order to enable phase spreading, all converters must be synchronized to the same switching clock.

The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments via the I^2C/SMBus interface. Refer to Application Note AN2033 for further details.

Output Sequencing

A group of Digital-DC modules or devices may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage in order to avoid latch-up from occurring. Multi-device sequencing can be achieved by configuring each device through the I^2C/SMBus interface.

Multiple device sequencing is configured by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group.

Refer to Application Note AN2033 for details on sequencing via the I^2C/SMBus interface.

Fault Spreading

Digital DC modules and devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the DDC bus. The other devices on the DDC bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

Active Current Sharing

Paralleling multiple ZL9101M modules can be used to increase the output current capability of a single power rail. By connecting the DDC pins of each module together and configuring the modules as a current sharing rail, the units will share the current equally within a few percent.

Figure 11 illustrates a typical connection for two modules.

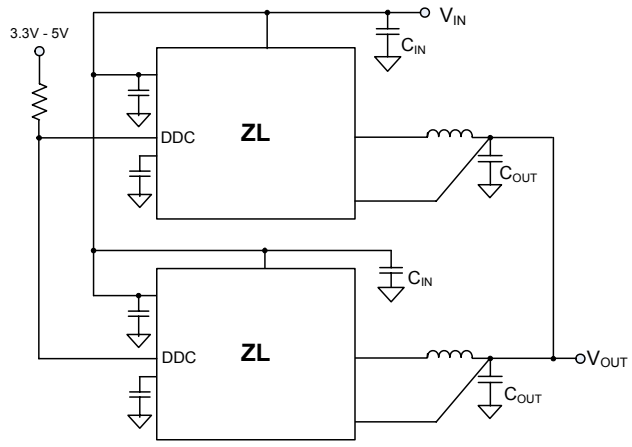


FIGURE 11. CURRENT SHARING GROUP

The ZL9101M uses a low-bandwidth, first-order digital current sharing technique to balance the unequal module output loading by aligning the load lines of member modules to a reference module.

Droop resistance is used to add artificial resistance in the output voltage path to control the slope of the load line curve,

calibrating out the physical parasitic mismatches due to power train components and PCB layout.

Upon system start-up, the module with the lowest member position as selected in ISHARE_CONFIG is defined as the reference module. The remaining modules are members. The reference module broadcasts its current over the DDC bus. The members use the reference current information to trim their voltages (V_{MEMBER}) to balance the current loading of each module in the system.

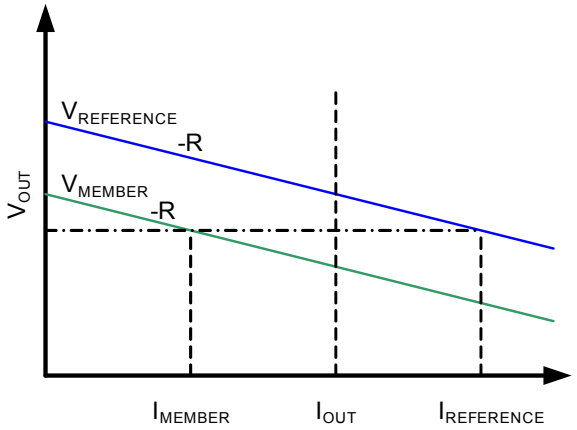


FIGURE 12. ACTIVE CURRENT SHARING

Figure 12 shows that, for load lines with identical slopes, the member voltage is increased towards the reference voltage which closes the gap between the inductor currents.

The relation between reference and member current and voltage is given by the following equation:

$$V_{MEMBER} = V_{OUT} + R \times \left(I_{REFERENCE} - I_{MEMBER} \right) \quad \text{(EQ. 2)}$$

where *R* is the value of the droop resistance.

The ISHARE_CONFIG command is used to configure the module for active current sharing. The default setting is a stand-alone non-current sharing module. A current sharing rail can be part of a system sequencing group.

For fault configuration, the current share rail is configured in a quasi-redundant mode. In this mode, when a member module fails, the remaining members will continue to operate and attempt to maintain regulation. Of the remaining modules, the module with the lowest member position will become the reference. If fault spreading is enabled, the current share rail failure is not broadcast until the entire current share rail fails.

The phase offset of (multi-phase) current sharing modules is automatically set to a value between 0° and 337.5° in 22.5° increments as follows:

$$Phase\ Offset = SMBus\ Address[4:0] - Current\ Share\ Position * 22.5° \quad \text{(EQ. 3)}$$

Please refer to Application Note AN2034 for additional details on current sharing.

Phase Adding/Dropping

The ZL9101M allows multiple power converters to be connected in parallel to supply higher load currents than can be addressed using a single-phase design. In doing so, the power converter is optimized at a load current range that requires all phases to be operational. During periods of light loading, it may be beneficial to disable one or more phases in order to eliminate the current drain and switching losses associated with those phases, resulting in higher efficiency.

The ZL9101M offers the ability to add and drop phases using a PMBus command in response to an observed load current change. All phases in a current share rail are considered active prior to the current sharing rail ramp to power-good.

Any member of the current sharing rail can be dropped. If the reference module is dropped, the remaining active module with the lowest member position will become the new reference.

Additionally, any change to the number of members of a current sharing rail will precipitate autonomous phase distribution within the rail where all active phases realign their phase position based on their order within the number of active members.

If the members of a current sharing rail are forced to shut down due to an observed fault, all members of the rail will attempt to re-start simultaneously after the fault has cleared.

Monitoring via I²C/SMBus

A system controller can monitor a wide variety of different ZL9101M system parameters through the I²C/SMBus interface.

The module can monitor for any number of power conversion parameters including but not limited to the following:

- Input voltage/Output voltage
- Output current
- Internal temperature
- Switching frequency
- Duty cycle

Please refer to Application Note AN2033 for details on how to monitor specific parameters via the I²C/SMBus interface.

Snapshot Parameter Capture

The ZL9101M offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The Snapshot functionality is enabled by setting bit 1 of MISC_CONFIG to 1.

See AN2033 for details on using SnapShot in addition to the parameters supported. The Snapshot feature enables the user to read parameters via a block read transfer through the SMBus. This can be done during normal operation, although it should be noted that reading the 22 bytes will occupy the SMBus for some time.

The SNAPSHOT_CONTROL command enables the user to store the snapshot parameters to Flash memory in response to a pending fault as well as to read the stored data from Flash memory after a fault has occurred. Table 3 describes the usage of this command. Automatic writes to Flash memory following a fault are triggered when any fault threshold level is exceeded, provided that the specific fault's response is to shut down (writing to Flash memory is not allowed if the device is configured to re-try following the specific fault condition). It should also be noted that the module's V_{DD} voltage must be maintained during the time when the controller is writing the data to Flash memory;

a process that requires between 700µs to 1400µs depending on whether the data is set up for a block write. Undesirable results may be observed if the device's V_{DD} supply drops below 3.0V during this process.

TABLE 3. SNAPSHOT_CONTROL COMMAND

DATA VALUE	DESCRIPTION
1	Copies current SNAPSHOT values from Flash memory to RAM for immediate access using SNAPSHOT command.
2	Writes current SNAPSHOT values to Flash memory. Only available when device is disabled.

In the event that the module experiences a fault and power is lost, the user can extract the last SNAPSHOT parameters stored during the fault by writing a 1 to SNAPSHOT_CONTROL (transfers data from Flash memory to RAM) and then issuing a SNAPSHOT command (reads data from RAM via SMBus).

Non-Volatile Memory and Device Security Features

The ZL9101M has internal non-volatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the module to a level that has been made available to them.

During the initialization process, the ZL9101M checks for stored values contained in its internal non-volatile memory. The ZL9101M offers two internal memory storage units that are accessible by the user as follows:

1. *Default Store*: The ZL9101M has a default configuration that is stored in the Default Store in the controller. The module can be restored to its default settings by issuing a RESTORE_DEFAULT_ALL command over the SMBus.
2. *User Store*: The user can modify certain power supply settings as described in this data sheet. The user would use the User Store to store their configuration.

Please refer to Application Note AN2033 for details on how to set specific security measures via the I^2C/SMBus interface.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
12/20/2010	FN7669.0	Initial release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ZL9101M

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

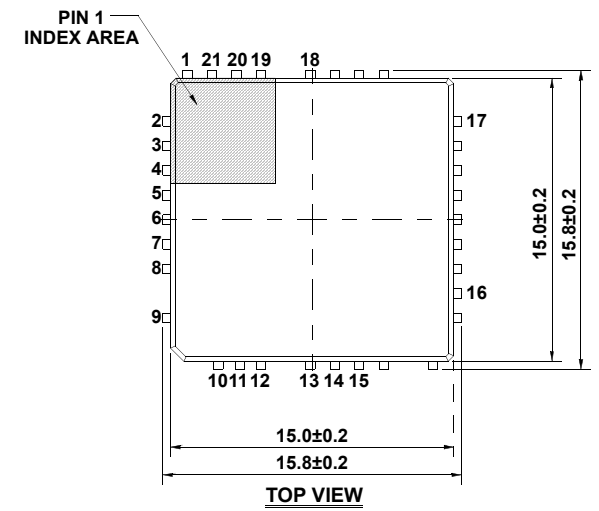
FITs are available from our website at http://rel.intersil.com/reports/search.php

Package Outline Drawing

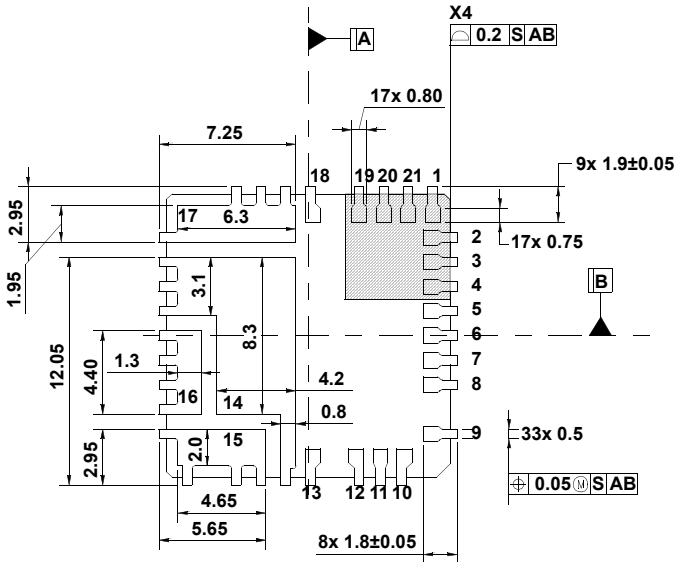
L21.15x15

21 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN)

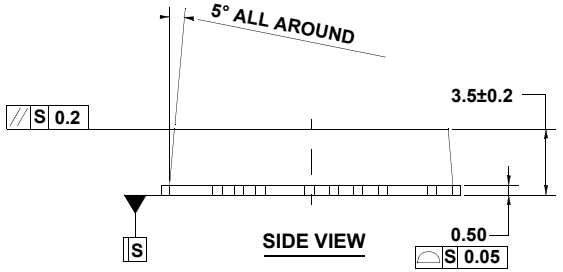
Rev 0, 10/10

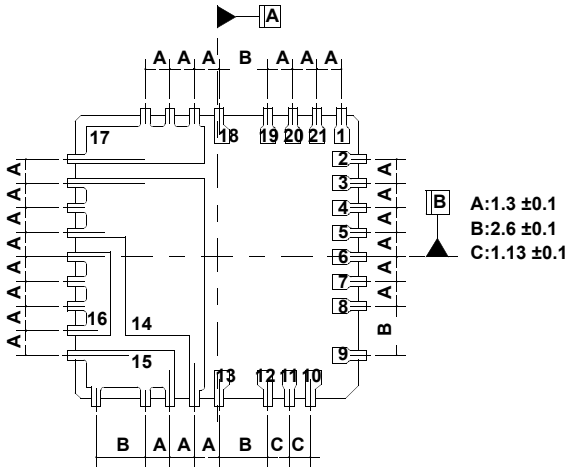


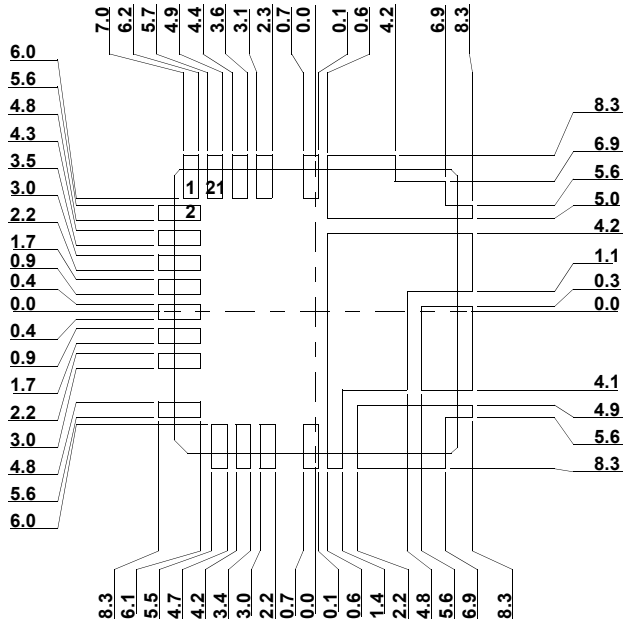
TOP VIEW



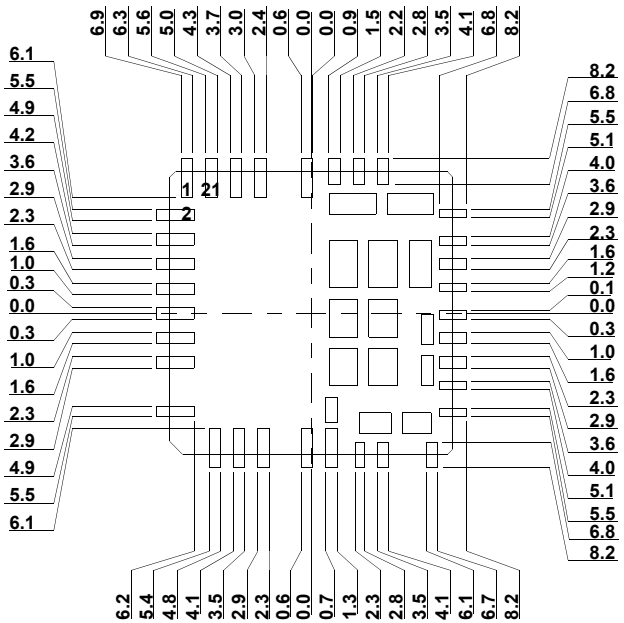
BOTTOM VIEW



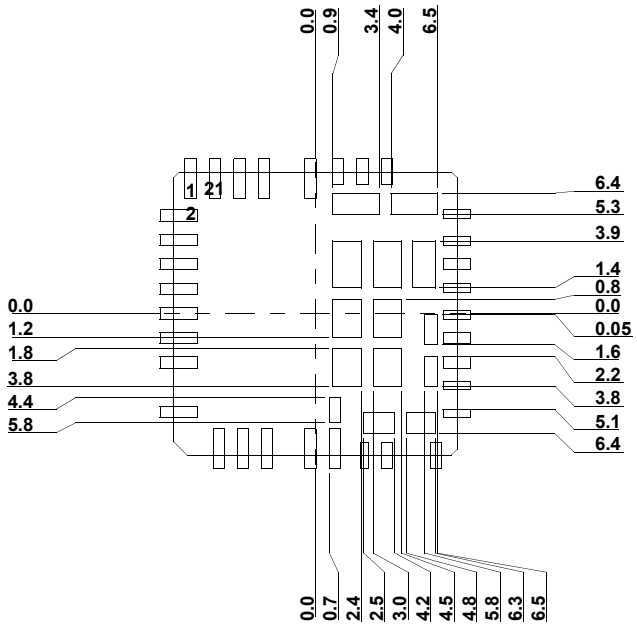




TYPICAL RECOMMENDED LAND PATTERN



STENCIL PATTERN WITH SQUARE PADS-1



STENCIL PATTERN WITH SQUARE PADS-2

NOTES:

1. **Dimensions are in millimeters.**
2. **Unless otherwise specified, tolerance : Decimal ± 0.2; Body Tolerance ±0.2mm**
3. **The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.**