Datasheet and Application

power electronics in motion
eupec

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Approved by: Michael Hornkamp
S/N: 010-04
Date of publication: 2003-12-05
Status: Target Data

EiceDRIVER™

2ED020I12-F

Dual IGBT Driver IC
for eupec Low and Medium Power IGBT Modules

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0 History

Revision 1.0	2003-01-24	First release
Revision 1.2	2003-05-16	Updated electrical characteristics
Revision 1.5	2003-12-05	New paper design Updated functional description Updated electrical characteristics New chapter “Diagrams” New chapter “Applications”

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1 Overview

The 2ED020I12-F is a high voltage, high speed power IGBT and MOSFET driver of the eupec *EiceDRIVER*™ family with interlocking high and low side referenced output channels. The floating high side driver may be supplied directly or by means of a bootstrap diode and capacitor. In addition to the logic input of each driver the 2ED020I12-F is equipped with a dedicated shutdown input. All logic inputs are compatible with 3.3 V and 5 V TTL. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. Both drivers are designed to drive an n-channel power IGBT or MOSFET which operates up to 1200 V. In addition, a general purpose operational amplifier and a general purpose comparator are provided, which may be used e.g. for current measurement or over current detection.

Product Highlights

- Fully operational to ±1200 V
- Gate drive supply range from 13 to 18 V
- Gate drive currents of +1 A / –2 A
- Matched propagation delay for both channels
- High dV/dt immunity
- General purpose operational amplifier
- General purpose comparator

Features

- Floating high side driver
- Under-voltage lockout for both channels
- 3.3 V and 5 V TTL compatible inputs
- CMOS Schmitt-triggered inputs with internal pull-down
- CMOS Schmitt-triggered shutdown with internal pull-up
- Non-inverting inputs
- Interlocking inputs
- Dedicated shutdown input with internal pull-up
- IEC compliant (pending)
- UL recognized (pending)

1.1 Coreless transformer (CLT) technology

In various IGBT and power MOSFET driver stages are optocoupler, level shifter or discrete transformer included to overcome the isolation barrier between the low side input and high side output. All of them have their typical advantages and disadvantages. As an alternative for low and medium power applications the coreless transformer technology combines almost all advantages and at the same time avoiding almost all disadvantages of these devices by a very cost efficient way and high voltage isolation capability.

The principle function of the CLT is realized by two coils which are compounded on silicon within one integrated circuit. The isolation between these coils can withstand in the current design at least up to 1200 V whereby a functional isolation is achieved. Figure 1 shows a schematic of the internal stages of the IC.

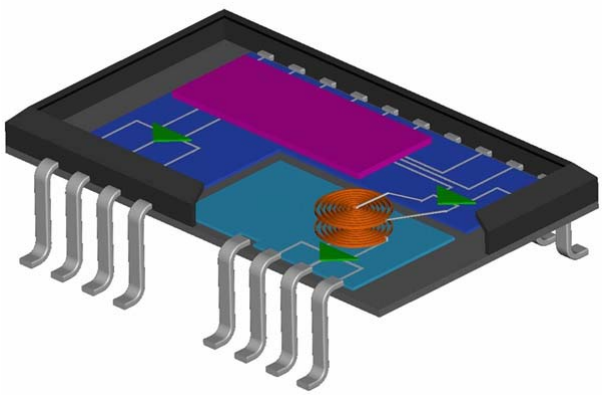
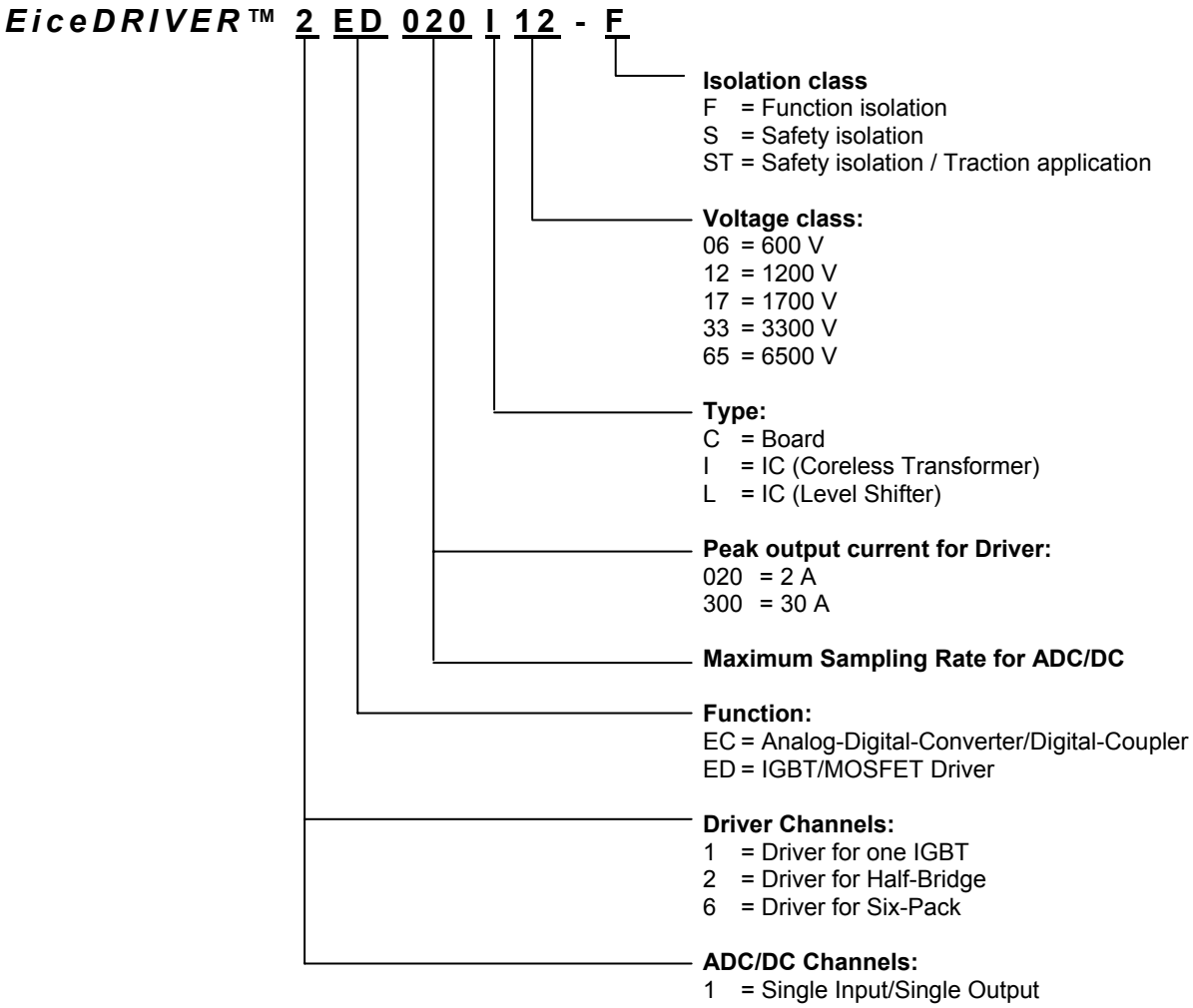


Figure 1 IC schematic

Each *EiceDRIVER*™ has a type number, which can be resolved by the following schemata:



2 Pin configuration and package outline

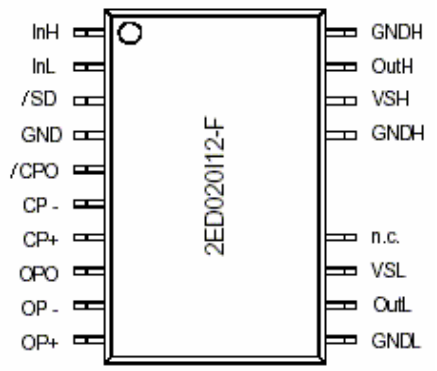
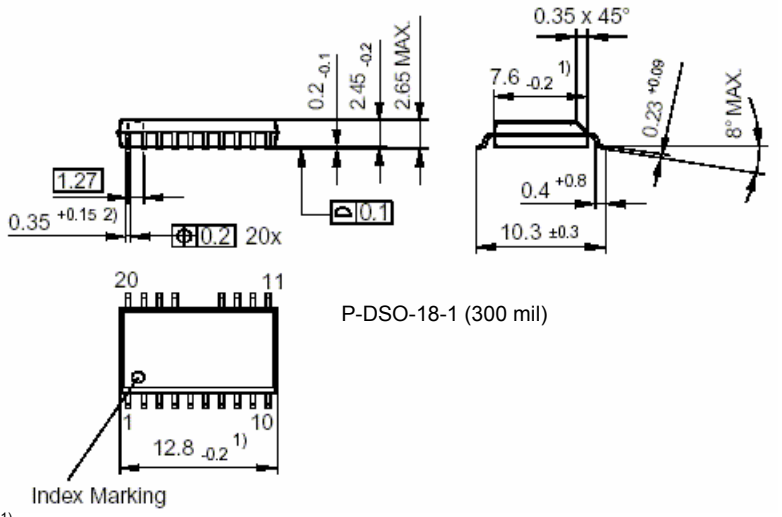


Figure 2 Pin configuration (top view)



1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

Figure 3 Package outline (all measures in mm)

Pin	Symbol	Function
1	InH	Logic input for high side driver
2	InL	Logic input for low side driver
3	/SD	Logic input for shutdown of both drivers
4	GND	Common ground
5	/CPO	Open drain output of general purpose comparator
6	CP-	Inverting input of general purpose comparator
7	CP+	Non-inverting input of general purpose comparator
8	OPO	Output of general purpose operational amplifier
9	OP-	Inverting input of general purpose operational amplifier
10	OP+	Non-inverting input of general purpose operational amplifier
11	GNDL	Low side supply ground
12	OutL	Low side gate driver output
13	VS	Low side supply voltage
14	n.c.	(not connected)
15	n.e.	(not existing)
16	n.e.	(not existing)
17	GNDH	High side supply ground
18	VSLH	High side supply voltage
19	OutH	High side gate driver output
20	GNDH	High side supply ground

3 Block diagram

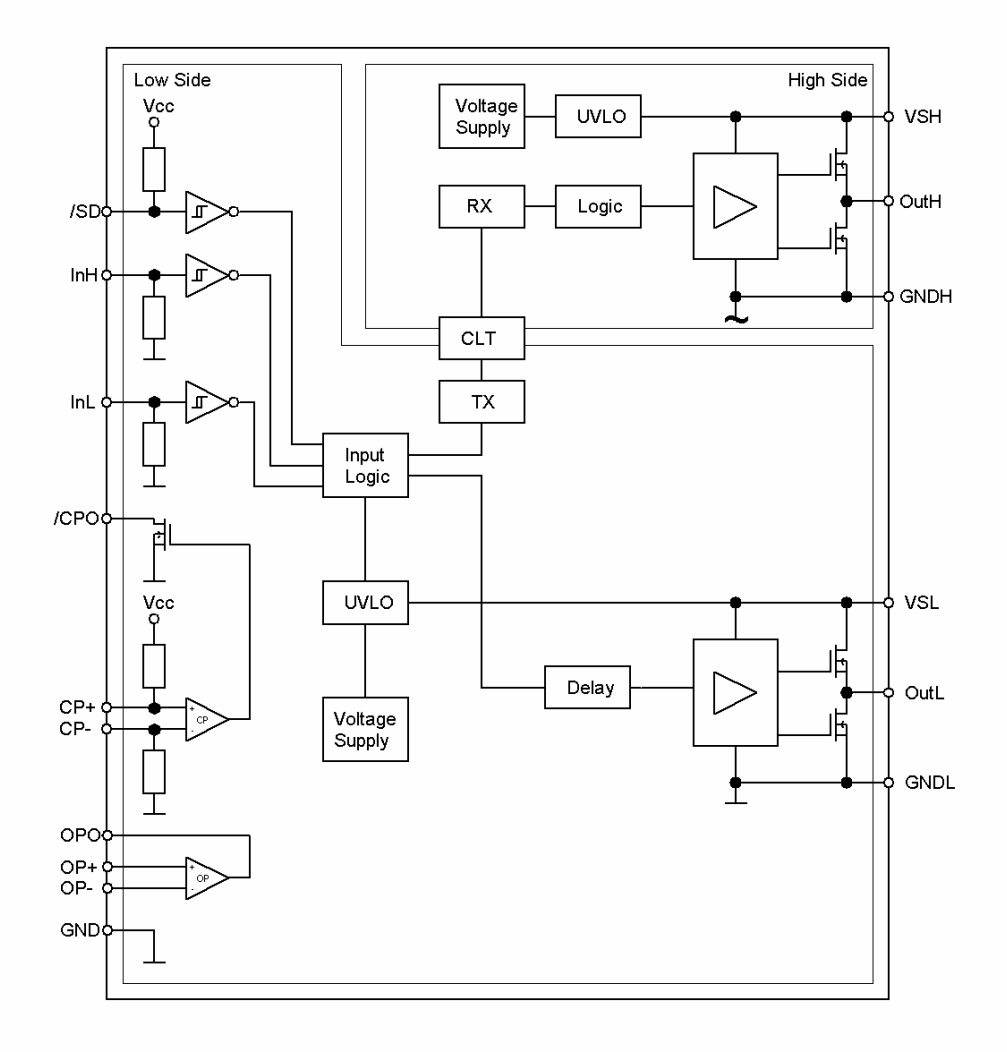


Figure 4 Block diagram

4 Functional description

4.1 Power supply

The power supply of both sides, VSL and VSH, is monitored by an under-voltage lockout block (UVLO) which enables operation of the corresponding side when the supply voltage reaches the “on” threshold of 12 V. Afterwards the internal voltage reference and the biasing circuit are enabled. When the supply voltage (VSL, VSH) drops below the “off” threshold of 11 V the circuit is disabled.

4.2 Logic inputs

The logic inputs InH, InL and /SD are fed into Schmitt-Triggers with thresholds compatible to 3.3 V and 5 V TTL. When /SD is enabled (low), InH and InL are disabled. If InH is high (while InL is low), OutH is enabled and vice versa. However, if both signals are high, they are internally disabled until both signals get low again. This is due to the interlocking logic of the device (see also Figure 5).

4.3 Gate driver

2ED020I12-F features two hard-switching gate drivers with n-channel output stages capable to source 1 A and to sink 2 A peak current. Both drivers are equipped with active-low-clamping capability. Furthermore, they feature a large ground bounce ruggedness in order to compensate ground bounces caused by a turn-off of the driven IGBT.

4.4 General purpose operational amplifier

This general purpose operational amplifier can be applied for current measurement of the driven low-side IGBT. It is dedicated for fast operation with a gain of at least 10. The OP is equipped with a -0.1 V to 2 V input stage and a rail-to-rail output stage which is capable to drive ±5 mA and is dedicated to drive an A/D converter.

4.5 General purpose comparator

The general purpose comparator can be applied for over-current detection of the low side IGBT. A dedicated offset as well as a pull-up and pull-down resistor has been introduced to its inputs for security reasons.

4.6 CLT

In order to enable signal transmission across the isolation barrier between low-side and high-side driver, a coreless transformer is employed. Signals, that are to be transmitted, are specially encoded by the transmitter and correspondingly restored by the receiver. In this way EMI due to variations of GNDH (dV_{GNDH}/dt) or the magnetic flux ($d\Phi/dt$) can be suppressed. To compensate the additional propagation delay of transmitter, coreless transformer and receiver, a dedicated propagation delay is introduced into the low-side driver.

5 Electrical parameters

5.1 Absolute maximum ratings

Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND. The pins GND and GNDL have to be connected externally through the shortest possible way.

Parameter	Symbol	Limit values		Unit	Remark
		min.	max.		
High side ground	V_{GNDH}	-1200	1200	V	
High side supply voltage	V_{VSH}	-0.3	20	V	[1]
High side gate driver output	V_{OutH}	-0.3	V_{VSH} + 0.3	V	[1]
Low side ground	V_{GNDL}	-0.3	5.3	V	
Low side supply voltage	V_{VSL}	-0.3	20	V	[2]
Low side gate driver output	V_{OutL}	-0.3	V_{VSL} + 0.3	V	[3]
Logic input voltages (InH, InL, /SD)	V_{In}	-0.3	5.3	V	
OP input voltages (OP-, OP+)	V_{OP}	-0.3	5.3	V	[4]
OP output voltage	V_{OPO}	-0.3	5.3	V	
CP input voltages (CP-, CP+)	V_{CP}	-0.3	5.3	V	[4]
CP output voltage	$V_{/CPO}$	-0.3	5.3	V	
CP output max. sink current	$I_{/CPO}$	—	5	mA	
High side ground, voltage transient	dV_{GNDH}/dt	-50	50	V/ns	
Package power dissipation @T_A=25°C	P_D	—	2	W	[5]
Thermal resistance (both chips active), junction to ambient	R_{THJA}	—	60	K/W	[6]
Thermal resistance (high side chip), junction to ambient	$R_{THJA(HS)}$	—	110	K/W	[6]
Thermal resistance (low side chip), junction to ambient	$R_{THJA(LS)}$	—	110	K/W	[6]
Junction temperature	T_J	—	150	°C	
Storage temperature	T_S	-55	150	°C	

[1] with reference to high side GNDH
[2] with reference to both GND and GNDL
[3] with reference to low side ground GNDL
[4] please note the different specifications for the operating range
[5] considering R_{THJA} = 60 K/W, e.g. both chips active
[6] device soldered to reference PCB without cooling area

5.2 Operating range

Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND.

Parameter	Symbol	Limit values		Unit	Remark
		min.	max.		
High side ground	V_{GNDH}	-1200	1200	V	
High side supply voltage	V_{VSH}	13	18	V	1)
Low side supply voltage	V_{VSL}	13	18	V	2)
Logic input voltages (InH, InL, /SD)	V_{In}	0	5	V	
OP input voltages (OP-, OP+)	V_{OP}	-0.1	2	V	
CP input voltages (CP-, CP+)	V_{CP}	-0.1	2	V	
Ambient temperature	T_A	-40	105	°C	

1) with reference to high side ground GNDH
2) with reference to both GND and GNDL

5.3 Electrical characteristics

The electrical characteristics involve the spread of values for the supply voltages, load and junction temperature given below. Typical values represent the median values, which are related to production processes. Unless otherwise noted all voltages are given with respect to ground (GND).
VSL = 15 V, VSH = 15 V[1], C_L = 1 nF, T_A = 25°C. Positive currents are assumed to be flowing into pins.

5.3.1 Voltage Supply

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
High side leakage current	I_{GNDH}	—	—	1	µA	V_{GNDH} = 1.2 kV V_{GNDL} = 0 V
High side quiescent supply current	I_{VSH}	—	1.7	—	mA	V_{VSH} = 15 V[1]
		—	—	500	µA	V_{VSH} = 10 V[1]
High side under-voltage lockout, upper threshold	V_{VSH}[1]	tbd	12	tbd	V	
High side under-voltage lockout hysteresis	ΔV_{VSH}	tbd	1	tbd	V	
Low side quiescent supply current	I_{VSL}	—	2.4	—	mA	V_{VSL} = 15 V
		—	—	500	µA	V_{VSL} = 10 V
Low side under-voltage lockout, upper threshold	V_{VSL}	tbd	12	tbd	V	
Low side under-voltage lockout hysteresis	ΔV_{VSL}	tbd	1	tbd	V	

1) with reference to high side ground GNDH

5.3.2 Logic inputs

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
Logic “1” input voltages (InH, InL, /SD)	V_{In}	2	—	—	V	
Logic “0” input voltages (InH, InL, /SD)	V_{In}	—	—	0.8	V	
Logic input voltages hystersis (InH, InL, /SD)	ΔV_{In}	—	0.6	—	V	
Logic “1” input current (InH, InL)	I_{In}	—	40	tbd	µA	V_{In} = 5 V
Logic “0” input current (InH, InL)	I_{In}	—	0	—	µA	V_{In} = 0 V
Logic “1” input current (/SD)	I_{In}	—	0	—	µA	V_{In} = 5 V
Logic “0” input current (/SD)	I_{In}	tbd	-40	—	µA	V_{In} = 0 V

5.3.3 Gate drivers

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
High side high level output voltage	$V_{VSH} – V_{OutH}$	—	1.4	tbd	V	I_{OutH} = -1 mA V_{InH} = 5 V
High side low level output voltage	V_{OutH} [1)]	—	—	0.1	V	I_{OutH} = 1 mA V_{InH} = 0 V
Low side high level output voltage	$V_{VSL} – V_{OutL}$	—	1.4	tbd	V	I_{OutH} = -1 mA V_{InH} = 0 V
Low side low level output voltage	V_{OutL}	—	—	0.1	V	I_{OutH} = 1 mA V_{InH} = 0 V
Output high peak current (OutL, OutH)	I_{Out}	—	—	-1	A	V_{In} = 5 V V_{Out} = 0 V
Output low peak current (OutL, OutH)	I_{Out}	2	—	—	A	V_{In} = 0 V V_{Out} = 15 V
High side active low clamping	V_{OutH} [1)]	—	—	3	V	V_{InH} = 0V VSH open I_{OutH} = 200 mA
Low side active low clamping	V_{OutL}	—	—	3	V	V_{InL} = 0V VSL open I_{OutL} = 200 mA

[1)] with reference to high side ground GNDH

5.3.4 Dynamic characteristics

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
Turn-on propagation delay	t_{on}	—	50	tbd	ns	ref. to Figure 6
Turn-off propagation delay	t_{off}	—	50	tbd	ns	ref. to Figure 6
Shutdown propagation delay	$t_{/SD}$	—	50	tbd	ns	ref. to Figure 7
Turn-on rise time	t_r	—	40	tbd	ns	ref. to Figure 6
Turn-off rise time	t_f	—	40	tbd	ns	ref. to Figure 6
Delay mismatch (high and low side turn-on/off)	Δt	-10	0	10	ns	ref. to Figure 8

5.3.5 General purpose operational amplifier

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
OP input offset voltage	ΔV_{In}	-15	0	15	mV	
OP input offset voltage drift	V_{Drift}	tbd	tbd	tbd	µV/K	
OP input high currents (OP-, OP+)	I_{In}	—	0	5	µA	V_{In} = 2 V
OP input high currents (OP-, OP+)	I_{In}	-5	0	—	µA	V_{In} = 0 V
OP high output voltage	V_{OPO}	4.9	—	—	V	V_{OP-} = 0 V V_{OP+} = 2 V
OP low output voltage	V_{OPO}	—	—	0.1	V	V_{OP-} = 2 V V_{OP+} = 0 V
OP output source current	I_{OPO}	—	—	-5	mA	V_{OP+} = 2 V V_{OP-} = 0 V V_{OPO} = 0V
OP output sink current	I_{OPO}	5	—	—	mA	V_{OP+} = 0 V V_{OP-} = 2 V V_{OPO} = 5V
OP open loop gain	A_{OL}	—	120	—	dB	
OP gain-bandwidth product	A x BW	—	60	—	MHz	[1]
OP phase margin	Φ	—	70	—	°	[1], [2]

[1] design value
[2] the minimum gain A ≥ 10 is recommended

5.3.6 General purpose comparator

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
CP input offset voltage	ΔV_{In}	—	-30	—	mV	$V_{CP+} = V_{CP-}$
CP input high current	I_{CP-}	—	20	—	µA	V_{CP-} = 5 V
CP input low current	I_{CP+}	—	-20	—	µA	V_{CP+} = 0 V
CP low output voltage	$V_{/CPO}$	—	—	0.2	V	V_{CP+} = 2 V $I_{/CPO}$ = 1 mA
CP output leakage current	$I_{/CPO}$	—	—	5	µA	V_{CP+} = 0 V V_{CP-} = 2 V $V_{/CPO}$ = 5 V
CP switch-on delay	t_d	—	100	—	ns	$R_{/CPO}$ = 4.7 kΩ V_{res} = 5 V $V_{/CPO}$ = 0.8 V
CP switch-off delay	t_d	—	300	—	ns	$R_{/CPO}$ = 4.7 kΩ V_{res} = 5 V $V_{/CPO}$ = 2 V

6 Diagrams

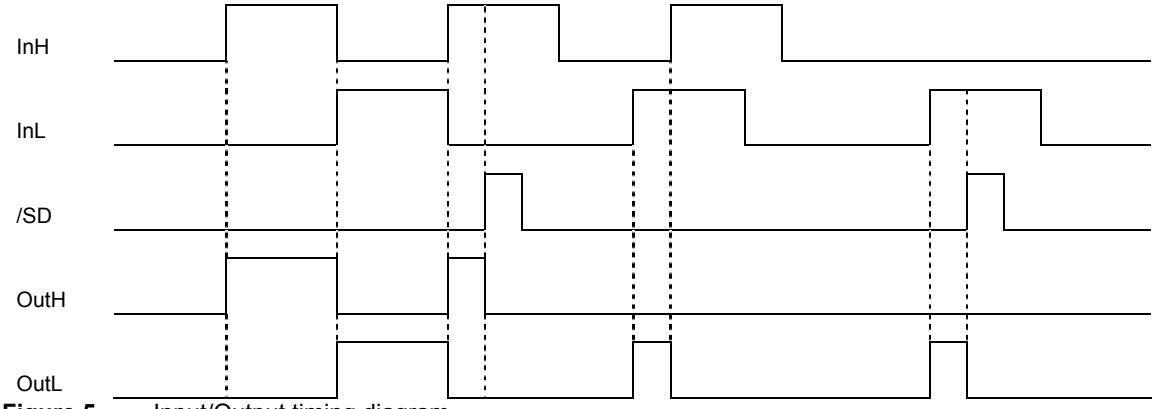


Figure 5 Input/Output timing diagram

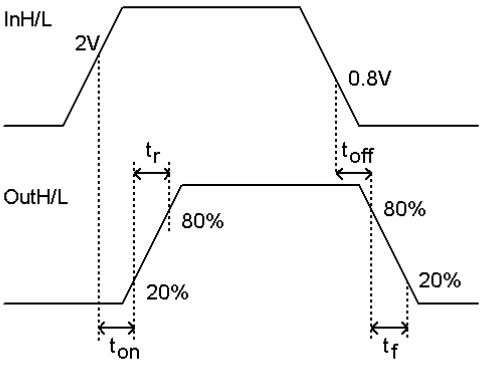


Figure 6 Switching time waveform definition

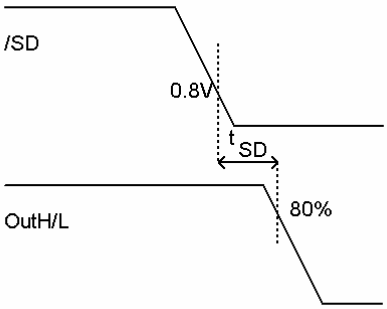


Figure 7 Shutdown waveform definition

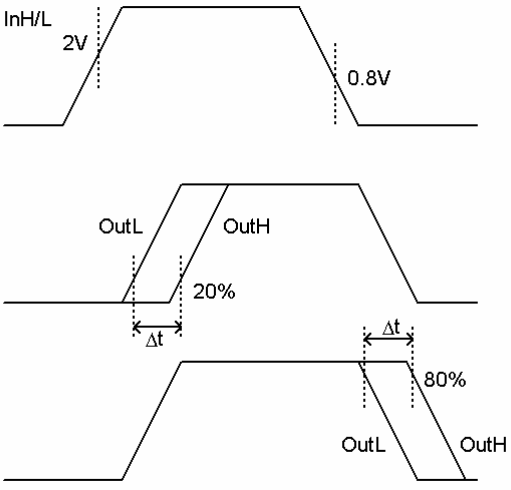


Figure 8 Delay matching waveform definitions

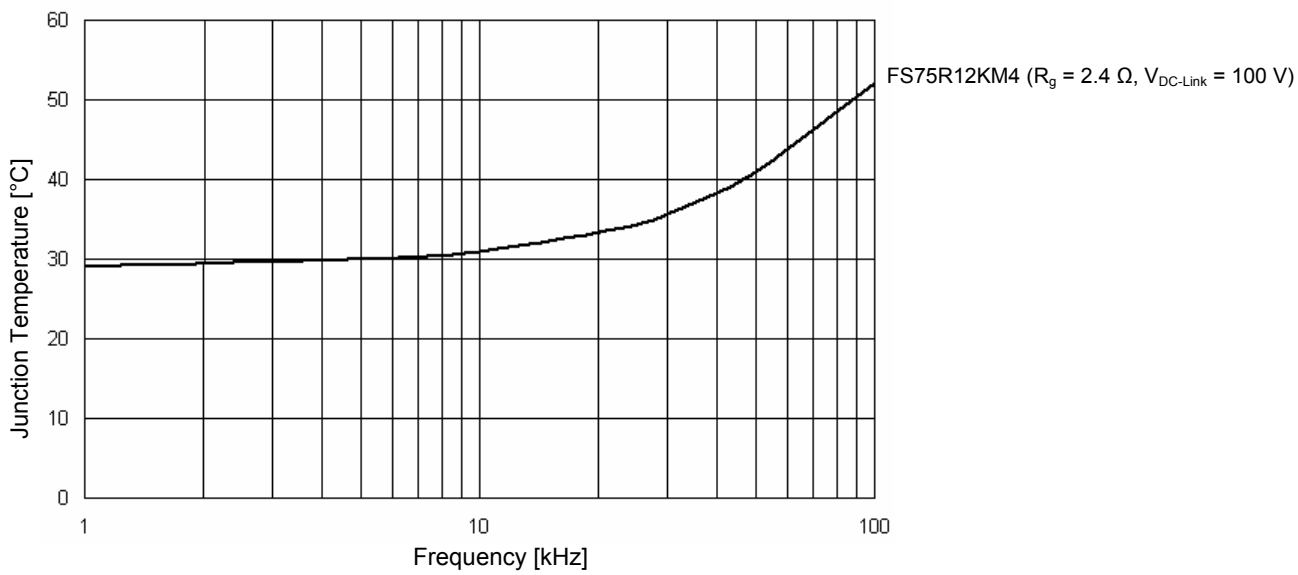


Figure 9 Junction Temperature vs. Frequency (V_{VSH} = V_{VSL} = 15 V, T_A = 25°C)

7 Application Notes

7.1 Power Supply

The floating high side driver may be supplied directly or by means of a bootstrap diode and capacitor. Either way, for a correct power-up it is recommended to put at the pins VSH and VSL an electrolytic or tantalum capacitor and additionally a ceramic capacitor of approximately 100 nF. The size of the electrolytic or tantalum capacitor depends on the gate capacitances of the driven IGBT or MOSFET, the switching frequency and additional gate resistors and/or capacitors.

For a safe start-up with a bootstrap diode and capacitor it is recommended first to switch on the low-side IGBT. Thus, the capacitor can be charged through the diode and provides sufficient gate voltage.

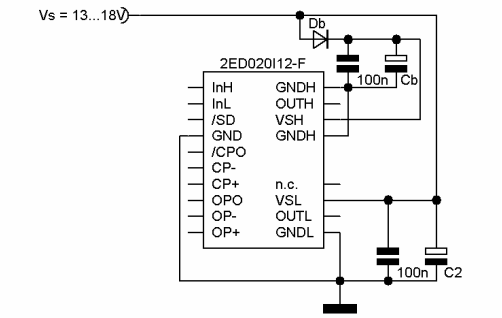


Figure 10 Bootstrap circuit

7.2 Ground reference

The pins GND and GNDL have to be connected externally through the shortest possible way. Thus, different ground references result for different applications as shown for instance in Figure 11.

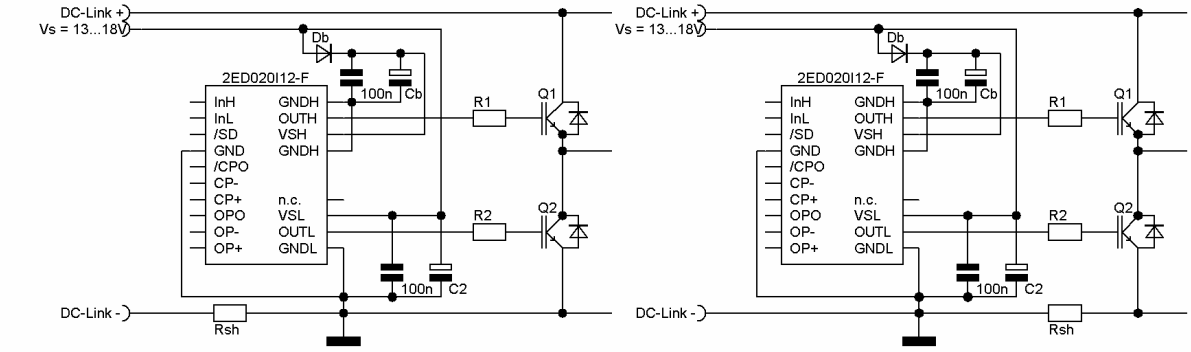


Figure 11 Ground reference

7.3 Operational Amplifier

To minimize the current consumption when the operational amplifier is not used, it is necessary to connect both inputs properly. For instance connect pin OP+ to 5 V and pin OP- to 0 V or vice versa.

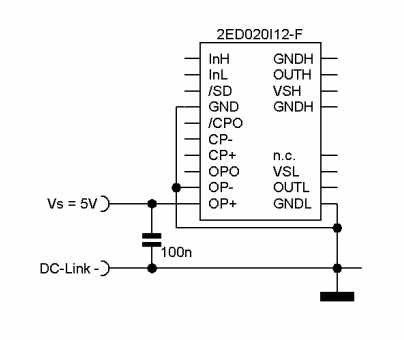


Figure 12 OPA not used

The operational amplifier is designed to operate with a minimum gain of 10, so that its output OPO has a stable behavior.

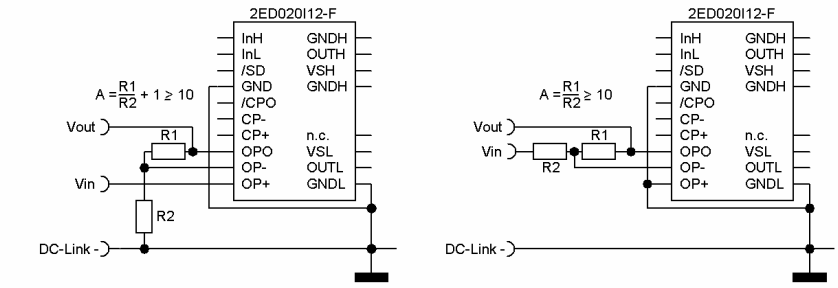


Figure 13 Minimum OPA gain

7.4 Comparator

The comparator has a designed input offset voltage of typical -30 mV to prioritize the CP+ input against the CP- input. If both input signals have the same potential, the output /CPO goes to low impedance.

In the following some example circuits using the general purpose comparator:

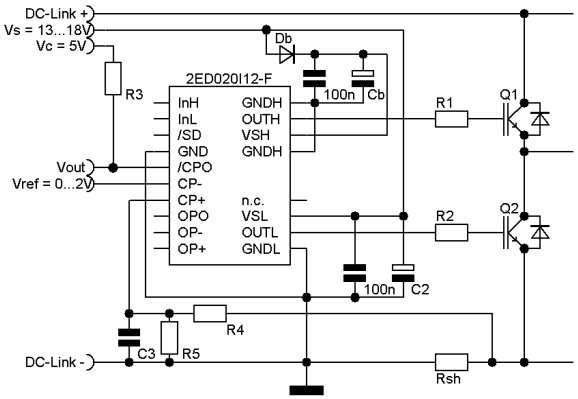


Figure 14 Over-current detection

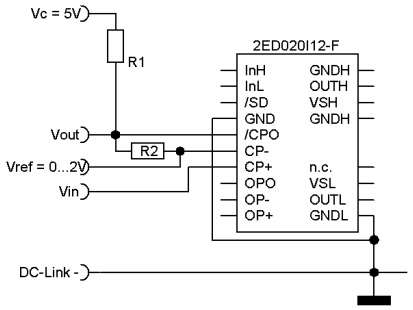


Figure 15 Comparator with hysteresis

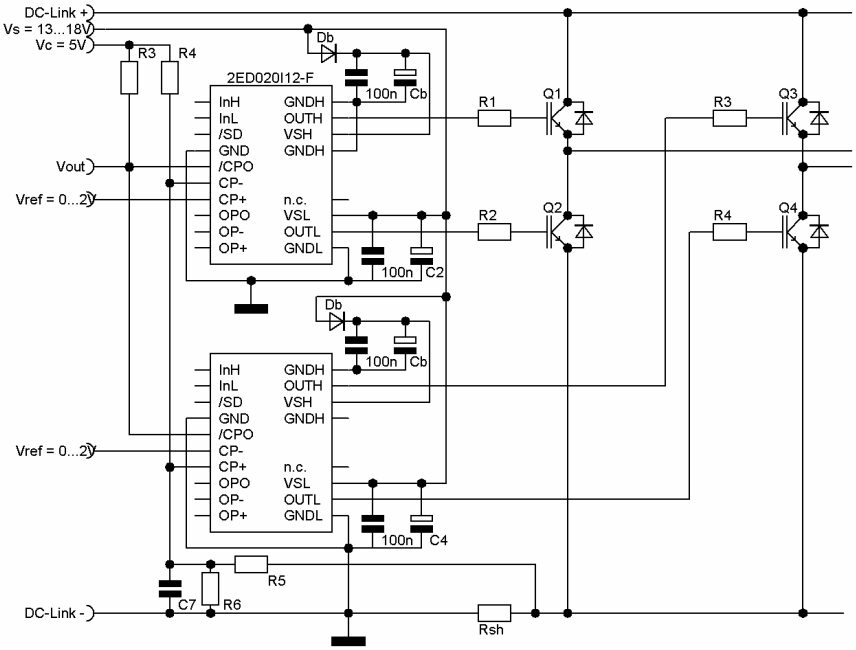


Figure 16 Over-current detection with Window Comparator

7.5 Logic inputs

The input pins InH, InL and /SD should be protected against EMI by ceramic capacitors according to Figure 17.

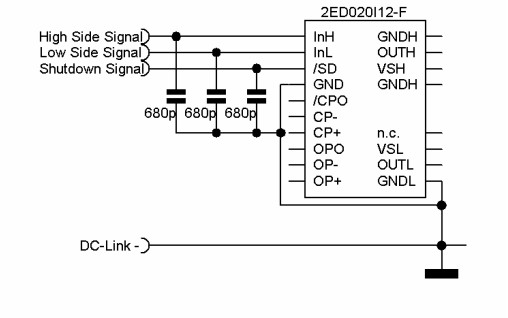


Figure 17 Logic inputs

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