AMI Semiconductor, Inc.
ULP Memory Solutions
670 North McCarthy Blvd. Suite 220
Milpitas, CA 95035
PH: 408-935-7777, FAX: 408-935-7770

N04L1630C2B

Advance Information

4Mb Ultra-Low Power Asynchronous CMOS SRAMs

256K × 16 bit POWER SAVER TECHNOLOGY ™

Overview

The N04L1630C2B is an integrated memory device containing a 4 Mbit Static Random Access Memory organized as 262,144 words by 16 bits. The device is designed and fabricated using AMI Semiconductor's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with two chip enable ($\overline{CE1}$ and CE2) controls and output enable ($\overline{OE}$) to allow for easy memory expansion. Byte controls ($\overline{UB}$ and $\overline{LB}$) allow the upper and lower bytes to be accessed independently and can also be used to deselect the device. The N04L1630C2B is optimized for the ultimate in low power and is suited for various applications where ultra-low-power is critical such as medical applications, battery backup and power sensitive hand-held devices. The unique page mode operation saves operating power while improving the performance over standard SRAMs. The device can operate over a very wide temperature range of -40^{o}C to +85^{o}C and is available in JEDEC standard packages compatible with other standard 256Kb x 16 SRAMs.

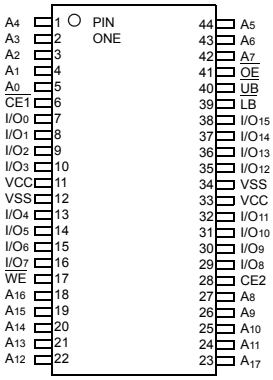
Features

- **Wide Power Supply Range**
  2.7 to 3.6 Volts
- **Very low standby current**
  1uA (Typical)
- **Very low operating current**
  2.0mA at 1µs (Typical)
- **Very low Page Mode operating current**
  0.8mA at 1µs (Typical)
- **Simple memory control**
  Dual Chip Enables ($\overline{CE1}$ and CE2)
  Byte control for independent byte operation
  Output Enable ($\overline{OE}$) for memory expansion
- **Very fast output enable access time**
  30ns $\overline{OE}$ Access Time
  55ns Random Access Time
  30ns Page Mode Access Time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**
- **RoHS Compliant TSOP and BGA packages**

Product Family

Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed Options	Standby Current (I_{SB}), Typical	Operating Current (Icc), Typical
N04L1630C2BB2	48-BGA Green	-40^{o}C to +85^{o}C	2.7V - 3.6V	55ns 70ns	1µA	2 mA @ 1MHz
N04L1630C2BT2	44-TSOP II Green					

Pin Configurations (4Mb)



TSOP II

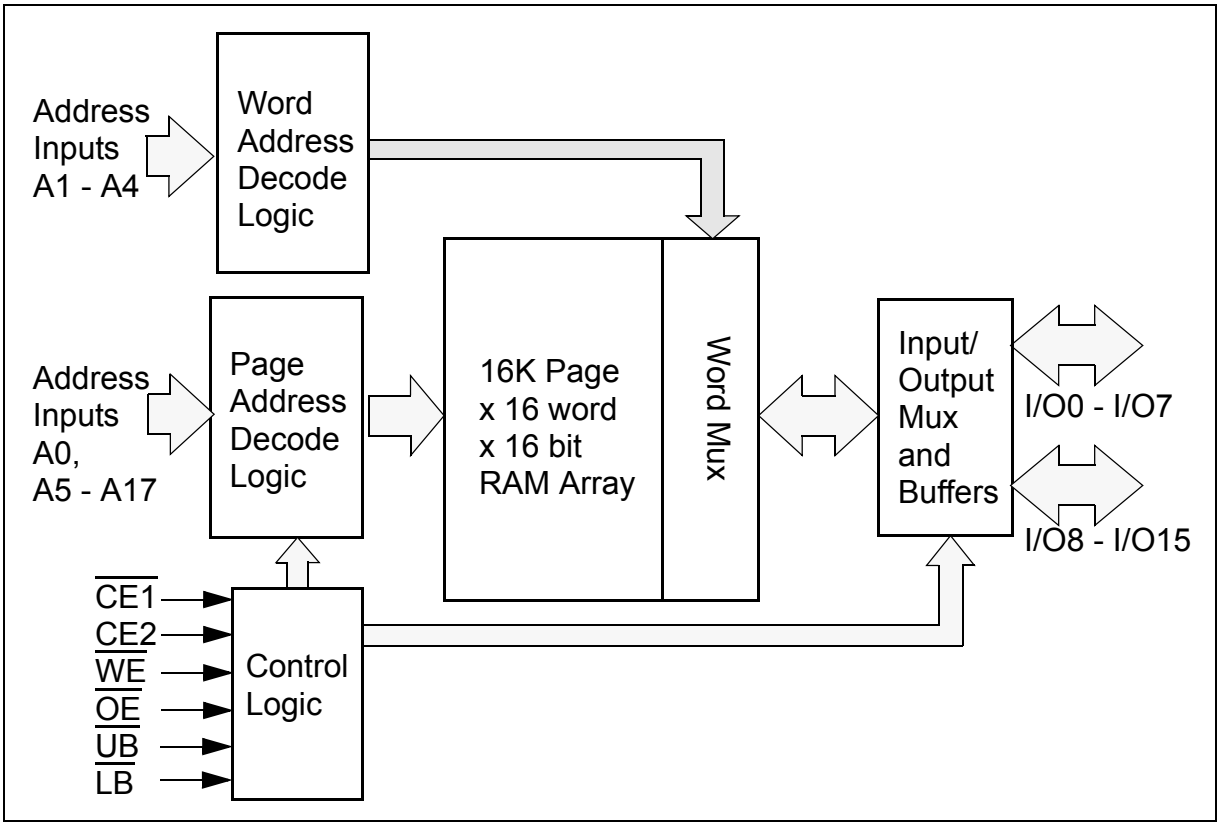
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	CE2
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE1}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	NC	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	NC	A_8	A_9	A_{10}	A_{11}	NC

48 Pin BGA (top)

Pin Descriptions

Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Enable Input
$\overline{UB}$	Upper Byte Enable Input
I/O_0-I/O_7	Lower Byte Data Input/Output
I/O_8-I/O_{15}	Upper Byte Data Input/Output
V_{CC}	Power
V_{SS}	Ground
NC	Not Connected

Functional Block Diagram



Functional Description

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O_0 - I/O_{15}[1]	MODE	POWER
H	X	X	X	X	X	High Z	Standby[2]	Standby
X	L	X	X	X	X	High Z	Standby[2]	Standby
L	H	X	X	H	H	High Z	Standby	Standby
L	H	L	X[3]	L[1]	L[1]	Data In	Write[3]	Active
L	H	H	L	L[1]	L[1]	Data Out	Read	Active
L	H	H	H	L[1]	L[1]	High Z	Active	Active

1. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - I/O_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown.

2. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.

3. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec	°C

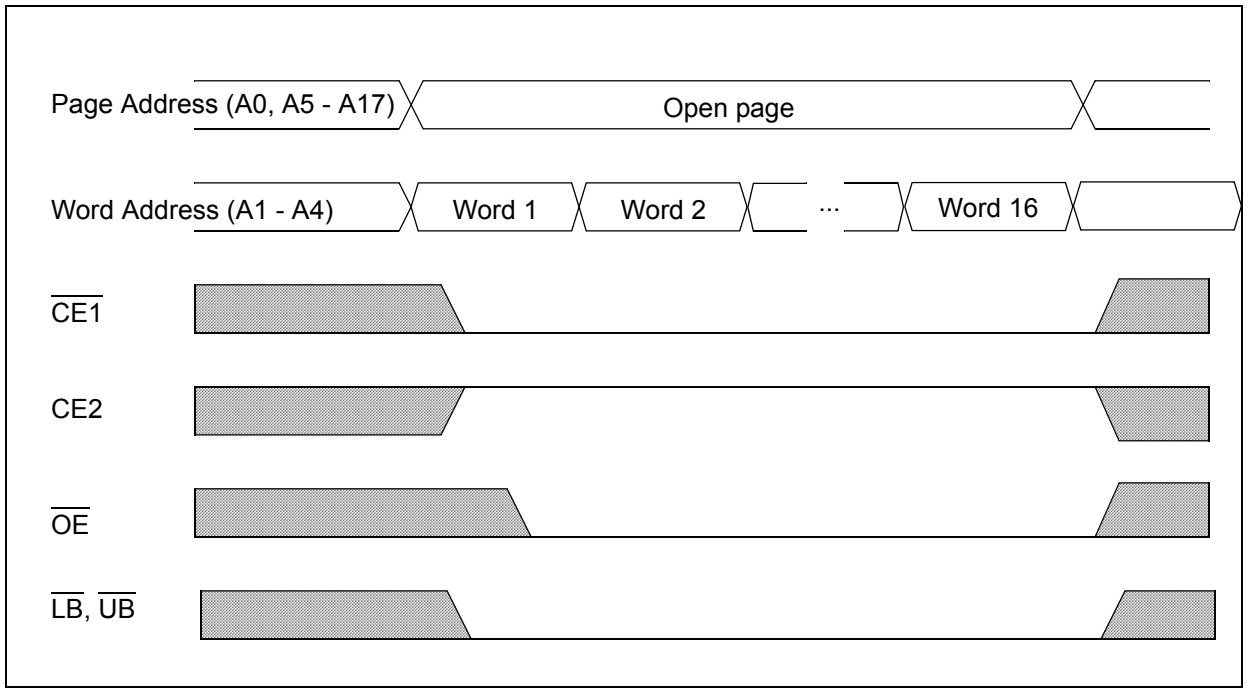
1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Test Conditions	Min.	Typ[1]	Max	Unit
Supply Voltage	V_{CC}		2.7	3.0	3.6	V
Data Retention Voltage	V_{DR}	Chip Disabled[3]	1.8			V
Input High Voltage	V_{IH}		0.7Vcc		V_{CC}+0.3	V
Input Low Voltage	V_{IL}		–0.3		0.6	V
Output High Voltage	V_{OH}	I_{OH} = -100uA	V_{CC}–0.2			V
		I_{OH} = -1mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 100uA			0.2	V
		I_{OL} = 2.1mA			0.4	
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}			0.5	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled			0.5	µA
Read/Write Operating Supply Current @ 1 µs Cycle Time[2]	I_{CC1}	V_{CC}=V_{CC}Max, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		2.5	3.0	mA
Read/Write Operating Supply Current @ 70 ns Cycle Time[2]	I_{CC2}	V_{CC}=V_{CC}Max, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		10	15.0	mA
Page Mode Operating Supply Current @ 70ns Cycle Time[2] (Refer to Power Savings with Page Mode Operation)	I_{CC3}	V_{CC}=V_{CC}Max, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		4	8	mA
Maximum Standby Current[3]	I_{SB1}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 85°C, V_{CC} = 3.6 V		1	10.0	µA
Maximum Data Retention Current[3]	I_{DR}	Vcc = 1.8V, V_{IN} = V_{CC} or 0 Chip Disabled, t_A= 85°C			5	µA

1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and not 100% tested.
2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
3. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS.

Power Savings with Page Mode Operation ($\overline{WE}$ = V_{IH})



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 16-bit words of data are read from the open page. By treating addresses A1-A4 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

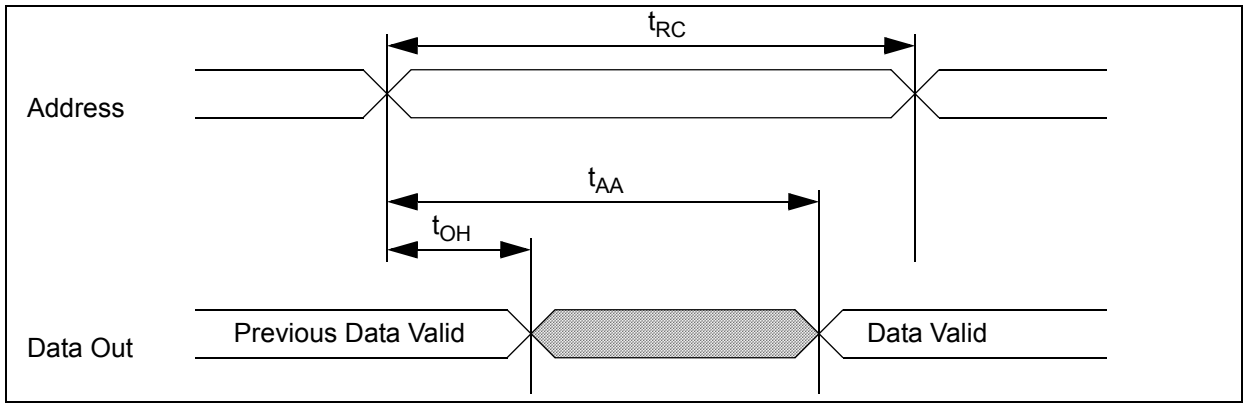
Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Output Load	CL = 30pF
Operating Temperature	-40 to +85 ^{o}C

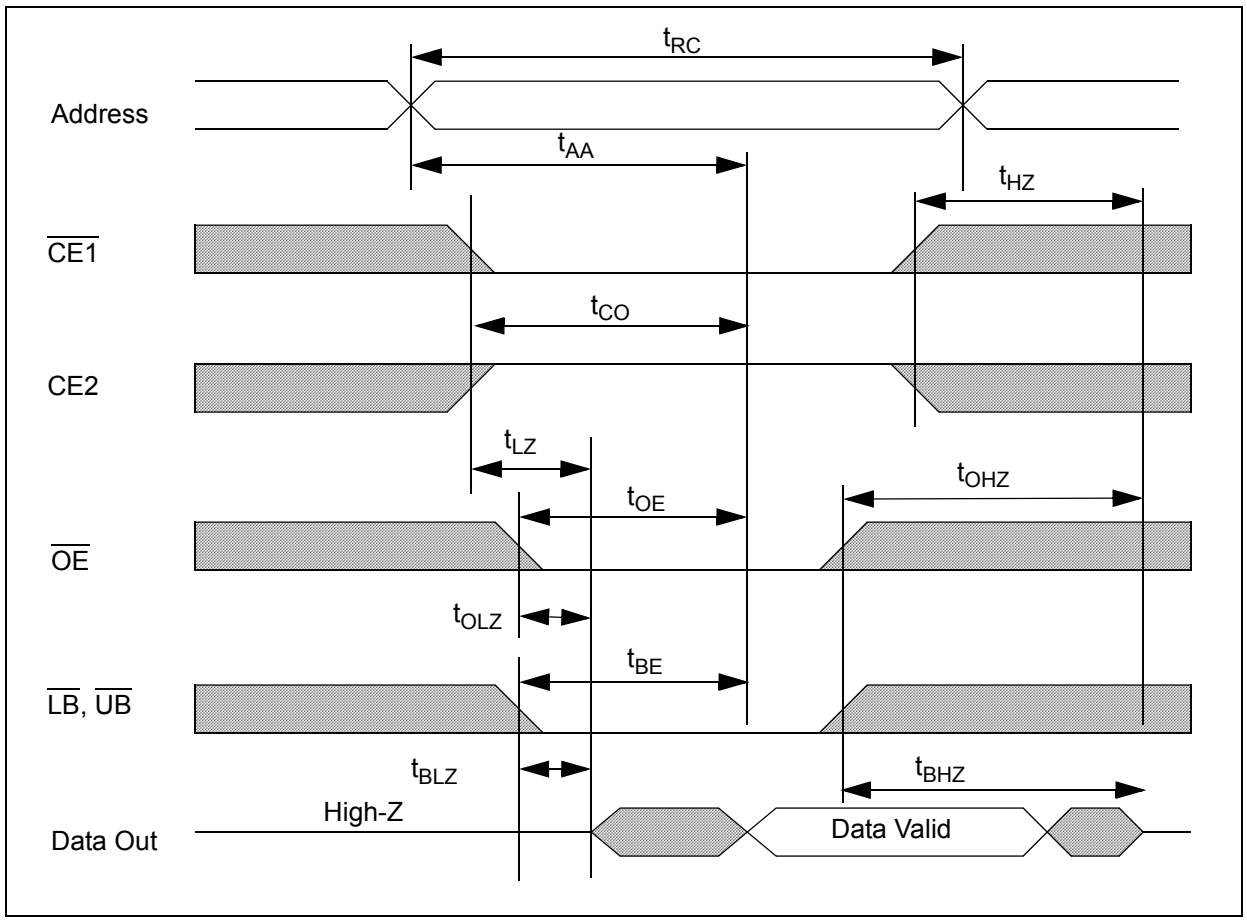
Timing

Item	Symbol	-55		-70		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	55		70		ns
Address Access Time	t_{AA}		55		70	ns
Page Mode Address Access Time	t_{AAP}		30		35	ns
Chip Enable to Valid Output	t_{CO}		55		70	ns
Output Enable to Valid Output	t_{OE}		30		35	ns
Byte Select to Valid Output	t_{BE}		55		70	ns
Chip Enable to Low-Z output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Byte Select to Low-Z Output	t_{BZ}	10		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	20	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	20	ns
Byte Select Disable to High-Z Output	t_{BHZ}	0	20	0	20	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Write Cycle Time	t_{WC}	55		70		ns
Chip Enable to End of Write	t_{CW}	45		50		ns
Address Valid to End of Write	t_{AW}	45		50		ns
Byte Select to End of Write	t_{BW}	45		50		ns
Write Pulse Width	t_{WP}	40		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		20		20	ns
Data to Write Time Overlap	t_{DW}	40		40		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	5		5		ns

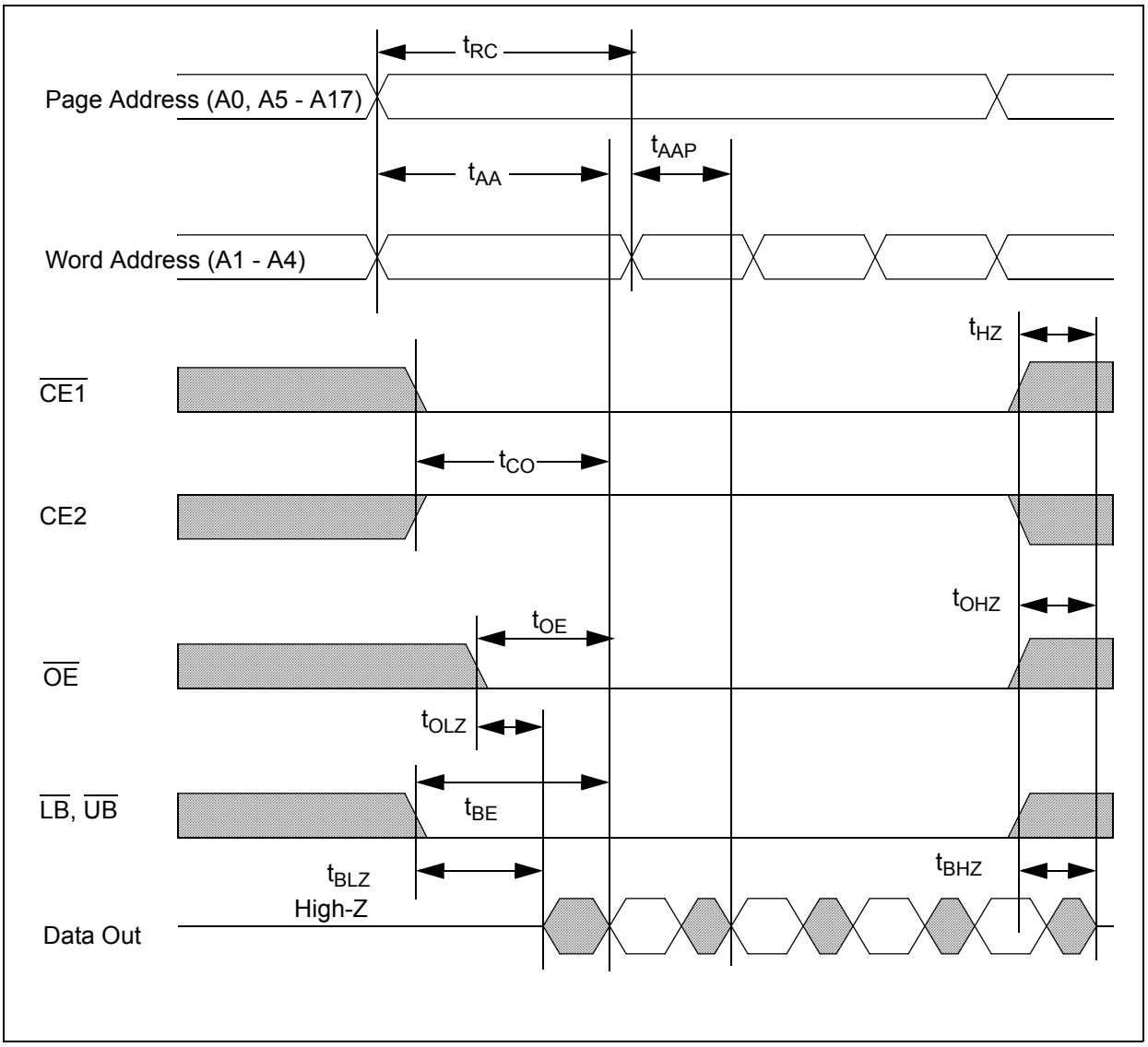
Timing of Read Cycle ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = CE2 = V_{IH})



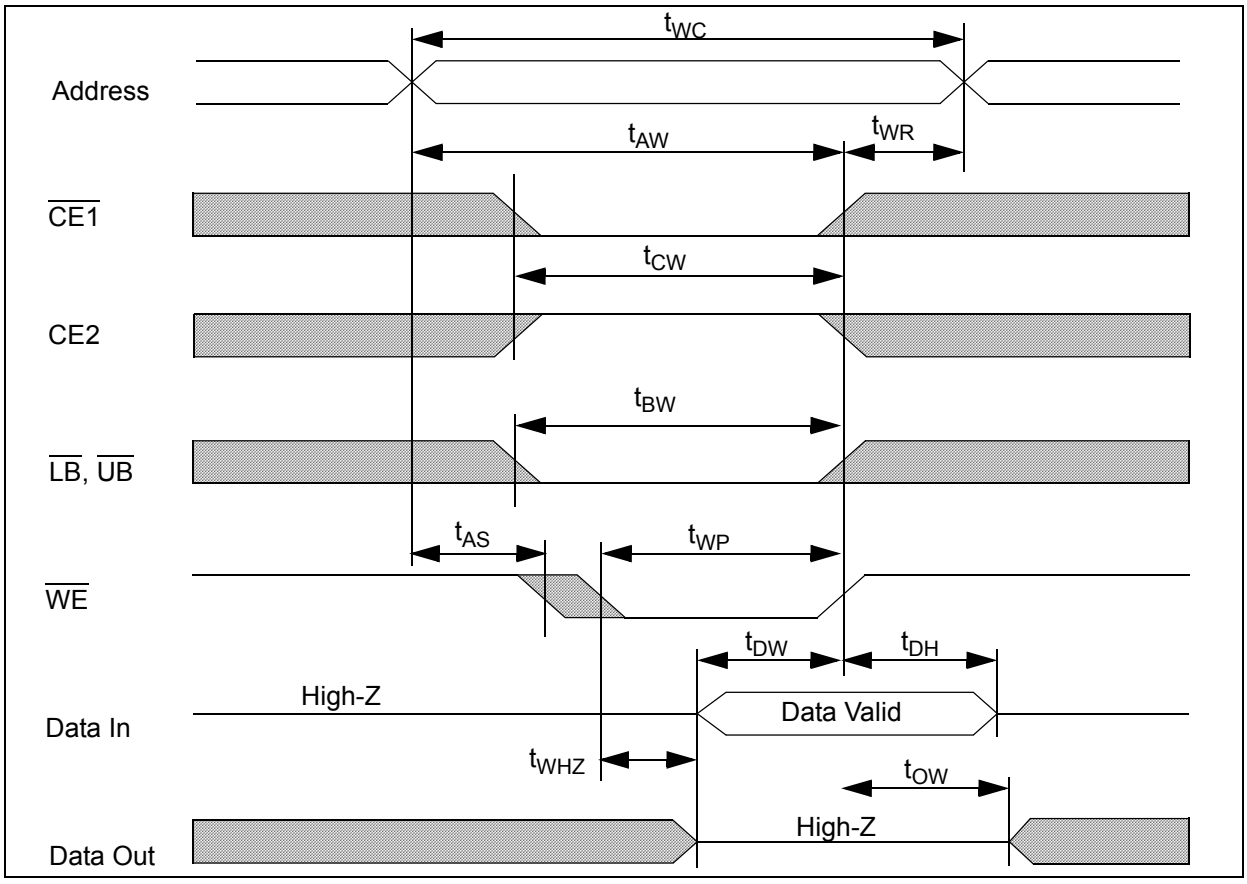
Timing Waveform of Read Cycle ($\overline{WE}$=V_{IH})



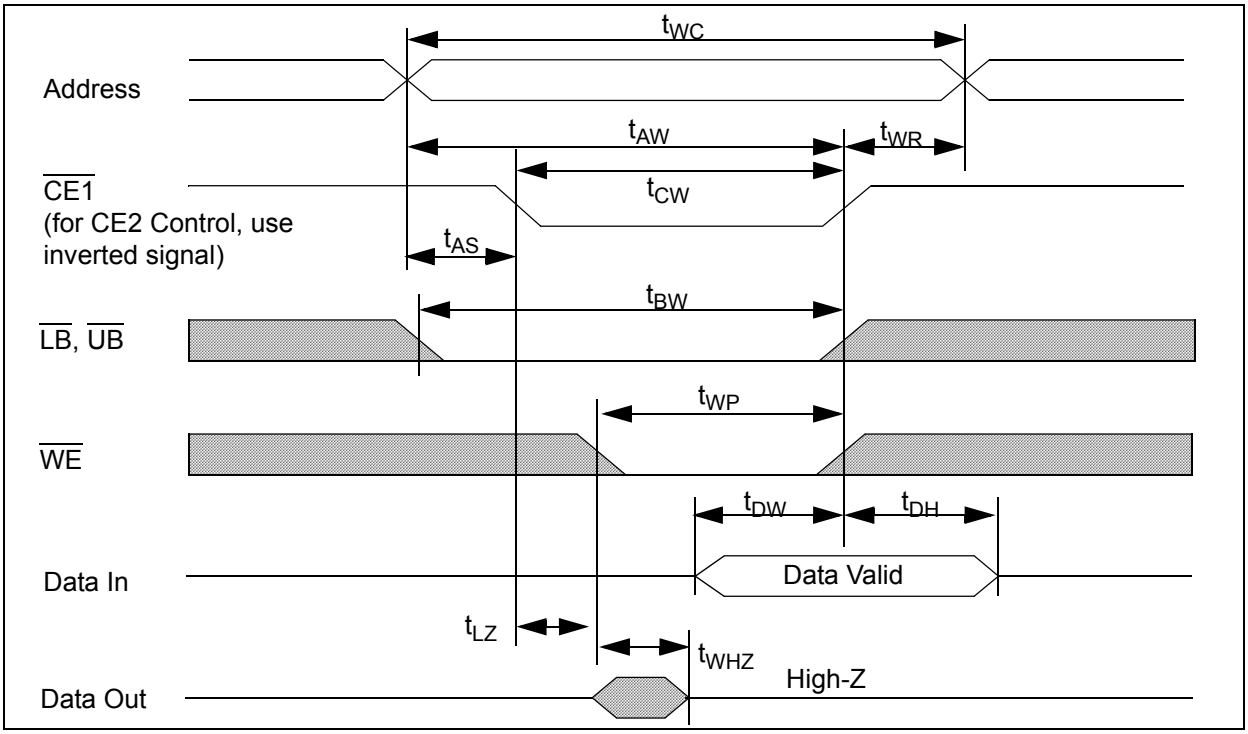
Timing Waveform of Page Mode Read Cycle ($\overline{WE}$ = V_{IH})



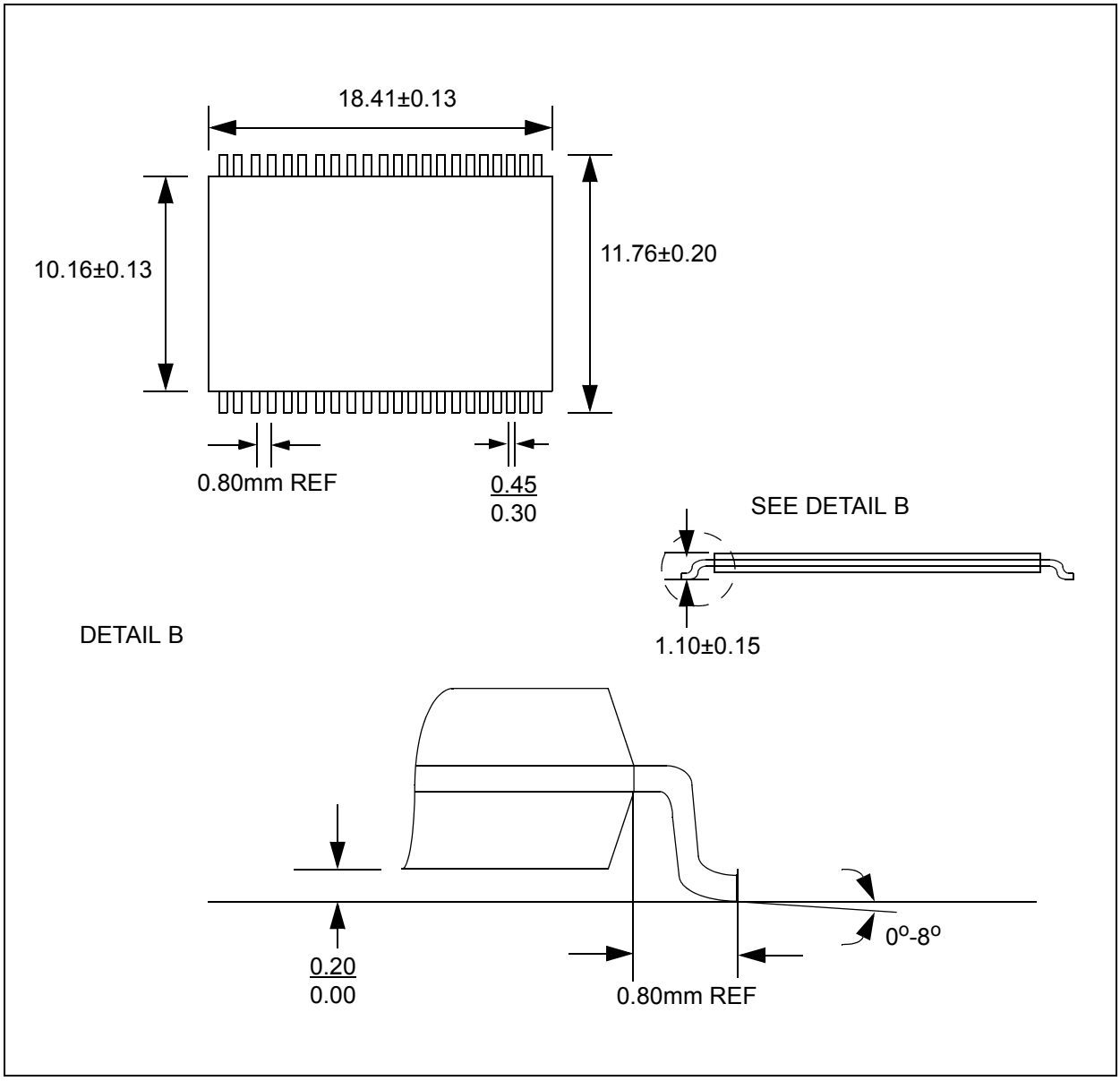
Timing Waveform of Write Cycle ($\overline{WE}$ control)



Timing Waveform of Write Cycle ($\overline{CE1}$ Control)

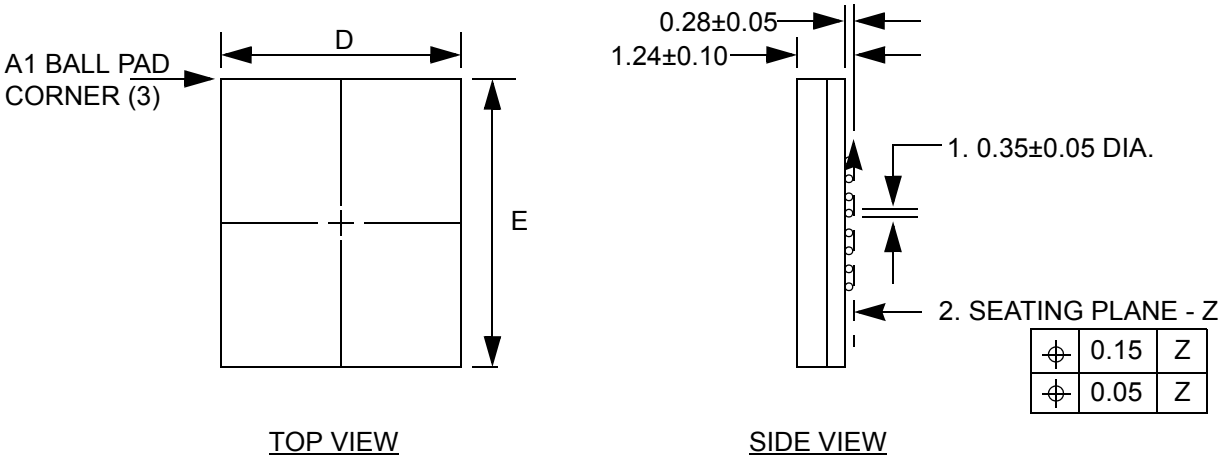


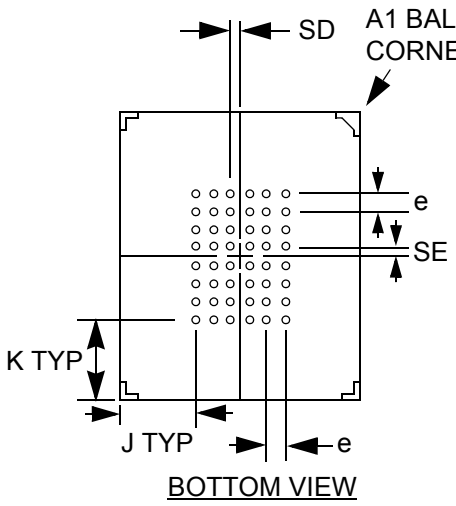
44-Lead TSOP II Package (T44)



Note:
1. All dimensions in inches (Millimeters)

Ball Grid Array Package



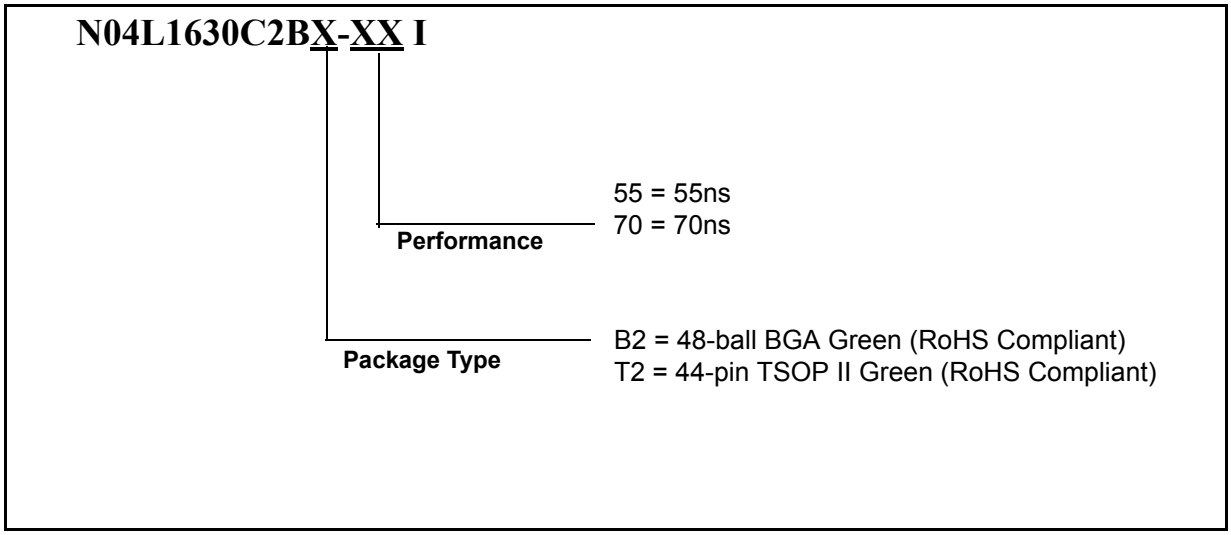


1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Ordering Information



Revision History

Revision	Date	Change Description
A	April 2003	Initial Advanced Release
B	August 2004	Changed part number to -30 from -3W and Vcc range to 2.7 V - 3.6V
C	January 2005	Change I_{DR} = 5 µA, I_{CC}(typ) = 2.5mA. Modified page mode address A1-A4 configuration.
D	January 2005	General Update
E	March 22, 2005	Changed tWP and tDW to 40ns for -55 and -70, to 45ns for -85
F	June 9, 2005	Added TSOP II Green Package Ordering Option
G	Dec. 2005	Added RoHS Compliant
H	July 2006	Added BGA package
I	September 2006	Converted to AMI Semiconductor