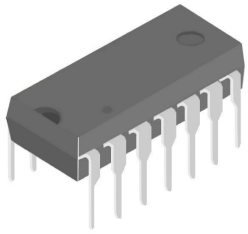
Oriental Excellence

SM339

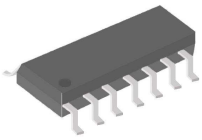
Quadruple Differential Comparator

FEATURES

- **Single or dual supplies**
- **Low Input Bias Current : 25nA**
- **Output Compatible with TTL, MOS, and CMOS**
- **Input Common–Mode Voltage Range to Ground**
- **Low Input Offset Voltage**
- **Low Input Offset Current**
- **Low Output Saturation Voltage**
- **Wide Supply Voltage Range**



DIP-14



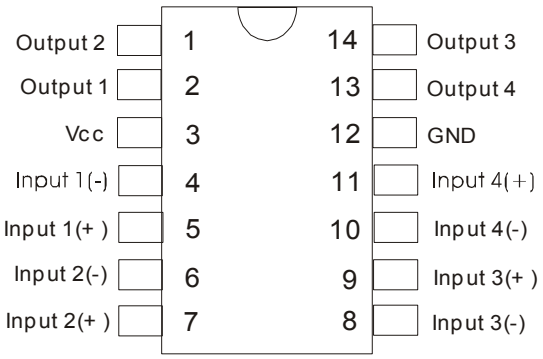
SOP-14

PRODUCT DESCRIPTION

The SM339 are designed for use in level detection, low-level sensing and memory applications in consumer automotive and industrial electronic applications.

The SM339 consists of four independent voltage comparators designed to operate from single power supply over a wide voltage range.

PIN CONFIGURATION



ORDERING INFORMATION

Part Number	Operating Temperature Range	Package Type
SM339N	-25℃~+85℃	DIP-14
SM339S	-25℃~+85℃	SOP-14

Quadruple Differential Comparator

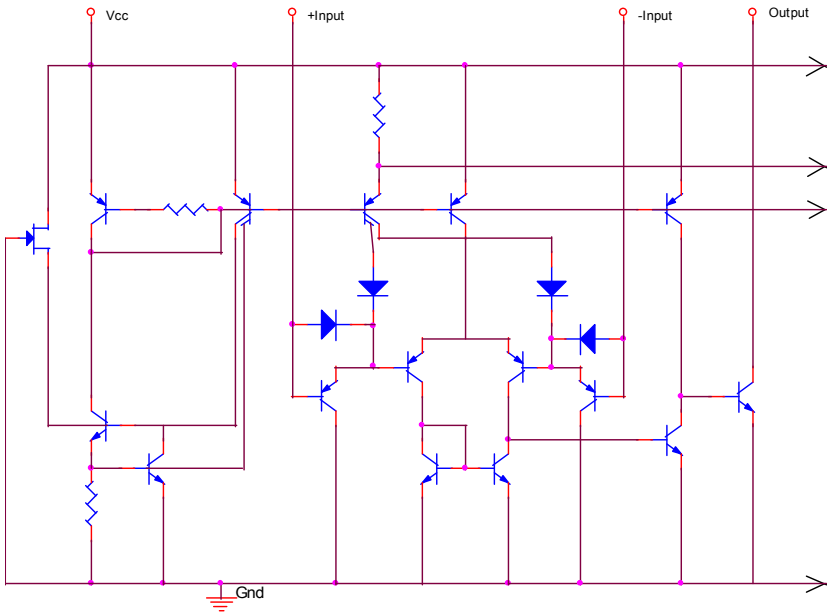
ABSOLUTE MAXIMUM RATING

Characteristics	SYMBOL	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	V
Input Differential Voltage Range	V_{IDR}	36	V
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	V
Output Short Circuit-to-Ground	I_{SC}	Continuous	mA
Power Dissipation t=25℃ Above 25℃	P_D	1.0 8.0	W mW/℃
Operating Ambient Temperature Range	T_A	-25 to 85	℃
Storage Temperature Range	T_S	-65 to 150	℃

Note：

1. The max. output current may be as high as 20mA, independent of the magnitude of Vcc, output short circuits to Vcc can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction becooming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the Vcc voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when inputs become ≥ ground or negative supply.
3. At the output switch point, V_O=1.4Vdc, R_S=100Ω with Vcc from 5.0 Vdc to 30 V, and over the full input common mode range (0V to Vcc= -1.5V).
4. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
5. Response time is specified with a 100mV step and 5.0mV of overdrive. For larger signals, 300ns is typical.
6. Positive excursions of input voltage may exceed the power supply level. As long as one of the inputs remain within the common-mode range, the comparator will provide the proper output state.

CIRCUIT SCHEMATIC



(Diagram shown is for 1 comparator)

Quadruple Differential Comparator

ELECTRICAL CHARACTERISTICS (Vcc=5.0Vdc, 0℃≤ TA ≤ 25℃, unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (3) T_A=25℃ T_A=0℃ to 70℃	V_{IO}	--- ---	±2.0 ---	±5.0 ±9.0	mV
Input Bias Current (3,4) T_A=25℃ T_A=0℃ to 70℃	I_{IB}	--- ---	25 ---	250 400	nA
Input Offset Current (3) T_A=25℃ T_A=0℃ to 70℃	I_{IO}	--- ---	±5.0 ---	±50 ±150	nA
Input Common Mode Voltage Range (6) T_A=25℃ T_A=0℃ to 70℃	V_{ICR}	 0 0	 --- ---	 Vcc –1.5 Vcc –2.0	V
Supply Current R_L=∞, T_A=25℃ R_L=∞, Vcc=30Vdc	I_{CC}	 --- ---	 0.8 1.0	 2.0 2.5	mA
Voltage Gain R_L ≥ 15K, Vcc= 15V	A_{VOL}	---	200	---	V/mV
Large Signal Response Time V1 = TTL Logic Swing. Vref = 1.4Vdc V_{RL}= 5.0 Vdc, R_L= 5.1K	---	---	300	---	ns
Response Time (6) V_{RL}= 5.0 Vdc, R_L= 5.1K	t_{TLH}	---	1.3	---	μs
Output Sink Current V1 (-) ≥ 1.0Vdc, V1(+) =0 Vdc Vo ≤ 1.5 Vdc	I_{Sink}	6.0	16	---	mA
Saturation Voltage V1 (-) ≥ 1.0Vdc, V1(+) =0 Vdc I_{Sink}≤ 4.0 mA, T_A=25℃ 0℃≤T_A≤70℃	V_{SAT}	 --- ---	 130 ---	 400 700	mV
Output Leakage Current V1(-)=0 Vdc, V1(+)≥1.0 Vdc Vo=5.0 Vdc, T_A=25℃ V1(-)=0 Vdc, V1(+)≥1.0 Vdc Vo = 30 Vdc, 0℃≤T_A≤70℃	I_{OL}	 --- ---	 0.1 ---	 --- 1000	nA
Input Differential Voltage (6) All Vin > GND or V – Supply 0℃≤ T_A ≤70℃	V_{ID}	---	---	Vcc	V

ELECTRICAL CHARACTERISTICS CURVES

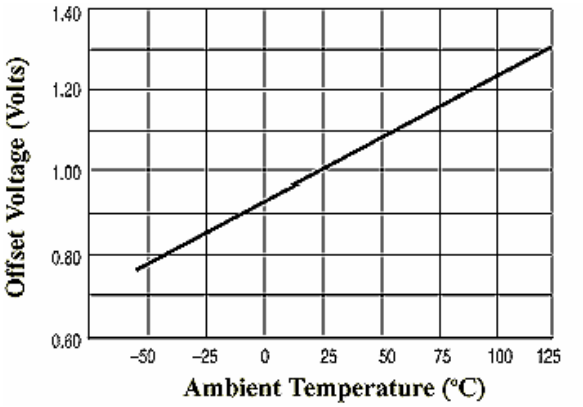


Fig 1.Normalized input offset voltage

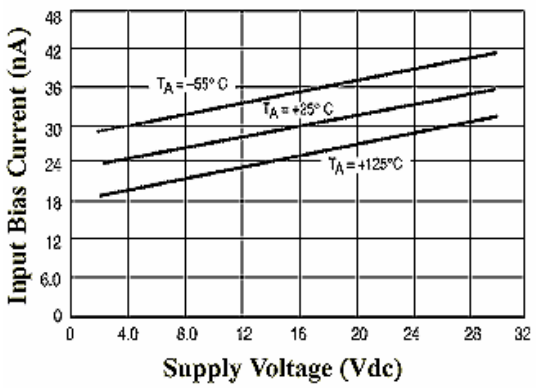


Fig 2.Input bias current

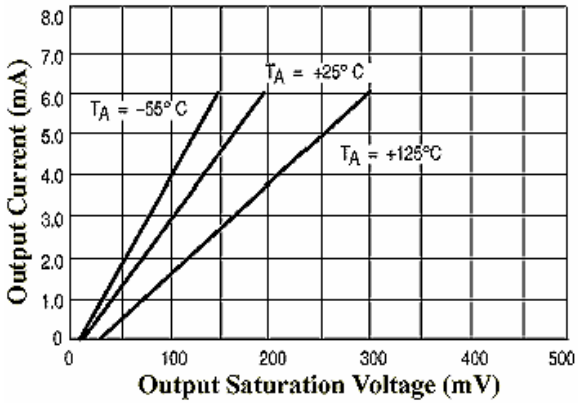


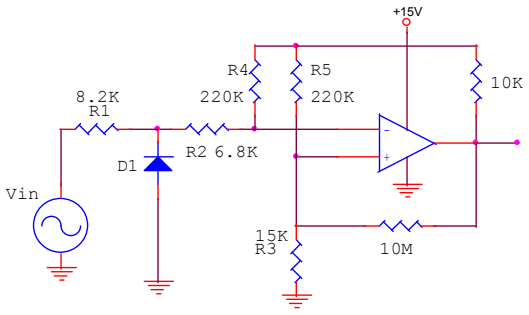
Fig 3.Output sink current versus output saturation voltage

APPLICATION INFORMATION

These dual comparators feature high gain , wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation , input resistors<10kΩ should be used.

The addition of positive feedback(<10mV) is also recommended. It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than-0.3V should not be used.

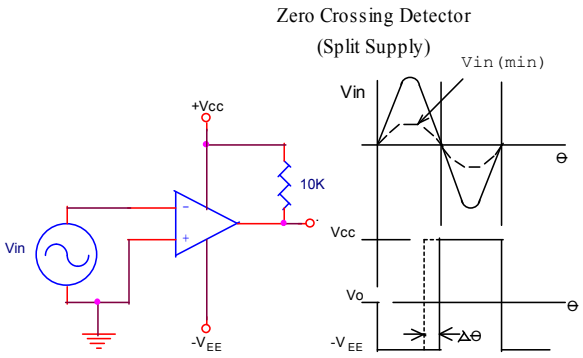


D1 prevents input from going negative by more than 0.6V

R1+R2=R3

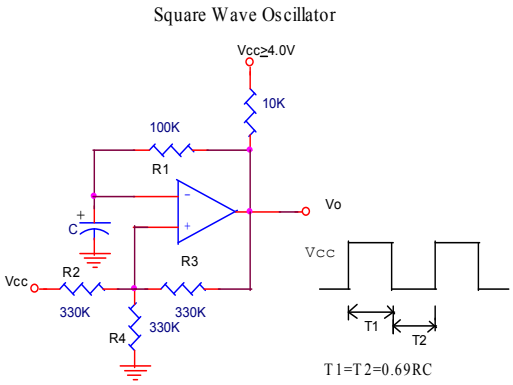
R3<=(R5/10) for small error in zero crossing

Fig 4.Zero crossing detector(single supply)



Vin(min)≈0.4V peak for 1% phase distortion(Δθ)

Fig 5.Zero crossing detector(split supply)



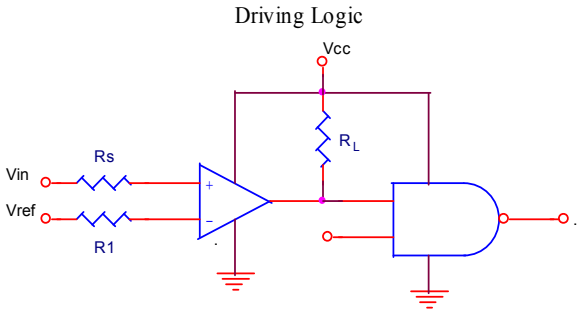
T1=T2=0.69RC

$f \approx \frac{7.2}{C(uF)}$

R2=R3=R4

R1≈ R2//R3//R4

Fig 6.Square wave oscillator

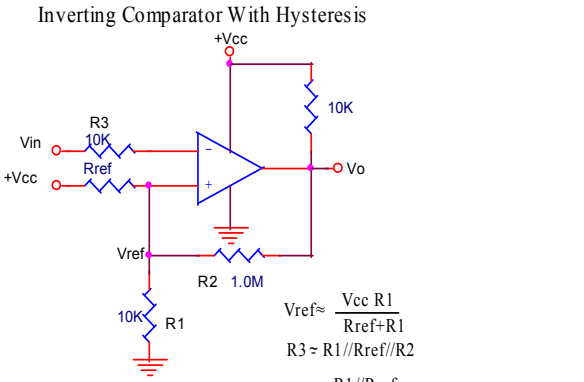


Rs=Source Resistance

R1≈Rs

Logic	Device	Vcc (V)	RL k
CMOS	1/4MC14001	+15	100
TTL	1/4MC7400	+5.0	10

Fig 7.Driving logic



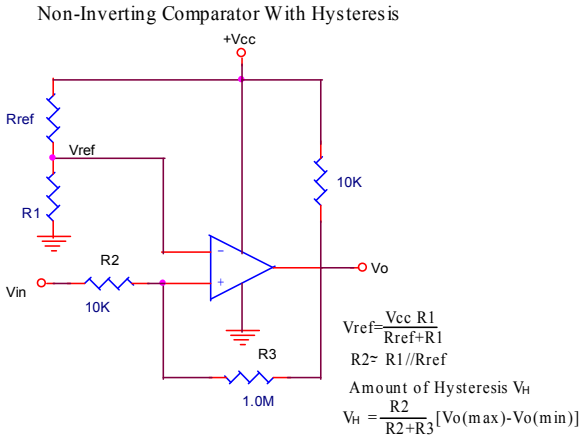
$Vref \approx \frac{Vcc\ R1}{Rref+R1}$

R3≈R1//Rref//R2

$V_H = \frac{R1//Rref}{R1//Rref+R2}$ [Vo(max)-Vo(min)]

R2> Rref//R1

Fig 8.Inverting comparator with hysteresis



$Vref = \frac{Vcc\ R1}{Rref+R1}$

R2≈ R1//Rref

Amount of Hysteresis V_H

$V_H = \frac{R2}{R2+R3}$[Vo(max)-Vo(min)]

Fig 9.Non-Inverting comparator with hysteresis