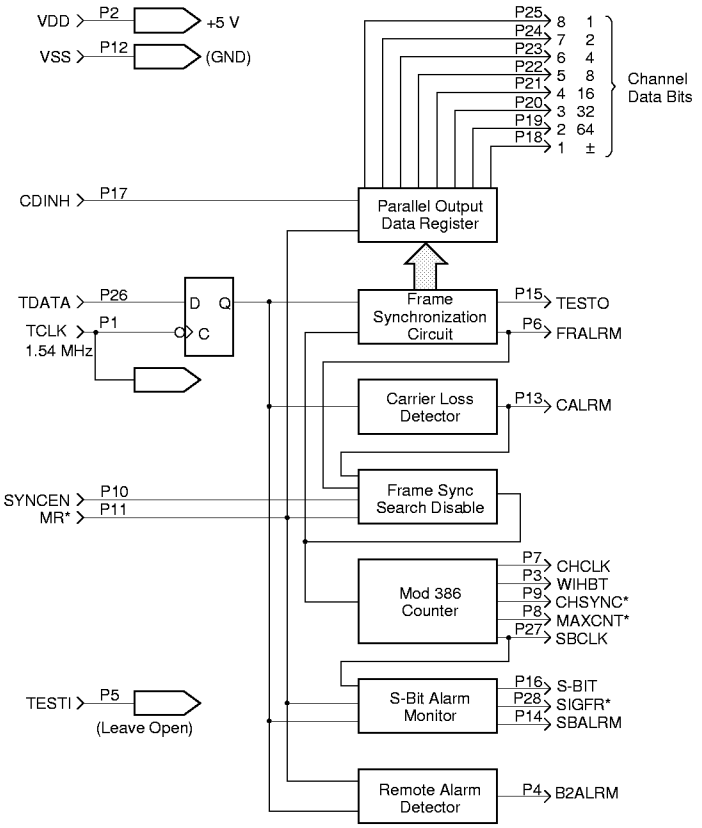
Bt8060

T-1 Serial Receiver

Distinguishing Features

- Synchronizes Serial T-1, D2 or T-1, D3 Signal in Less Than 5 ms.
- Extracts 8-Bit Parallel Channel Data
- Provides Timing Signals to Capture and Synchronize Channel and Frame Information
- Monitors and Detects
  - Errors in Signaling Bit Pattern
  - Loss of Frame Sync
  - Loss of Carrier
  - Remote Alarm Reporting
- Single 5 V Supply
- LSTTL Schottky Compatibility

Functional Block Diagram



Product Description

The Brooktree T-1 Receiver processes serial unipolar data of a T-1, D2 or T-1, D3 line from which data and a 1.544 MHz clock have been extracted.

Frame synchronization is accomplished by locating the frame bit (F_T) alternating every 386 bits. Loss of frame sync is indicated if a frame bit error occurs within two to four F-bit frames since the previous frame bit error.

A loss of carrier is indicated if 31 consecutive bit times yield zeros at the input. Carrier loss is reset and frame sync search begins when a one reappears at the TDATA input.

Signaling bits, which occur 193 bit positions after a framing bit, are monitored to detect signaling frames. The Signaling Frame (SIGFR) output identifies the present frame as a signaling frame. The S-bit output at that time identifies which signaling frame is being processed.

Remote alarm reporting is detected by monitoring the second received bit of every channel sample of every frame. An alarm is indicated if 255 consecutive bit-2 zeros are received.

Channel data bits are output by an 8-bit parallel register. The rising edge of the Channel Clock (CHCLK) signal indicates the extraction of new output channel data.

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Brooktree®

Product Description *(continued)*

Several signals developed from a mod-386 counter are provided to aid external processing and storage of channel data. For example, signals are provided to increment counters, synchronize counters, and strobe data into memories.

The Brooktree T-1 Receiver chip operates on a single 5 V supply and directly interfaces to the low-power TTL Schottky logic family. The receiver is packaged in a 28-pin Dual In-line Package (DIP). The pin configuration is shown in Figure 1.

Timing relationships are shown in Figures 2 through 4.

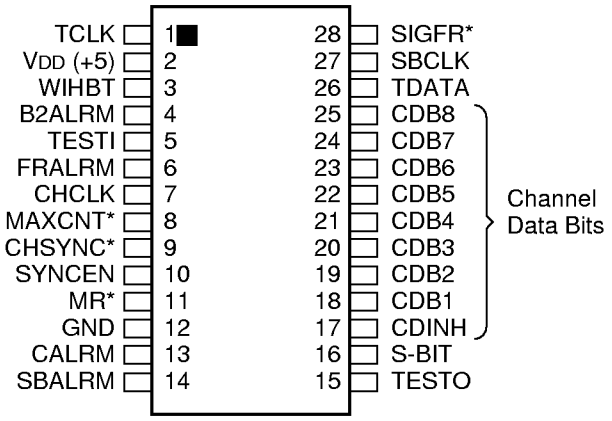


Figure 1. Pin Configuration.

Circuit Connections

T-1 Receiver Inputs

Any input less than or equal to 0.8 V equals logical zero, low, zero. Any input greater than or equal to 2.0 V equals logical one, high, one. A transition from a low level to a high level is called a "rising edge," while the converse is true for the "falling edge."

Unipolar T-1–D2 and T-1–D3 Serial Data Input (TDATA)

Unipolar T-1 data is clocked on the falling edge of TCLK. Thereafter, TDATA is processed on the rising edge of TCLK. TDATA must be stable 100 ns before and remain stable 100 ns after the falling edge of TCLK.

T-1 CLOCK (TCLK)

Typical clock frequency is 1.544 MHz. Maximum clock frequency is 1.85 MHz. The T-1 bit period is bounded by the rising edges of TCLK. Input levels must be greater than 2.4 V for logical one and less than or equal to 0.8 V for logical zero.

Frame Synchronization Enable (SYNCEN)

SYNCEN provides a means to disable the automatic resync search initiated by a Frame Alarm (FRALRM) condition. If the SYNCEN signal is low, synchronization function is inhibited and remains inhibited until SYNCEN transitions high. SYNCEN must be stable 200 ns before the rising edge of FRALRM in order to inhibit the synchronization function.

Master Reset (MR*)

When MR* is low, it performs an initialization clear of the T-1 receiver; SBALRM and CALRM are reset to low levels while FRALRM, CHCLK, WIHBT, and CHSYNC* are set to high levels. Frame synchronization search begins on the rising edge of MR* if SYNCEN signal has been high for 200 ns. Minimum pulse width is one T-1 clock period.

Channel Data Inhibit (CDINH)

CDINH provides a means to disable channel data bit outputs. When at a high level, CDINH forces channel data bits 1 through 7 high. Bit 8, the least significant channel data bit, is not controlled by CDINH.

Brooktree Device Test Input (TESTI)

TESTI is used only for Brooktree device testing. No connection to TESTI is required for normal operation.

Ground And Power (V_{SS} AND V_{DD})

V_{SS} = Ground, 0 VDC
V_{DD} = +5.0 ± 0.25 VDC

Circuit Connections *(continued)*

T-1 Receiver Outputs

T-1 receiver outputs are low power TTL Schottky compatible.

One ≥ 2.4 Vdc; zero ≤ 0.4 Vdc

A 12 K Ω pull-up to V_{DD} is required for CMOS.

Channel Data Bits 1 through 8 [CDB (1-8)]

Bit 1 is the sign bit, bit 2 is the most significant bit, and bit 8 is the least significant bit. If CDINH is low, new parallel channel data becomes valid within 200 ns after the rising edge of CHCLK and remains valid until the next rising edge of CHCLK. If CDINH is high, channel data bits 1 through 7 are forced to a high level. Bit 8, the least significant bit, is not controlled by CDINH. Channel data bits 1 through 7 are enabled or disabled within 300 ns by CDINH. (See Figures 2 through 4.)

Channel Clock (CHCLK)

The rising edge of CHCLK indicates a change of parallel output channel data. CHCLK is four TCLK high, then four TCLK low, except when an F- or S-bit is received. Then CHCLK is five TCLK high and four TCLK low. (See Figures 2 and 3.)

Channel Sync (CHSYNC*)

Channel Sync occurs once in a 24-channel period, making it suitable for synchronizing external counters to the T-1 Frame rate. CHSYNC* goes low one TCLK period before the falling edge of CHCLK at channel 24 data sample time. CHSYNC* returns high one TCLK period after the next rising edge of CHCLK. (see Figures 2 through 4.

Brooktree Device Test Output (TESTO)

TESTO is designed to aid Brooktree device testing. No connection is required for normal operation.

Write Inhibit (WIHBT)

WIHBT covers the parallel channel data transition period, and is suitable for clocking or strobing channel data into external memories. WIHBT is high for two TCLK periods, beginning one TCLK period before the rising edge of CHCLK. (See Figures 2 and 3.)

Maximum Count Of 386 Modulus (MAXCNT*)

MAXCNT* is low for one TCLK period, marking the completion of a two-frame period corresponding to the expected receipt of an F-bit at the TDATA input. (See Figures 3 and 4.)

S-bit Clock (SBCLK)

SBCLK will be high during the S-bit frame and low during the F-bit frame. The transitions will occur within 300 ns after the rising edge of TCLK as channel 24 data is being transferred to the parallel channel outputs. (See Figures 2 through 4.)

Signaling Bit Output (S-BIT)

The S-bit output will have the same digital level as the previous S-bit received that occurred two frames before the receipt of the current S-bit. An S-bit output transition occurs one TCLK period after the rising edge of SBCLK.

During a signaling frame when (SIGFR* is low), frame 6 or A-highway signaling is identified by low S-bit output. If S-bit is high during a signaling frame, frame 12 or B-highway signaling is identified. (See Figures 2 through 4.)

Signaling Frame (SIGFR*)

SIGFR* identifies frame 6 or 12 when low. If the sequence of five consecutively received S-bits is either 0111X or 1X001 (left to right, as received), SIGFR* will go low after the rising edge but at least 375 ns before the falling edge of WIHBT corresponding to channel-1 data sample time. SIGFR* returns high one frame later (193 bits). (See Figures 2 through 4.)

S-bit Alarm (SBALRM)

SBALRM goes high if the sequence of the five S-bits received contains four consecutive ones (01111), and remains high until three consecutive zero bits are preceded and followed by a one S-bit (10001). The actual transition of SBALRM output occurs after the rising edge but at least 375 ns before the falling edge of WIHBT corresponding to channel-1 data sample time.

Circuit Connections *(continued)*

Bit 2 Alarm (B2ALRM)

B2ALRM goes high, detecting a remote alarm condition, if 255 consecutive channel data samples are received with bit 2 low. B2ALRM returns low upon the receipt of any channel sample with bit 2 high.

Carrier Loss Alarm (CALRM)

A carrier loss is detected and CALRM is set high if 31 consecutive low-level TDATA bits are received.

Frame Error Alarm (FRALRM)

FRALRM detects an out-of-frame condition. FRALRM goes high if:

1. The framing synchronization function is in progress
2. Within 250 ns after the falling edge of MR*
3. An F-bit is received that is not the inverse of the last F-bit, and if the same condition also occurred two, three, or four F-bit frames earlier (two out of five F-bit errors).
4. Within 250 ns after the falling edge of CALRM (CALRM being reset by a high level TDATA bit).

FRALRM goes low upon completion of the synchronization function or within 250 ns after the rising edge of CALRM (a carrier-loss condition during a frame-synchronization function).

Output Clock Signals During Frame Synchronization Function

Following the declaration of frame sync loss (when FRALRM goes high), output signals will continue normally for a two-frame period with the exception of CHSYNC, which has the above mentioned second frame sync pulse inhibited. Following the two-frame period CHCLK, CHSYNC, and WIHBT are held high until frame sync has been located, as indicated by the falling edge of FRALRM. With typical data patterns, frame synchronization takes less than 5 ms. (See Figure 5.)

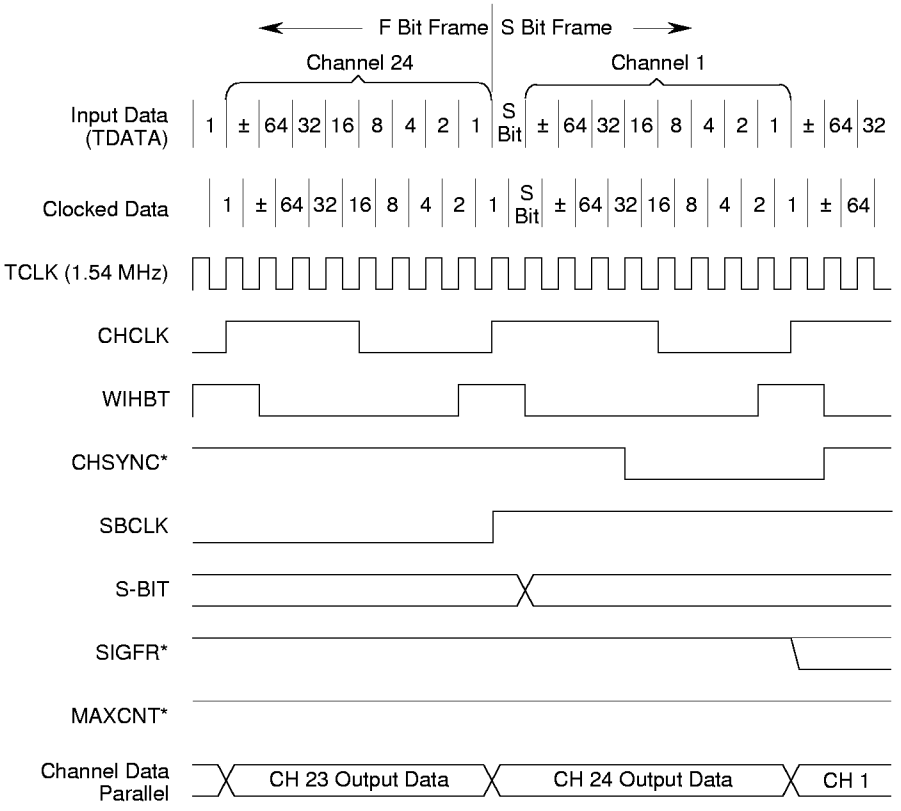


Figure 2. Signal Relationships at Beginning of F_S Frame (S-BIT).

Circuit Connections *(continued)*

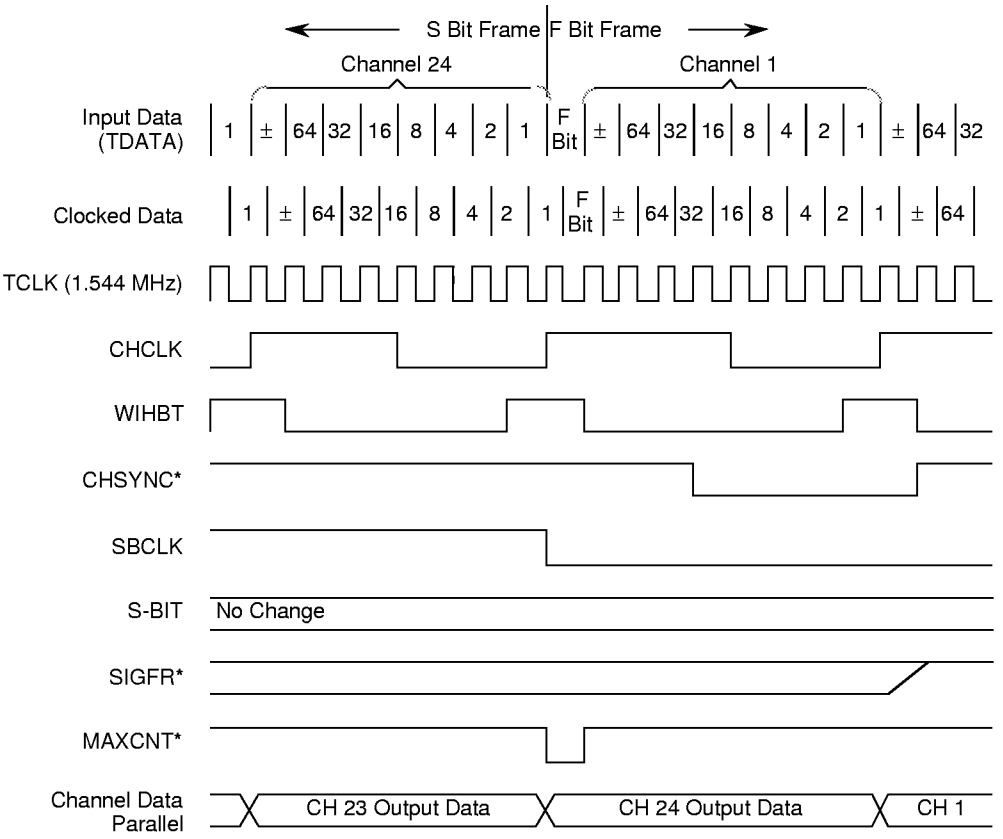
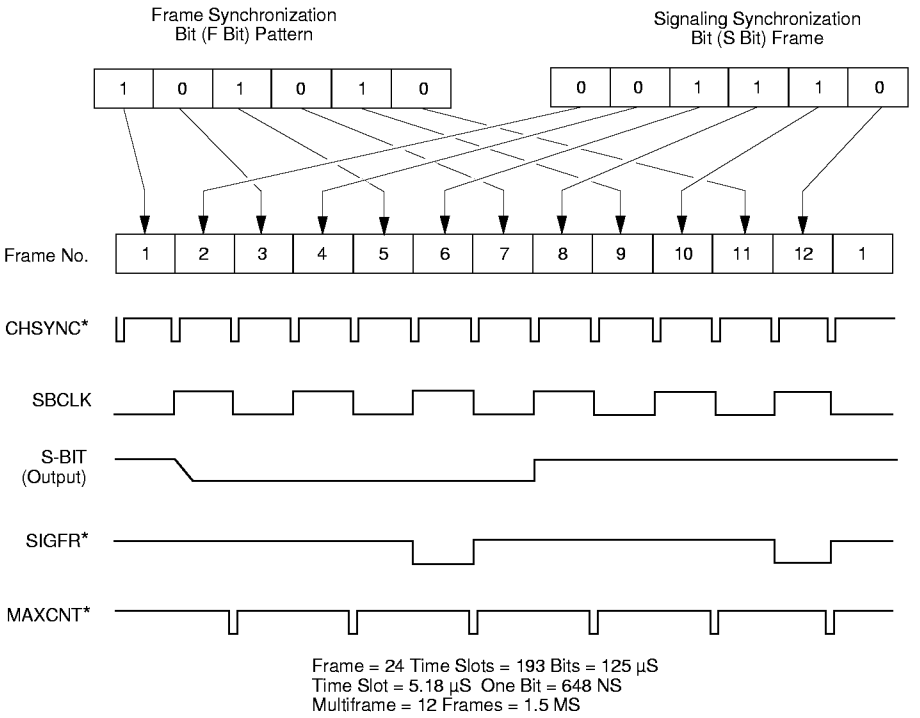


Figure 3. Signal Relationship During Frame Alarm and Search for Resynchronization.

Output	Max Delay (NS)
CHCLK	300
CHSYNC*	300
WIHBT	300
MAXCNT*	300
SBCLK	400
S-BIT	400
SIGFR*	475
SBALRM	475
B2ALRM	450
CALRM	300
FRALRM	900
CDB (1–8)	400

Table 1. Output Propagation Delay (Worst Case, from Rising Edge of TCLK).

Circuit Connections *(continued)*



F Bit (F_T) Alignment Signal
(Odd-Numbered Frames)

Frame	First Bit
1	1
3	0
5	1
7	0
9	1
11	0

S Bit (F_S) Alignment Signal
(Even-Numbered Frames)

Frame	First Bit
2	0
4	0
6	1
8	1
10	1
12	0

Figure 4. Multiframe Signal Relationships.

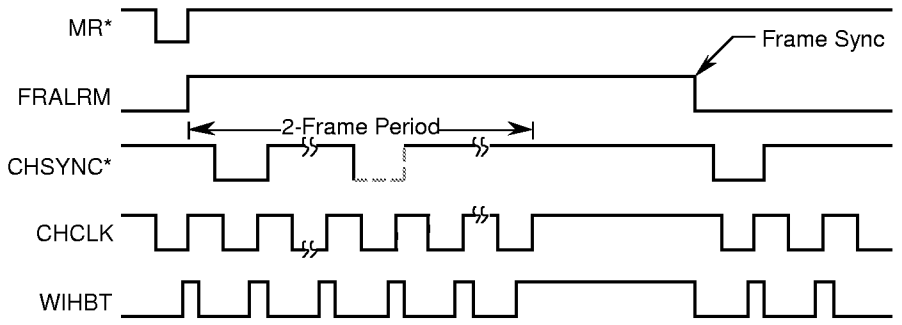


Figure 5. Signal Relationship During Frame Alarm and Search for Resynchronization.

Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature Range	T_{STG}	–55 to +150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

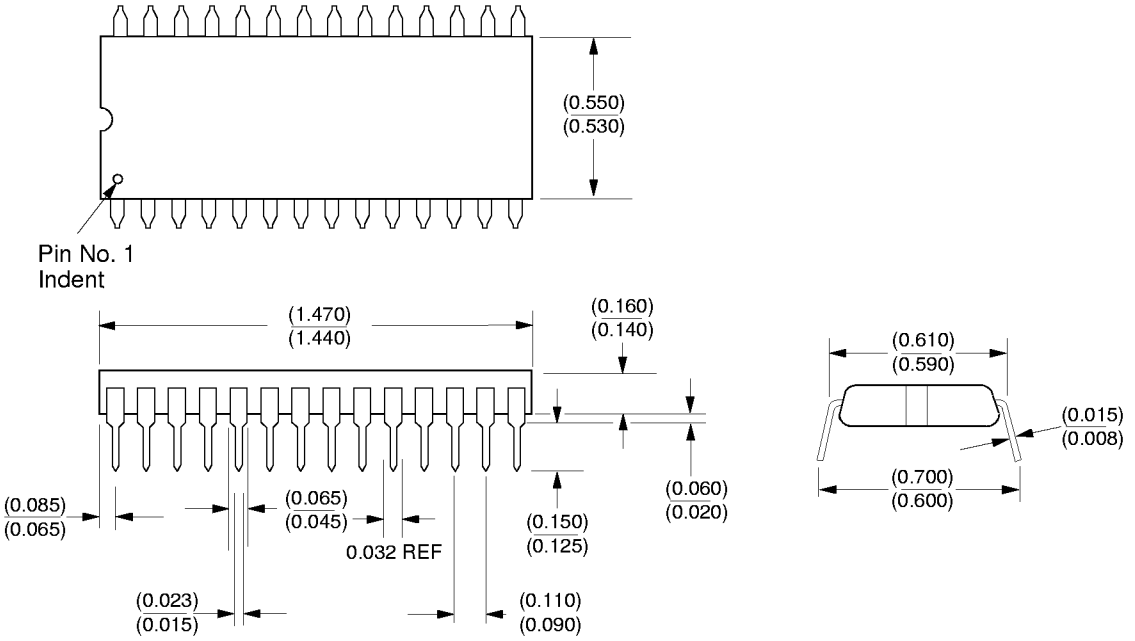
(V_{DD} = +5 V ±5%, T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Logical One Voltage	V_{IH}	2.0	VDD + 0.3	V
Input Logical Zero Voltage	V_{IL}	–0.3	0.8	V
Output Logical One Voltage	V_{OH}	2.4		V
Output Logical Zero Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	–100		µA
Output Sink Current	I_{OL}	400		µA
Clock Frequency	T_{CLK}		1.85	MHz
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation	P_{DSS}		550	mW

Ordering Information

Part Number	Package	Temperature Range
Bt8060KP	28-Pin Plastic DIP	0°C to 70°C
Bt8060KC	28-Pin Ceramic DIP	0°C to 70°C
Bt8060EP	28-Pin Plastic DIP	–40°C to 85°C

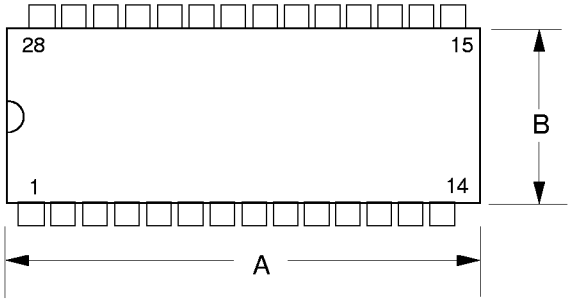
Package Diagram



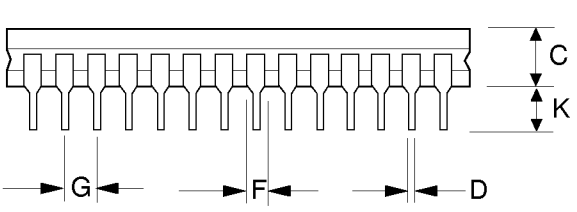
Note: Dimensions are given in inches.

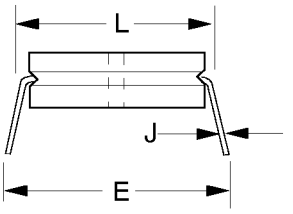
28-Pin Plastic Dip

Package Diagram



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	36.32	37.34	1.430	1.470
B	12.95	13.46	0.510	0.530
C	3.68	4.19	0.145	0.165
D	0.41	0.51	0.016	0.020
E	16.26	17.27	0.640	0.680
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	4.19	4.95	0.165	0.195
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
REF: PD28S/GP00-D310				





28-Pin Ceramic DIP