

**NEC****MOS INTEGRATED CIRCUIT** **$\mu$ PD78042A, 78043A, 78044A, 78045A****8-BIT SINGLE-CHIP MICROCOMPUTER****DESCRIPTION**

The  $\mu$ PD78042A,  $\mu$ PD78043A,  $\mu$ PD78044A, and  $\mu$ PD78045A are 8-bit single-chip microcomputers that incorporate many hardware peripherals such as an FIP<sup>®</sup> controller/driver, 8-bit resolution A/D converter, timer, serial interface, and interrupt controller.

In addition to these standard mask ROM models, one-time PROM models that can operate in the same voltage range, EPROM models, and various development tools are being developed.

The functions of these microcomputers are described in detail in the following User's Manual. Be sure to read this manual when you design a system using any of these microcomputers.

$\mu$ PD78044A Sub-Series User's Manual : IEU-1394

78K/0 Series User's Manual, Instruction : IEU-1372

**FEATURES**

- High-capacity ROM and RAM

Item Product name	Program memory (ROM)	Data memory		
		Internal high-speed RAM	Buffer RAM	FIP display RAM
$\mu$ PD78042A	16K bytes	512 bytes	64 bytes	48 bytes
$\mu$ PD78043A	24K bytes			
$\mu$ PD78044A	32K bytes	1024 bytes		
$\mu$ PD78045A	40K bytes			

- Wide range of instruction execution time
  - from high-speed (0.4  $\mu$ s) to ultra low-speed (122  $\mu$ s)
- I/O ports: 68
- FIP controller/driver: total display outputs: 34
- 8-bit resolution A/D converter: 8 channels
- Serial interface: 2 channels
- Timer: 6 channels
- Power supply voltage:  $V_{DD} = 2.7$  to 6.0 V

**APPLICATIONS**

VCRs, audio systems, etc.

**ORDERING INFORMATION**

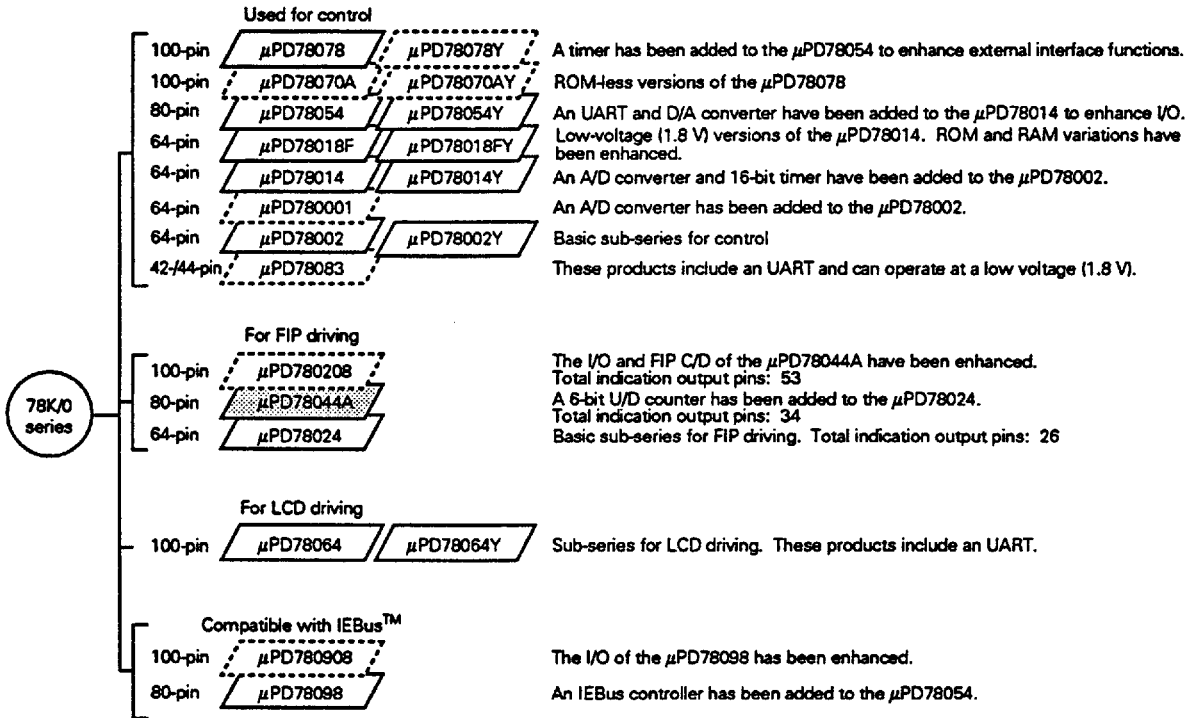
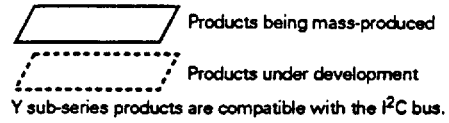
Part number	Package
$\mu$ PD78042AGF- $\times\times\times$ -3B9	80-pin plastic QFP (14 x 20 mm)
$\mu$ PD78043AGF- $\times\times\times$ -3B9	80-pin plastic QFP (14 x 20 mm)
$\mu$ PD78044AGF- $\times\times\times$ -3B9	80-pin plastic QFP (14 x 20 mm)
$\mu$ PD78045AGF- $\times\times\times$ -3B9	80-pin plastic QFP (14 x 20 mm)

Remark " $\times\times\times$ " indicates ROM code number.

The information in this document is subject to change without notice.

★ 78K/0 SERIES PRODUCT DEVELOPMENT

The 78K/0 series products were developed as shown below. The sub-series names are indicated in frames.



The table below shows the main differences between sub-series.

Function Sub-series name		ROM capacity	Timer				8-bit A/D	8-bit D/A	Serial interface	I/O	Minimum V <sub>DD</sub>	External expansion
			8-bit	16-bit	Watch	WDT						
For control	μPD78078	32K-60K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART:1ch)	88 pins	1.8 V	○
	μPD78070A	—								61 pins	2.7 V	
	μPD78054	16K-60K	2ch	—	—	—	—	2ch	69 pins	2.0 V		
	μPD78018F	8K-48K							53 pins	1.8 V		
	μPD78014	8K-32K	—	—	—	—	—	1ch	39 pins	2.7 V	—	
	μPD780001	8K										
	μPD78002	8K-16K							53 pins	○		
	μPD78083	8K-16K							1ch (UART:1ch)	33 pins		1.8 V
For FIP driving	μPD780208	32K-40K	2ch	1ch	1ch	1ch	8ch	—	2ch	74 pins	2.7 V	—
	μPD78044A	16K-40K								68 pins		
	μPD78024	24K-32K								54 pins		
For LCD driving	μPD78064	16K-32K	2ch	1ch	1ch	1ch	8ch	—	2ch (UART:1ch)	57 pins	2.0 V	—
Compatible with IEBus	μPD780908	60K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART:1ch)	88 pins	2.7 V	○
	μPD78098	32K-60K								69 pins		

FUNCTIONAL OUTLINE

Product name		μPD78042A	μPD78043A	μPD78044A	μPD78045A
Internal memory	ROM	16K bytes	24K bytes	32K bytes	40 K bytes
	Internal high-speed RAM	512 bytes		1024 bytes	
	Buffer RAM	64 bytes			
	FIP display RAM	48 bytes			
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle		Variable instruction execution time			
		For main system clock : 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 5.0 MHz)			
		For subsystem clock : 122 μs (at 32.768 kHz)			
Instruction set		<ul style="list-style-type: none"> <li>• Multiplication/division (8 bits × 8 bits, 16 bits + 8 bits)</li> <li>• Bit (set, reset, test, Boolean algebra)</li> </ul>			
I/O ports (including those multiplexed with FIP pins)		Total : 68 lines <ul style="list-style-type: none"> <li>• CMOS input : 2 lines</li> <li>• CMOS I/O : 27 lines</li> <li>• N-ch open-drain : 5 lines</li> <li>• P-ch open-drain I/O : 16 lines</li> <li>• P-ch open-drain output : 18 lines</li> </ul>			
FIP controller/driver		Total : 34 lines <ul style="list-style-type: none"> <li>• Segments : 9 to 24 lines</li> <li>• Digits : 2 to 16 lines</li> </ul>			
A/D converter		<ul style="list-style-type: none"> <li>• 8-bit resolution × 8 channels</li> <li>• Power supply voltage: V<sub>DD</sub> = 4.0 to 6.0 V</li> </ul>			
Serial interface		<ul style="list-style-type: none"> <li>• 3-line/SBI/2-line mode selectable : 1 channel</li> <li>• 3-line mode (with automatic transmission/reception function of up to 64 bytes) : 1 channel</li> </ul>			
Timer		<ul style="list-style-type: none"> <li>• 16-bit timer/event counter : 1 channel</li> <li>• 8-bit timer/event counter : 2 channels</li> <li>• Watch timer : 1 channel</li> <li>• Watchdog timer : 1 channel</li> <li>• 6 bit up/down counter : 1 channel</li> </ul>			
Timer output		3 lines (one for 14-bit PWM output)			
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz (at main system clock of 5.0 MHz) 32.768 kHz (at subsystem clock of 32.768 kHz)			
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz (at 5.0 MHz: main system clock)			
Vectored interrupt	Maskable interrupt	Internal 10 lines, external 4 lines			
	Non-maskable interrupt	Internal 1 line			
	Software interrupt	Internal 1 line			
Text input		Internal 1 line			
Power supply voltage		V <sub>DD</sub> = 2.7 to 6.0 V			
Package		80-pin plastic QFP (14 × 20 mm)			

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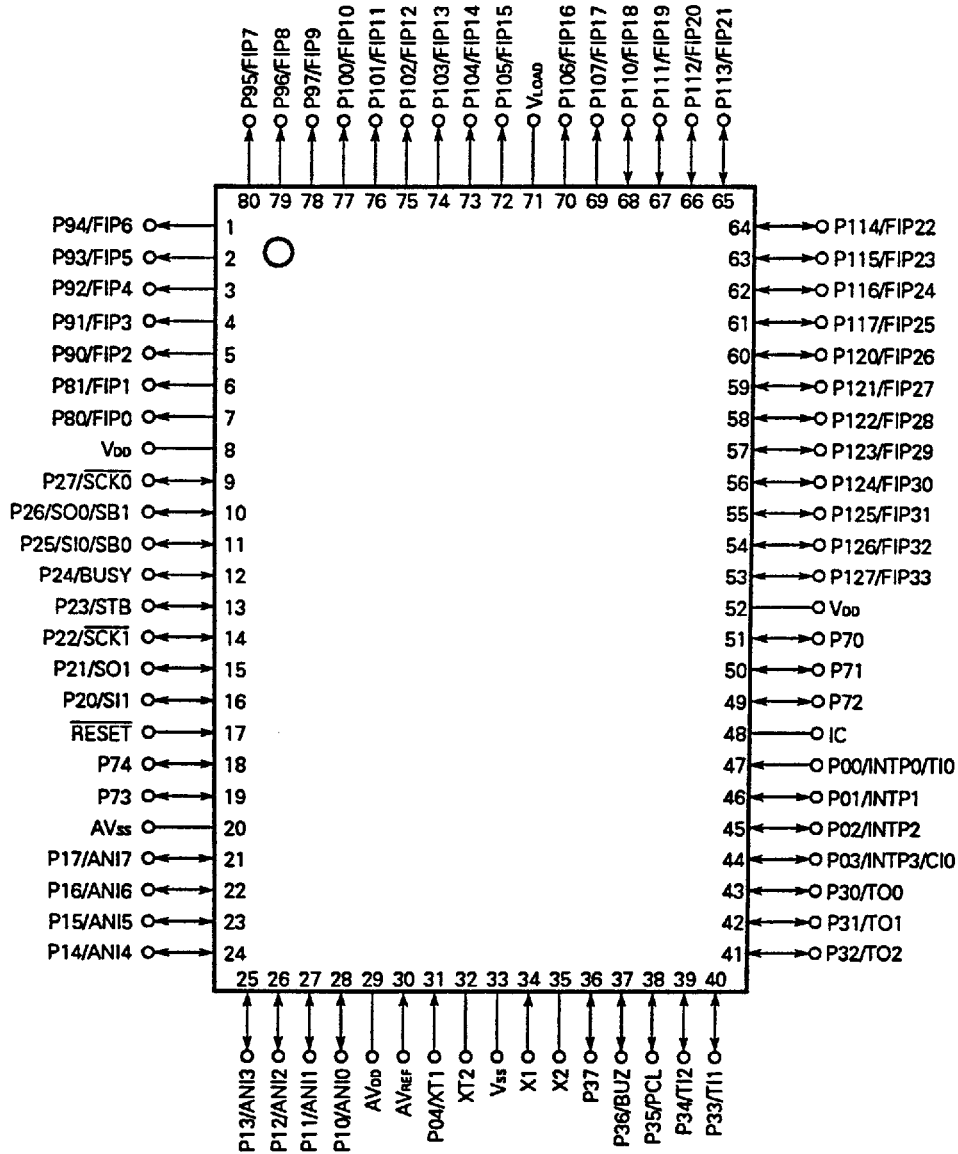
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1. PIN CONFIGURATION (TOP VIEW)

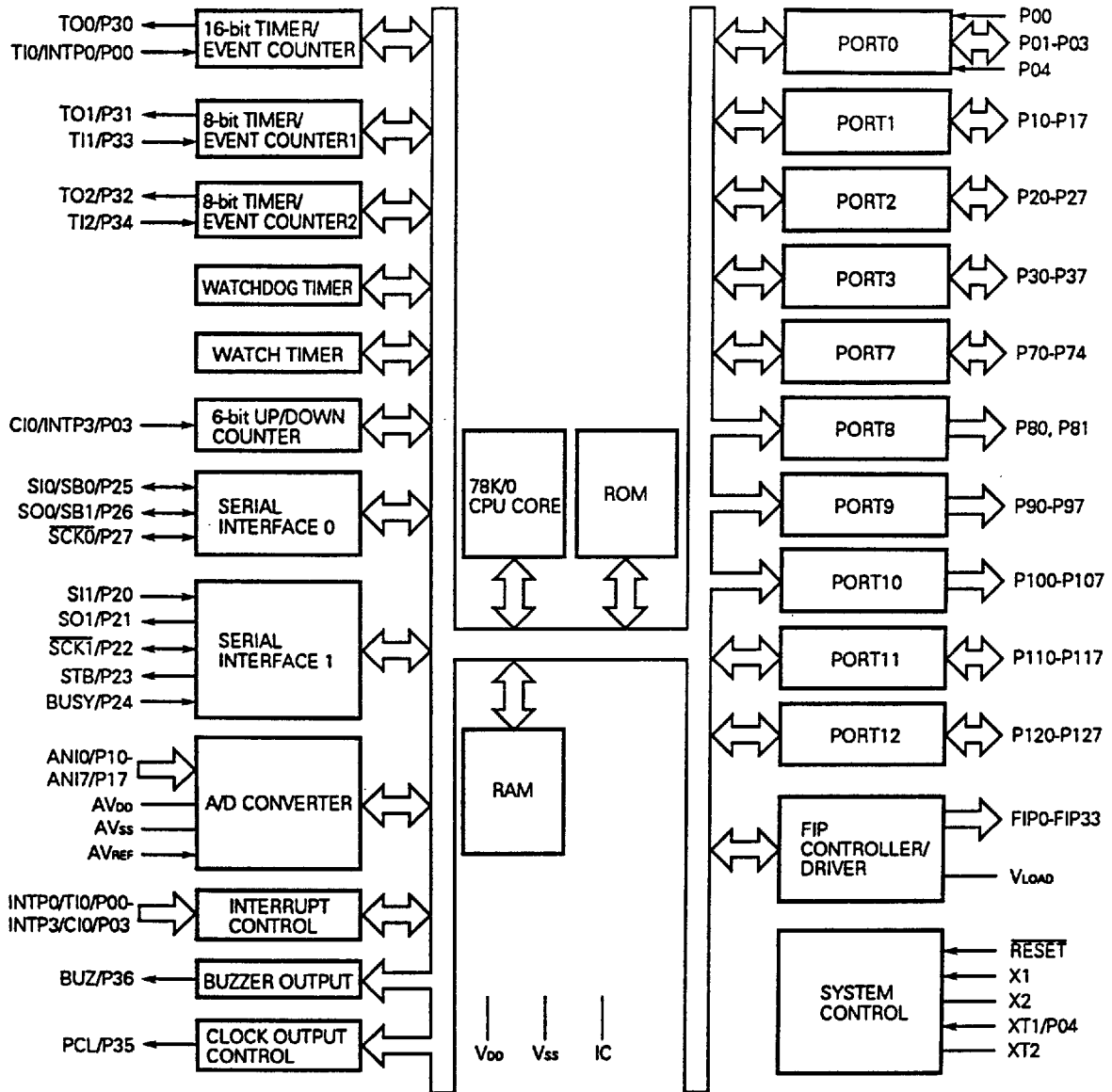
- 80-pin plastic QFP (14 × 20 mm)  
 μPD78042AGF-xxx-3B9, μPD78043AGF-xxx-3B9  
 μPD78044AGF-xxx-3B9, μPD78045AGF-xxx-3B9



- Cautions**
1. Connect the IC (Internally Connected) pins directly to the Vss.
  2. Connect the AVDD pin to the VDD pin.
  3. Connect the AVSS pin to the VSS pin.

P00-P04	: Port0	$\overline{SCK0}, \overline{SCK1}$	: Serial Clock
P10-P17	: Port1	PCL	: Programmable Clock
P20-P27	: Port2	BUZ	: Buzzer Clock
P30-P37	: Port3	STB	: Strobe
P70-P74	: Port7	BUSY	: Busy
P80,P81	: Port8	FIP0-FIP33	: Fluorescent Indicator Panel
P90-P97	: Port9	V <sub>LOAD</sub>	: Negative Power Supply
P100-P107	: Port10	X1,X2	: Crystal (Main System Clock)
P110-P117	: Port11	XT1,XT2	: Crystal (Subsystem Clock)
P120-P127	: Port12	$\overline{RESET}$	: Reset
INTP0-INTP3	: Interrupt From Peripherals	ANI0-ANI7	: Analog Input
TI0-TI2	: Timer Input	AV <sub>DD</sub>	: Analog Power Supply
TO0-TO2	: Timer Output	AV <sub>SS</sub>	: Analog Ground
CIO	: Counter Input	AV <sub>REF</sub>	: Analog Reference Voltage
SB0,SB1	: Serial Bus	V <sub>DD</sub>	: Power Supply
SI0,SI1	: Serial Input	V <sub>SS</sub>	: Ground
SO0,SO1	: Serial Output	IC	: Internally Connected

2. BLOCK DIAGRAM



Remark The capacities of the internal ROM and RAM differ depending on the product.



3. PINS FUNCTIONS

3.1 PORT PINS (1/2)

Pin name	I/O	Function	On reset	Shared by:	
P00	Input	Port 0 5-bit I/O port  Can be specified for input or output in 1-bit units. When used as an input port pin, a pull-up resistor can be connected through software.	Input only	Input	INTP0/TI0
P01	I/O		Input only	Input	INTP1
P02					INTP2
P03					INTP3/CI0
P04 <sup>Note 1</sup>	Input		Input only	Input	XT1
P10-P17	I/O	Port 1 8-bit I/O port Can be specified for input or output in 1-bit units. When used as an input port pin, a pull-up resistor can be connected through software. <sup>Note 2</sup>	Input	ANI0-ANI7	
P20	I/O	Port 2 8-bit I/O port Can be specified for input or output in 1-bit units. When used as an input port pin, a pull-up resistor can be connected through software.	Input	S11	
P21				SO1	
P22				$\overline{\text{SCK1}}$	
P23				STB	
P24				BUSY	
P25				SI0/SB0	
P26				SO0/SB1	
P27				$\overline{\text{SCK0}}$	
P30	I/O	Port 3 8-bit I/O port Can be specified for input or output in 1-bit units. Can directly drive LEDs. When used as an input port pin, a pull-up resistor can be connected through software. A pull-down resistor can be connected in 1-bit units by the mask option.	Input	TO0	
P31				TO1	
P32				TO2	
P33				TI1	
P34				TI2	
P35				PCL	
P36				BUZ	
P37				—	

- Notes**
1. When the P04/XT1 pins is used as an input port pin, bit 6 (FRC) of the processor clock control register must be set to 1. At this time, do not use the feedback resistor of the subsystem clock oscillator circuit.
  2. When the P10/ANI0 through P17/ANI7 pins are used as the analog input lines of the A/D converter, be sure to place the port 1 in the input mode. In this case, the pull-up resistors are automatically unused.

3.1 PORT PINS (2/2)

Pin name	I/O	Function	On reset	Shared by:
P70-P74	I/O	Port 7 5-bit N-ch open-drain I/O port Can be specified for input or output in 1-bit units. Can directly drive LEDs. A pull-up resistor can be connected in 1-bit units by the mask option.	Input	—
P80, P81	Output	Port 8 2-bit P-ch open-drain high-voltage output port. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether $V_{LOAD}$ or $V_{SS}$ is connected can be specified in bit units).	Output	FIP0, FIP1
P90-P97	Output	Port 9 8-bit P-ch open-drain high-voltage output port. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether $V_{LOAD}$ or $V_{SS}$ is connected can be specified in 4-bit units).	Output	FIP2-FIP9
P100-P107	Output	Port 10 8-bit P-ch open-drain high-voltage output port. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether $V_{LOAD}$ or $V_{SS}$ is connected can be specified in 4-bit units).	Output	FIP10-FIP17
P110-P117	I/O	Port 11 8-bit P-ch open-drain high-voltage I/O port. Can directly drive LEDs. Can be specified for input or output in 1-bit units. A pull-down resistor can be connected in 1-bit units by the mask option (whether $V_{LOAD}$ or $V_{SS}$ is connected can be specified in 4-bit units).	Input	FIP18-FIP25
P120-P127	I/O	Port 12 8-bit P-ch open-drain high-voltage I/O port Can directly drive LEDs. Can be specified for input or output in 1-bit units. A pull-down resistor can be connected in 1-bit units by the mask option (whether $V_{LOAD}$ or $V_{SS}$ is connected can be specified in 4-bit units).	Input	FIP26-FIP33

3.2 PINS OTHER THAN PORT PINS (1/2)

Pin name	I/O	Function	On reset	Shared by:
INTP0	Input	Valid edge (rising, falling, or both rising and falling edges) can be specified.	Input	P00/T10
INTP1				P01
INTP2		External interrupt input		P02
INTP3		Falling edge-active external interrupt input	Input	P03/C10
SI0	Input	Serial data input lines of serial interface	Input	P25/SB0
SI1				P20
SO0	Output	Serial data output lines of serial interface	Input	P26/SB1
SO1				P21
SB0	I/O	Serial data I/O lines of serial interface	Input	P25/SI0
SB1				P26/SO0
$\overline{\text{SCK0}}$	I/O	Serial clock I/O lines of serial interface	Input	P27
$\overline{\text{SCK1}}$				P22
STB	Output	Automatic transmission/reception strobe output line of serial interface	Input	P23
BUSY	Input	Automatic transmission/reception busy input line of serial interface	Input	P24
T10	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
T11		External count clock input to 8-bit timer (TM1)		P33
T12		External count clock input to 8-bit timer (TM2)		P34
TO0	Output	16-bit timer output (multiplexed with 14-bit PWM output)	Input	P30
TO1		8-bit timer output		P31
TO2				P32
C10	Input	Clock input to up/down counter	Input	P03/INTP3
PCL	Output	Clock output (for trimming main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
FIP0, FIP1	Output	High-voltage, high-current digit/segment output of FIP controller/driver	Output	P80, P81
FIP2-FIP9				P90-P97
FIP10-FIP15	Output	High-voltage, high-current digit/segment output of FIP controller/driver	Output	P100-P105
FIP16, FIP17	Output	High-voltage segment output of FIP controller/driver	Output	P106, P107
FIP18-FIP25			Input	P110-P117
FIP26-FIP33			Input	P120-P127
V <sub>LOAD</sub>	—	Connects pull-down resistor to FIP controller/driver	—	—

3.2 PINS OTHER THAN PORT PINS (2/2)

Pin name	I/O	Function	On reset	Shared by:
ANI0-ANI7	Input	A/D converter analog input lines	Input	P10-P17
AV <sub>REF</sub>	Input	A/D converter reference voltage input line	—	—
AV <sub>DD</sub>	—	Analog power supply to A/D converter. Connected to the V <sub>DD</sub> pin.	—	—
AV <sub>SS</sub>	—	A/D converter ground line. Connected to the V <sub>SS</sub> pin.	—	—
<u>RESET</u>	Input	System reset input	—	—
X1	Input	Connect crystal for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Connect crystal for subsystem clock oscillation	Input	P04
XT2	—		—	—
V <sub>DD</sub>	—	Positive power supply	—	—
V <sub>SS</sub>	—	Ground potential	—	—
IC	—	Internal connection. Connected directly to the V <sub>SS</sub> pin.	—	—

3.3 PIN I/O CIRCUITS AND PROCESSING OF UNUSED PINS

Table 3-1 shows the I/O circuit type of each pin and the processing of unused pins.  
For the configuration of the I/O circuit of each type, refer to Fig. 3-1.

Table 3-1 I/O Circuit Type

Pin name	I/O Circuit type	I/O	Recommended connections when unused			
P00/INTP0/TI0	2	Input	Connected to V <sub>ss</sub> .			
P01/INTP1	8-A	I/O	Individually connected to V <sub>ss</sub> with a resistor.			
P02/INTP2						
P03/INTP3/CI0						
P04/XT1	16	Input	Connected to V <sub>DD</sub> or V <sub>ss</sub> .			
P10/ANI0-P17/ANI7	11	I/O	Individually connected to V <sub>DD</sub> or V <sub>ss</sub> with a resistor.			
P20/SI1	8-A					
P21/SO1	5-A					
P22/SCK1	8-A					
P23/STB	5-A					
P24/BUSY	8-A					
P25/SI0/SB0	10-A					
P26/SO0/SB1						
P27/SCK0						
P30/TO0	5-C					
P31/TO1						
P32/TO2						
P33/TI1	8-B					
P34/TI2						
P35/PCL	5-C					
P36/BUZ						
P37						
P70-P74	13-B	Output	Open			
P80/FIP0, P81/FIP1	14-A					
P90/FIP2-P97/FIP9						
P100/FIP10-P107/FIP17	15-C	I/O	Individually connected to V <sub>DD</sub> or V <sub>ss</sub> with a resistor.			
P110/FIP18-P117/FIP25						
P120/FIP26-P127/FIP33	2	Input	—			
RESET						
XT2				16	—	Open
AV <sub>REF</sub>						Connected to V <sub>ss</sub> .
AV <sub>DD</sub>						Connected to V <sub>DD</sub> .
AV <sub>SS</sub>						Connected to V <sub>ss</sub> .
V <sub>LOAD</sub>						
IC						Connected directly to V <sub>ss</sub> .

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Fig. 3-1 Pin I/O Circuits (1/2)

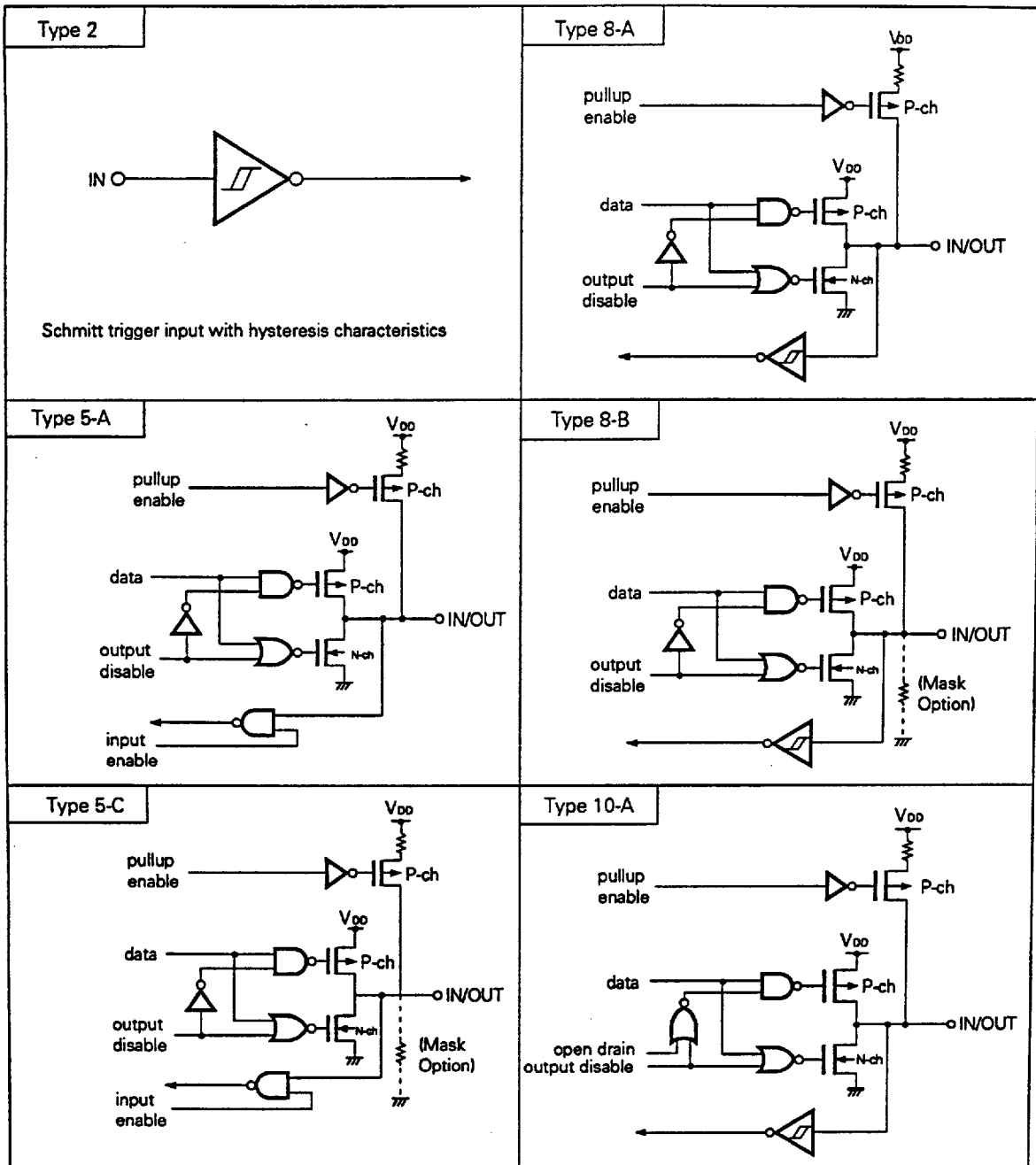
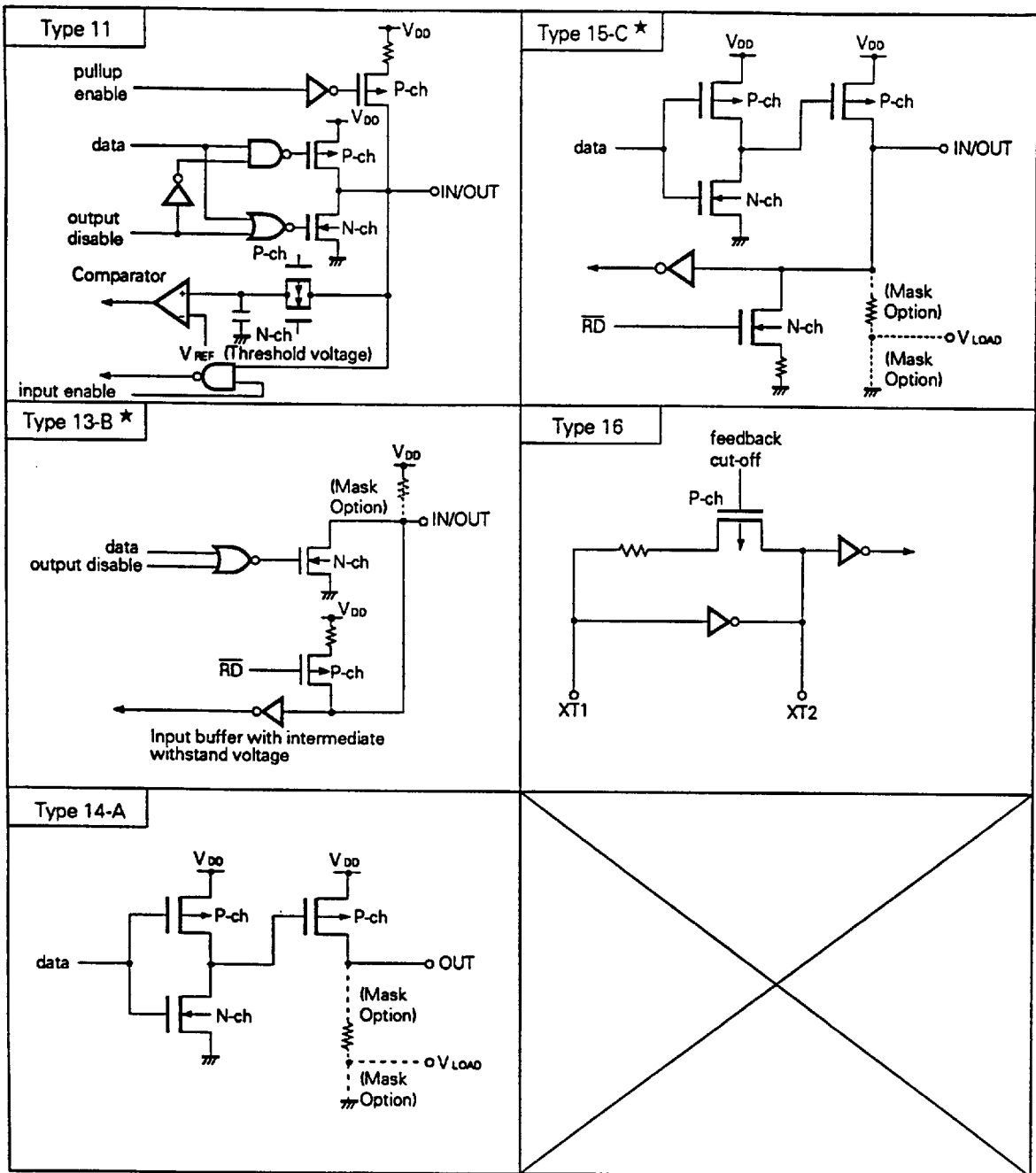


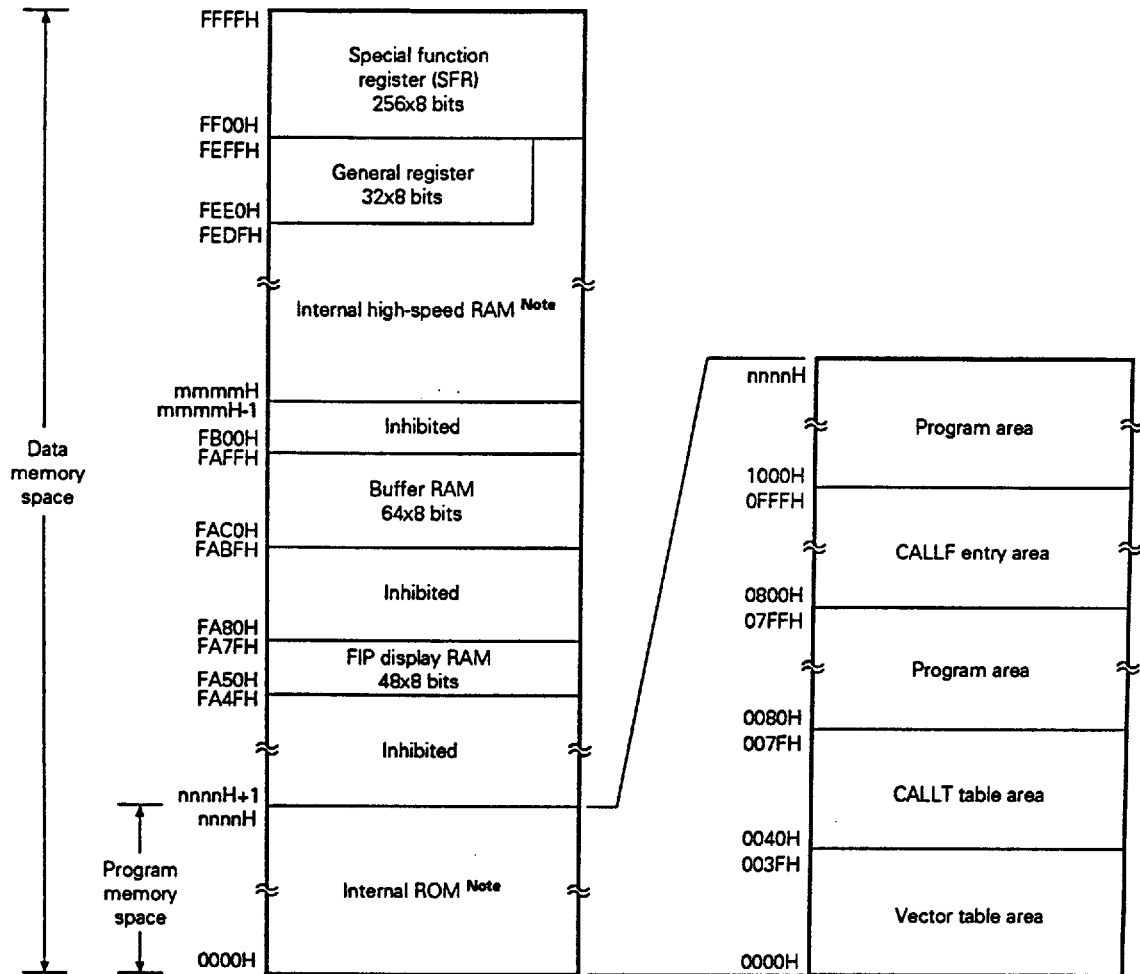
Fig. 3-1 Pin I/O Circuits (2/2)



4. MEMORY SPACE

Fig. 4-1 shows the memory map for μPD78042A, μPD78043A, μPD78044A, and μPD78045A.

Fig. 4-1 Memory Map



**Note** The internal ROM and internal high-speed RAM capacities vary depending on the product. (Refer to the table below.)

Product name	Last Address of Internal ROM nnnnH	First address of internal high-speed RAM mmmH
μPD78042A	3FFFH	FD00H
μPD78043A	5FFFH	FB00H
μPD78044A	7FFFH	
μPD78045A	9FFFH	



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O ports are classified into the following 5 kinds:

- CMOS input (P00, P04) : 2
- CMOS input/output (P01 - P03, ports 1 - 3) : 27
- N-ch open-drain input/output (port 7) : 5
- P-ch open-drain output (ports 8 - 10) : 18
- P-ch open-drain input/output (ports 11 and 12) : 16

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Total : 68

Table 5-1 Port Function

Product	Pin	Function
Port 0	P00, P04	Input port
	P01-P03	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 1	P10-P17	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 2	P20-P27	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 3	P30-P37	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software. Pull-down resistor can be connected in 1-bit units by the mask option. Can directly drive LED.
Port 7	P70-P74	N-ch open-drain I/O port. Can be specified for input or output in 1-bit units. Pull-up resistor can be connected in 1-bit units by the mask option. Can directly drive LED.
Port 8	P80, P81	P-ch open-drain high-voltage output port. Pull-down resistor can be connected in 2-bit units by the mask option (connection to $V_{LOAD}$ or $V_{SS}$ can be specified in 2-bit units). Can directly drive LED.
Port 9	P90-P97	P-ch open-drain high-voltage output port. Pull-down resistor can be connected in 1-bit units by the mask option (connection to $V_{LOAD}$ or $V_{SS}$ can be specified in 4-bit units). Can directly drive LED.
Port 10	P100-P107	P-ch open-drain high-voltage output port. Pull-down resistor can be connected in 1-bit units by the mask option (connection to $V_{LOAD}$ or $V_{SS}$ can be specified in 4-bit units). Can directly drive LED.
Port 11	P110-P117	P-ch open-drain high-voltage I/O port. Can be specified for input or output in 1-bit units. Pull-down resistor can be connected in 1-bit units by the mask option (connection to $V_{LOAD}$ or $V_{SS}$ can be specified in 4-bit units). Can directly drive LED.
Port 12	P120-P127	P-ch open-drain high-voltage I/O port. Can be specified for input or output in 1-bit units. Pull-down resistor can be connected in 1-bit units by the mask option (connection to $V_{LOAD}$ or $V_{SS}$ can be specified in 4-bit units). Can directly drive LED.

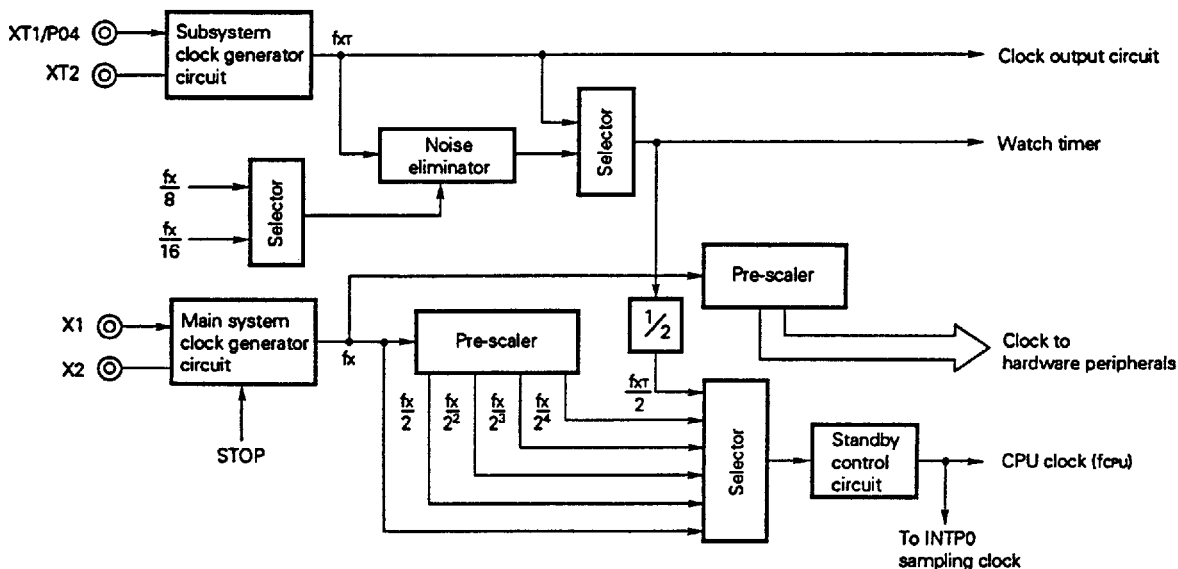
5.2 CLOCK GENERATOR CIRCUIT

The clock generator circuit has two kinds of generator circuits: the main system clock and subsystem clock. The instruction time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (with main system clock: 5.0 MHz)
- 122 μs (with subsystem clock: 32.768 kHz)

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Fig. 5-1 Clock Generator Circuit Block Diagram



5.3 TIMER/EVENT COUNTER

Six channels of timer/event counters are provided.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel
- 6-bit up/down counter : 1 channel

Table 5-2 Timer/Event Counter Groups and Configurations

		16-bit timer/ event counter	8-bit timer/ event counter	Watch timer	Watchdog timer	6-bit up/ down counter
Group	Interval timer	1 channel	2 channels	1 channel	1 channel	—
	External event counter	1 channel	2 channels	—	—	1 channel
Function	Timer output	1 output	2 outputs	—	—	—
	PWM output	1 output	—	—	—	—
	Pulse width measurement	1 input	—	—	—	—
	Square wave output	1 output	2 outputs	—	—	—
	Interrupt Request	1	2	1	1	1
	Test input	—	—	1 input	—	—

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Fig. 5-2 16-Bit Timer/Event Counter Block Diagram

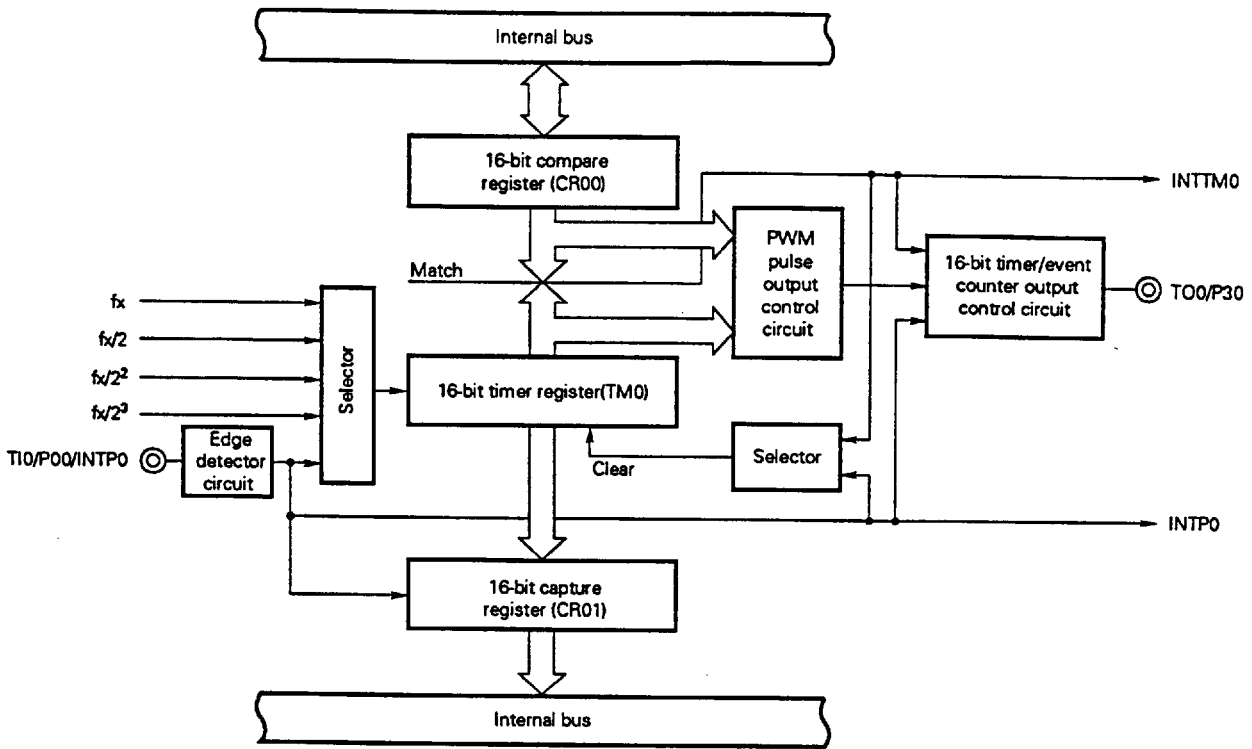


Fig. 5-3 8-Bit Timer/Event Counter Block Diagram

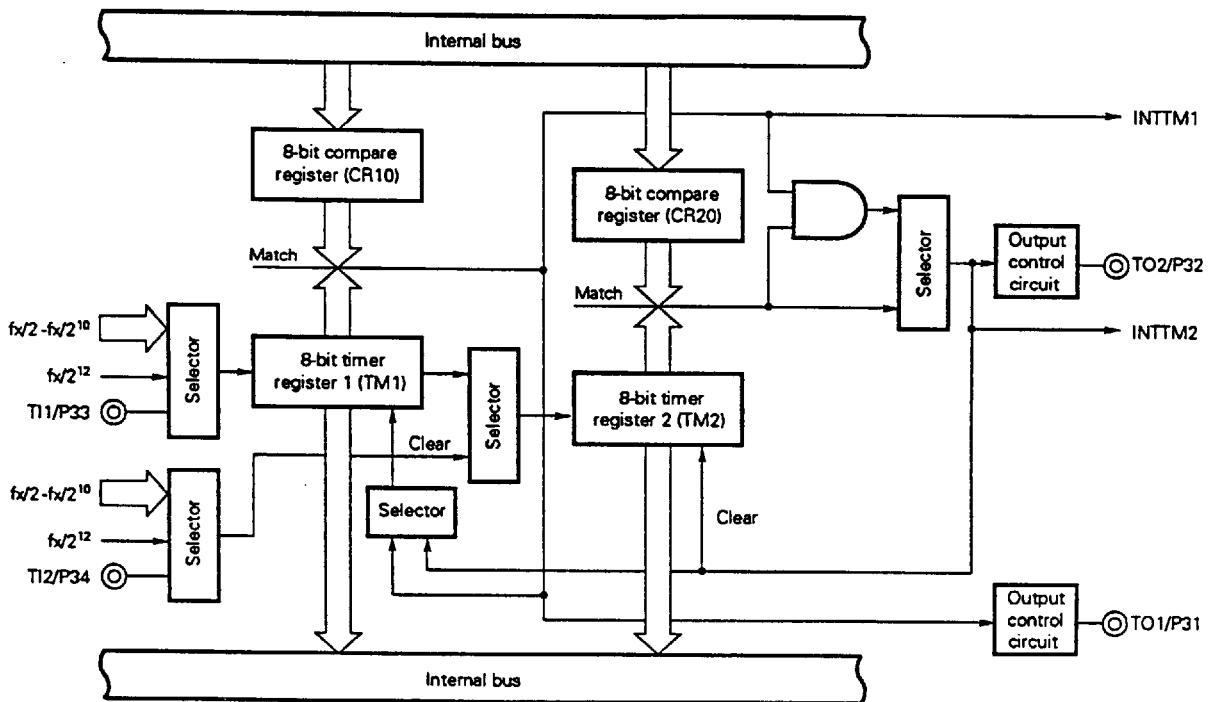


Fig. 5-4 Watch Timer Block Diagram

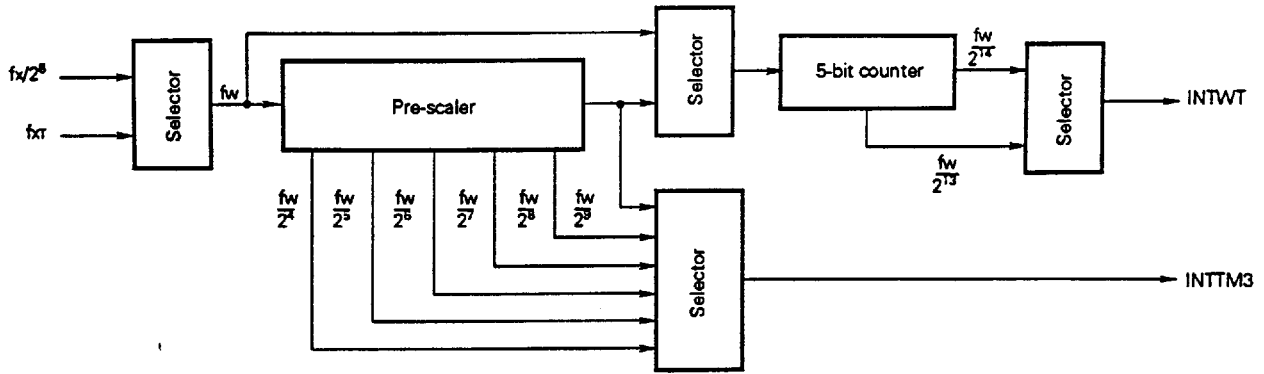


Fig. 5-5 Watchdog Timer Block Diagram

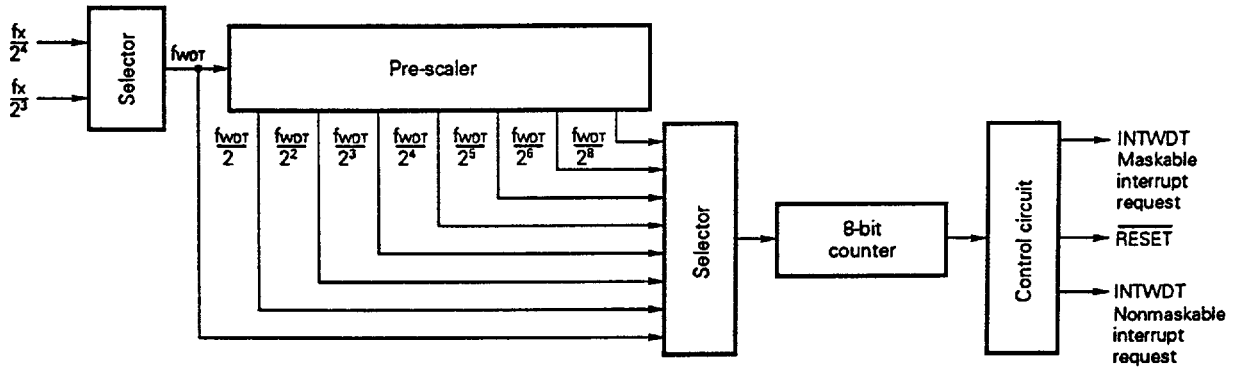
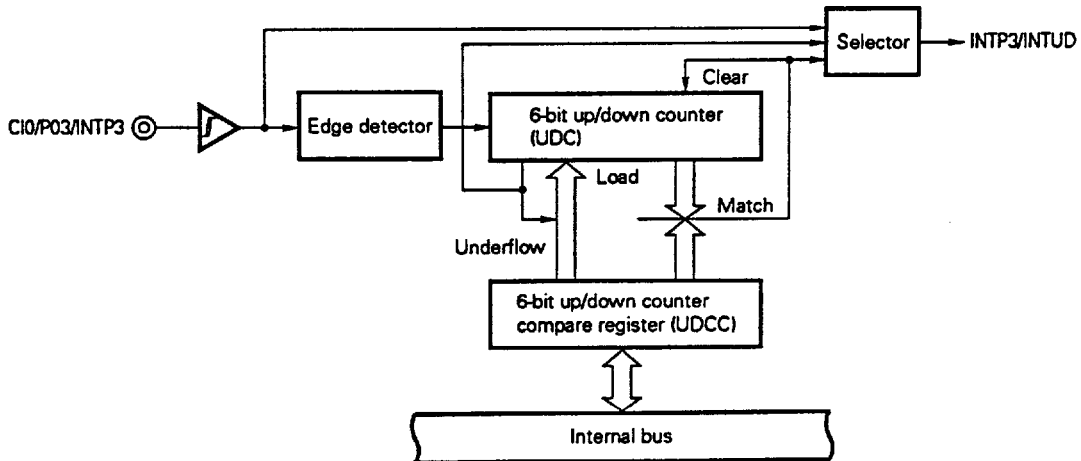


Fig. 5-6 6-Bit Up/Down Counter Block Diagram



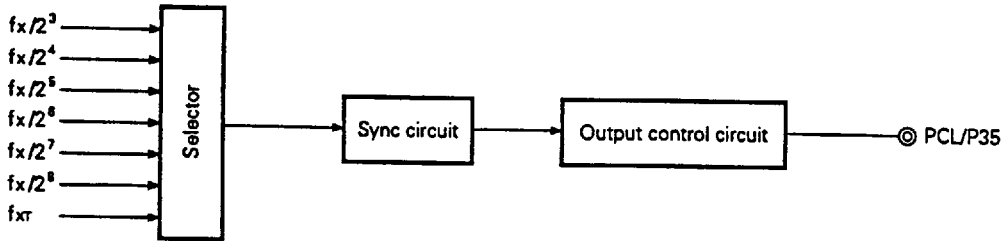
**Caution** When using the 6-bit up/down counter, set the CI0/P03/INTP3 pin in the input mode (set bit 3 of port mode register 0 (PM03) to 1).

**5.4 CLOCK OUTPUT CONTROL CIRCUIT**

Clocks of the following frequencies can be output to the clock:

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz (with main system clock: 5.0 MHz)
- 32.768 kHz (with subsystem clock: 32.768 kHz)

**Fig. 5-7 Clock Output Control Circuit Block Diagram**

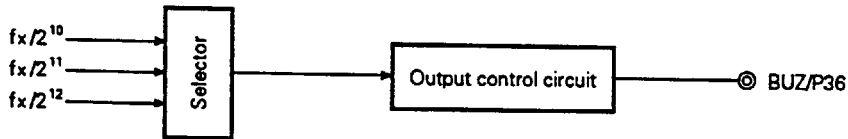


**5.5 BUZZER OUTPUT CONTROL CIRCUIT**

Clocks of the following frequencies can be output to the buzzer:

- 1.2 kHz/2.4 kHz/4.9 kHz (with main system clock: 5.0 MHz)

**Fig. 5-8 Buzzer Output Control Circuit Block Diagram**



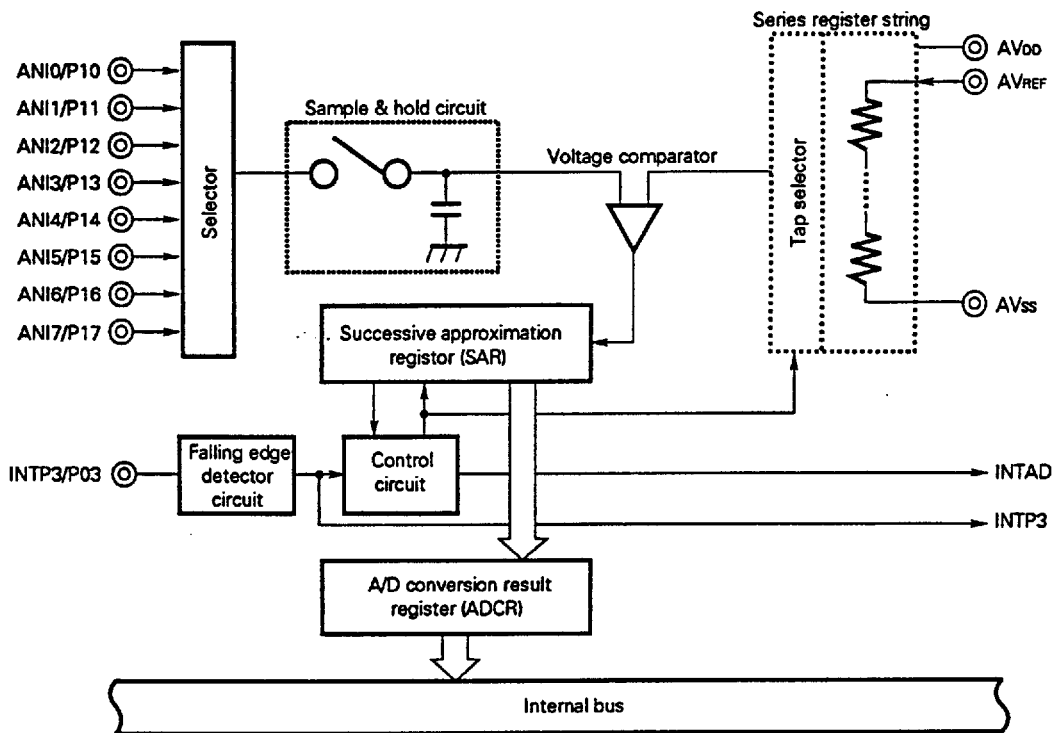
5.6 A/D CONVERTER

An 8-bit resolution 8-channel A/D converter is provided.

This A/D converter can be started in the following two modes:

- Hardware start
- Software start

Fig. 5-9 A/D Converter Block Diagram



5.7 SERIAL INTERFACE

Two channels of clocked serial interfaces are provided.

- Serial interface channel 0
- Serial interface channel 1

Table 5-3 Serial Interface Groups and Functions

Function	Serial interface channel 0	Serial interface channel 1
3-line serial I/O mode	• (MSB/LSB first selectable)	• (MSB/LSB first selectable)
SBI (serial bus interface) mode	• (MSB first)	—
2-line serial I/O mode	• (MSB first)	—
3-wire serial I/O mode with automatic transmission/reception function	—	• (MSB/LSB first selectable)

Fig. 5-10 Serial Interface Channel 0 Block Diagram

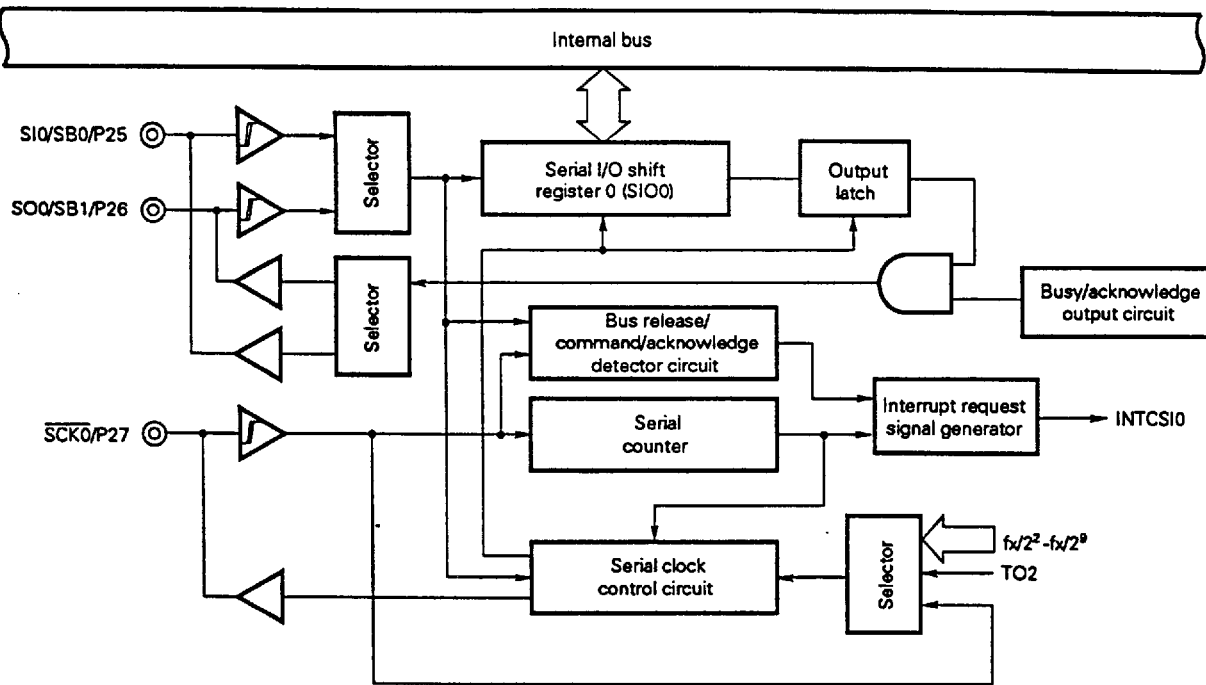
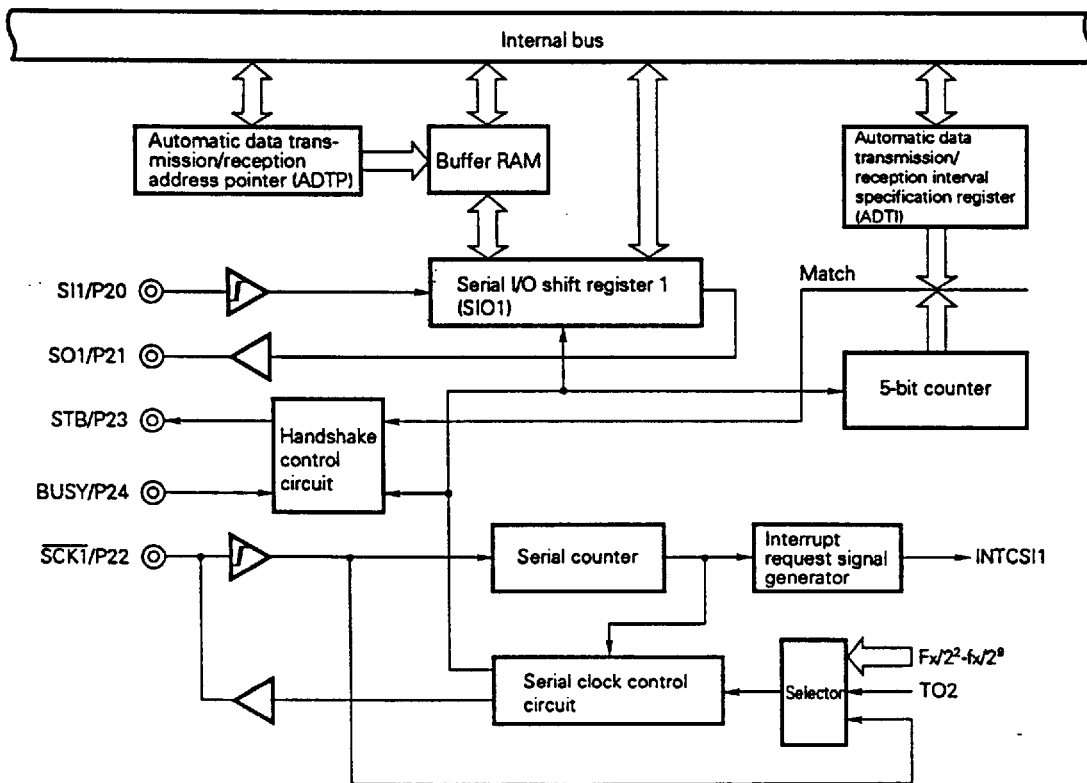


Fig. 5-11 Serial Interface Channel 1 Block Diagram

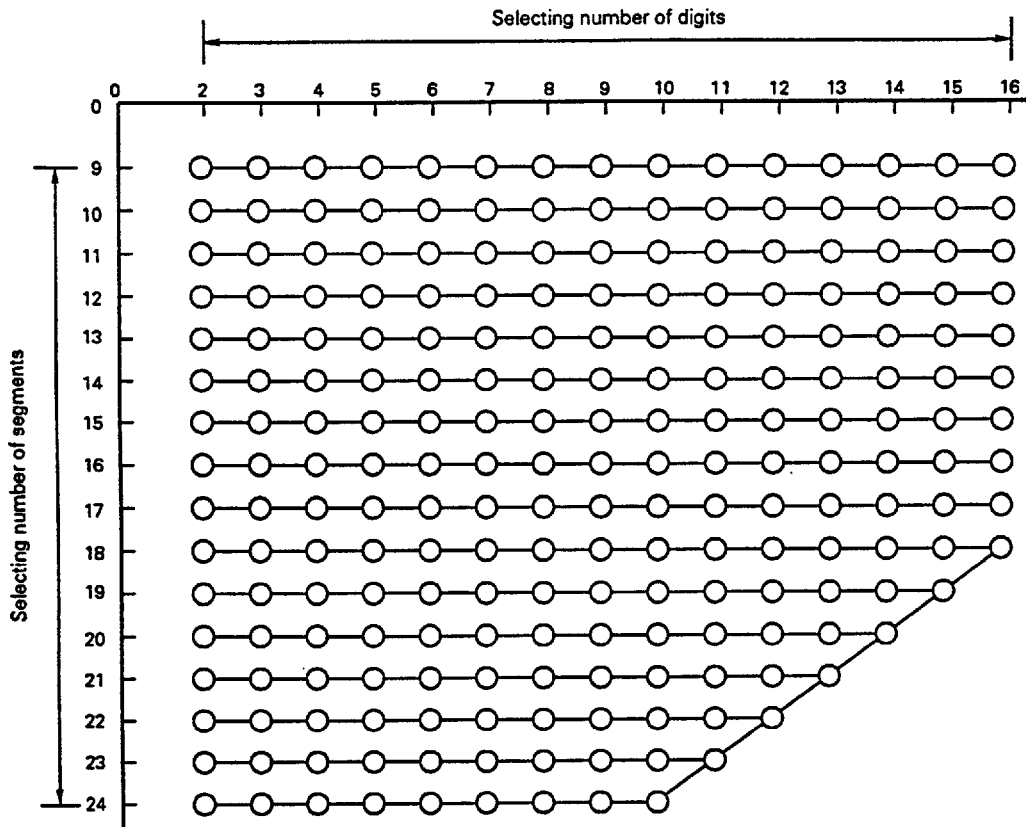


5.8 FIP CONTROLLER/DRIVER

An FIP controller/driver having the following features is provided:

- (a) Automatic output of segment signals (DMA operation) and digit signals by automatically reading display data
- (b) Display mode registers (DSPM0 and DSPM1) that can control an FIP of 9 to 24 segments and 2 to 16 digits
- (c) Port pins not used for FIP display can be used as output port or I/O port pins.
- (d) Display mode register (DSPM1) can adjust luminance in eight steps.
- (e) Hardware suitable for key scan application using segment pins
- (f) High-voltage output buffer (FIP driver) that can directly drive an FIP
- (g) Display output pins can be connected to a pull-down resistor by the mask option.

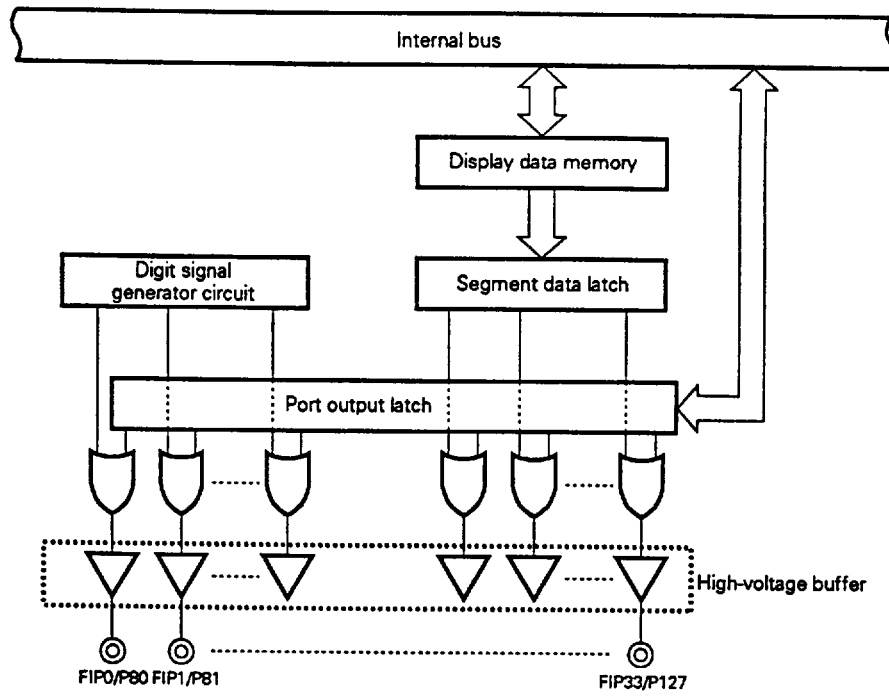
Fig. 5-12 Selecting Display Modes



**Caution** If the total number of digits and segments exceeds 34, the specified number of digits takes precedence.



Fig. 5-13 FIP Controller/Driver Block Diagram



6. INTERRUPT FUNCTION AND TEST FUNCTION

6.1 INTERRUPT FUNCTION

The following three types of interrupt functions are available:

- Non-maskable interrupt : 1
- Maskable interrupt : 13
- Software interrupt : 1

Table 6-1 Interrupt Source List

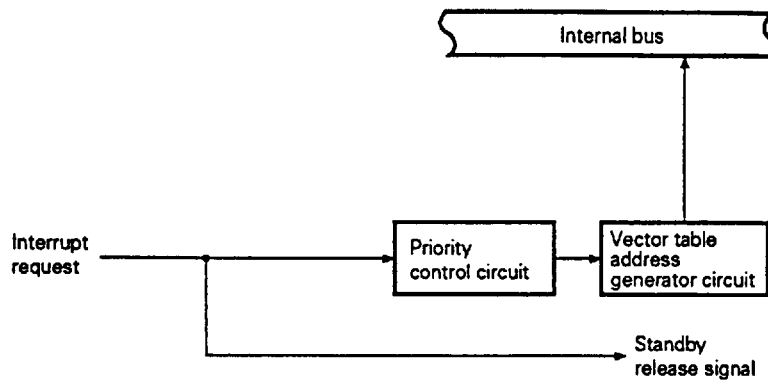
Interrupt type	Note 1 Default priority	Interrupt source		Internal/ external	Vector table address	Note 2 Basic configuration type	
		Name	Trigger				
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)	
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			External	0006H
	1	INTP0	Pin input edge detection	0008H	(D)		
	2	INTP1					
	3	INTP2					
	4	INTP3					
		4	INTUD	Up/down counter match signal generation	Internal	000CH	(B)
		5	INTCSI0	End of serial interface channel 0 transfer	Internal	000EH	(B)
		6	INTCSI1	End of serial interface channel 1 transfer		0010H	
		7	INTTM3	Reference time interval signal from watch timer		0012H	
		8	INTTM0	16-bit timer/event counter match signal generation		0014H	
		9	INTTM1	8-bit timer/event counter 1 match signal generation		0016H	
		10	INTTM2	8-bit timer/event counter 2 match signal generation		0018H	
		11	INTAD	End of A/D converter conversion		001AH	
	12	INTKS	Key scan timing from FIP controller/driver	001CH			
Software	—	BRK	Execution of BRK instruction	Internal	003EH	(E)	

Notes 1. Default priority is the priority order when several maskable interrupts are generated at the same time. 0 is the highest order and the 12 is the lowest order.

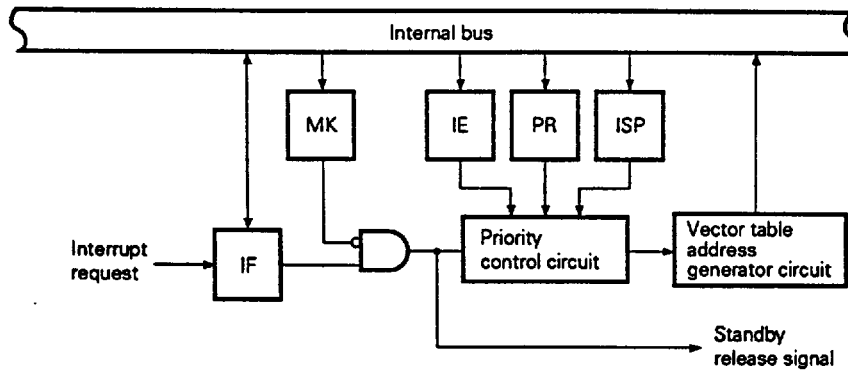
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Fig. 6-1.

Fig. 6-1 Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

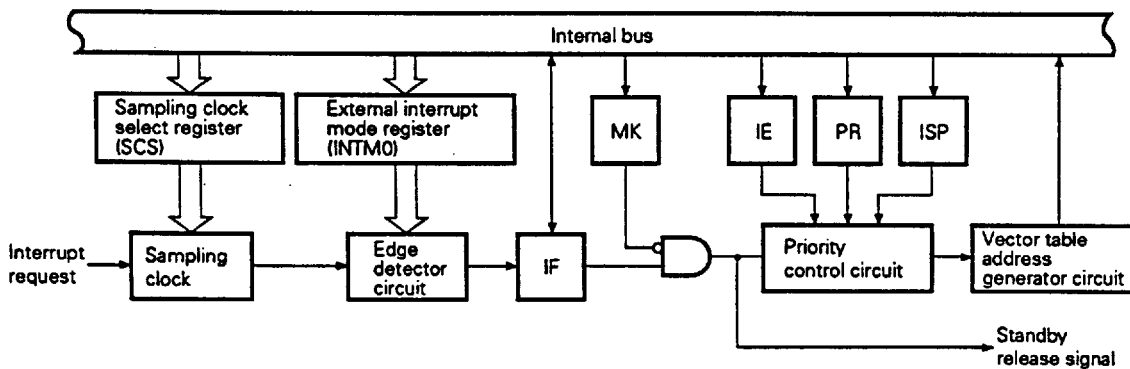
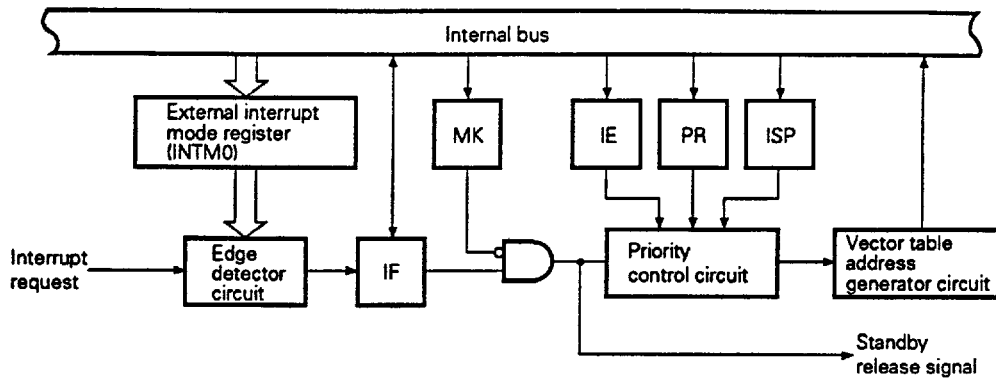
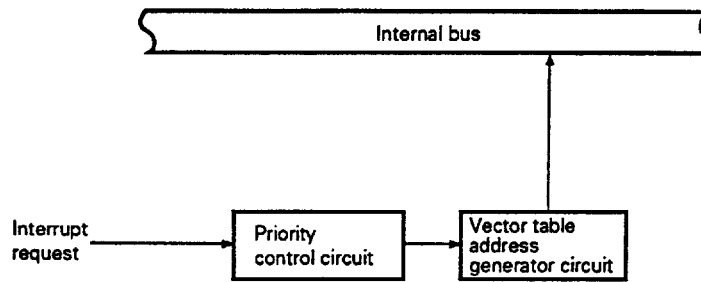


Fig. 6-1 Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



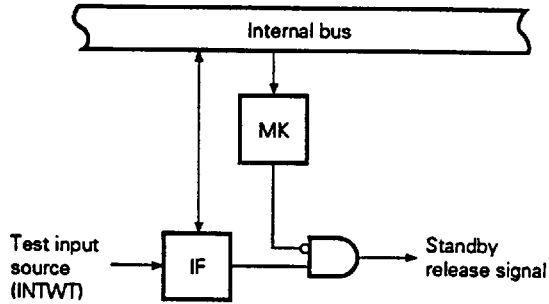
- IF : Interrupt request flag
- IE : Interrupt enable flag
- ISP : In-service priority flag
- MK : Interrupt mask flag
- PR : Priority specification flag

6.2 TEST FUNCTION

The following test function is available.

Test input source		Internal/external
Name	Trigger	
INTWT	Overflow of watch timer	Internal

Fig. 6-2 Basic Configuration of Test Function



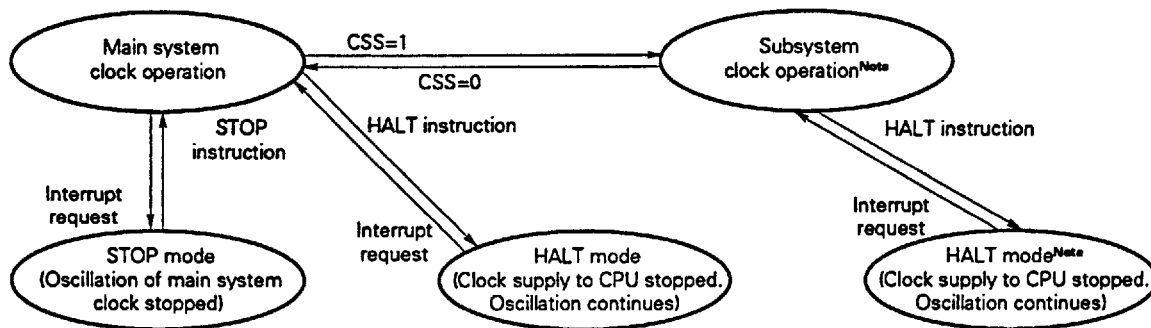
IF : Test request flag  
 MK : Test mask flag

### 7. STANDBY FUNCTION

The standby function is to reduce the current dissipation of the system and can be effected in the following two modes:

- **HALT mode:** In this mode, the operating clock of the CPU is stopped. By using this mode in combination with the normal operation mode, the system can be operated intermittently, so that the average current dissipation can be reduced.
- **STOP mode:** Oscillation of the main system clock is stopped. All the operations on the main system clock are stopped, and therefore, the current dissipation of the system can be minimized with only the subsystem clock oscillating.

Fig. 7-1 Standby Function



**Note** By stopping the main system clock, the current dissipation can be reduced. When the CPU operates on the subsystem clock, stop the main system clock by setting the MCC. The STOP instruction cannot be used.

**Caution** When the main system clock is stopped and the subsystem clock is operating, to switch again from the subsystem clock to the main system clock, allow sufficient time for the oscillation to settle before switching, by coding the program accordingly.

### 8. RESET FUNCTION

The system can be reset in the following two modes:

- External reset by **RESET** pin
- Internal reset by watchdog timer that detects hang up

9. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second operand / First operand	#byte	A	r <sup>Note</sup>	sfr	saddr	laddr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	Saddr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
rl											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
laddr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except for r=A

(2) 16-bit instruction

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second operand / First operand	#word	AX	rp <sup>Note</sup>	sfrp	saddrp	laddr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	<sup>Note</sup> MOVW						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
laddr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp=BC, DE, HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second operand / First operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	Saddr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1



**(4) Call/Branch instruction**

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second operand First operand	AX	laddr16	laddr11	[addr5]	Saddr16
Basic operation	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound operation					BT BF BTCLR DBNZ

**(5) Other instructions**

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)

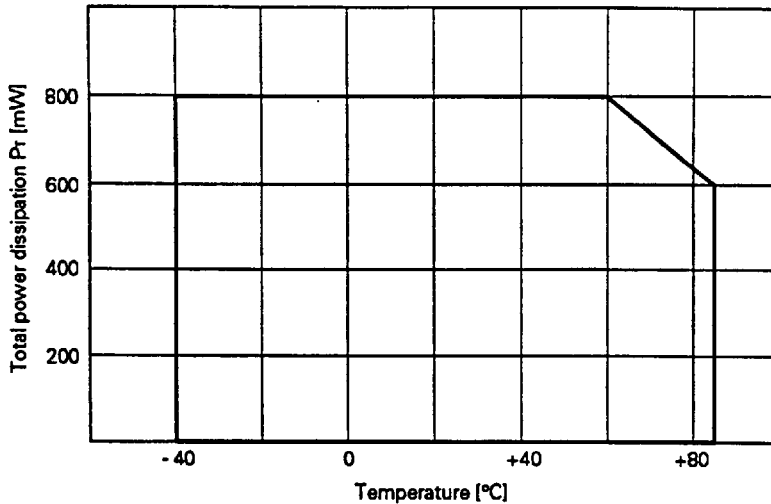
Parameter	Symbol	Conditions		Rating	Unit
Power supply voltage	V <sub>DD</sub>			-0.3 to +7.0	V
	V <sub>LOAD</sub>			V <sub>DD</sub> - 40 to V <sub>DD</sub> + 0.3	V
	AV <sub>DD</sub>			-0.3 to V <sub>DD</sub> + 0.3	V
	AV <sub>REF</sub>			-0.3 to V <sub>DD</sub> + 0.3	V
	AV <sub>SS</sub>			-0.3 to +0.3	V
Input voltage	V <sub>I1</sub>	P00-P04, P10-P17 (except when used as analog input pins), P20-P27, P30-P37, X1, X2, XT2, RESET		-0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>I2</sub>	P70-P74	N-ch open drain	-0.3 to +16 <sup>Note 1</sup>	V
	V <sub>I3</sub>	P110-P117, P120-P127	P-ch open drain	V <sub>DD</sub> - 40 to V <sub>DD</sub> + 0.3	V
Output voltage	V <sub>O1</sub>	P01-P03, P10-P17, P20-P27, P30-P37		-0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>O2</sub>	P70-P74		-0.3 to +16 <sup>Note 1</sup>	V
	V <sub>O3</sub>	P80, P81, P90-P97, P100-P107, P110-P117, P120-P127		V <sub>DD</sub> - 40 to V <sub>DD</sub> + 0.3	V
Analog input voltage	V <sub>AN</sub>	ANI0-ANI7	Analog input pin	AV <sub>SS</sub> - 0.3 to AV <sub>REF</sub> + 0.3	V
Output current, high	I <sub>OH</sub>	P01-P03, P10-P17, P20-P27, P30-P37 per pin		-10	mA
		P01-P03, P10-P17, P20-P27, P30-P37 total		-30	mA
		P80, P81, P90-P97, P100-P107, P110-P117, P120-P127 per pin		-30	mA
		P80, P81, P90-P97, P100-P107, P110-P117, P120-P127 total		-120	mA
Output current, low	I <sub>OL</sub>	P01-P03, P10-P17, P20-P27, P30-P37, P70-P74 per pin	Peak value	30	mA
			rms value	15 <sup>Note 2</sup>	mA
		P70-P74 total	Peak value	100	mA
			rms value	60 <sup>Note 2</sup>	mA
		P01-P03, P10-P17, P20-P27, P30-P37 total	Peak value	50	mA
			rms value	20 <sup>Note 2</sup>	mA
Total power dissipation	P <sub>T</sub> <sup>Note 3</sup>	T <sub>A</sub> = -40 to +60 °C		800	mW
				600	mW
Operating ambient temperature	T <sub>A</sub>			-40 to +85	°C
Storage temperature	T <sub>stg</sub>			-65 to +150	°C

**Caution** Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

**Remark** Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.

**Notes** 1. For pins to which pull-up resistors are connected by the mask option, the rating is -0.3 to V<sub>DD</sub> + 0.3.  
 2. To obtain the rms value, calculate [rms value] = [peak value] × √duty.

Notes 3. Permissible total power dissipation differs depending on the temperature (see the following figure).



**How to calculate total power dissipation**

The following three power dissipation are available for the μPD78042A, μPD78043A, μPD78044A and μPD78045A. The sum of the three power dissipation should be less than the total power dissipation Pr (80 % or less of ratings is recommended).

- ① CPU power dissipation: calculate  $V_{DD} (MAX.) \times I_{DD1} (MAX.)$ .
- ② Output pin power dissipation: Normal output and display output are available. Power dissipation when maximum current flows into each output pin is added.
- ③ Pull-down resistor power dissipation: Power dissipation by pull-down resistor connected to display output pin by the mask option.

**Example** 9 segments × 11 digits, 4LED outputs,  $V_{DD} = 5 V \pm 10 \%$ , 5.0 MHz oscillation  
 13 mA (MAX.) flows into segment pin and timing pin. 10 mA (MAX.) flows into LED output pin. The voltage of the FIP (voltage of  $V_{LOAD}$ ) is -30 V.  
 Other output power dissipation is considered to be small.

- ① CPU power dissipation :  $5.5 V \times 21.6 mA = 118.8 mW$
- ② Pin power dissipation : Segment pin .....  $2 V \times 13 mA \times 9 lines = 234 mW$   
 Timing pin .....  $2 V \times 13 mA = 26 mW$   
 LED output .....  $\left[ \frac{10}{15} \times 2 V \right] \times 10 mA \times 4 lines = 53.3 mW$
- ③ Pull-down resistor power dissipation:  $\left[ \frac{(30 + 5.5 V)^2}{25 k\Omega} \right] \times 7 lines = 352.9 mW$

The total power dissipation = ① + ② + ③ = 785 mW (< Pr = 800 mW)

In this example, if the temperature range is  $T_A = -40 \text{ °C}$  to  $+60 \text{ °C}$ , the permissible total power dissipation is 800 mW from the graph above, so there is no problem in power dissipation of 785 mW. However, when the total power dissipation exceeds the rating of the permissible total power dissipation, it is necessary to lower the power dissipation.

Lowering the power dissipation can be realized by reducing the number of internal pull-down resistors.

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 6.0 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note 1</sup>		1		5	MHz
		Oscillation stabilization time <sup>Note 2</sup>				4	ms
Crystal resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note 1</sup>		1	4.19	5	MHz
		Oscillation stabilization time <sup>Note 2</sup>	V <sub>DD</sub> = 4.5 to 6.0 V			10 30	ms
External clock		X1 input frequency (f <sub>x</sub> ) <sup>Note 1</sup>		1		5	MHz
		X1 input high, low-level width (t <sub>0H</sub> , t <sub>0L</sub> )		100		500	ns

Notes 1. It indicates only the oscillator characteristics. For the instruction execution time, see the AC Characteristics.

2. Time required until oscillation becomes stable after V<sub>DD</sub> is applied or the STOP mode is disabled.

Cautions 1. If the main system clock oscillator is to be used, wire the area inside the broken line square as follows to avoid influence of wiring capacitance:

- Make wiring as short as possible.
  - Do not cross other signal lines.
  - Do not get close to lines with fluctuating large current.
  - Make sure that the connecting points of the capacitor of the oscillator always have the same electric potential as V<sub>SS</sub>.
  - Do not connect the oscillator to a ground pattern that conducts a large current.
  - Do not take out signal from the oscillator.
2. When switching to the main system clock again after the subsystem clock has been used with the main system clock stopped, be sure to set the program to provide enough time for the oscillation to stabilize.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 6.0 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f <sub>XT</sub> ) <sup>Note 1</sup>		32	32.768	35	kHz
		Oscillation stabilization time <sup>Note 2</sup>	V <sub>DD</sub> = 4.5 to 6.0 V		1.2	2	s
External clock		XT1 input frequency (f <sub>XT</sub> ) <sup>Note 1</sup>		32		50	kHz
		XT1 input high, low-level width (t <sub>XTH</sub> , t <sub>XTL</sub> )		10		15	μs

Notes 1. It indicates only the oscillator characteristics. For the instruction execution time, see the AC Characteristics.

2. Time required until oscillation becomes stable after V<sub>DD</sub> reaching MIN. of oscillation voltage range.

Cautions 1. If the subsystem clock oscillator is to be used, wire the area inside the broken line square as follows to avoid influence of wiring capacitance:

- Make wiring as short as possible.
- Do not cross other signal lines.
- Do not get close to lines with fluctuating large current.
- Make sure that the connecting points of the capacitor of the oscillator always have the same electric potential as V<sub>SS</sub>.
- Do not connect the oscillator to a ground pattern that conducts a large current.
- Do not take out signal from the oscillator.

2. The subsystem clock oscillator is more likely to have malfunctions due to noise than the main system clock oscillator because gain for the subsystem clock oscillator is made lower to reduce current consumption. When using the subsystem clock, be careful about how to connect wires.

RECOMMENDED OSCILLATOR CONSTANT

Main system clock: Ceramic resonator (T<sub>A</sub> = -40 to +85 °C)

Manufacturer	Part number	Frequency (MHz)	Recommended circuit constant		Oscillation voltage range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg.	CSA5.00MG	5.00	30	30	2.7	6.0	
	CST5.00MGW	5.00	—	—	2.7	6.0	Capacitor contained
Matsushita Electronic Parts	EFOEN5004A (T)	5.00	33	33	2.7	6.0	
	EFOEC5004A	5.00	—	—	2.7	6.0	Capacitor contained

★  
★

Subsystem clock: Crystal (T<sub>A</sub> = -40 to +85 °C)

Manufacturer	Part number	Frequency (kHz)	Recommended circuit constant			Oscillation voltage range	
			C3 (pF)	C4 (pF)	R (kΩ)	MIN. (V)	MAX. (V)
Kyocera	KF-38G-12P0200	32.768	15	22	220	2.7	6.0

CAPACITANCE (T<sub>A</sub> = 25 °C, V<sub>DD</sub> = V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input capacitance	C <sub>IN</sub>	f = 1 MHz Unmeasured pins returned to 0 V			15	pF	
Output capacitance	C <sub>OUT</sub>	f = 1 MHz Unmeasured pins returned to 0 V			35	pF	
Input/output capacitance	C <sub>IO</sub>	f = 1 MHz Unmeasured pins returned to 0 V			15	pF	
							P01-P03, P10-P17, P20-P27, P30-P37
							P70-P74
					35	pF	
		P110-P117, P120-P127					

**Remark** Unless otherwise specified, the characteristics of the shared pin are the same as the characteristics of the port pin.

POWER SUPPLY VOLTAGE (T<sub>A</sub> = -40 to +85 °C)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
CPU <sup>Note 1</sup>		2.7 <sup>Note 2</sup>		6.0	V
Display controller		4.5		6.0	V
PWM mode of 16-bit timer/event counter (TM0)		4.5		6.0	V
A/D converter		4.0		6.0	V
Other hardware		2.7		6.0	V

**Notes 1.** Except for system clock oscillator, display controller, and PWM.

**2.** Operating power supply voltage range differs depending on the cycle time. See the AC Characteristics.

DC CHARACTERISTICS (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V <sub>IH1</sub>	P21, P23	0.7V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	P00-P03, P20, P22, P24-P27, P33, P34, RESET	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH3</sub>	P70-P74	N-ch open drain	0.7V <sub>DD</sub>	15 <sup>Note 1</sup>	V
	V <sub>IH4</sub>	X1, X2 <sup>Note 2</sup>		V <sub>DD</sub> - 0.5	V <sub>DD</sub>	V
	V <sub>IH5</sub>	XT1/P04, XT2 <sup>Note 2</sup>	V <sub>DD</sub> = 4.5 to 6.0 V	V <sub>DD</sub> - 0.5	V <sub>DD</sub>	V
				V <sub>DD</sub> - 0.3	V <sub>DD</sub>	V
	V <sub>IH6</sub>	P10-P17, P30-P32, P35-P37	V <sub>DD</sub> = 4.5 to 6.0 V	0.65V <sub>DD</sub>	V <sub>DD</sub>	V
			0.7V <sub>DD</sub>	V <sub>DD</sub>	V	
V <sub>IH7</sub>	P110-P117, P120-P127	V <sub>DD</sub> = 4.5 to 6.0 V	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	
			V <sub>DD</sub> - 0.5	V <sub>DD</sub>	V	
Low-level input voltage	V <sub>IL1</sub>	P21-P23	0		0.3V <sub>DD</sub>	V
	V <sub>IL2</sub>	P00-P03, P20, P22, P24-P27, P33, P34, RESET	0		0.2V <sub>DD</sub>	V
	V <sub>IL3</sub>	P70-P74	V <sub>DD</sub> = 4.5 to 6.0 V	0	0.3V <sub>DD</sub>	V
				0	0.2V <sub>DD</sub>	V
	V <sub>IL4</sub>	X1, X2 <sup>Note 2</sup>	0		0.4	V
	V <sub>IL5</sub>	XT1/P04, XT2 <sup>Note 2</sup>	V <sub>DD</sub> = 4.5 to 6.0 V	0	0.4	V
				0	0.3	V
V <sub>IL6</sub>	P10-P17, P30-P32, P35-P37	0		0.3V <sub>DD</sub>	V	
V <sub>IL7</sub>	P110-P117, P120-P127	V <sub>DD</sub> - 35		0.3V <sub>DD</sub>	V	
High-level output voltage	V <sub>OH</sub>	P01-P03, P10-P17, P20-P27, P30-P37, P80, P81, P90-P97, P100-P107, P110-P117, P120-P127	V <sub>DD</sub> = 4.5 to 6.0 V I <sub>OH</sub> = -1 mA		V <sub>DD</sub> - 1.0	V
			I <sub>OH</sub> = -100 μA		V <sub>DD</sub> - 0.5	V
Low-level output voltage	V <sub>OL1</sub>	P30-P37, P70-P74	V <sub>DD</sub> = 4.5 to 6.0 V, I <sub>OL</sub> = 15 mA	0.4	2.0	V
		P01-P03, P10-P17, P20-P27	V <sub>DD</sub> = 4.5 to 6.0 V, I <sub>OL</sub> = 1.6 mA		0.4	V
	V <sub>OL2</sub>	SB0, SB1, SCK0	V <sub>DD</sub> = 4.5 to 6.0 V, With open-drain and pull-up (R = 1 kΩ)		0.2V <sub>DD</sub>	V
	V <sub>OL3</sub>	P01-P03, P10-P17, P20-P27, P30-P37, P70-P74	I <sub>OL</sub> = 400 μA		0.5	V

- Notes 1. Pins to which pull-up resistors are connected by the mask option become V<sub>DD</sub>.  
 2. If the X1 pin is used for high-level voltage input, the X2 pin is used for low-level voltage input, or vice versa. This is also true for the XT1/P04 pin and XT2 pin.

Remark Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.

DC CHARACTERISTICS (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input leakage current	I <sub>LH1</sub>	V <sub>IN</sub> = V <sub>DD</sub>	P00-P03, P10-P17, P20-P27, P30-P37, RESET			3	μA
	I <sub>LH2</sub>		X1, X2, XT1/P04, XT2			20	μA
	I <sub>LH3</sub>	V <sub>IN</sub> = 15 V	P70-P74			80	μA
	I <sub>LH4</sub>	P110-P117, P120-P127, V <sub>IN</sub> = V <sub>DD</sub>	V <sub>DD</sub> = 4.5 to 6.0 V			3 <sup>Note 1</sup>	μA
					3 <sup>Note 2</sup>	μA	
Low-level input leakage current	I <sub>L1</sub>	V <sub>IN</sub> = 0 V	P00-P03, P10-P17, P20-P27, P30-P37, RESET			-3	μA
	I <sub>L12</sub>		X1, X2, XT1/P04, XT2			-20	μA
	I <sub>L13</sub>		P70-P74			-3 <sup>Note 3</sup>	μA
	I <sub>L14</sub>		P110-P117, P120-P127			-10	μA
★ High-level output leakage current <sup>Note 4</sup>	I <sub>LOH1</sub>	V <sub>OUT</sub> = V <sub>DD</sub>	P01-P03, P10-P17, P20-P27, P30-P37, P80, P81, P90-P97, P100-P107, P110-P117, P120-P127			3	μA
	I <sub>LOH2</sub>	V <sub>OUT</sub> = 15 V	P70-74, N-ch open drain			80	μA
★ Low-level output leakage current <sup>Note 4</sup>	I <sub>LOL1</sub>	V <sub>OUT</sub> = 0 V	P01-P03, P10-P17, P20-P27, P30-P37, P70-P74			-3	μA
	I <sub>LOL2</sub>	V <sub>OUT</sub> = V <sub>LOAD</sub> = V <sub>DD</sub> - 35 V	P80, P81, P90-P97, P100-107, P110-P117, P120-P127			-10	μA
Display output current	I <sub>OO</sub>	V <sub>DD</sub> = 4.5 to 6.0 V, V <sub>CS</sub> - V <sub>DD</sub> - 2 V		-13	-18		mA
Mask option pull-up resistor	R <sub>1</sub>	V <sub>IN</sub> = 0 V, P70-P74		20	40	90	kΩ
Software pull-up resistor	R <sub>2</sub>	V <sub>IN</sub> = 0 V P01-P03, P10-P17, P20-P27, P30-P37	V <sub>DD</sub> = 4.5 to 6.0 V	15	40	90	kΩ
				20		500	kΩ
Mask option pull-down resistor	R <sub>3</sub>	P80, P81, P90-P97, P100-P107, P110-P117, P120-P127	V <sub>CS</sub> - V <sub>LOAD</sub> = 35 V	25	70	135	kΩ
			V <sub>CS</sub> - V <sub>SS</sub> = 5 V	20	55	100	kΩ
	R <sub>4</sub>	P30-P37, V <sub>IN</sub> = V <sub>DD</sub>	40	80	150	kΩ	

- Notes**
1. The maximum value is 50 μA for only 1.5 clocks (PCC = 00H) during the read instruction execution of ports 11 and 12 (P11, P12). Otherwise, it is 3 μA.
  2. The maximum value is 30 μA for only 1.5 clocks (PCC = 00H) during the read instruction execution of ports 11 and 12 (P11, P12). Otherwise, it is 3 μA.
  3. The maximum value is -150 μA for only 1.5 clocks (PCC = 00H) during the read instruction execution of port 7 (P7). Otherwise, it is -3 μA.
  4. Current which flows in the built-in pull-up or pull-down resistor is not included.

**Remark** Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.



DC CHARACTERISTICS (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply current <sup>Note 1</sup>	I <sub>DD1</sub>	5.0 MHz crystal oscillation Operating mode	V <sub>DD</sub> = 5.0 V ±10% <sup>Note 2</sup>	7.2	21.6	mA
			V <sub>DD</sub> = 3.0 V ±10% <sup>Note 3</sup>	0.9	2.7	mA
	I <sub>DD2</sub>	5.0 MHz crystal oscillation HALT mode	V <sub>DD</sub> = 5.0 V ±10%	1.3	3.9	mA
			V <sub>DD</sub> = 3.0 V ±10%	550	1650	μA
	I <sub>DD3</sub>	32.768 kHz crystal oscillation Operating mode <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V ±10%	60	120	μA
			V <sub>DD</sub> = 3.0 V ±10%	35	70	μA
	I <sub>DD4</sub>	32.768 kHz crystal oscillation HALT mode <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V ±10%	25	50	μA
			V <sub>DD</sub> = 3.0 V ±10%	5	10	μA
I <sub>DD5</sub>	XT1 = 0 V STOP mode Feedback resistor connected	V <sub>DD</sub> = 5.0 V ±10%	1	20	μA	
		V <sub>DD</sub> = 3.0 V ±10%	0.5	10	μA	
I <sub>DD6</sub>	XT1 = 0 V STOP mode Feedback resistor not connected	V <sub>DD</sub> = 5.0 V ±10%	0.1	20	μA	
		V <sub>DD</sub> = 3.0 V ±10%	0.05	10	μA	

Notes 1. This current excludes the AV<sub>REF</sub> current, port current, and current which flows in the built-in pull-down resistor (mask option).

2. When operating at high-speed mode (when the processor clock control register is set to 00H)

3. When operating at low-speed mode (when the processor clock control register is set to 04H)

4. When the main system clock is stopped

AC CHARACTERISTICS

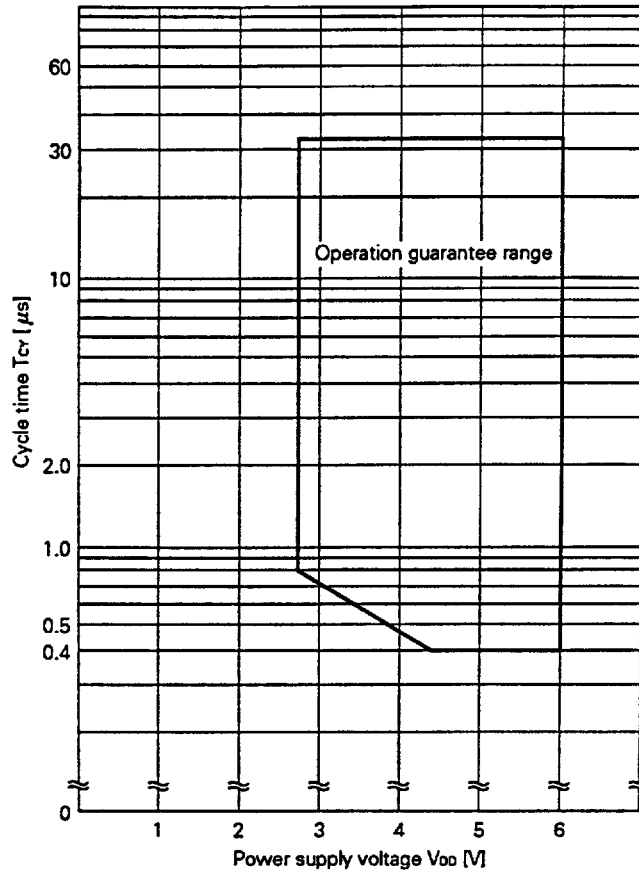
(1) Basic operation (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T <sub>CY</sub>	Operated with main system clock	V <sub>DD</sub> = 4.5 to 6.0 V	0.4	32	μs
				0.8	32	μs
		Operated with subsystem clock	80 <sup>Note 1</sup>	122	125	μs
Tl1, 2 input frequency	f <sub>TI</sub>	V <sub>DD</sub> = 4.5 to 6.0 V	0		2	MHz
			0		138	kHz
Tl1, 2 input high, low-level width	t <sub>TH</sub>	V <sub>DD</sub> = 4.5 to 6.0 V	250			ns
	t <sub>TL</sub>		3.6			μs
Interrupt input high, low-level width	t <sub>INTH</sub>	INTP0	8/f <sub>imm</sub> <sup>Note 2</sup>			μs
	t <sub>INTL</sub>		INTP1-INTP3	10		
RESET low-level width	t <sub>RBL</sub>		10			μs

Notes 1. Value when external clock input is used as subsystem clock. When crystal is used, the value becomes 114 μs.

2. Selection of f<sub>imm</sub> = f<sub>x</sub>/2<sup>N+1</sup>, f<sub>x</sub>/64, f<sub>x</sub>/128 is available (N = 0 to 4) by bits 0 and 1 of sampling clock select register (SCS0, SCS1).

T<sub>cy</sub> vs V<sub>DD</sub> (with main system clock operated)



(2) Serial interface (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 6.0 V)

(a) Three-wire serial I/O mode ( $\overline{\text{SCK}}$ : Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t <sub>KCY1</sub>	V <sub>DD</sub> = 4.5 to 6.0 V	800			ns
			3200			ns
$\overline{\text{SCK}}$ high, low-level width	t <sub>KH1</sub> t <sub>KL1</sub>	V <sub>DD</sub> = 4.5 to 6.0 V	t <sub>KCY1</sub> /2 - 50			ns
			t <sub>KCY1</sub> /2 - 150			ns
SI setup time to $\overline{\text{SCK}}\uparrow$	t <sub>SK1</sub>		100			ns
SI hold time from $\overline{\text{SCK}}\uparrow$	t <sub>SH1</sub>		400			ns
$\overline{\text{SCK}}\downarrow \rightarrow \text{SO}$ output delay time	t <sub>KSO1</sub>	C = 100 pF <sup>Note</sup>	V <sub>DD</sub> = 4.5 to 6.0 V		300	ns
					1000	ns

Note C is a load capacitance of the  $\overline{\text{SCK}}$  or SO output line.

(b) Three-wire serial I/O mode ( $\overline{\text{SCK}}$ : External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY2}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		800			ns
				3200			ns
$\overline{\text{SCK}}$ high, low-level width	$t_{\text{KH2}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		400			ns
	$t_{\text{KL2}}$			1600			ns
SI setup time to $\overline{\text{SCK}}\uparrow$	$t_{\text{SIK2}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		100			ns
SI hold time from $\overline{\text{SCK}}\uparrow$	$t_{\text{KH2}}$			400			ns
$\overline{\text{SCK}}\downarrow \rightarrow \text{SO}$ output delay time	$t_{\text{KSO2}}$	$C = 100 \text{ pF}^{\text{Note}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$			300	ns
						1000	ns
$\overline{\text{SCK}}$ rise time and fall time	$t_{\text{r2}}$					160	ns
	$t_{\text{f2}}$						ns

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Note C is a load capacitance of the SO output line.

(c) SBI mode ( $\overline{\text{SCK}}$ : Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY3}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		800			ns
				3200			ns
$\overline{\text{SCK}}$ high, low-level width	$t_{\text{KH3}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		$t_{\text{KCY3}}/2-50$			ns
	$t_{\text{KL3}}$			$t_{\text{KCY3}}/2-150$			ns
SB0, SB1 setup time to $\overline{\text{SCK}}\uparrow$	$t_{\text{SIK3}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		100			ns
				300			ns
SB0, SB1 hold time from $\overline{\text{SCK}}\uparrow$	$t_{\text{KH3}}$			$t_{\text{KCY3}}/2$			ns
$\overline{\text{SCK}}\downarrow \rightarrow \text{SB0, SB1}$ output delay time	$t_{\text{KSO3}}$	$R = 1 \text{ k}\Omega, C = 100 \text{ pF}^{\text{Note}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	0		250	ns
				0		1000	ns
$\overline{\text{SCK}}\uparrow \rightarrow \text{SB0, SB1}\downarrow$	$t_{\text{KSH}}$			$t_{\text{KCY3}}$			ns
SB0, SB1 $\downarrow \rightarrow \overline{\text{SCK}}\downarrow$	$t_{\text{SKK}}$			$t_{\text{KCY3}}$			ns
SB0, SB1 high-level width	$t_{\text{SHH}}$			$t_{\text{KCY3}}$			ns
SB0, SB1 low-level width	$t_{\text{SHL}}$			$t_{\text{KCY3}}$			ns

Note R is a load resistance of the  $\overline{\text{SCK}}$ , SB0, or SB1 output line, and C is its load capacitance.

(d) SBI mode ( $\overline{\text{SCK}}$ : External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY4}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	800			ns	
			3200			ns	
$\overline{\text{SCK}}$ high, low- level width	$t_{\text{KH4}}$ $t_{\text{KL4}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	400			ns	
			1600			ns	
SB0, SB1 setup time to $\overline{\text{SCK}}\uparrow$	$t_{\text{SK4}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	100			ns	
			300			ns	
SB0, SB1 hold time from $\overline{\text{SCK}}\uparrow$	$t_{\text{KH4}}$		$t_{\text{KCY4}}/2$			ns	
$\overline{\text{SCK}}\downarrow \rightarrow$ SB0, SB1 output delay time	$t_{\text{KS04}}$	$R = 1 \text{ k}\Omega, C = 100 \text{ pF}$ <sup>Note</sup>	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	0		300	ns
				0		1000	ns
$\overline{\text{SCK}}\uparrow \rightarrow$ SB0, SB1 $\downarrow$	$t_{\text{KS8}}$		$t_{\text{KCY4}}$			ns	
SB0, SB1 $\downarrow \rightarrow \overline{\text{SCK}}\downarrow$	$t_{\text{SK8}}$		$t_{\text{KCY4}}$			ns	
SB0, SB1 high- level width	$t_{\text{SH4}}$		$t_{\text{KCY4}}$			ns	
SB0, SB1 low-level width	$t_{\text{SL4}}$		$t_{\text{KCY4}}$			ns	
$\overline{\text{SCK}}$ rise time and fall time	$t_{\text{R4}}$ $t_{\text{F4}}$				160	ns	

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Note R is a load resistance of the SB0 or SB1 output line, and C is its load capacitance.

(e) Two-wire serial I/O mode ( $\overline{\text{SCK}}$ : Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY5}}$	$R = 1 \text{ k}\Omega, C = 100 \text{ pF}$ <sup>Note</sup>	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	1600			ns
				3800			ns
$\overline{\text{SCK}}$ high-level width	$t_{\text{KH5}}$		$t_{\text{KCY5}}/2 - 160$			ns	
$\overline{\text{SCK}}$ low- level width	$t_{\text{KL5}}$		$t_{\text{KCY5}}/2 - 50$			ns	
SB0, SB1 setup time to $\overline{\text{SCK}}\uparrow$	$t_{\text{SK5}}$		300			ns	
SB0, SB1 hold time from $\overline{\text{SCK}}\uparrow$	$t_{\text{KH5}}$		600			ns	
$\overline{\text{SCK}}\downarrow \rightarrow$ SB0, SB1 output delay time	$t_{\text{KS05}}$	$R = 1 \text{ k}\Omega, C = 100 \text{ pF}$ <sup>Note</sup>	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	0		250	ns
				0		1000	ns

Note R is a load resistance of the  $\overline{\text{SCK}}$ , SB0, or SB1 output line, and C is its load capacitance.

(f) Two-wire serial I/O mode ( $\overline{\text{SCK}}$ : External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY6}}$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	1600			ns	
			3800			ns	
$\overline{\text{SCK}}$ high-level width	$t_{\text{KH6}}$		650			ns	
$\overline{\text{SCK}}$ low- level width	$t_{\text{KL6}}$		800			ns	
SB0, SB1 setup time to $\overline{\text{SCK}}\uparrow$	$t_{\text{SK6}}$		100			ns	
SB0, SB1 hold time from $\overline{\text{SCK}}\uparrow$	$t_{\text{KH6}}$		$t_{\text{KCY6}}/2$			ns	
$\overline{\text{SCK}}\downarrow \rightarrow$ SB0, SB1 output delay time	$t_{\text{KS06}}$	$R = 1 \text{ k}\Omega, C = 100 \text{ pF}$ <sup>Note</sup>	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	0		300	ns
				0		1000	ns
$\overline{\text{SCK}}$ rise time and fall time	$t_{\text{R6}}$ $t_{\text{F6}}$				160	ns	

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Note R is a load resistance of the SB0 or SB1 output line, and C is its load capacitance.

(g) 3-wire serial I/O mode with automatic transmission/reception function ( $\overline{SCK}$ : internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	$t_{KCY7}$	$V_{DD} = 4.5 \text{ to } 6.0 \text{ V}$	800			ns
			3200			ns
$\overline{SCK}$ high, low-level width	$t_{KH7}$	$V_{DD} = 4.5 \text{ to } 6.0 \text{ V}$	$t_{KCY7}/2-50$			ns
	$t_{KL7}$		$t_{KCY7}/2-150$			ns
SI setup time to $\overline{SCK}\uparrow$	$t_{SIK7}$		100			ns
SI hold time from $\overline{SCK}\uparrow$	$t_{KSH7}$		400			ns
$\overline{SCK}\downarrow \rightarrow$ SO output delay time	$t_{KS07}$	C = 100 pF <sup>Note</sup>	$V_{DD} = 4.5 \text{ to } 6.0 \text{ V}$		300	ns
					1000	ns
$\overline{SCK}\uparrow \rightarrow$ STB $\uparrow$	$t_{SS0}$		$t_{KCY7}/2-100$		$t_{KCY7}/2+100$	ns
Strobe signal high level width	$t_{SSW}$		$t_{KCY7}-30$		$t_{KCY7}+30$	ns
Busy signal setup time (to busy signal detection timing)	$t_{BS}$		100			ns
Busy signal hold time (to busy signal detection timing)	$t_{BSH}$		100			ns
Busy inactive $\rightarrow \overline{SCK}\downarrow$	$t_{SPS}$				$2t_{KCY7}$	ns

Note C is a load capacitance of the  $\overline{SCK}$  or SO output line.

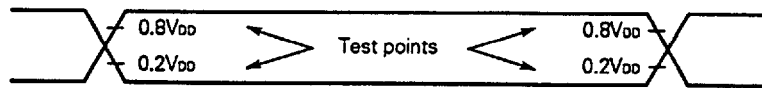
(h) 3-wire serial I/O mode with automatic transmission/reception function ( $\overline{SCK}$ : external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	$t_{KCY6}$	$V_{DD} = 4.5 \text{ to } 6.0 \text{ V}$	800			ns
			3200			ns
$\overline{SCK}$ high, low-level width	$t_{KH6}$	$V_{DD} = 4.5 \text{ to } 6.0 \text{ V}$	400			ns
	$t_{KL6}$		1600			ns
SI setup time to $\overline{SCK}\uparrow$	$t_{SIS6}$		100			ns
SI hold time from $\overline{SCK}\uparrow$	$t_{KSH6}$		400			ns
$\overline{SCK}\downarrow \rightarrow$ SO output delay time	$t_{KS06}$	C = 100 pF <sup>Note</sup>	$V_{DD} = 4.5 \text{ to } 6.0 \text{ V}$		300	ns
					1000	ns
$\overline{SCK}$ rise time and fall time	$t_{rs}$				160	ns
	$t_{rf}$				160	ns

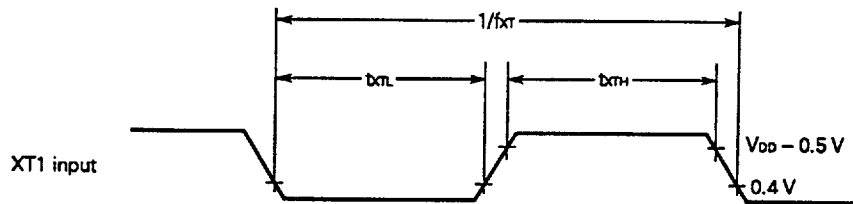
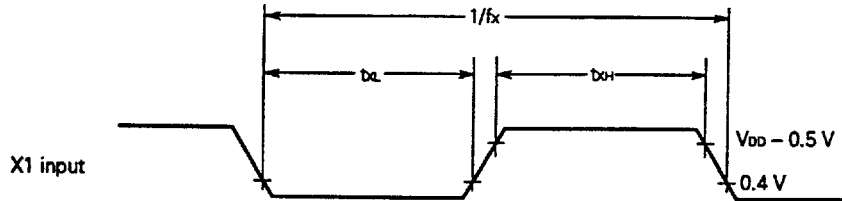
Note C is a load capacitance of the SO output line.

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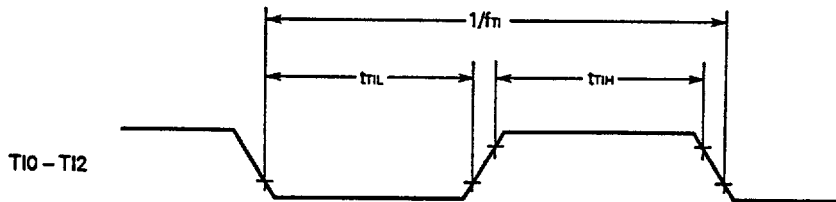
AC timing test points (except X1, XT1 input)



Clock timing

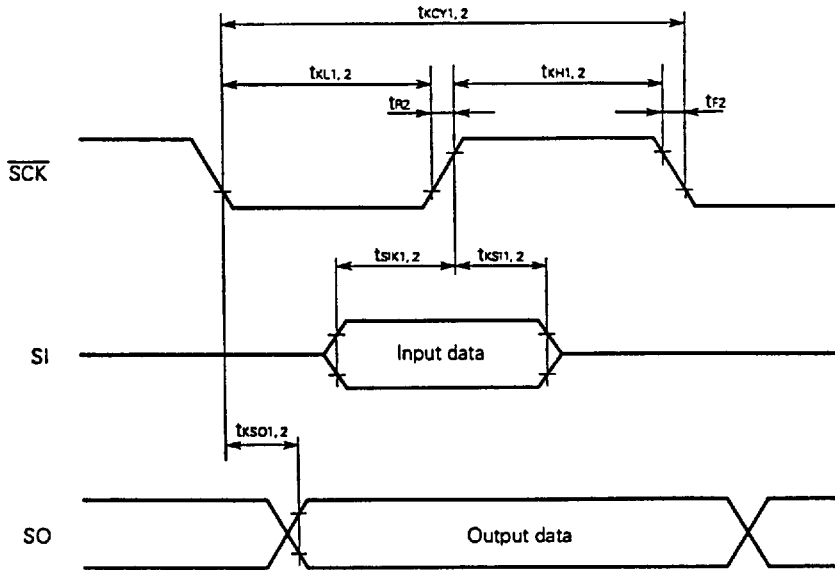


T1 timing



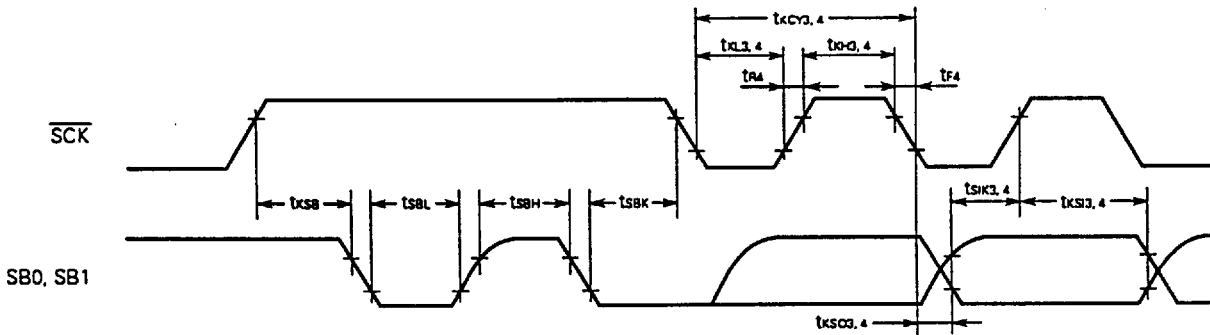
Serial transfer timing

3-wire serial I/O mode:



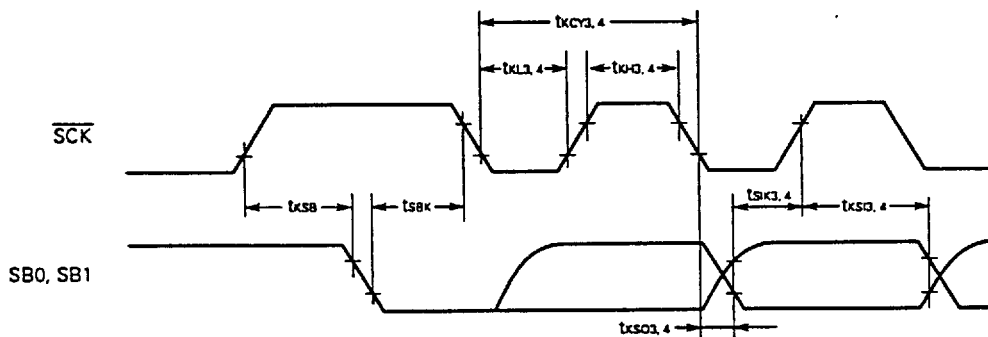
★

SBI mode (bus release signal transfer):

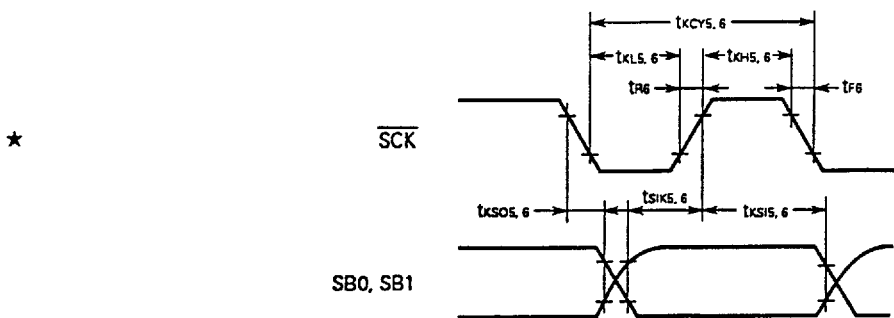


★

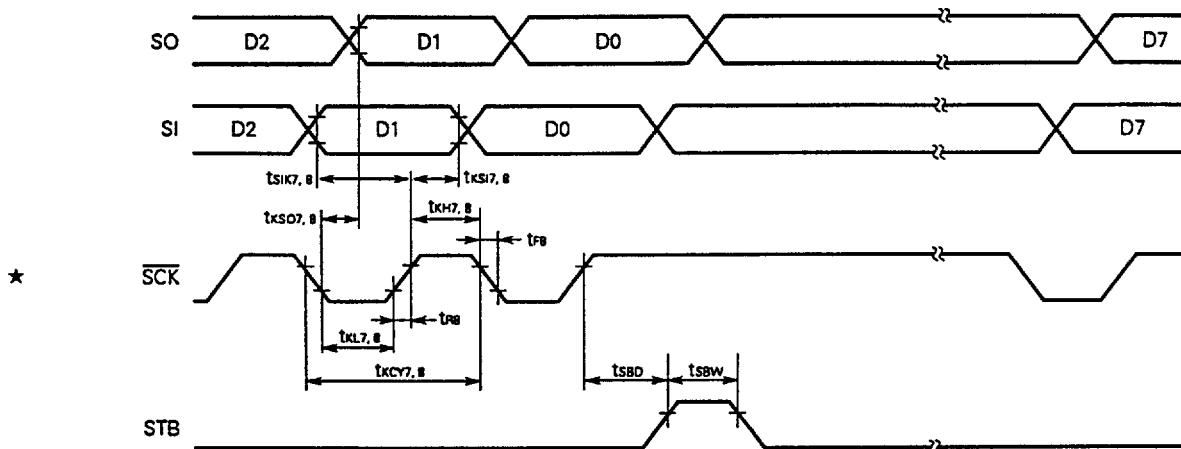
SBI mode (command signal transfer):



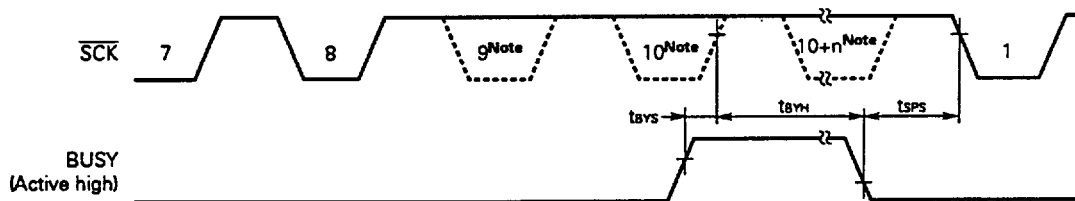
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmission/reception function:



3-wire serial I/O mode with automatic transmission/reception function (busy processing):



Note  $\overline{\text{SCK}}$  does not become low actually at this point, but is indicated so to conform to the timing specification.



A/D Converter Characteristics (T<sub>A</sub> = -40 to +85 °C, AV<sub>DD</sub> = V<sub>DD</sub> = 4.0 to 6.0 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error <sup>Note 1</sup>					0.8	%
Conversion time <sup>Note 2</sup>	t <sub>CONV</sub>	1 MHz ≤ f <sub>x</sub> ≤ 5.0 MHz	19.1		200	μs
Sampling time <sup>Note 3</sup>	t <sub>SAMP</sub>		2.86		30	μs
Analog signal input voltage	V <sub>IAN</sub>		AV <sub>SS</sub>		AV <sub>REF</sub>	V
Reference voltage	AV <sub>REF</sub>		4.0		AV <sub>DD</sub>	V
AV <sub>REF</sub> resistor	R <sub>AVREF</sub>		4	14		kΩ
AV <sub>DD</sub> current	I <sub>DD</sub>			200	400	μA

Notes 1. Quantization error (±1/2LSB) is not included. This parameter is indicated as the ratio to the full-scale value.

2. Set the A/D conversion time to 19.1 μs or more.

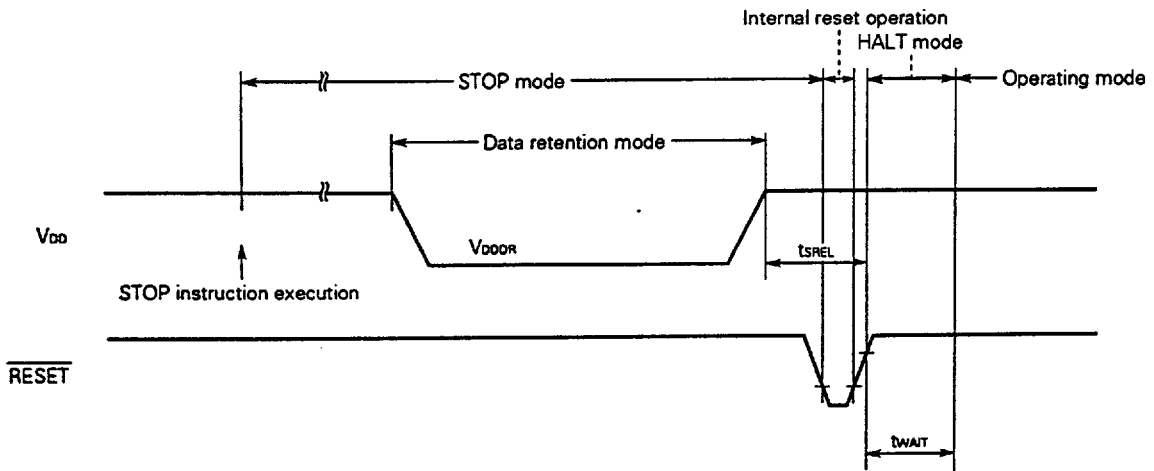
3. Sampling time depends on the conversion time.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T<sub>A</sub> = -40 to +85 °C)

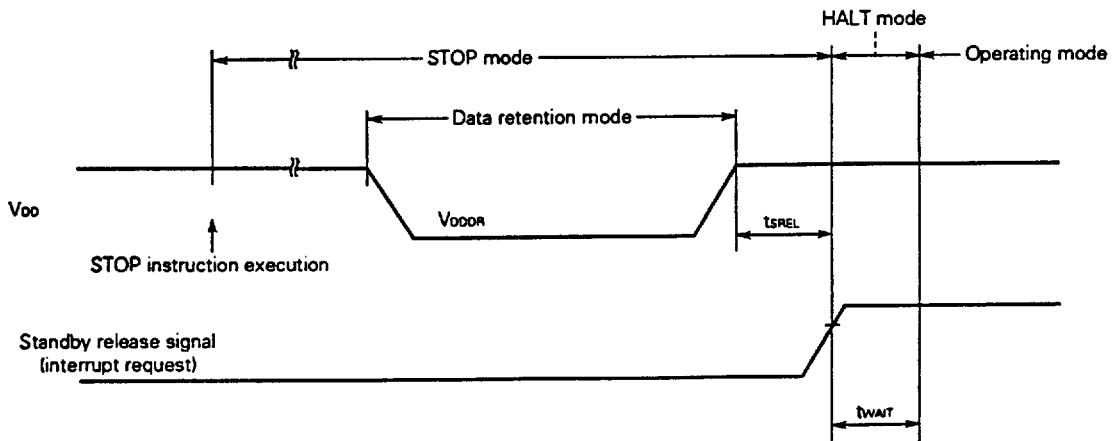
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V <sub>DDDR</sub>		2.0		6.0	V
Data retention supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 2.0 V Subsystem clock stopped, Feedback resistor not connected		0.1	10	μA
Release signal set time	t <sub>SREL</sub>		0			μs
Oscillation stabilization wait time	t <sub>WAIT</sub>	Release by $\overline{\text{RESET}}$		2 <sup>17</sup> /f <sub>x</sub>		ms
		Release by interrupt		Note		ms

Note Selection of 2<sup>12</sup>/f<sub>x</sub>, 2<sup>14</sup>/f<sub>x</sub> to 2<sup>17</sup>/f<sub>x</sub> is available by bits 0 to 2 of oscillation stabilization time select register (OSTS0 to OSTS2).

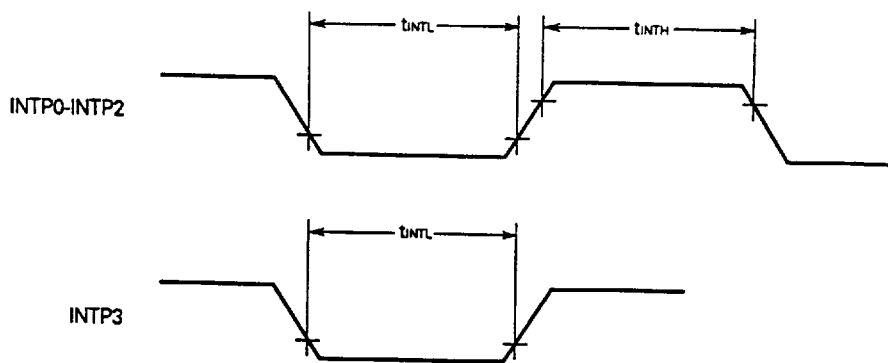
Data retention timing (STOP mode release by  $\overline{\text{RESET}}$ )



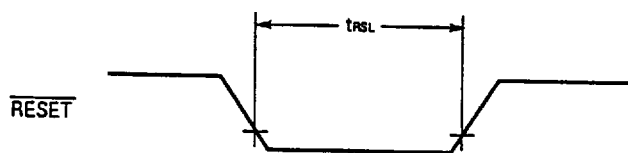
Data retention timing (standby release signal: STOP mode release by interrupt signal)



Interrupt input timing



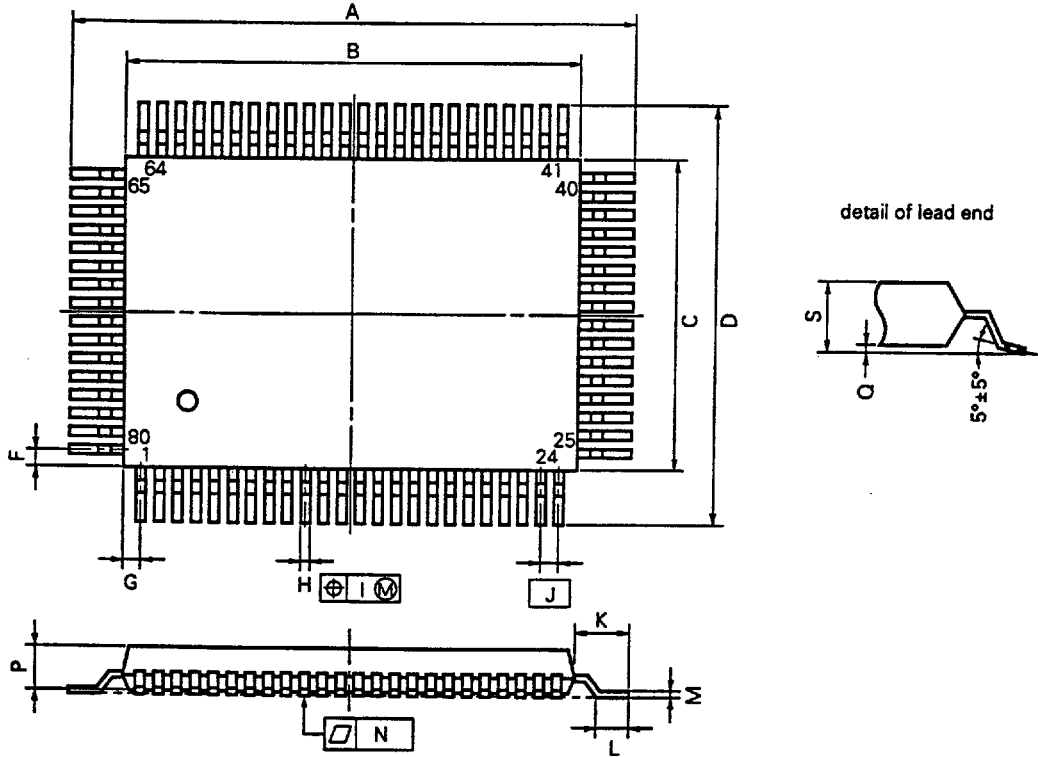
$\overline{\text{RESET}}$  input timing



11. PACKAGE DRAWINGS

PACKAGE DRAWING OF MASS-PRODUCED PRODUCT

80 PIN PLASTIC QFP (14x20)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

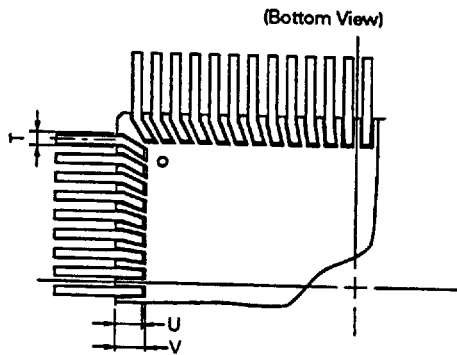
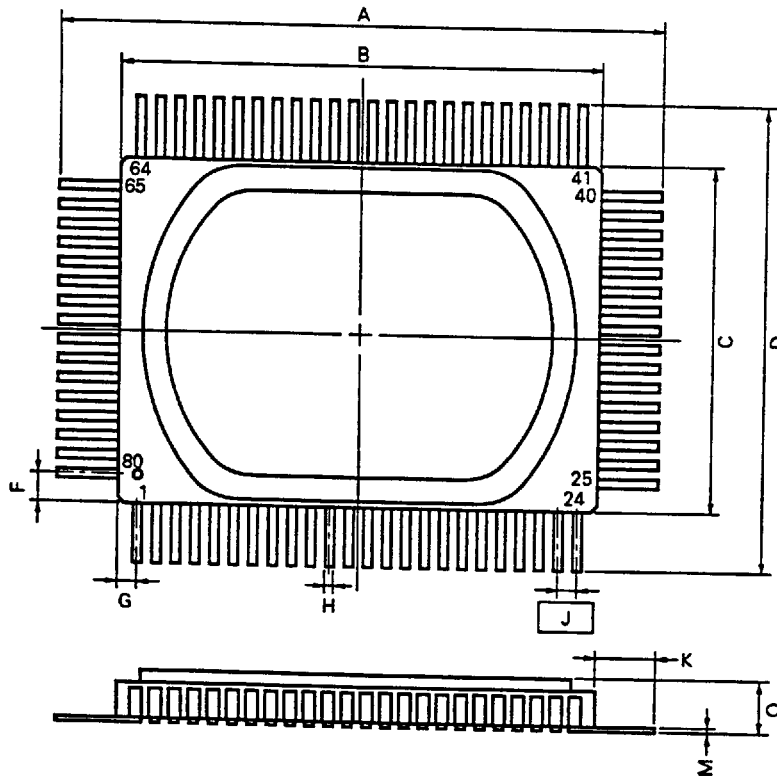
P80GF-80-3B9-2

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	0.014 <sup>+0.004</sup> <sub>-0.006</sub>
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071 <sup>+0.008</sup> <sub>-0.006</sub>
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.06</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Caution The ES product is different from the corresponding mass-produced product in shape and material. See "PACKAGE DRAWING OF ES PRODUCT."

PACKAGE DRAWING OF ES PRODUCT

80 PIN CERAMIC QFP (14 × 20) (FOR ES)



X80B-80A-1

ITEM	MILLIMETERS	INCHES
A	24.7±0.4	0.972±0.016
B	20.0	0.787
C	14.2	0.559
D	18.9±0.4	0.744±0.016
F	1.1	0.043
G	0.8	0.031
H	0.32	0.013
J	0.8 (T.P.)	0.031 (T.P.)
K	2.35±0.15	0.093±0.006
M	0.15	0.006
Q	2.7 MAX.	0.107 MAX.
T	0.55	0.022
U	1.0	0.039
V	1.2	0.047

12. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD78042A, μPD78043A, μPD78044A, μPD78045A.

For details of the recommended soldering conditions, refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 12-1 Soldering Conditions for Surface-Mount Devices

μPD78042AGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)

μPD78043AGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)

μPD78044AGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)

μPD78045AGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)

Soldering process	Soldering conditions	Recommended conditions
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (210 °C or more) Maximum allowable number of reflow processes: 2 <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	IR35-00-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (200 °C or more) Maximum allowable number of reflow processes: 2 <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	VP15-00-2
Wave soldering	Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow process: 1 Preheating temperature: 120 °C max. (measured on the package surface)	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for one side of a device)	-

**Caution** Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

APPENDIX A DEVELOPMENT TOOLS

The following tools are available for development of systems using the μPD78042A, μPD78043A, μPD78044A, and μPD78045A:

Software for Language Processing

RA78K/0 <sup>Notes 1, 2, 3</sup>	Assembler package common to 78K/0 series	
CC78K/0 <sup>Notes 1, 2, 3</sup>	C compiler package common to 78K/0 series	
DF78044 <sup>Notes 1, 2, 3</sup>	Device file common to μPD78044 sub-series	★
CC78K/0-L <sup>Notes 1, 2, 3</sup>	C compiler library source file common to 78K/0 series	

PROM Writing Tools

PG-1500	PROM programmer	
PA-78P048GF PA-78P048KL-S	Programmer adapter connected to PG-1500	
PG-1500 Controller <sup>Notes 1, 2</sup>	Control program for PG-1500	

Debugging Tools

IE-78000-R	In-circuit emulator common to 78K/0 series	
IE-78000-R-BK	Break board common to 78K/0 series	
IE-78044-R-EM	Emulation board common to μPD78044 sub-series	
EP-78130GF-R	Emulation probe common to μPD78134 sub-series	
EV-9200G-80	Socket mounted to user system created for 80-pin plastic QFP	
SM78K0 <sup>Notes 4, 5</sup>	System simulator common to 78K/0 series	★
SD78K/0 <sup>Notes 1, 2</sup>	Screen debugger for IE-78000-R	
DF78044 <sup>Notes 1, 2, 4, 5</sup>	Device file common to μPD78044 sub-series	

Real-Time OS

RX78K/0 <sup>Notes 1, 2, 3</sup>	Real-time OS for 78K/0 series	
MX78K0 <sup>Notes 1, 2, 3</sup>	OS for 78K/0 series	★

- Notes 1. PC-9800 series (MS-DOS™) base  
 2. IBM PC/AT™ (PC DOS™) base  
 3. HP9000 series 300™ and HP9000 series 700™ (HP-UX™) base, SPARCstation™ (Sun OS™) base, EWS-4800 series (EWS-UX/V) base  
 4. PC-9800 series (MS-DOS + Windows™) base  
 5. IBM PC/AT (PC DOS + Windows) base

**Fuzzy Inference Development Support Systems**

FE9000 <sup>Note 1</sup> , FE9200 <sup>Note 3</sup>	Fuzzy knowledge data creation tool
FT9080 <sup>Note 1</sup> , FT9085 <sup>Note 2</sup>	Translator
FI78K0 <sup>Notes 1, 2</sup>	Fuzzy inference module
FD78K0 <sup>Notes 1, 2</sup>	Fuzzy inference debugger

- Notes**
1. PC-9800 series (MS-DOS) base
  2. IBM PC/AT (PC DOS) base
  3. IBM PC/AT (PC DOS + Windows) base

**Remarks** 1. Refer to the *78K/0 Series Selection Guide* (IF-1185) for development tools manufactured by third parties.

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2. The RA78K/0, CC78K/0, SM78K0, and SD78K/0 are used with the DF78044.



APPENDIX B RELATED DOCUMENTS

★

Documents Related to Devices

Document name	Document No.	
	Japanese	English
μPD78044A Sub-Series User's Manual	IEU-860	IEU-1394
μPD78042A, 78043A, 78044A, 78045A Data Sheet	This data sheet	IC-3317
μPD78P048A Product Information	IP-8892	IP-3408
μPD78044A Sub-Series Special Function Registers	IEM-5588	—
78K/0 Series User's Manual, Instruction	IEU-849	IEU-1372
78K/0 Series Instruction Summary Sheet	IEM-5522	—
78K/0 Series Instruction Set	IEM-5521	—

Documents Related to Development Tools (User's Manual)

Document name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller	PC-9800 series (MS-DOS) base	EEU-704	To be created
	IBM PC series (PC DOS) base	EEU-5008	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78044-R-EM		EEU-833	EEU-1424
EP-78130GF-R		EEU-943	—
SM78K0 System Simulator	Reference	EEU-5002	To be released soon
SD78K/0 Screen Debugger PC-9800 series (MS-DOS) base	Tutorial	EEU-852	—
	Reference	EEU-816	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) base	Tutorial	To be created	EEU-1414
	Reference	EEU-993	EEU-1413

**Caution** The above documents may be revised without notice. Use the latest versions when you design an application system.

Documents Related to Software to be Incorporated into the Product (User's Manual)

Document name		Document No.	
		Japanese	English
78K/0 Series Real-Time OS	Basic	EEU-912	—
	Installation	EEU-911	—
	Technical	EEU-913	—
OS for 78K/0 Series MX78K0	Basic	EEU-5010	—
Tool for Creating Fuzzy Knowledge Data		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System, Translator		EEU-829	EEU-1444
78K/0 Series Fuzzy Inference Development Support System, Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System, Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document name	Document No.	
	Japanese	English
Package Manual	IEI-635	IEI-1213
SMD Surface Mount Technology Manual	IEI-616	IEI-1207
Quality Grades on NEC Semiconductor Device	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	—
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Device	MEI-603	MEI-1202
Guide for Products Related to Micro-Computer: Other Companies	MEI-604	—

**Caution** The above documents may be revised without notice. Use the latest versions when you design an application system.