# 天鈺科技股份有限公司
## *Eureka Microelectronics, Inc.*

| 文件名稱 DOC Title ： | 文件編號 DOC NO ：TPL7603-01 |
|---|---|
| **EK7603 Data Sheet** | 版　本　REV ：0.2 |
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文件制/修訂一覽表　Revision History

| 版本 REV. | 修訂日期 REV Date | 生效日期 Eff. Date | 修訂頁次 REV. Page | 制/修訂項目/ 內容 Revise item / Content |
|---|---|---|---|---|
| 0.1 | 2003/1/27 | 2003/3/20 | | New Issue |
| 0.2 | 2003/6/5 | 2003/6/17 | P.5 | 1.　OSEL = H or open → H |
| | | | | 　　OSEL = L → L or open |
| | | | | 2. When EDGSL = L → L or open |

# Eureka Microelectronics, Inc.

# EK7603

## *PRELIMINARY* Rev. 0.2

## DATA SHEET

## 402/480-Output TFT LCD Analog Source Driver

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# EUREKA

# EK7603

## Table of Contents

# *EUREKA* EK7603

## 402/480- Output TFT LCD Analog Source Driver

### 1. GENERAL DESCRIPTION

The EK7603 is an analog, fully color, source driver for TFT LCD panels designed for camera, TV etc. Analog R, G and B signal are applied directly on the chip. For each of the 402/480 outputs, the voltage is sampled and buffered to the panel. With a double sample and hold circuit a new voltage can be sample whereas the previous sample voltage is applied to the panel.

According to different modes, the 3 input voltages (VA, VB, VC) can be applied on different output to support various pixel array types.

The 3 input voltages (VA, VB, VC) can be sampled simultaneously or sequentially to have a better flexibility with the input voltage. Using enable signal (STHx), several chips can be cascaded for large panel.

### 2. FEATURES

- 402/480 analog source driver outputs (OSEL)
- High frequency Sampling 10MHz
- Automatic low power consumption mode after data capture (gated clock)
- Bi-directional shift capability (L/R)
- Simultaneous or Sequential RGB acquisition mode (MODE)
- RGB color selection to match different types of color filters (Q1H, Q2H)
- Output enable signal edge selectable (EDGSL)
- Logic power supply voltage $V_{DD}$: 2.7V – 5.25V
- LCD power supply voltage $AV_{DD}$: 4.5V – 5.5V
- Output dynamic range $AV_{SS}$+0.2V to $AV_{DD}$-0.2V
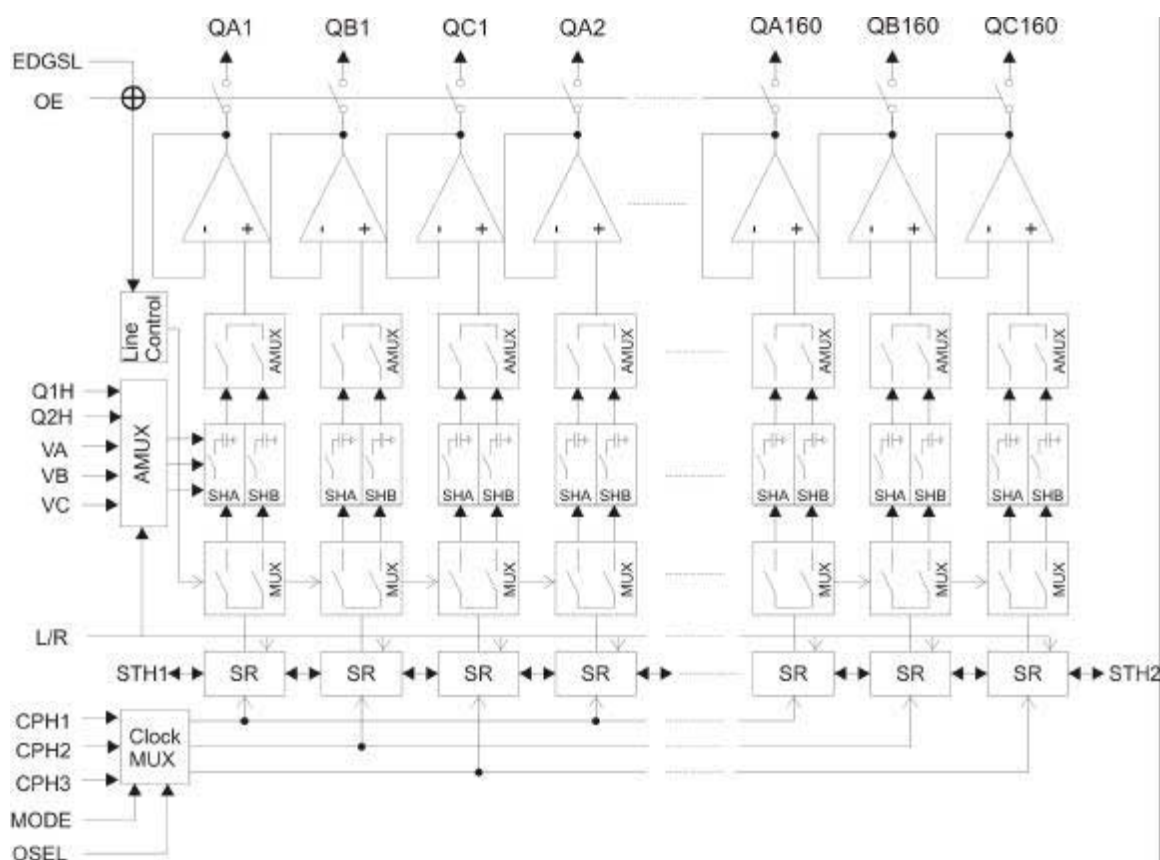- Bare chip with gold bumper for COG application

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### 3. BLOCK DIAGRAM



**Fig. 1 Block diagram**

● **Clock MUX**

Selects if the sampling is simultaneous or sequential. Also gates the clock.

● **3 x 134/160-bit bi-directional shift register**

Generates enable signals for sequential sampling 134/160 groups of 3 input colors.

● **Line control**

Select sample circuit SHA or SHB and the high impedance output state

● **SH control MUX**

Select which sample and hold circuit samples the analog input value.

● **AMUX**

According to the controls signals, selects which input color goes to which group of outputs.

● **Sample and hold Circuit (SHA, SHB)**

Sample the input voltage when the enable signal of the shift register is generated and hold this value until it is stored on the panel.

● **Buffers**

Drive the sample grayscale voltage on the panel.

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**4.   PIN FUNCTION DESCRIPTION**

**Table 1.**   Pin description

| Signal Name | Pin Type | Function |
|---|---|---|
| Qa1 to Qa160<br>Qb1 to Qb160<br>Qc1 to Qc160 | Output | Liquid-crystal application voltages<br>Each QaX, QbX or QcX correspond to one of the analog sample input signal VA, VB or VC. |
| VA<br>VB<br>VC | Input | Video input signal<br>Analog video input signal that is sampled internally and applied to the panel. |
| L/R | Input | Controls the display data shift direction<br>L/R = H :   STH1 input, Qa1→Qc160,   STH2 output.<br>L/R = L :   STH2 input, Qc160→Qa1, STH1 output. |
| STH1 | Bi-direction | Right shift start pulse<br>L/R = H :   Becomes the start pulse input pin<br>L/R = L :   Becomes the start pulse output pin |
| STH2 | Bi-direction | Left shift start pulse<br>L/R = H :   Becomes the start pulse output pin<br>L/R = L :   Becomes the start pulse input pin |
| CPH1<br>CPH2<br>CPH3 | Input | Sampling clock input<br>Refers to the analog data-sampling clock. The sampling starts at the first rising edge of CPH1 when STH1 (L/R = H) is activated. The sampling can be simultaneous or sequential.<br><br>When in simultaneous mode (MODE = H), the sampling is made during CPH1 period for all output, but CPH2 and CPH3 must be fixed to $V_{DD}$ or $V_{SS}$.<br><br>When in sequential mode (MODE = L, L/R = H), the sampling is made according the table below:<br>CPH1 control the sampling for Qa1→Qa160<br>CPH2 control the sampling for Qb1→Qb160<br>CPH3 control the sampling for Qc1→Qc160<br>When in sequential mode (MODE = L, L/R = L), the sampling is made according the table below:<br>CPH1 control the sampling for Qc160→Qc1<br>CPH2 control the sampling for Qb160→Qb1<br>CPH3 control the sampling for Qa160→Qa1 |
| OE | Input | Load line<br>The sampled voltages are connecting to the panel at the rising/falling edge (EDGSL) of OE. The outputs of SHA(B) that was in sample mode are applied to the panel, whereas the SHB(A) becomes ready to sample new values. |
| OSEL | Input<br>(Pull-down) | Number of output selection<br>OSEL = H : 402 output mode<br>OSEL = L or open : 480 outputs mode<br>Output pins Qx68→ Qx93 are invalid in 402-output mode. |
| EDGSL | Input<br>(Pull-down) | Output enable signal edge select.<br>When EDGSL = H, OE will be active at falling edge.<br>When EDGSL = L or open, OE will be active at rising edge. |
| MODE | Input<br>(Pull-down) | Sampling mode selection<br>MODE = H: Simultaneous sampling<br>MODE = L or open: Sequentially sampling |

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| Q1H Q2H | Input (Pull-down) | Color selection input Q1H and Q2H select which input voltage (VA, VB, VC) correspond to QaX, QbX, QcX outputs. |
|---|---|---|
| $V_{DD}$ | Power | Logic part power supply |
| $V_{SS}$ | Power | Logic part ground |
| $AV_{DD}$ | Power | Analog part power supply |
| $AV_{SS}$ | Power | Analog part ground |

## 5. FUNCTIONAL DESCRIPTION

### 5.1 Operation Timing
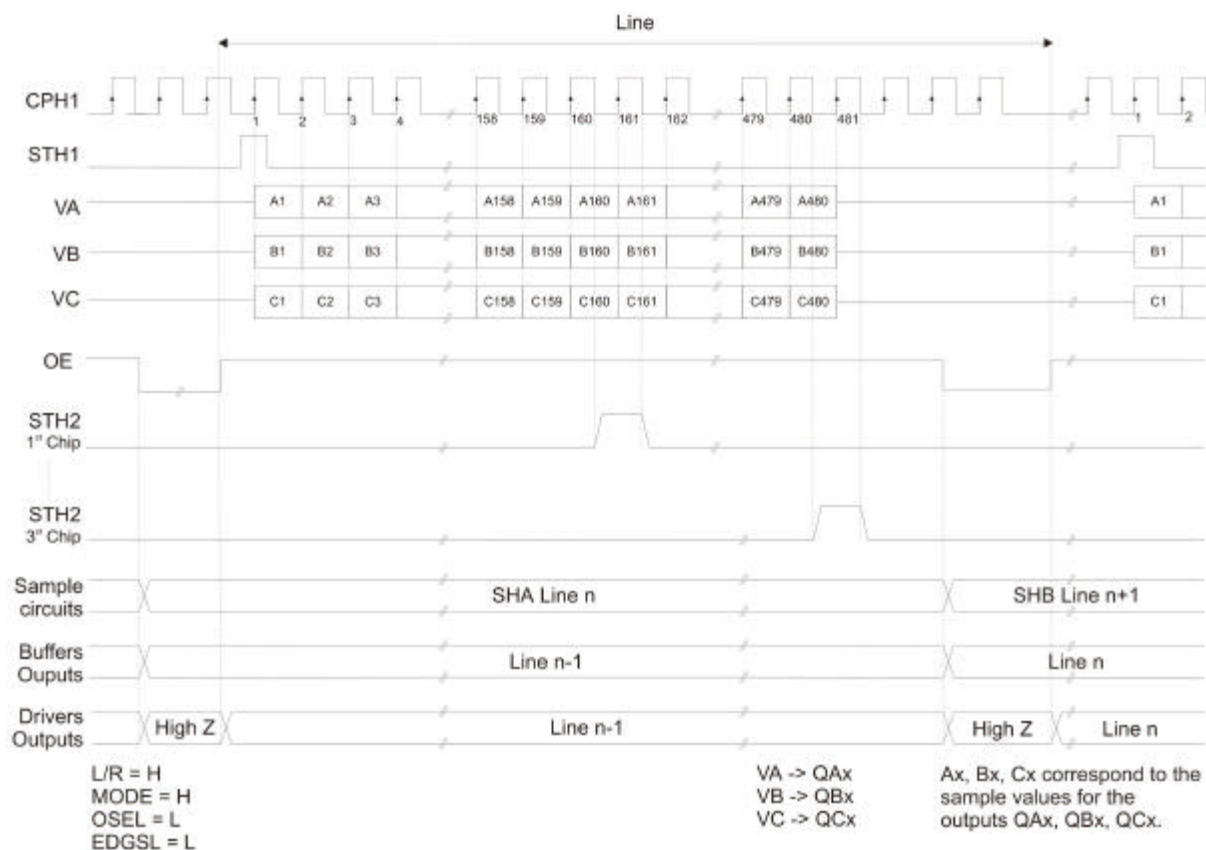


**Fig. 2** Operation timing diagram

The start condition is initiated by applying a start pulse to the enable input pin (STH1 when L/R = H) at the beginning of each line on the first chip. During the next 134/160 CPH1 rising edges, this source driver sample 134/160 times 3 display input voltage (3 RGB dot x 134/160 pixels). After sampling the 134/160th group of input voltages, it activates the enable output signal (STH2 when L/R= H) to enable the following chip.

As soon as the loading of the input voltage is achieved for a complete line, the controller activates the OE

signal to force the 402/480 output buffers in a high impedance state. Then the outputs of SHA(B) that were in sample mode are applied to the output buffers, whereas the SHB(A) becomes ready to sample new values. Finally, at the rising edge of OE, the 402/480 output buffers drive the sample voltages to the panel.

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## 5.2 Number of output selection
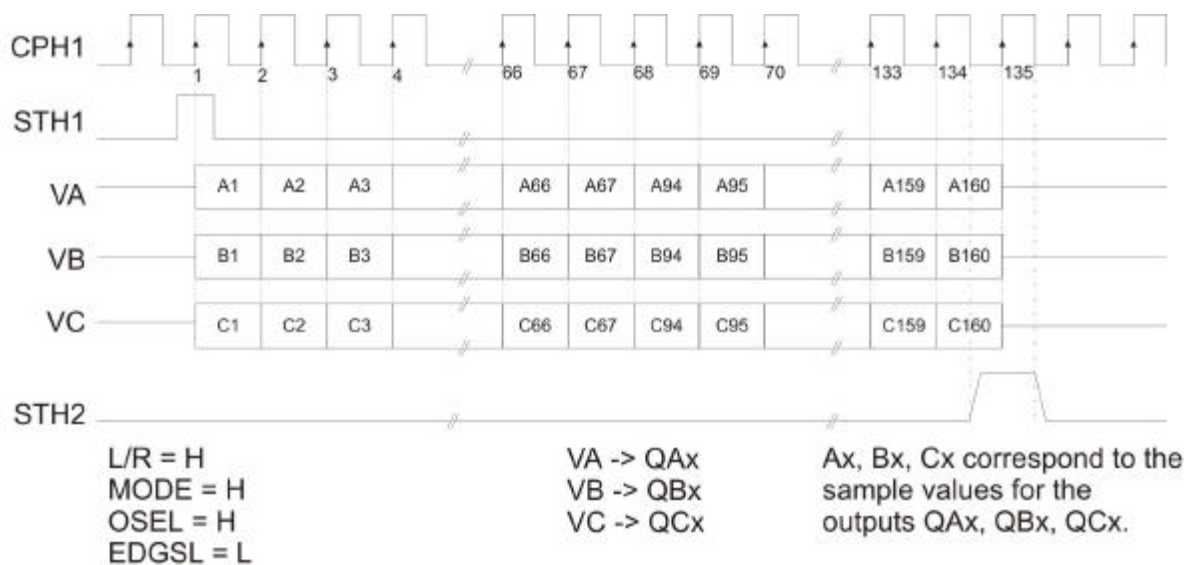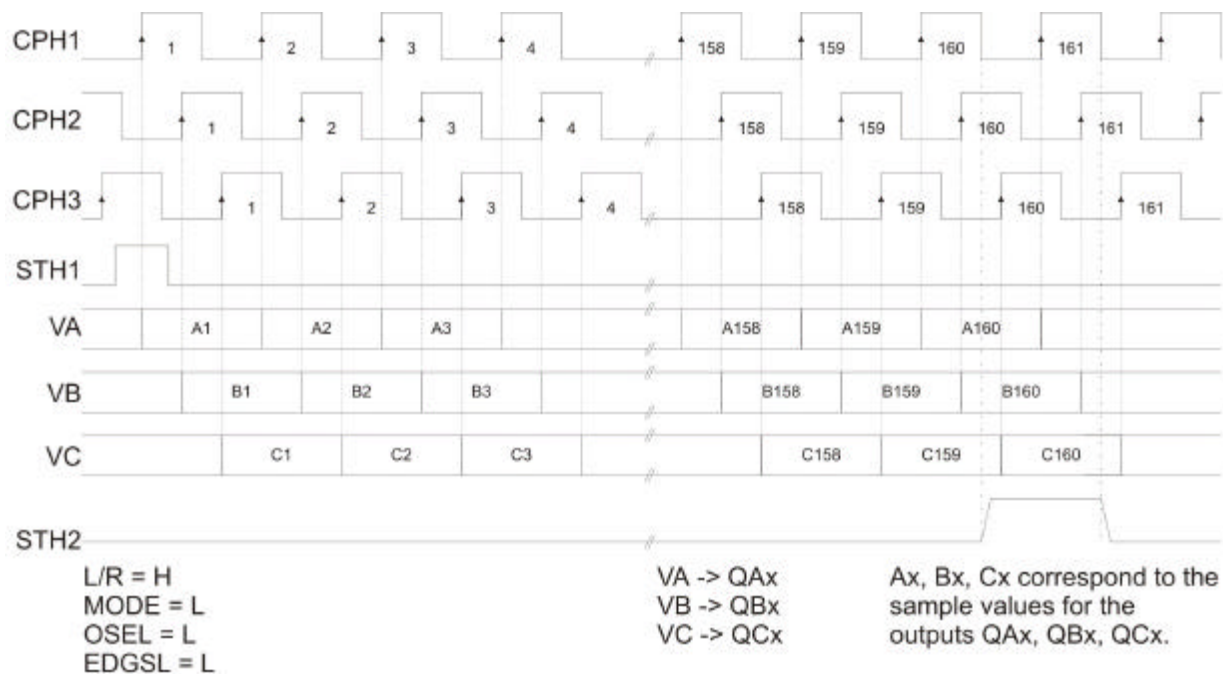


**Fig. 3** 402-output mode timing diagram

The OSEL pin allows using the chip as a 402-output or a 480-output driver. When 402-output mode is selected, outputs Qa68 to Qc93 are unavailable and the sampling pass from Qa67 to Qa94, Qb67 to Qb94 and Qc67 to Qc94. Then the sampling of the whole chip is made in 134 CPH1 periods.

## 5.3 Sampling modes
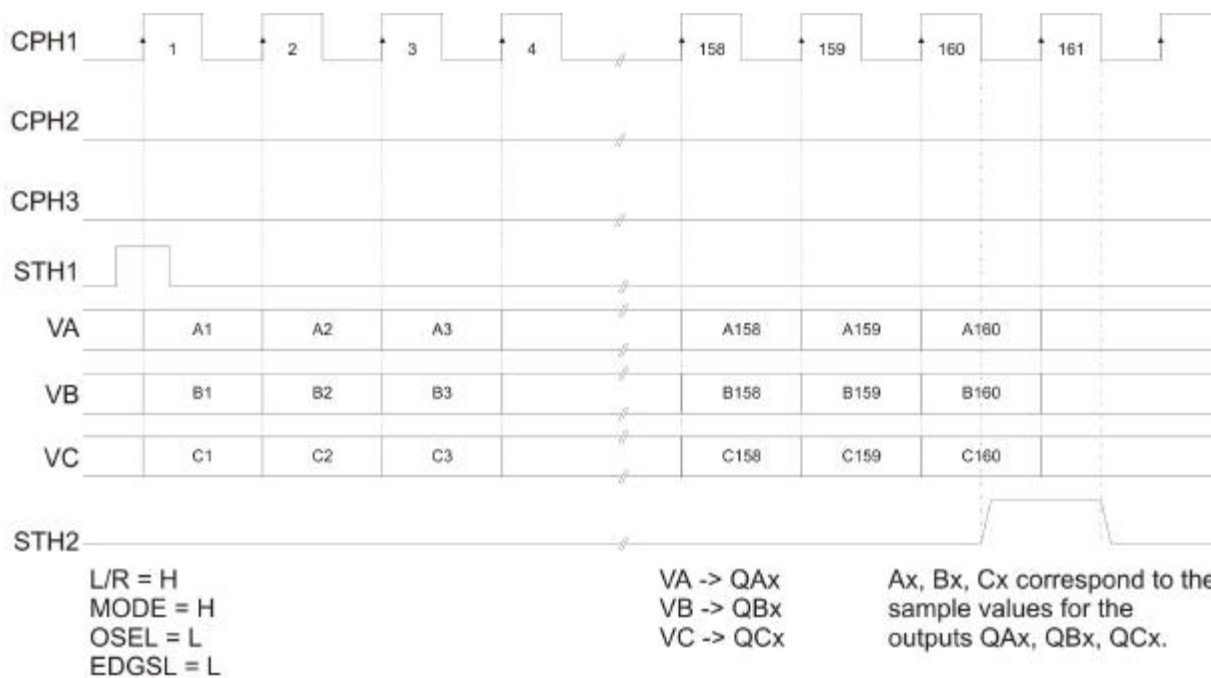


**Fig. 4** Simultaneous sampling mode

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Each input is sampled simultaneously synchronised with CPH1 rising edge.

STH2 signal is generated at the falling edge of the 134/160$^{th}$ period of CPH1 since the start pulse.



L/R = H                         VA -> QAx              Ax, Bx, Cx correspond to the
MODE = L                        VB -> QBx              sample values for the
OSEL = L                        VC -> QCx              outputs QAx, QBx, QCx.
EDGSL = L

**Fig. 5** Sequential sampling mode

Each input is sampled sequentially synchronised with the associated rising edge of the corresponding clock. CPH1 controls the sample for QAx outputs, CPH2 controls the sample for QBx outputs and CPH3 controls the sample for QCx outputs.

STH2 signal is generated at the falling edge of the 134/160$^{th}$ period of CPH1 since the start pulse.

## 5.4 Color mode selection

The Q1H and Q2H control the color selection to match various color filters in shown as following table.

**Table 2.**    Color mode selection table

| Q1H | Q2H | QA | QB | QC |
|-----|-----|-----|-----|-----|
| L | L | VA | VB | VC |
| L | H | VC | VA | VB |
| H | X | VB | VC | VA |

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**5.5 Relationship between OE and output waveform**
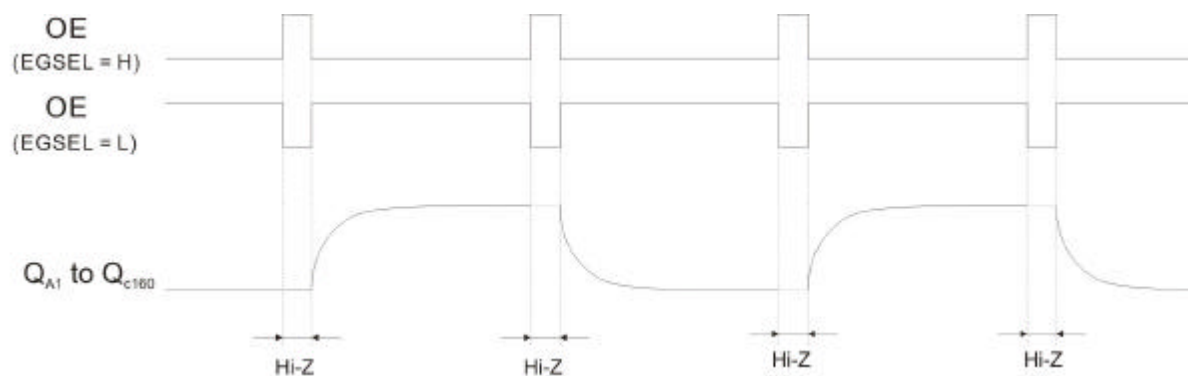


**Fig. 6** OE timing diagram

At OE rising/falling edge, the sample voltages are output on the panel. As long as OE is active, the 402/480 output buffers are forced in a high impedance state.

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## 6.  ABSOLUTE MAXIMUM RATINGS

### 6.1 Absolute maximum ratings

**Table 3.**  Absolute maximum ratings ($V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Logic Part Supply Voltage | $V_{DD}$ | -0.5 to +7.0V | V |
| Analog Part Supply Voltage | $AV_{DD}$ | -0.5 to +7.0V | V |
| Logic Part Input Voltage | $V_{I1}$ | -0.5 to VDD + 0.5 | V |
| Video Input Voltage | $V_{I2}$ | -0.5 to AVDD + 0.5 | V |
| Logic Part Output Voltage | $V_{O1}$ | -0.5 to VDD + 0.5 | V |
| Driver Part Output Voltage | $V_{O2}$ | -0.5 to AVDD + 0.5 | V |
| Storage Temperature | $T_{STG}$ | -55 to +125 | °C |

**Caution: If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum rating, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum rating.**

### 6.2 Recommended operating range

**Table 4.**  Recommended operating range ($V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Logic Part Supply Voltage | $V_{DD}$ | | 2.7 | | 5.25 | V |
| Analog Part Supply Voltage | $AV_{DD}$ | | 4.5 | | 5.5 | V |
| Video Input Voltage | $V_{VIDEO}$ | | $AV_{SS}$ + 0.2 | | $AV_{DD}$ - 0.2 | V |
| Operating Ambient Temperature | $T_A$ | | -30 | | 75 | °C |
| Maximum Clock Frequency | $F_{CPH}$ | | | | 10 | MHz |
| OE period | $T_{OE}$ | | | 64 | 200 | µs |

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## 7. ELECTRICAL CHARACTERISTICS

### 7.1 DC characteristics

**Table 5.** DC characteristics

($T_A$= -30 to +75°C, $V_{DD}$= 2.7V to 5.25V, $AV_{DD}$= 4.5V to 5.5V, $V_{SS}$=$AV_{SS}$=0V)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Logic High-level Input Voltage | $V_{DIH}$ | | $0.7*V_{DD}$ | | $V_{DD}$ | V |
| Logic Low-level Input Voltage | $V_{DIL}$ | | 0.0 | | $0.3*V_{DD}$ | V |
| Logic Input Leakage Current | $I_{LIL}$ | | | | ±1.0 | µA |
| Video Input Leakage Current | $I_{VIL}$ | | | | ±1.0 | µA |
| Logic High-level Output Voltage | $V_{OH}$ | STH1(STH2), $I_{OH}$=-400µA | $V_{DD}$ - 0.4 | | | V |
| Logic Low-level Output Voltage | $V_{OL}$ | STH1(STH2), $I_{OL}$=+400µA | | | 0.4 | V |
| Output Voltage Range | $V_0$ | | 0.2 | | $AV_{DD}$ - 0.2 | V |
| Output Voltage Deviation | $\Delta V_0$ | Note 1 | | | ±20 | mV |
| Logic Part Dynamic Current Consumption | $I_{DD}$ | Note 2 | | **TBD** | **TBD** | mA |
| Driver Part Dynamic Current Consumption | $I_{ADD}$ | Note 3 | | **TBD** | **TBD** | mA |

Note 1: Deviation between input voltage and output value. Voltage on the output pin 30us after

the rinsing edge of OE. $V_{VIDEO}$= 0.2V to $AV_{DD}$-0.2V.

Note 2:  $F_{CPH1}$=10MHz,In Simultaneous Clock Mode, $T_{OE}$=63µs, $T_{IWL}$ = 5us, No load.

Note 3: Video input = $AV_{DD}$/2, No Load.

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**7.2 AC characteristics**

**Table 6.**  AC characteristics

($T_A$= -30 to +75°C, $V_{DD}$= 2.7V to 5.25V, $V_{SS}$=$AV_{SS}$=0V, $T_R$ = $T_F$ = 5.0ns)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Clock Period | $T_{CP}$ | | 100 | | | ns |
| Clock high-level width | $T_{CWH}$ | | 40 | | | ns |
| Clock low-level width | $T_{CWL}$ | | 40 | | | ns |
| Delay time Between Clocks | $T_{C12}$, $T_{C23}$ | | 15 | | $1/2*T_{CP}$ | ns |
| STH Setup Time | $T_{SS}$ | | 10 | | | ns |
| STH Hold Time | $T_{SH}$ | | 10 | | | ns |
| OE high-level width | $T_{IWH}$ | | 30 | | | μs |
| OE low-level width | $T_{IWL}$ | | 160 | | | ns |
| OE -STH Timing | $T_{OE-STH}$ | | **TBD** | | | ns |
| STH Pulse Delay Time | $T_{SD}$ | $C_L$ =20pF | | | 20 | ns |
| Driver Output Delay Time | $T_{DD}$ | $C_L$ =25pF, $R_L$=25kΩ | | 12 | 20 | μs |

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**7.3 Timing chart**

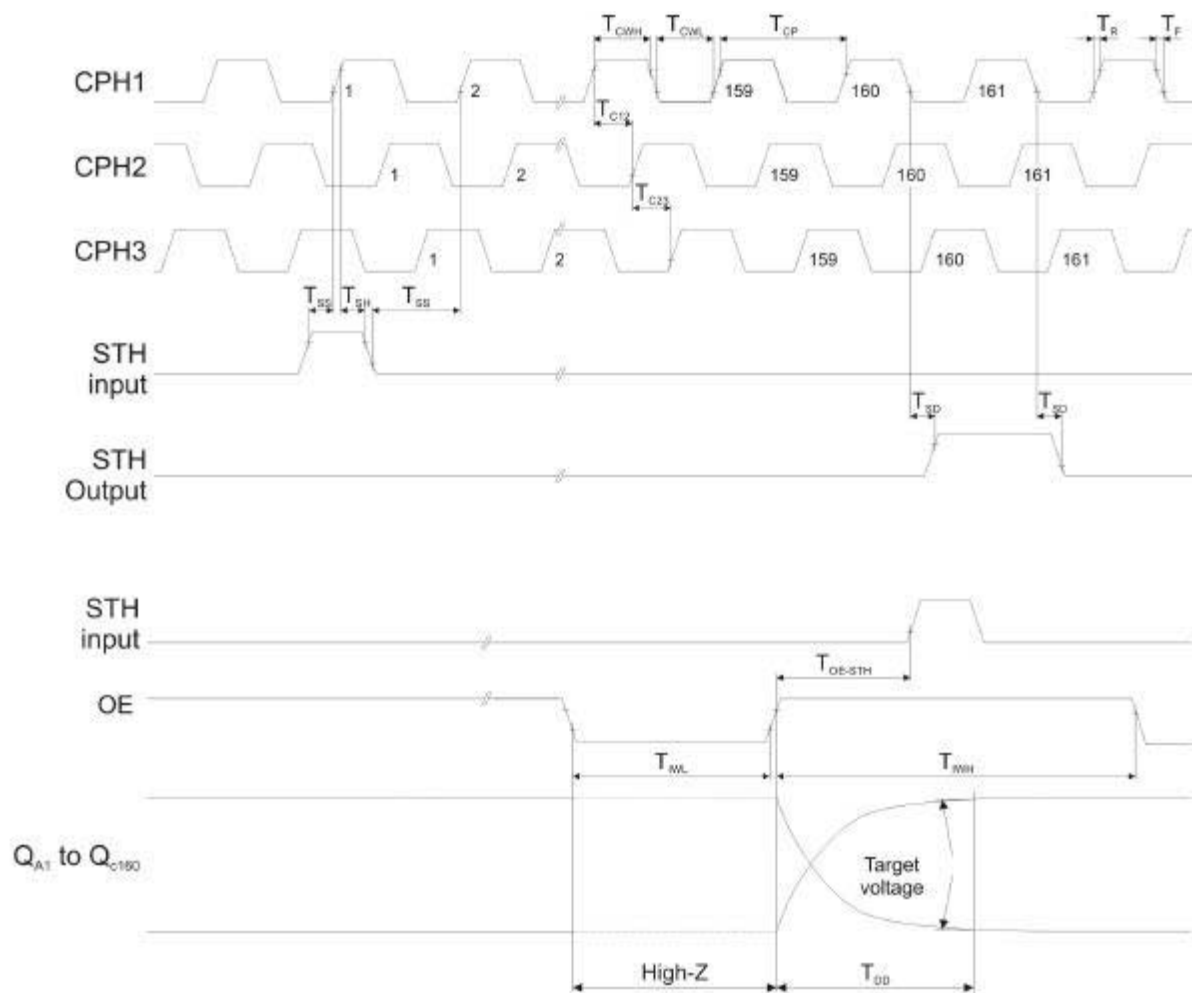Unless otherwise specified, the input level is defined to $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$



**Fig. 7** Timing

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## 8. DEFINITIONS

### 8.1 Date sheet status and application information

| Data sheet status | |
|---|---|
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

### 8.2 Life support application

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Eureka customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Eureka for any damages resulting from such improper use or sale.