
eKA8565A

USB Audio Controller

Product Specification

Doc. VERSION 0.1


ELAN MICROELECTRONICS CORP.

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PRELIMINARY



Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial Preliminary Version	2006/09/08

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1 General Description

The eKA8565A is a USB digital audio controller with audio data processing that supports 16-bit 2-channel format at 48kHz, 44.1kHz, 32kHz or 8kHz sampling rate. The device has an integrated USB transceiver, USB core, MCU, DAC, ADC, and I²S Input/Output. It can handle a high-level USB protocol, and manages user interface via HID I/O pins.

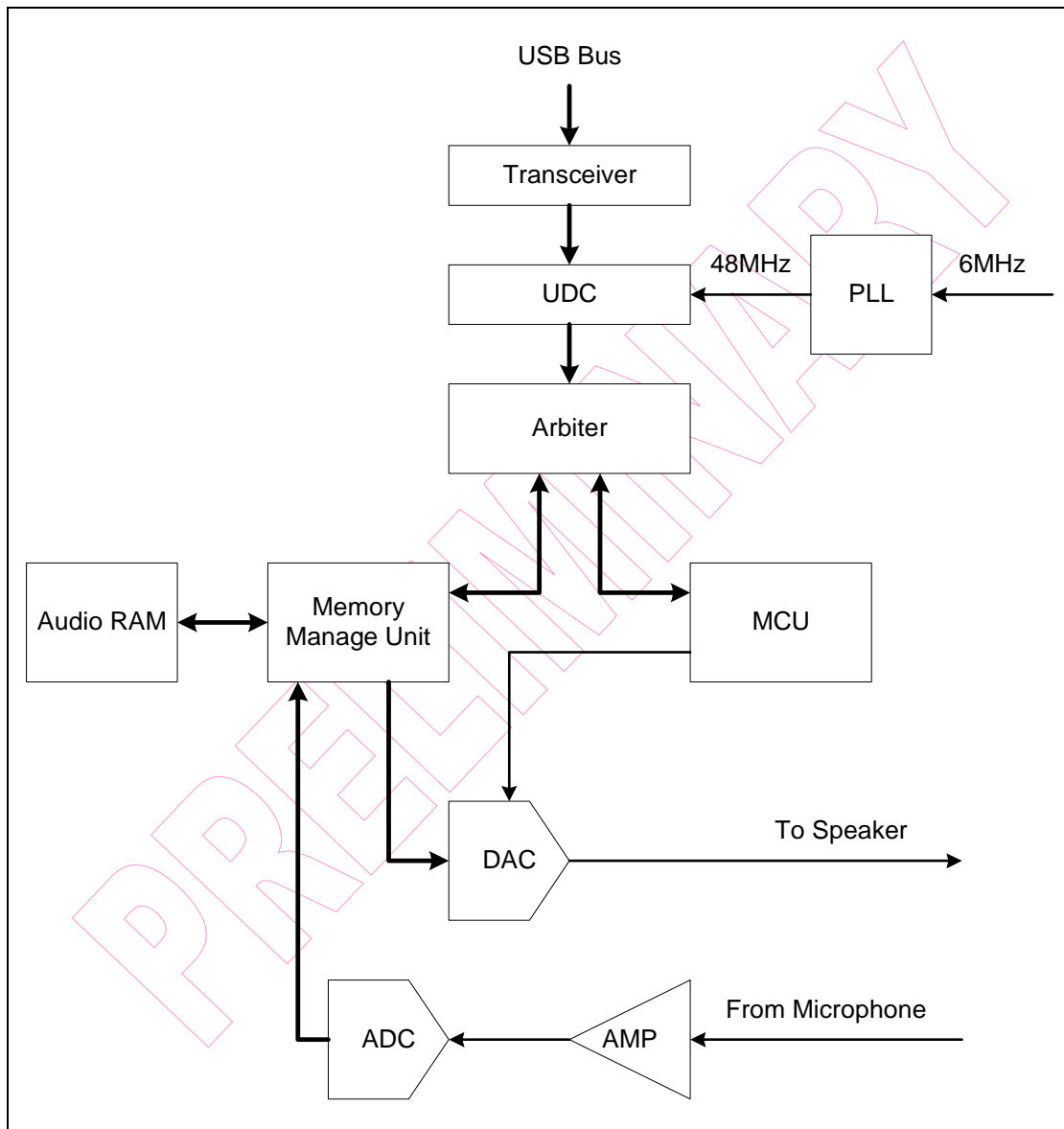
2 Features

- USB Specification v1.1 Compliant
- USB Audio and Human Interface Device (HID) Class v1.1 Compliant
- Supports 12 Mbits/s Full Speed Serial Data Transmission
- Supports 48kHz, 44.1kHz, 32kHz, 8kHz sampling rate
- Single oscillator: 6MHz
- Audio buffer size: 192×16 bits × 2
- Total of four Endpoints: Endpoint 0 for control transfer, Endpoint 1 for audio streaming out, Endpoint 2 for streaming in, Endpoint 3 for HID
- Supports stereo/mono playback
- Built-in 2-channel D/A Converter with 10-bit resolution
- Built-in 1-channel A/D converter with 10-bit resolution
- Alternative settings supported by the audio streaming-out interface:
 - ALT-0: (default setting) zero isochronous bandwidth
 - ALT-1: 16-bit PCM 2 channel
- Alternative settings supported by the audio streaming-in interface:
 - ALT-0: (default setting) zero isochronous bandwidth
 - ALT-1: 16-bit PCM stereo
- 2K×13 on-chip program ROM
- 32 bytes of general purpose RAM (R20~R3F)
- RC Oscillator with internal RC
- 5 level stack for subroutine nesting
- Key scan I/O pins (P50~P55, P60~P63)
- Software control output pins (P56, P57)
- Support buzzer/LED output pin (P56 P57)
- Port 5 and Port6 with pull-up resistors
- Wake-up pin in Port 5 and Port6
- MCU run at 6 MHz frequency
- Package: 48-pin LQFP

3 Application

- Skype (including key scan function)

4 Block Diagram



5 Pin Configuration

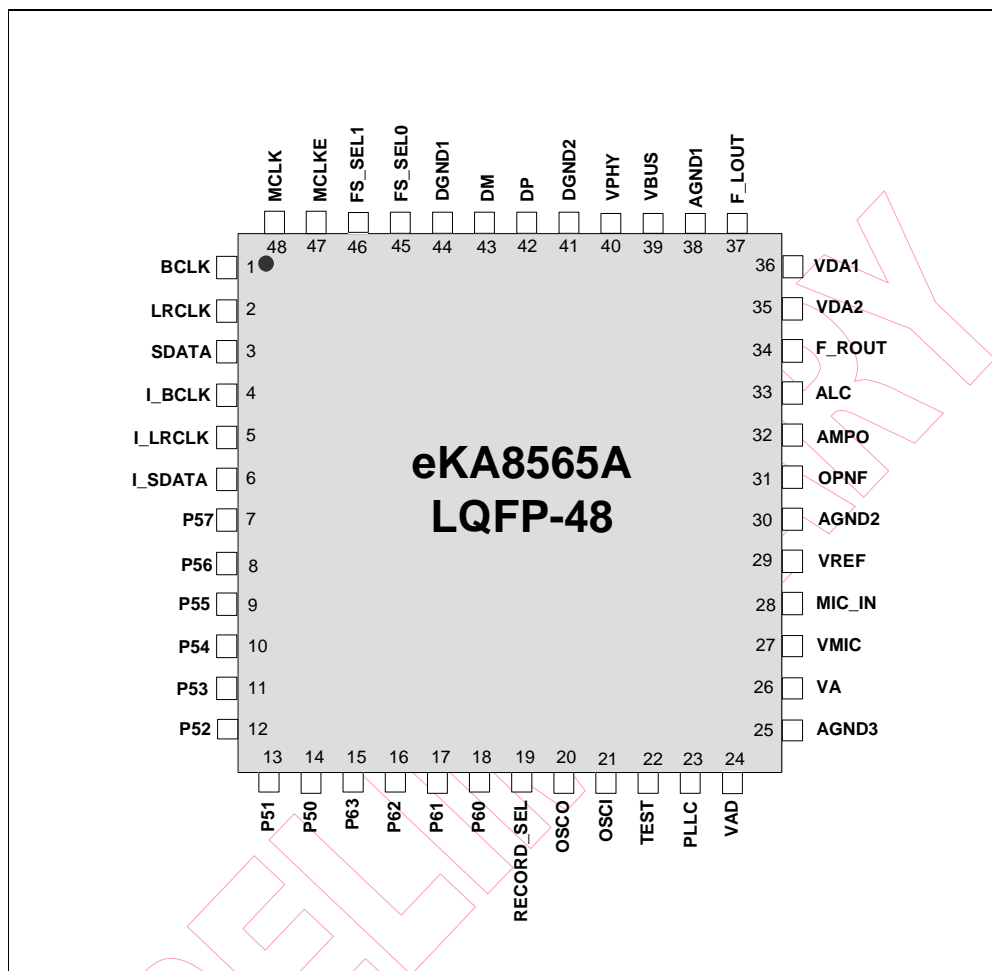


Fig 5-1 48-Pin Configuration of EKA8565A LQFP Type

6 Pin Assignment

Symbol	Pin No.	I/O	Function
BCLK	1	O	BCLK for I ² S interface
LRCLK	2	O	LRCLK for I ² S interface
SDATA	3	O	I ² S interface for FL, FR output
I_BCLK	4	I	BCLK for I ² S interface
I_LRCLK	5	I	LRCLK for I ² S interface
I_SDATA	6	I	I ² S interface for FL, FR input
P57, P56	7, 8	O	AP control output pin
P55 ~ P50, P63~P60	9~18	I/O	Key scan pin
RECORD_SEL	19	I	Record select pin. 1 : I ² S record 0 : ADC record An internal pull-low resistor is connected to DGND.
OSCO	20	O	Crystal output
OSCI	21	I	Crystal input
Test	22	I	Test mode select pin Test = 0, enter normal mode Test = 1, enter test mode An internal pull-low resistor is connected to DGND.
PLLC	23	I	External capacitor for PLL
VAD	24	PWR	ADC analog power supply pin
AGND3	25	-	A/D and PLL ground pin
VA	26	PWR	Analog power supply pin
VMIC	27	O	Power supply for external MIC
MIC_IN	28	I	Microphone analog input pin
Vref	29	O	Bandgap reference output
AGND2	30	-	MIC ground pin

Symbol	Pin No.	I/O	Function															
OPNF	31	I	Non-inverting type amplifier. Normally, a feedback resistor connects from AMPO to OPNF and a gain resistor connects to MIC.															
AMPO	32	O	Gain amplifier output and negative feedback terminal for MIC															
ALC	33	I	Automatic Level Control adjustment pin for MIC															
F_ROUT	34	O	Front right channel analog audio output pin															
VDA2	35	PWR	DAC analog power supply Pin 2															
VDA1	36	PWR	DAC analog power supply Pin 1															
F_LOUT	37	O	Front left channel analog audio output pin															
AGND1	38	PWR	2-channel D/A ground pin															
VBUS	39	PWR	USB bus power supply pin															
VPHY	40	PWR	PHY and PLL power supply pin															
DGND2	41	-	PHY ground pin															
DP	42	I/O	USB plus data line interface															
DM	43	I/O	USB minus data line interface															
DGND1	44	PWR	Digital ground pin															
FS_SELO FS_SEL1	45,46	I	<p>I²S's Sample Frequency</p> <table border="1"> <thead> <tr> <th></th> <th>Sample Frequency</th> <th>MCLK</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>32kHz</td> <td>8.192 MHz</td> </tr> <tr> <td>01</td> <td>8kHz</td> <td>2.048 MHz</td> </tr> <tr> <td>10</td> <td>44.1kHz</td> <td>11.2896 MHz</td> </tr> <tr> <td>11</td> <td>48kHz</td> <td>12.288 MHz</td> </tr> </tbody> </table> <p>Internal pull-high resistors are connected to VD.</p>		Sample Frequency	MCLK	00	32kHz	8.192 MHz	01	8kHz	2.048 MHz	10	44.1kHz	11.2896 MHz	11	48kHz	12.288 MHz
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11	48kHz	12.288 MHz																
MCLKE	47	I	<p>External MCLK enable pin.</p> <p>0 : use external MCLK and MCLK pin is input pin 1 : use internal MCLK and MCLK pin is output pin</p> <p>An internal pull-high resistor is connected to VD.</p>															
MCLK	48	I/O	Crystal oscillator I/O pin															

7 Function Description

The eKA8565A is a USB Audio Controller that transmits/receives audio data stream to/from the host through its Audio Streaming interface. The Audio Data Format supports 16-bit, 2-channel, and 48kHz, 44.1kHz, 32kHz, 8kHz PCM. It has three interfaces. Interface 1 supports four sampling frequencies. The sampling rate is changed by FS_SEL0 and FS_SEL1. For Interface 2, this device transmits data at a rate that is locked to frame timing. When user uses the recording format (ex. 8kHz) to record speech other than 48kHz stereo format, the application software will transform 48kHz data to 8kHz data. Interface 3 is HID pipe which is used to read button status.

The eKA8565A also supports key scan, LED on/off and Buzzer on/off function.

8 Absolute Maximum Rating

Symbol	Min	Max	Unit
Temperature under bias	0	70	°C
Storage temperature	-65	150	°C
Input voltage	-0.5	6.0	V
Output voltage	-0.5	6.0	V

9 Electrical Characteristic

9.1 DC Electrical Characteristic

Ta=0°C~70°C, VBus=5V, DGND=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIL	Input Leakage Current	VIN = VBus, DGND	-	-	±1	μA
VIH	Input High Voltage	-	2.0	-	-	V
VIL	Input Low Voltage	-	-	-	2.0	V
VIHX	Clock Input High Voltage	OSCI	2.5	-	-	V
VILX	Clock Input Low Voltage	OSCI	-	-	1.0	V
VOH1	Output High Voltage (Port 5, Port 6)	IOH = -10.0mA	2.4	-	-	V
VOH2	Output High Voltage (I ² S Interface Pin)	IOH = -6.67mA	2.4	-	-	V
VOL1	Output Low Voltage (Port 5, Port 6) (P5 : Normal Mode)	IOL = 10.0mA	-	-	0.4	V
VOL2	Output Low Voltage (P5 : LED driver Mode)	IOL = 10.0mA VBus = 5 V	-10%	1.3	+10%	V
VOL3	Output Low Voltage (I ² S Interface Pin)	IOL = 6.67mA	-	-	0.4	V
IPH	Pull-high Current (Port 5 and Sel_Vref pin)	Pull-high active, input pin at DGND (PH resistor = 25KΩ)	-20%	-125	+20%	μA
IPL	Pull-low Current (Test pin)	Test pin at VBus (PL resistor = 25KΩ)	-20%	125	+20%	μA
ISB1	Power Down Current	All input and I/O pin at VBus, output pin floating, WDT disabled	-	-	50	μA
ISB2	Power Down Current	All input and I/O pin at VBus, output pin floating, WDT enabled	-	-	100	μA
ICC	Operating Supply Current	Fosc= 6.0 MHz , output pin floating	-	-	10	mA

9.2 Analog Electrical Characteristic

Parameter	Condition	Min	Typ	Max	Unit
ADC					
ADC Resolution	-	-	10	-	Bits
ADC Sampling Frequency	-	-	48	-	kHz
Internal High Reference Voltage for ADC	-	-	2.55	-	V
Internal Low Reference Voltage for ADC	-	-	0.75	-	V
Pre-Amplifier Spec.					
Pre-Amplifier Voltage Gain	-	19.5	20	20.5	dB
Gain Amplifier Spec.					
Voltage Amplifier Gain	-	49	50	51	dB
Output Voltage Swing	-	-	1.6	-	Vp-p
Output Voltage	-	0.85	-	2.45	V
ALC Circuit Spec.					
ALC Detection Level	MIC input = 7.5mV	-40	-	-	dBm
ALC Operating Range	-	36	40	44	dB
LPF Spec					
Pass-Band Ripple	-	-	-	0.5	dB
Pass-Band Cutoff Frequency	-	-	4	-	kHz
Stop-Band Attenuation @ 24kHz	-	70	-	-	dB
Stop-Band Attenuation @ 48kHz	-	90	-	-	dB
DAC					
DAC Resolution	-	-	10	-	Bits
DAC Sampling Frequency	-	-	48	-	kHz
Reference Voltage (Vref)	-	1.45	1.65	1.85	V
Minimum Analog Output Voltage	-	0.45	0.65	0.85	V
Maximum Analog Output Voltage	-	2.45	2.65	2.85	V
Full Scale Voltage Range	VDA=3.3V	-5%	2.0	+5%	V
Analog Output Impedance at Each Output Pin	-	-	-	200	Ω
Analog Output Capacitance at Each Output Pin	-	-	-	20	pF
External Load Impedance	-	-	32	-	Ω
Volume Control Step	-	-	16	-	Step

10 Application Circuit

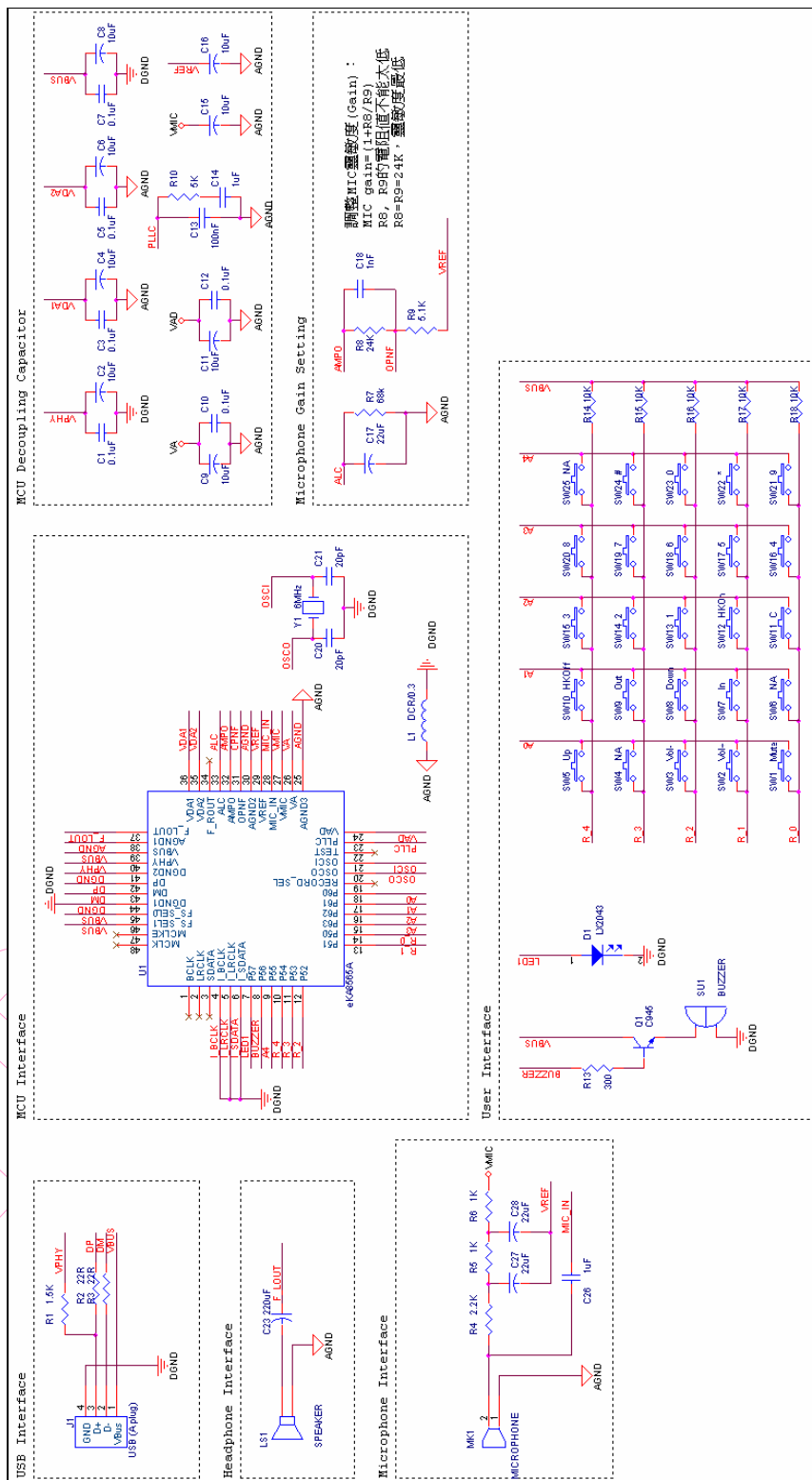


Fig 10-1 EKA8565A 48-pin Application Circuit

11 I²S Interface Signal

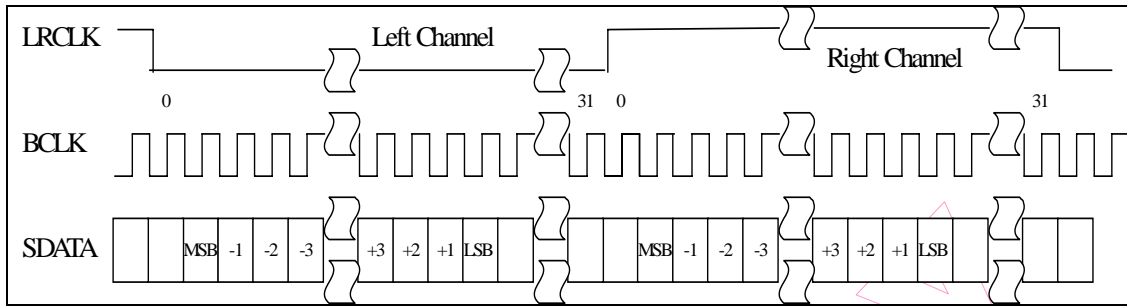


Fig 11-1 I²S Justified Audio Stream Format

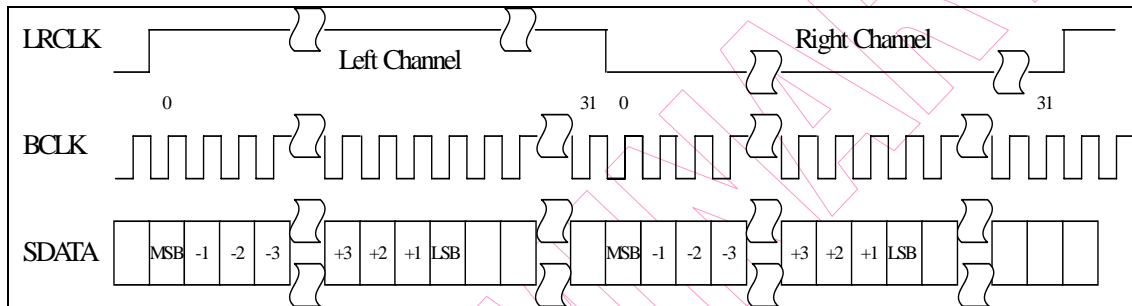


Fig 11-2 Left Justified Audio Stream Format

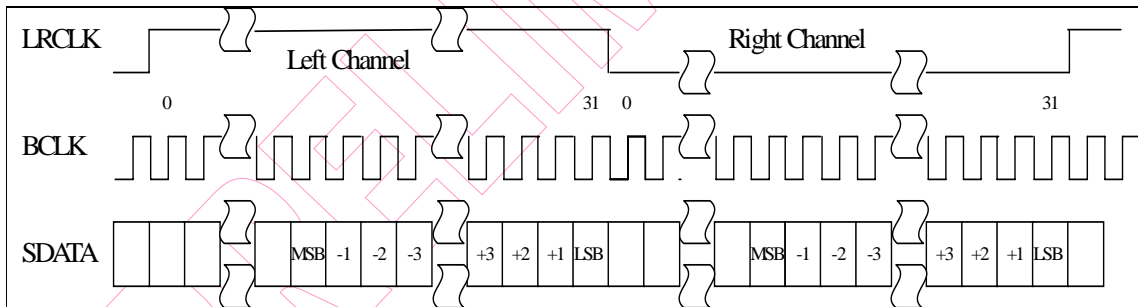


Fig 11-3 Right Justified Audio Stream Format

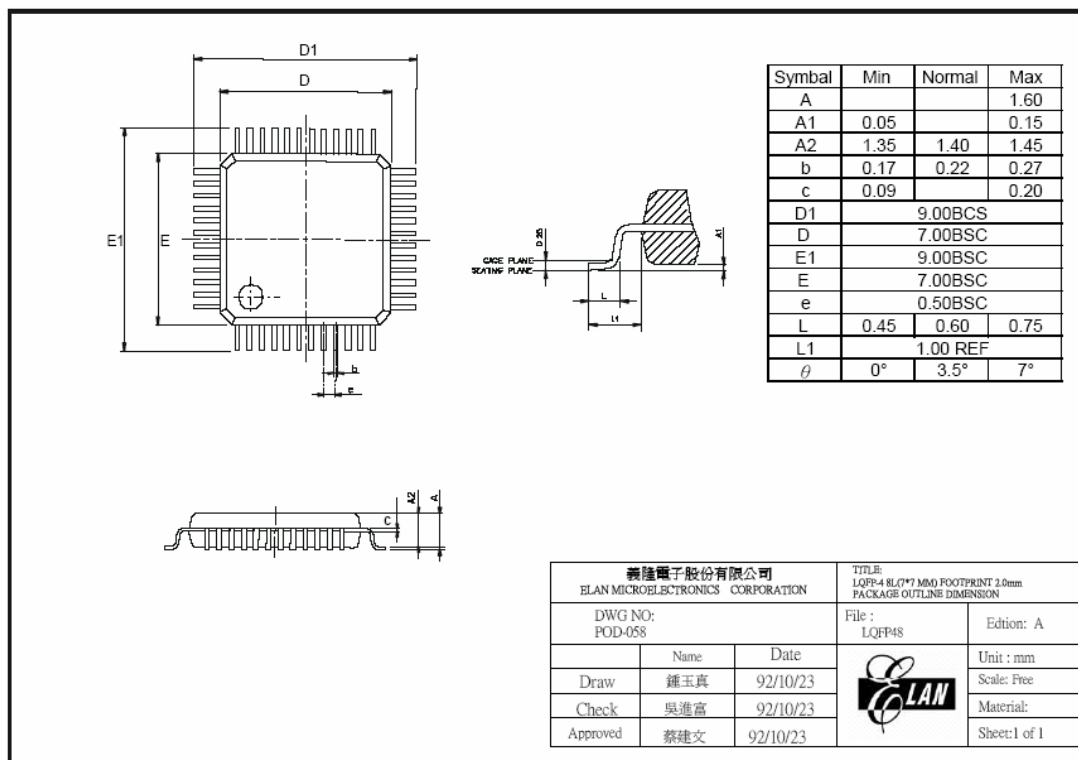
The LRCLK and BCLK are derived from MCLK. The frequency ratio

MCLK : LRCLK:BCLK = 256: 1 : 64.

The frequency of LRCLK equals the sampling rate 48kHz, 44.1kHz, 32kHz or 8kHz based on FS_SEL0 and FS_SEL1 pins status.

12 Package

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