

Precision, Low Noise FGA™ Voltage References

The ISL21009 FGA™ voltage references are extremely low power, high precision, and low noise voltage references fabricated on Intersil's proprietary Floating Gate Analog technology. The ISL21009 features very low noise ($4\mu\text{V}_{\text{P-P}}$ for 0.1Hz to 10Hz), low operating current (180 μA , Max), and 3ppm/°C of temperature drift. In addition, the ISL21009 family features guaranteed initial accuracy as low as $\pm 0.5\text{mV}$

This combination of high initial accuracy, low drift, and low output noise performance of the ISL21009 enables versatile high performance control and data acquisition applications with low power consumption.

Available Options

PART NUMBER	V _{OUT} OPTION (V)	INITIAL ACCURACY (mV)	TEMPCO. (ppm/°C)
ISL21009BFB812Z <i>Coming Soon</i>	1.250	± 0.5	3
ISL21009CFB812Z <i>Coming Soon</i>	1.250	± 1.0	5
ISL21009DFB812Z <i>Coming Soon</i>	1.250	± 2.0	10
ISL21009BFB825Z	2.500	± 0.5	3
ISL21009CFB825Z	2.500	± 1.0	5
ISL21009DFB825Z	2.500	± 2.0	10
ISL21009BFB850Z	5.000	± 0.5	3
ISL21009CFB850Z	5.000	± 1.0	5
ISL21009DFB850Z	5.000	± 2.0	10

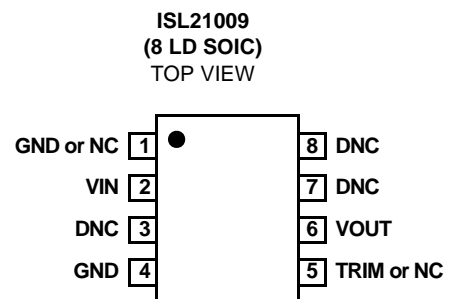
Features

- Output Voltages 1.25V, 2.500V, 5.000V
- Initial Accuracy $\pm 0.5\text{mV}$, $\pm 1.0\text{mV}$, $\pm 2.0\text{mV}$
- Input Voltage Range Up to 16.5V
- Output Voltage Noise $4\mu\text{V}_{\text{P-P}}$ (0.1Hz to 10Hz)
- Supply Current 180 μA (Max)
- Temperature Coefficient . . . 3ppm/°C, 5ppm/°C, 10ppm/°C
- Output Current Capability $\pm 7.0\text{mA}$
- Operating Temperature Range -40°C to +125°C
- Package 8 Ld SOIC
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- High Resolution A/Ds and D/As
- Digital Meters
- Bar Code Scanners
- Basestations
- Battery Management/Monitoring
- Industrial/Instrumentation Equipment

Pinout



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	GND or NC	Can be either Ground or No Connect
4	GND	Ground Connection
2	VIN	Power Supply Input Connection
6	VOUT	Voltage Reference Output Connection
5	TRIM	Allows user trim typically $\pm 2.5\%$. Leave Unconnected when unused.
3,7,8	DNC	Do Not Connect; Internal Connection – Must Be Left Floating

Ordering Information

PART NUMBER (Note)	PART MARKING	V _{OUT} OPTION (V)	GRADE	QUANTITY PER REEL/TUBE	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL21009BFB825Z	21009BF Z25	2.500	±0.5mV, 3ppm/°C	100	-40 to +125	8 Ld SOIC	M8.15
ISL21009BFB825Z-TK	21009BF Z25	2.500	±0.5mV, 3ppm/°C	1000	-40 to +125	8 Ld SOIC	M8.15
ISL21009CFB825Z	21009CF Z25	2.500	±1.0mV, 5ppm/°C	100	-40 to +125	8 Ld SOIC	M8.15
ISL21009CFB825Z-TK	21009CF Z25	2.500	±1.0mV, 5ppm/°C	1000	-40 to +125	8 Ld SOIC	M8.15
ISL21009DFB825Z	21009DF Z25	2.500	±2.0mV, 10ppm/°C	100	-40 to +125	8 Ld SOIC	M8.15
ISL21009DFB825Z-TK	21009DF Z25	2.500	±2.0mV, 10ppm/°C	1000	-40 to +125	8 Ld SOIC	M8.15
ISL21009BFB850Z	21009BF Z50	5.000	±0.5mV, 3ppm/°C	100	-40 to +125	8 Ld SOIC	M8.15
ISL21009BFB850Z-TK	21009BF Z50	5.000	±0.5mV, 3ppm/°C	1000	-40 to +125	8 Ld SOIC	M8.15
ISL21009CFB850Z	21009CF Z50	5.000	±1.0mV, 5ppm/°C	100	-40 to +125	8 Ld SOIC	M8.15
ISL21009CFB850Z-TK	21009CF Z50	5.000	±1.0mV, 5ppm/°C	1000	-40 to +125	8 Ld SOIC	M8.15
ISL21009DFB850Z	21009DF Z50	5.000	±2.0mV, 10ppm/°C	100	-40 to +125	8 Ld SOIC	M8.15
ISL21009DFB850Z-TK	21009DF Z50	5.000	±2.0mV, 10ppm/°C	1000	-40 to +125	8 Ld SOIC	M8.15

NOTES:

A) Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

B) Add "-T" suffix for tape and reel

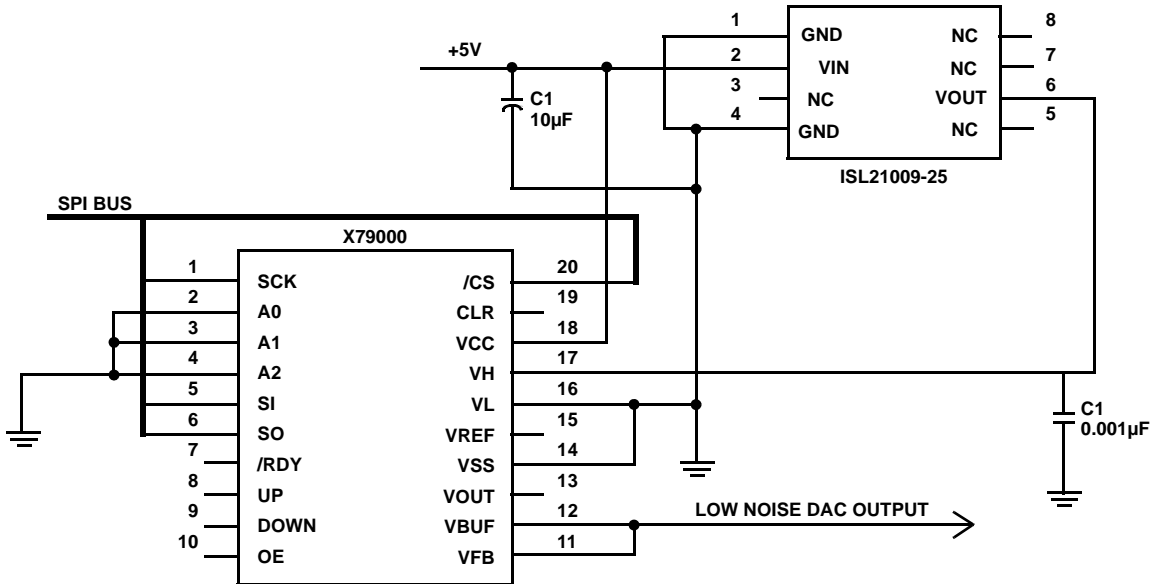


FIGURE 1. TYPICAL APPLICATION PRECISION 12-BIT SUBRANGING DAC

Electrical Specifications (ISL21009-50, $V_{OUT} = 5.0V$)

$V_{IN} = 10.0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output Voltage			5.000		V
V_{IN}	Input Voltage Range		5.5		16.5	V
I_{IN}	Supply Current			95	180	μA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$5.5V \leq V_{IN} \leq 16.5V$		20	90	$\mu V/V$
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: $0mA \leq I_{OUT} \leq 7mA$		10	60	$\mu V/mA$
		Sinking: $-7mA \leq I_{OUT} \leq 0mA$		20	100	$\mu V/mA$
$\Delta V_{OUT}/\Delta T_A$	Thermal Hysteresis (Note 2)	$\Delta T_A = +125^{\circ}C$		50		ppm

NOTES:

- Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, $-40^{\circ}C$ to $+125^{\circ}C = +165^{\circ}C$.
- Thermal Hysteresis is the change of V_{OUT} measured @ $T_A = +25^{\circ}C$ after temperature cycling over a specified range, ΔT_A . V_{OUT} is read initially at $T_A = +25^{\circ}C$ for the device under test. The device is temperature cycled and a second V_{OUT} measurement is taken at $+25^{\circ}C$. The difference between the initial V_{OUT} reading and the second V_{OUT} reading is then expressed in ppm. For $\Delta T_A = +165^{\circ}C$, the device under test is cycled from $+25^{\circ}C$ to $+125^{\circ}C$ to $-40^{\circ}C$ to $+25^{\circ}C$.
- Guaranteed by device characterization and/or correlation to other device tests.
- FGA voltage reference long term drift is a logarithmic characteristic. Changes that occur after the first few hundred hours of operation are significantly smaller with time, asymptotically approaching zero beyond 1,000 hours. Because of this decreasing characteristics, long term drift is specified in $ppm/\sqrt{1kHrs}$.

Typical Performance Curves (ISL21009-25) ($R_{EXT} = 100k\Omega$)

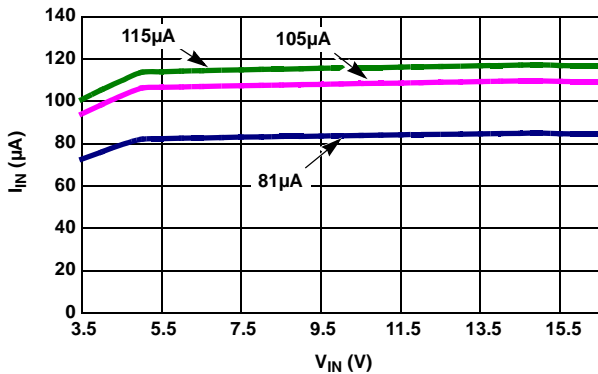


FIGURE 2. I_{IN} vs V_{IN} 3 UNITS

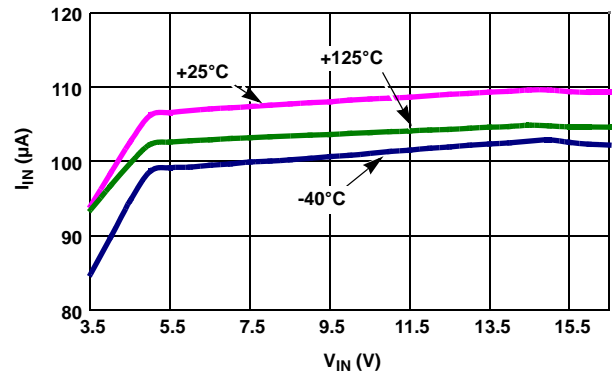


FIGURE 3. I_{IN} vs V_{IN} , 3 TEMPERATURES

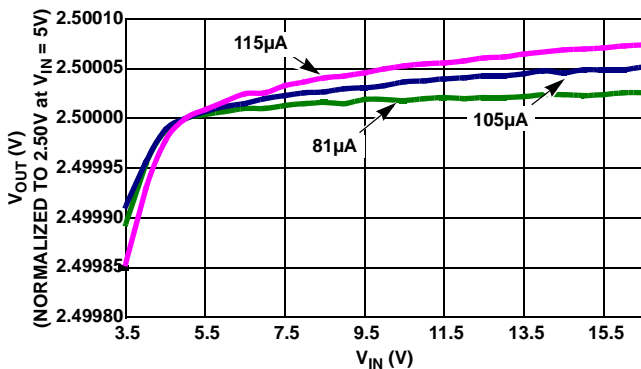


FIGURE 4. LINE REGULATION

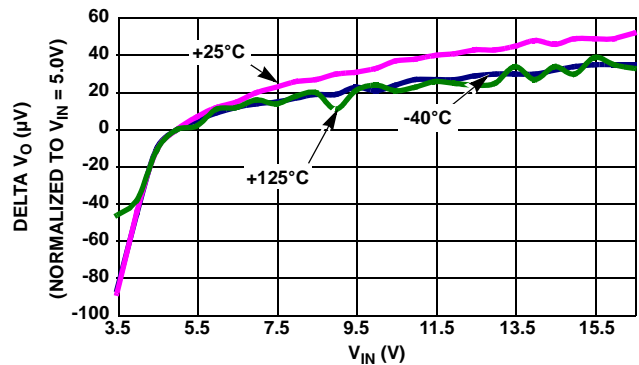


FIGURE 5. LINE REGULATION OVER TEMPERATURE

Typical Performance Curves (ISL21009-25) ($R_{EXT} = 100k\Omega$) (Continued)

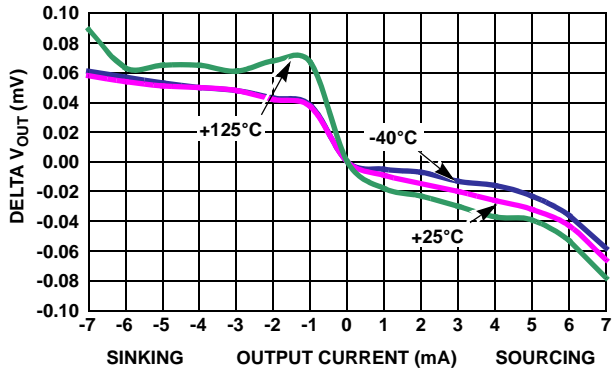


FIGURE 6. LOAD REGULATION

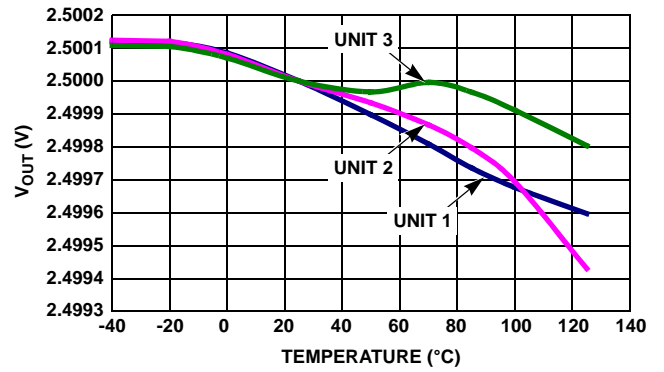


FIGURE 7. V_{OUT} vs TEMPERATURE

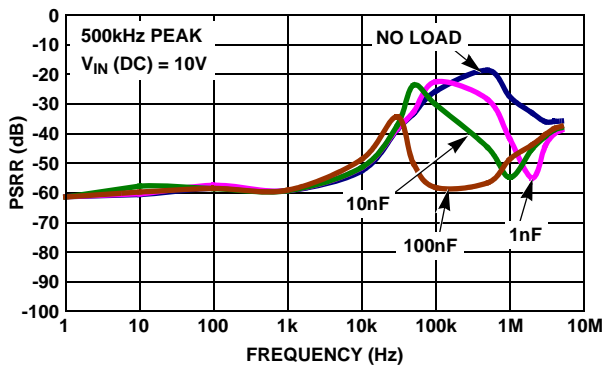


FIGURE 8. PSRR AT DIFFERENT CAPACITIVE LOADS

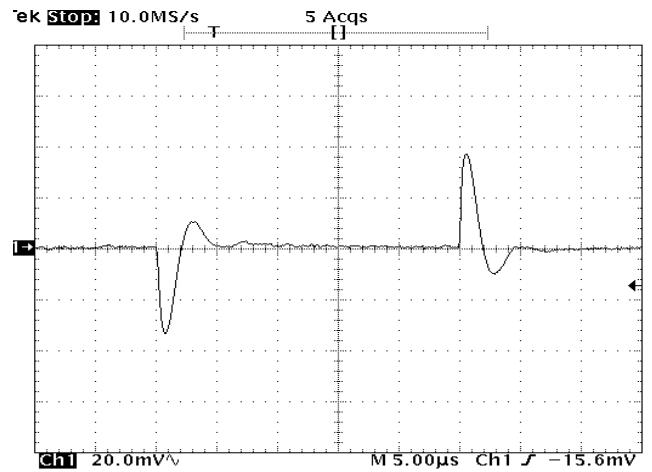


FIGURE 9. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

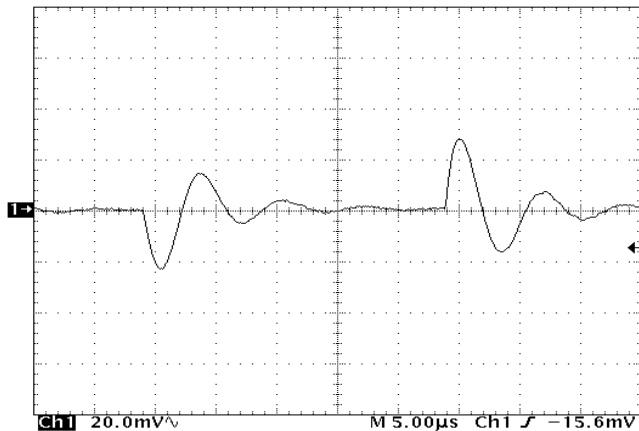


FIGURE 10. LINE TRANSIENT RESPONSE, 0.001 μ F LOAD CAPACITANCE

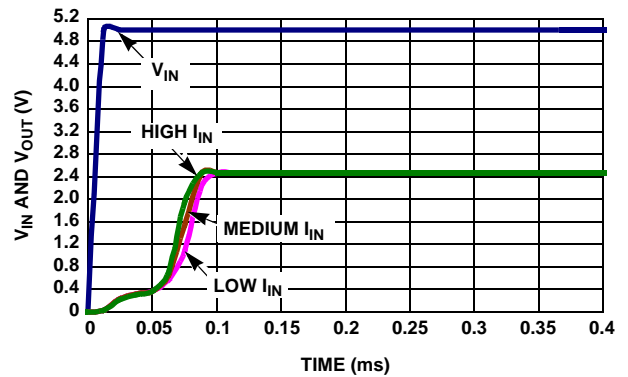


FIGURE 11. TURN ON TIME

Typical Performance Curves (ISL21009-25) ($R_{EXT} = 100k\Omega$) (Continued)

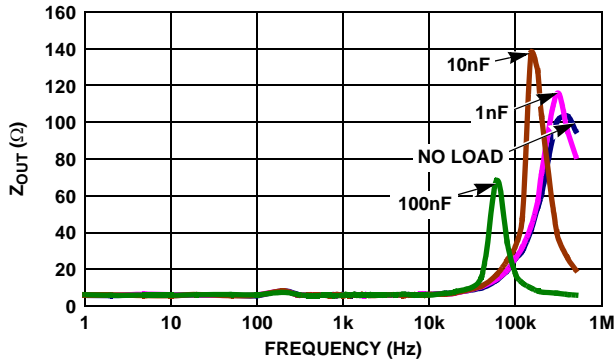


FIGURE 12. Z_{OUT} vs FREQUENCY

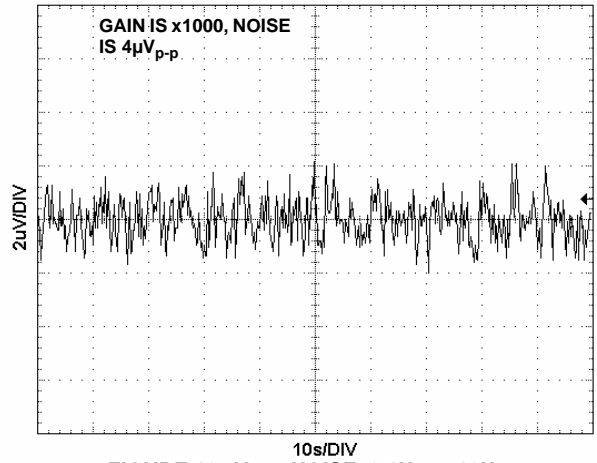


FIGURE 13. V_{OUT} NOISE, 0.1Hz to 10Hz

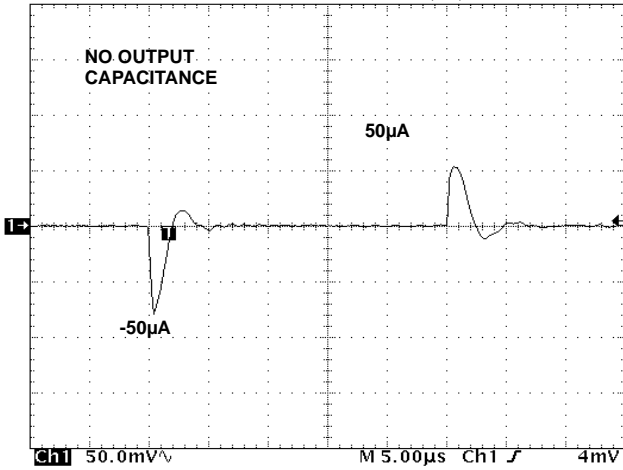


FIGURE 14. LOAD TRANSIENT RESPONSE

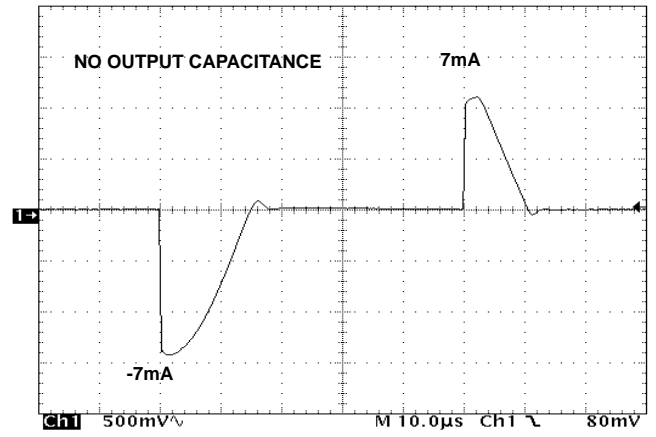


FIGURE 15. LOAD TRANSIENT RESPONSE

Typical Performance Curves (ISL21009-50) ($R_{EXT} = 100k\Omega$)

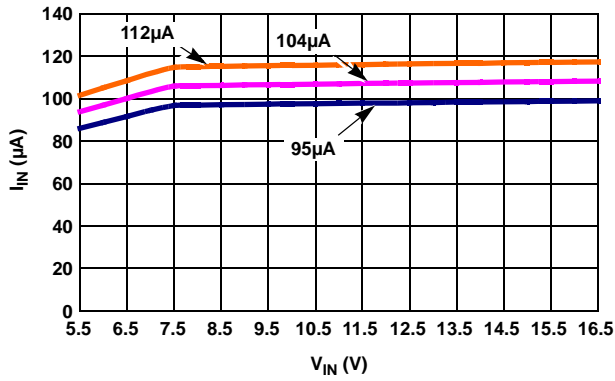


FIGURE 16. I_{IN} vs V_{IN} 3 UNITS

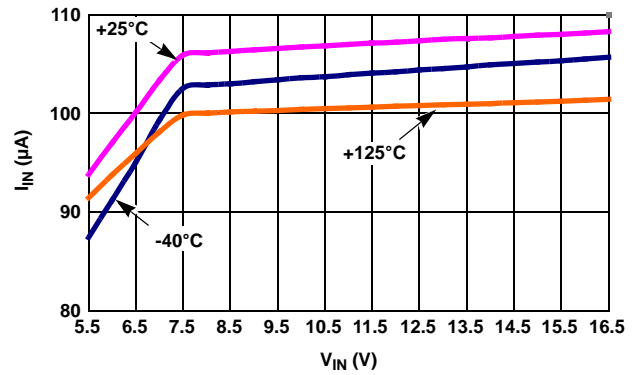


FIGURE 17. I_{IN} vs V_{IN} , 3 TEMPERATURES

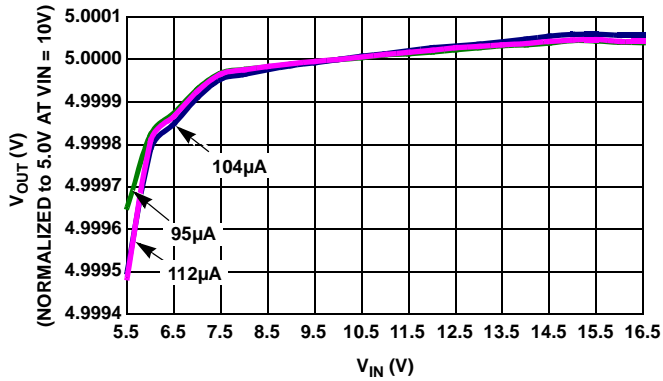


FIGURE 18. LINE REGULATION

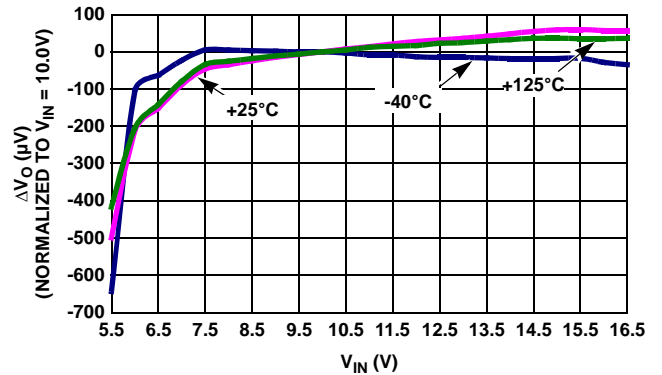


FIGURE 19. LINE REGULATION OVER TEMPERATURE

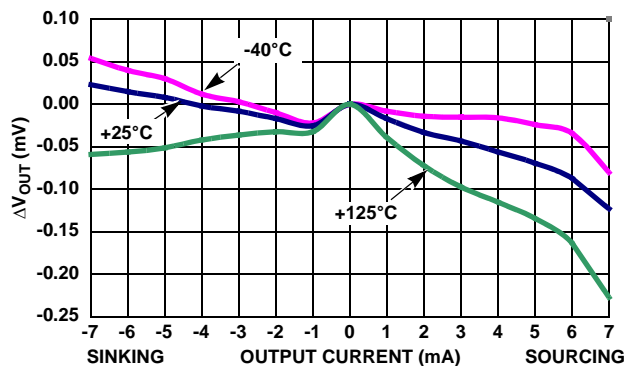


FIGURE 20. LOAD REGULATION

Typical Performance Curves (ISL21009-50) ($R_{EXT} = 100k\Omega$) (Continued)

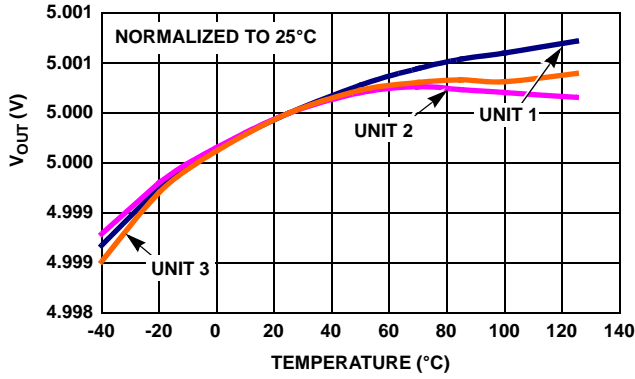


FIGURE 21. V_{OUT} vs TEMPERATURE

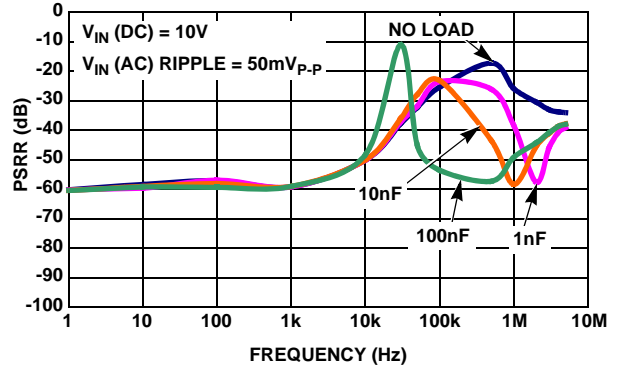


FIGURE 22. PSRR AT DIFFERENT CAPACITIVE LOADS

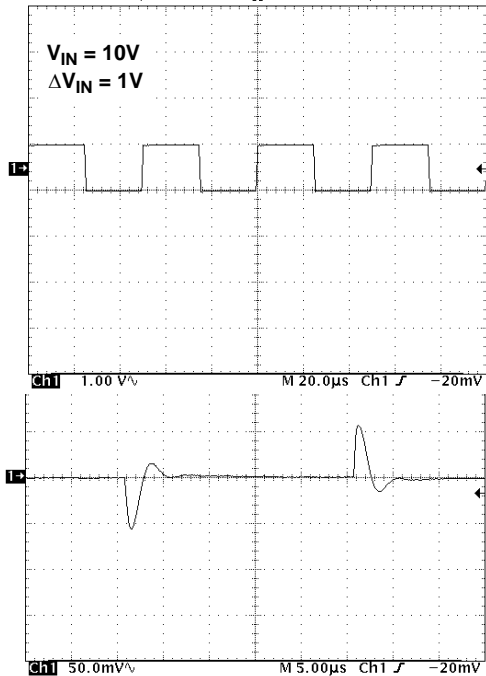


FIGURE 23. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

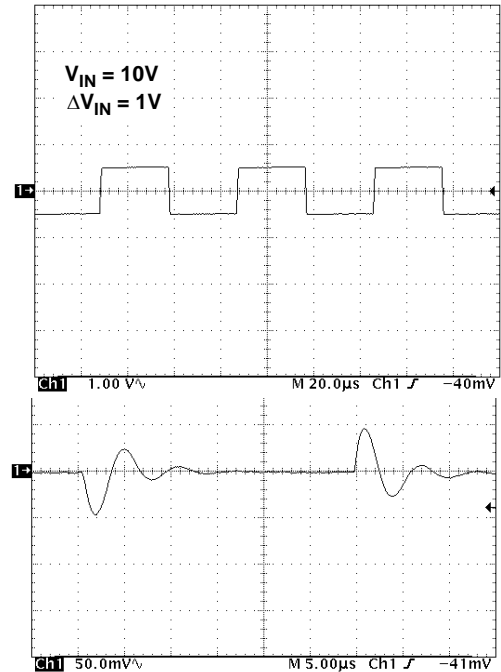


FIGURE 24. LINE TRANSIENT RESPONSE, 0.001 μ F LOAD CAPACITANCE

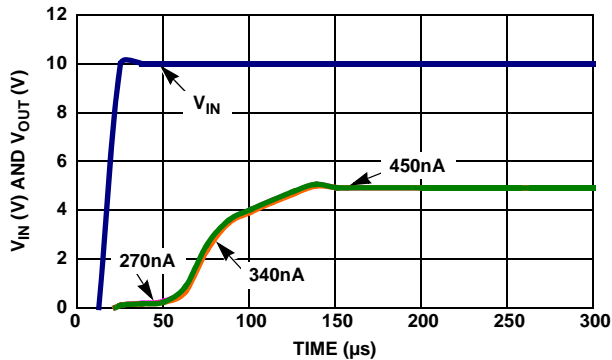


FIGURE 25. TURN ON TIME

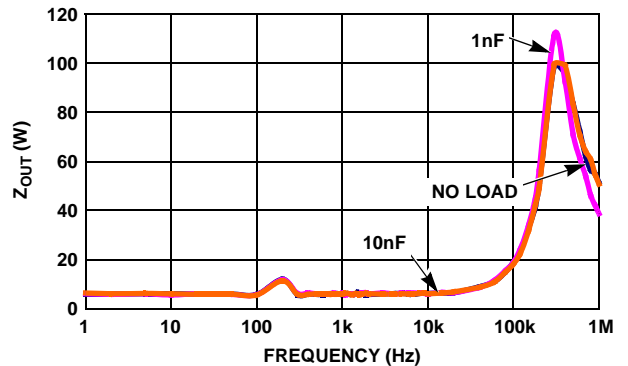
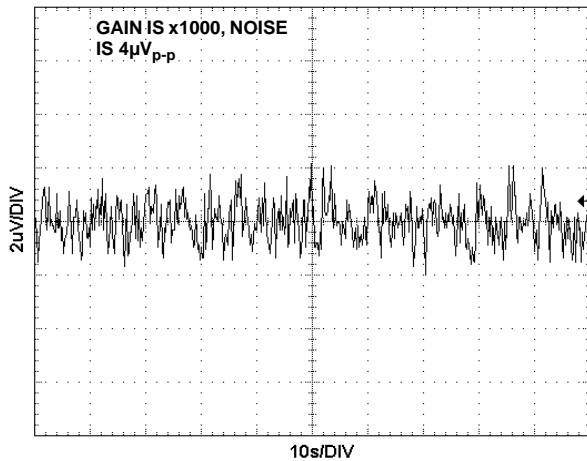
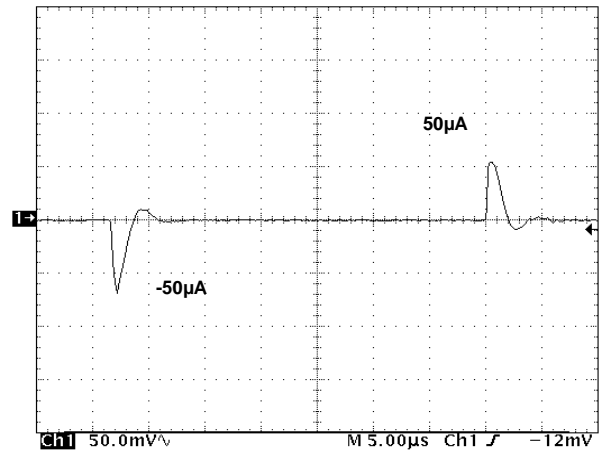
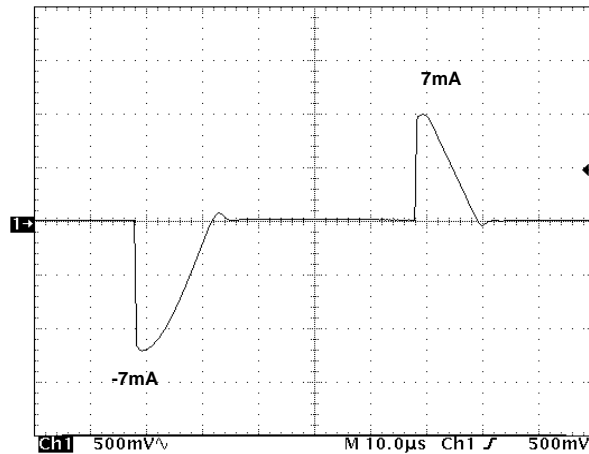


FIGURE 26. Z_{OUT} vs FREQUENCY

Typical Performance Curves (ISL21009-50) ($R_{EXT} = 100k\Omega$) (Continued)

FIGURE 27. V_{OUT} NOISE, 0.1Hz to 10Hz

FIGURE 28. LOAD TRANSIENT RESPONSE

FIGURE 29. LOAD TRANSIENT RESPONSE

Applications Information

FGA Technology

The ISL21009 voltage reference uses floating gate technology to create references with very low drift and supply current. Essentially the charge stored on a floating gate cell is set precisely in manufacturing. The reference voltage output itself is a buffered version of the floating gate voltage. The resulting reference device has excellent characteristics which are unique in the industry: very low temperature drift, high initial accuracy, and almost zero supply current. Also, the reference voltage itself is not limited by voltage bandgaps or zener settings, so a wide range of reference voltages can be programmed (standard voltage settings are provided, but customer-specific voltages are available).

The process used for these reference devices is a floating gate CMOS process, and the amplifier circuitry uses CMOS transistors for amplifier and output transistor circuitry. While providing excellent accuracy, there are limitations in output noise level and load regulation due to the MOS device characteristics. These limitations are addressed with circuit techniques discussed in other sections.

Micropower Operation

The ISL21009 consumes extremely low supply current due to the proprietary FGA technology. Low noise performance is achieved using optimized biasing techniques. Supply current is typically $95\mu A$ and noise is $4\mu V_{P-P}$ benefiting precision, low noise portable applications such as handheld meters and instruments.

Data Converters in particular can utilize the ISL21009 as an external voltage reference. Low power DAC and ADC circuits will realize maximum resolution with lowest noise.

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a plastic SOIC package which will subject the die to mild stresses when the PC board is heated and cooled and slightly changes shape. Placing the device in areas subject to slight twisting can cause degradation of the accuracy of the reference voltage due to these die stresses. It is normally best to place the device near the edge of a board, or the shortest side, as the axis of bending is most limited at that location. Mounting the device in a cutout also minimizes flex. Obviously mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically $4\mu\text{V}_{\text{P-P}}$. The noise measurement is made with a bandpass filter made of a 1 pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.9Hz bandwidth. Noise in the 10kHz to 1MHz bandwidth is approximately $40\mu\text{V}_{\text{P-P}}$ with no capacitance on the output. This noise measurement is made with a 2 decade bandpass filter made of a 1 pole high-pass filter with a corner frequency at 1/10 of the center frequency and 1-pole low-pass filter with a corner frequency at 10 times the center frequency. Load capacitance up to 1000pF can be added but will result in only marginal improvements in output noise and transient response. The output stage of the ISL21009 is not designed to drive heavily capacitive loads, so for load capacitances above $0.001\mu\text{F}$ the noise reduction network shown in Figure 30 is recommended. This network reduces noise significantly over the full bandwidth. Noise is reduced to less than $20\mu\text{V}_{\text{P-P}}$ from 1Hz to 1MHz using this network with a $0.01\mu\text{F}$ capacitor and a $2\text{k}\Omega$ resistor in series with a $10\mu\text{F}$ capacitor. Also, transient response is improved with higher value output capacitor. The $0.01\mu\text{F}$ value can be increased for better load transient response with little sacrifice in output stability.

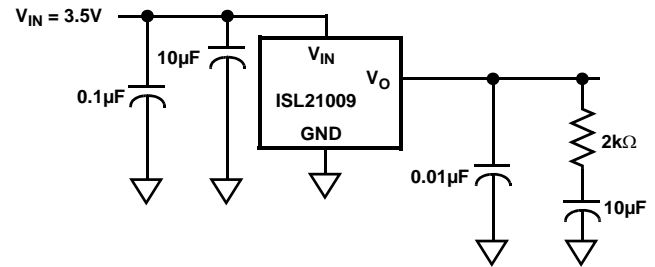


FIGURE 30. HANDLING HIGH LOAD CAPACITANCE

Turn-On Time

The ISL21009 devices have low supply current and thus the time to bias up internal circuitry to final values will be longer than with higher power references. Normal turn-on time is typically $100\mu\text{s}$. This is shown in Figure 11. Circuit design must take this into account when looking at power up delays or sequencing.

Temperature Coefficient

The limits stated for temperature coefficient (tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, $(V_{\text{HIGH}} - V_{\text{LOW}})$, and divide by the temperature extremes of measurement $(T_{\text{HIGH}} - T_{\text{LOW}})$. The result is divided by the nominal reference voltage (at $T = +25^\circ\text{C}$) and multiplied by 10^6 to yield ppm/ $^\circ\text{C}$. This is the "Box" method for specifying temperature coefficient.

Output Voltage Adjustment

The output voltage can be adjusted up or down by 2.5% by placing a potentiometer from V_{out} to ground, and connecting the wiper to the TRIM pin. The TRIM input is high impedance, so no series resistance is needed. The resistor in the potentiometer should be a low tempco ($<50\text{ppm}/^\circ\text{C}$) and the resulting voltage divider should have very low tempco $<5\text{ppm}/^\circ\text{C}$. A digital potentiometer such as the ISL95810 provides a low tempco resistance and excellent resistor and tempco matching for trim applications.

Typical Application Circuits

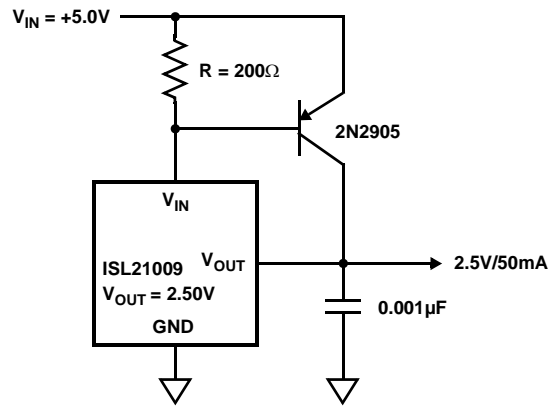


FIGURE 31. PRECISION 2.5V 50mA REFERENCE

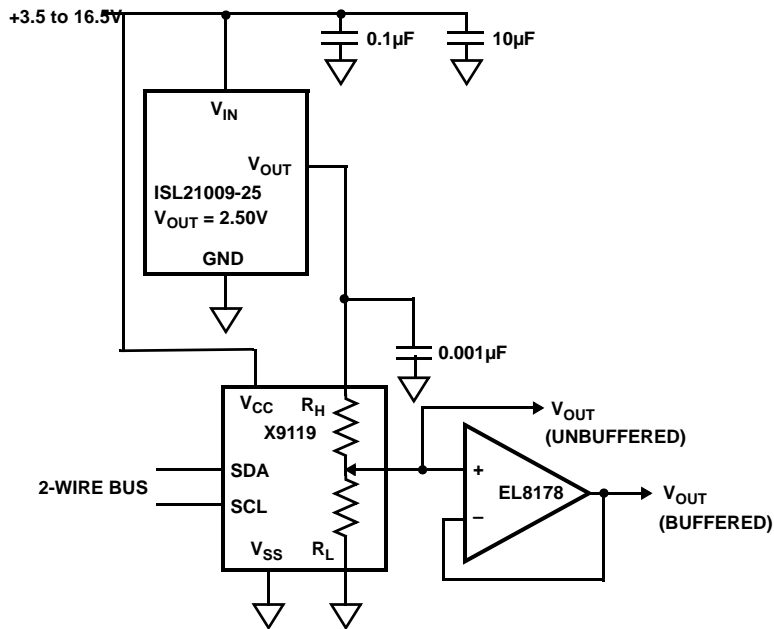


FIGURE 32. 2.5V FULL SCALE LOW-DRIFT, LOW NOISE, 10-BIT ADJUSTABLE VOLTAGE SOURCE

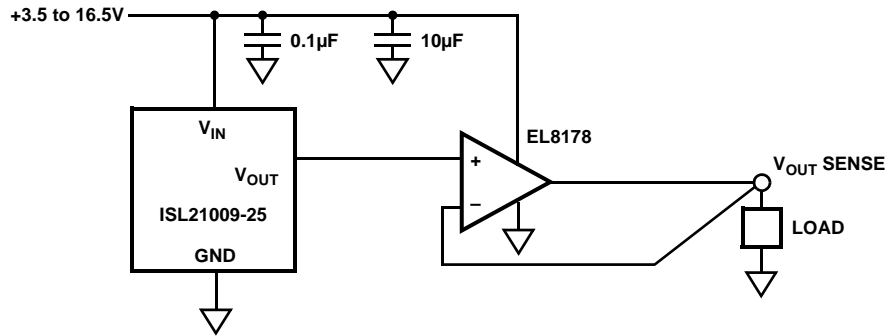


FIGURE 33. KELVIN SENSED LOAD

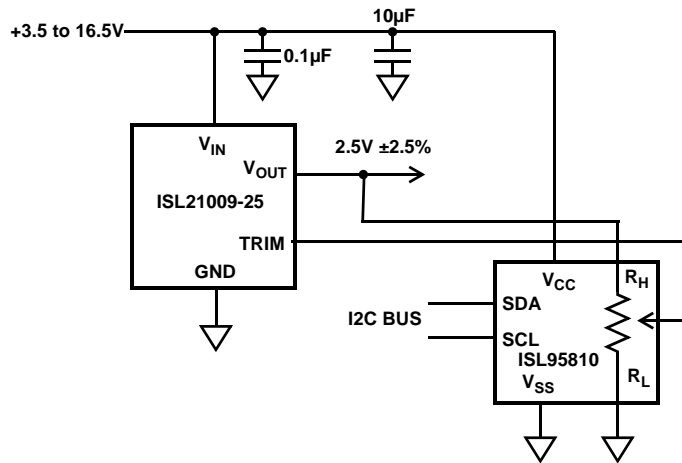
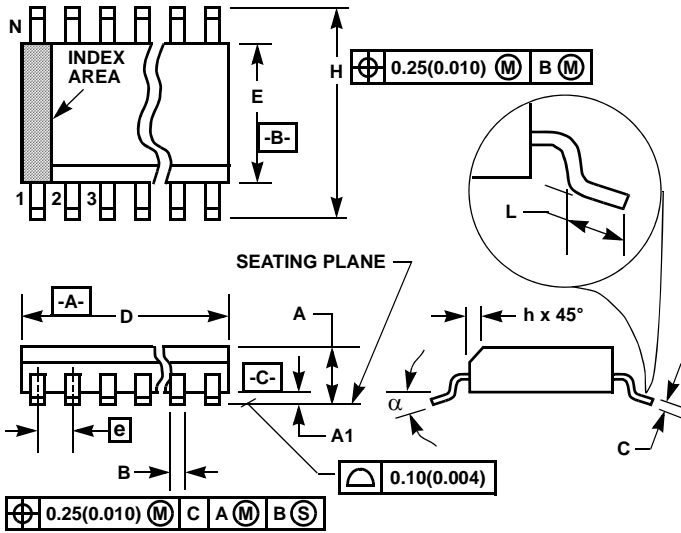


FIGURE 34. OUTPUT ADJUSTMENT USING THE TRIM PIN

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
a	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 1 6/05

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