MT6223 GSM/GPRS Baseband Processor Technical Brief

Revision 1.02

Jun 13, 2007

Revision History

Revision	Date	Comments
1.00	May29, 2007	First Release
1.01	Jun 7th, 2007	Add MT6223P product branch
1.02	Jun 13, 2007	1. Correct the typo in row number of TFBGA dimension 2. BPI_BUS2 should be placed in ball number R3, and number U2 have no ball out
1.03	Jun 14, 2007	1. Modify TFBGA diagram figure

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1. System Overview

MT6223 is an entry level chipset solution with class 12 GPRS/GSM modem. It integrates only only analog baseband but also power management blocks into one chip and can greatly reduce the component count and make smaller PCB size. Besides, MT6223 is capable of SAIC (Single Antenna Interference Cancellation) and AMR speech. Based on 32 bit ARM7EJ-S™ RISC processor, MT6223 provides an unprecedented platform for high quality modem performance.

Typical application diagram is shown in **Figure** 1.

Platform

MT6223 runs the ARM7EJ-S™ RISC processor at up to 52Mhz, thus providing best trade-off between system performance and power consumption.

For large amount of data transfer, high performance DMA (Direct Memory Access) with hardware flow control is implemented, which greatly enhances the data movement speed while reducing MCU processing load.

Targeted as a modem-centric platform for mobile applications, MT6223 also provides hardware security digital rights management for copyright protection. For further safeguarding, and to protect manufacturer's development investment, hardware flash content protection is also provided to prevent unauthorized porting of software load.

Memory

MT6223 supports up to 4 external state-of-the-art devices through its 8/16-bit host interface. Devices such as burst/page mode Flash, page mode SRAM, and Pseudo SRAM are supported including ADMUX type devices. For greatest compatibility, the memory interface can also be used to connect to legacy devices such as Color/Parallel LCD, and multi-media companion chip are all supported through this interface. To minimize power consumption and ensure low noise, this interface is designed for flexible I/O voltage and allows lowering of supply voltage down to 1.8V. The driving strength is configurable for signal integrity adjustment. The data bus also employs retention technology to prevent the bus from floating during turn over.

Multi-media

MT6223 utilize high resolution audio DAC, digital audio, and audio synthesis technology to provide superior audio features., e.g. MP3 ring tone. For MT6223P, MP3 player is also supported.

Connectivity, and Storage

MT6223 supports UART as well as Bluetooth interface. Also, necessary peripheral blocks are embedded for a voice centric phone: Keypad Scanner with the capability to detect multiple key presses, SIM Controller, Alerter, Real Time Clock, PWM, Serial LCD Controller, and General Purpose Programmable I/Os.

Furthermore, to provide more configuration and bandwidth for display, an additional 9-bit parallel interface is incorporated.

For MT6223P, software memory card control is provided through LCD interface, including SD and mini SD, etc. Therefore high quality MP3 playback of 48kHz sampling with 320kbps format can be supported

Audio

Using a highly integrated mixed-signal Audio Front-End, architecture of MT6223 allows for easy audio interfacing with direct connection to the audio transducers. The audio interface integrates D/A and A/D Converters for Voice band, as well as high resolution Stereo D/A Converters for Audio band. In addition, MT6223 also provides Stereo Input and Analog Mux. MT6223 also supports AMR codec to adaptively optimize speech and audio quality.

Radio

MT6223 integrates a mixed-signal Baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. It contains gain and offset calibration mechanisms, and filters with programmable coefficients for comprehensive compatibility control on RF modules. This approach also allows the usage of a high resolution D/A Converter for controlling VCXO or crystal, thus reducing the need for expensive TCVCXO. MT6223 achieve great MODEM performance by utilizing 14-bit high resolution A/D Converter in the RF downlink path. Furthermore, to reduce the need for extra external current-driving

component, the driving strength of some BPI outputs is designed to be configurable.

Debug Function

The JTAG interface enables in-circuit debugging of software program with the ARM7EJ-S core. With this standardized debugging interface, MT6223 provides developers with a wide set of options in choosing ARM development kits from different third party vendors.

Low Power Features

MT6223 offers various low-power features to help reduce system power consumption. These features include Pause Mode of 32KHz clocking at Standby State, Power Down Mode for individual peripherals, and Processor Sleep Mode. In addition, MT6223 are also fabricated in advanced low leakage CMOS process, hence providing an overall ultra low leakage solution.

Power Management

MT6223 integrates all regulators that a voice-centric phone needs. Seven LDOs optimized for Specific GSM/GPRS baseband sub-systems are included, and a RF transceiver needed LDO is also built-in. Besides Li-Ion battery charge function, SIM card level shifter interface, two open-drain output switches to control the LED and vibrator are equipped. Other power management schemes such as thermal overload protection, Under Voltage Lock-out Protection (UVLO), over voltage protection and oower-on reset and start-up timer are also MT6223 features. Besides, 3 NMOS switches controlling the RGB LEDs are also embedded to reduce BOM coount.

Package

The MT6223 device is offered in 9mm×9mm, 224-ball, 0.5 mm pitch, TFBGA package.

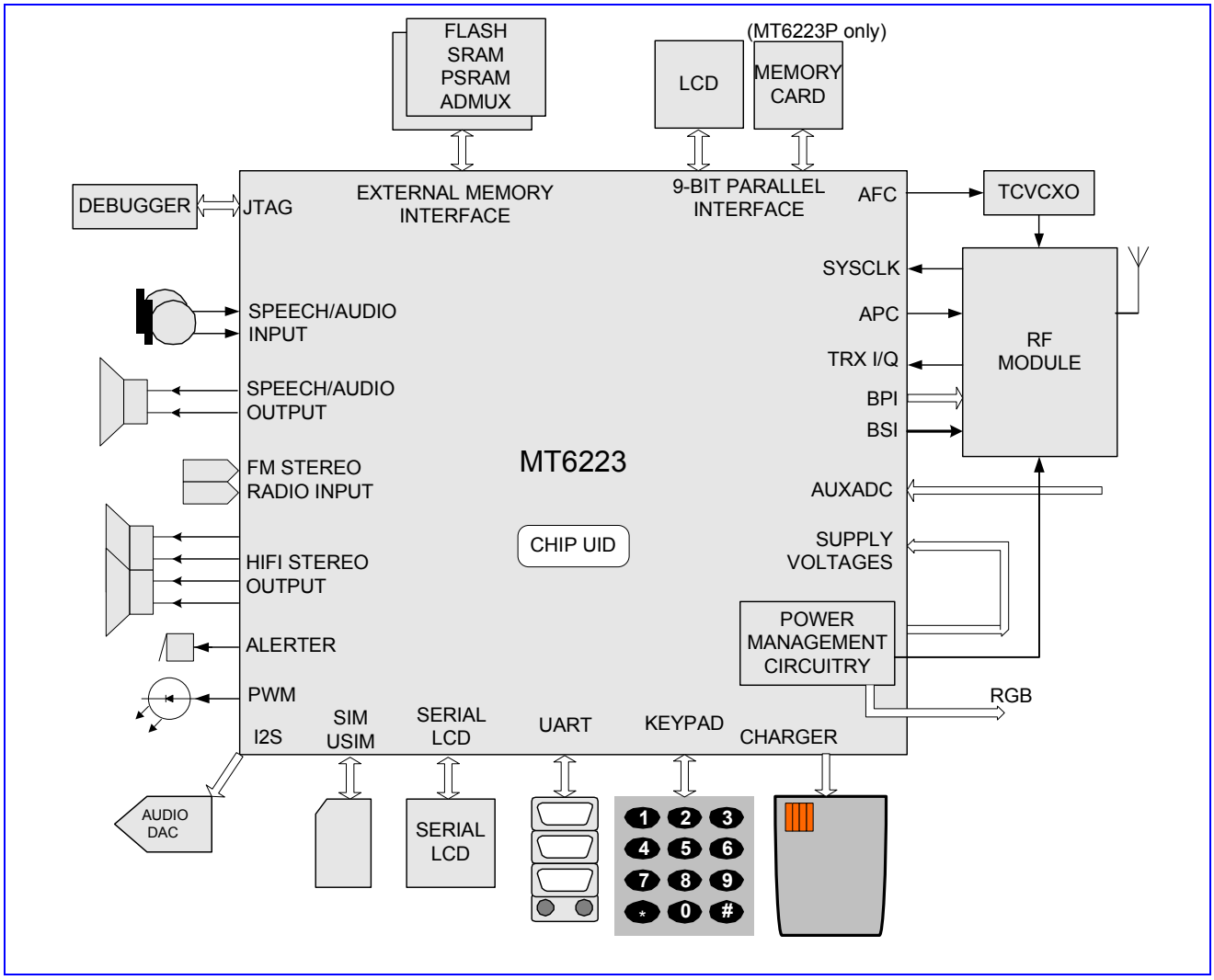


Figure 1 Typical application of MT6223.

1.1 Platform Features

- **General**
  - Integrated voice-band, audio-band and base-band analog front ends
  - TFBGA 9mm×9mm, 224-ball, 0.5 mm pitch package
- **MCU Subsystem**
  - ARM7EJ-S 32-bit RISC processor
  - High performance multi-layer AMBA bus
  - Java hardware acceleration for fast Java-based games and applets
  - Operating frequency: 26/52 MHz
  - Dedicated DMA bus
  - 7 DMA channels
  - 320K bits on-chip SRAM
  - On-chip boot ROM for Factory Flash Programming
  - Watchdog timer for system crash recovery
  - 3 sets of General Purpose Timer
  - Circuit Switch Data coprocessor
  - Division coprocessor
- **External Memory Interface**
  - Supports up to 4 external devices
  - Supports 8-bit or 16-bit memory components with maximum size of up to 32M Bytes each
  - Supports Flash and SRAM/PSRAM with Page Mode or Burst Mode
  - Supports ADMUX
  - Industry standard 9-bit Parallel LCD Interface
  - Supports multi-media companion chips with 8/16 bits data width
  - Flexible I/O voltage of 1.8V ~ 2.8V for memory interface
  - Configurable driving strength for memory interface
- **User Interfaces**
  - 5-row × 7-column keypad controller with hardware scanner
  - Supports multiple key presses for gaming
  - SIM/USIM Controller with hardware T=0/T=1 protocol control
  - Real Time Clock (RTC) operating with a separate power supply
  - General Purpose I/Os (GPIOs)
  - 2 Sets of Pulse Width Modulation (PWM) Output
  - Alerter Output with Enhanced PWM or PDM
  - 6 external interrupt lines
- **Security**
  - Supports security key and 59 bit chip unique ID
- **Connectivity**
  - 3 UARTs with hardware flow control and speed up to 921600 bps
  - DAI/PCM and I2S interface for Audio application
  - Memory card interface is provided for MT6223P
- **Low Power Schemes**
  - Power Down Mode for analog and digital circuits
  - Processor Sleep Mode
  - Pause Mode of 32KHz clocking at Standby State
  - 3-channel Auxiliary 10-bit A/D Converter for application usage other than battery monitoring
- **Power and Supply Management**
  - 2.8V to 5.5V Input Range
  - Charger Input up to 8V
  - Seven LDOs Optimized for Specific GSM Sub-systems
  - One LDO for RF transceiver

- High Operation Efficiency and Low Stand-by Current
- Li-Ion Battery Charge function
- SIM Card Interface
- Two Open-Drain Output Switches to Control the LED and Vibrator
- Three NMOS switches to control RGB LEDs
- Thermal Overload Protection
- Under Voltage Lock-out Protection
- Over Voltage Protection
- Power-on Reset and Start-up Timer

■ **Test and Debug**

- Built-in digital and analog loop back modes for both Audio and Baseband Front-End
- DAI port complying with GSM Rec.11.10
- JTAG port for debugging embedded MCU

1.2 MODEM Features

- **Radio Interface and Baseband Front End**
  - GMSK modulator with analog I and Q channel outputs
  - 10-bit D/A Converter for uplink baseband I and Q signals
  - 14-bit high resolution A/D Converter for downlink baseband I and Q signals
  - Calibration mechanism of offset and gain mismatch for baseband A/D Converter and D/A Converter
  - 10-bit D/A Converter for Automatic Power Control
  - 13-bit high resolution D/A Converter for Automatic Frequency Control
  - Programmable Radio RX filter with adaptive bandwidth control
  - Dedicated Rx filter for FB acquisition
  - 2 Channels Baseband Serial Interface (BSI) with 3-wire control
  - Bi-directional BSI interface. RF chip register read access with 3-wire or 4-wire interface.
  - 10-Pin Baseband Parallel Interface (BPI) with programmable driving strength
  - Multi-band support
- **Voice and Modem CODEC**
  - Dial tone generation
  - Voice Memo
  - Noise Reduction
  - Echo Suppression
  - Advanced Sidetone Oscillation Reduction
  - Digital sidetone generator with programmable gain
  - Two programmable acoustic compensation filters
  - GSM/GPRS quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS Modem
  - GSM Circuit Switch Data
  - GPRS Class 12
- **Voice Interface and Voice Front End**
  - Two microphone inputs sharing one low noise amplifier with programmable gain and automatic gain control (AGC) mechanism
  - Voice power amplifier with programmable gain
  - 2nd order Sigma-Delta A/D Converter for voice uplink path
  - D/A Converter for voice downlink path
  - Supports half-duplex hands-free operation
  - Compliant with GSM 03.50

1.3 Multi-Media Features

- **LCD Interface**
  - Dedicated Parallel Interface supports 2 external 8/9 bit Parallel Interface, and Serial interface for LCM
  - For MT6223P, memory card interface is shared with LCD interface. And the software memory card control is available for MP3 playback
- **LCD Controller**
  - Supports simultaneous connection to up to 3 parallel LCD or 2 serial LCD modules
  - Supports LCM format: RGB332, RGB444, RGB565, RGB666, RGB888
  - Supports LCD module with maximum resolution up to 176x220 at 24bpp
  - 2 layer blending
  - Supports hardware display rotation for each layer
- **Audio CODEC**
  - Wavetable synthesis with up to 64 tones
  - Advanced wavetable synthesizer capable of generating simulated stereo
  - Wavetable including GM full set of 128 instruments and 47 sets of percussions
  - PCM Playback and Record
  - Digital Audio Playback
- **Audio Interface and Audio Front End**
  - Supports I2S interface
  - High resolution D/A Converters for Stereo Audio playback
  - Stereo analog input for stereo audio source
  - Analog multiplexer for Stereo Audio
  - FM Radio Recording
  - Stereo to Mono Conversion

1.4 General Description

Figure 2 details the block diagram of MT6223. Based on a dual-processor architecture, MT6223 integrate both an ARM7EJ-S core and 2 digital signal processor cores. ARM7EJ-S is the main processor that is responsible for running 2G and 2.5G protocol software. Digital signal processors handle the MODEM algorithms as well as advanced audio functions. Except for some mixed-signal circuitries, the other building blocks in MT6223 are connected to either the microcontroller or one of the digital signal processor.
Specifically, both MT6223 consist of the following subsystems:

- Microcontroller Unit (MCU) Subsystem - includes an ARM7EJ-S RISC processor and its accompanying memory management and interrupt handling logics.
- Digital Signal Processor (DSP) Subsystem - includes 2 DSP cores and their accompanying memory, memory controller, and interrupt controller.
- MCU/DSP Interface - where the MCU and the DSPs exchange hardware and software information.
- Microcontroller Peripherals - includes all user interface modules and RF control interface modules.
- Microcontroller Coprocessors - runs computing-intensive processes in place of Microcontroller.
- DSP Peripherals - hardware accelerators for GSM/GPRS/EGDE channel codec.
- Voice Front End - the data path for converting analog speech from and to digital speech.
- Audio Front End - the data path for converting stereo audio from stereo audio source
- Baseband Front End - the data path for converting digital signal from and to analog signal of RF modules.
- Timing Generator - generates the control signals related to the TDMA frame timing.
- Power, Reset and Clock subsystem - manages the power, reset, and clock distribution inside MT6223
- LDOs, Power-on sequences, swicthes and SIM level shifters.

Details of the individual subsystems and blocks are described in following Chapters.

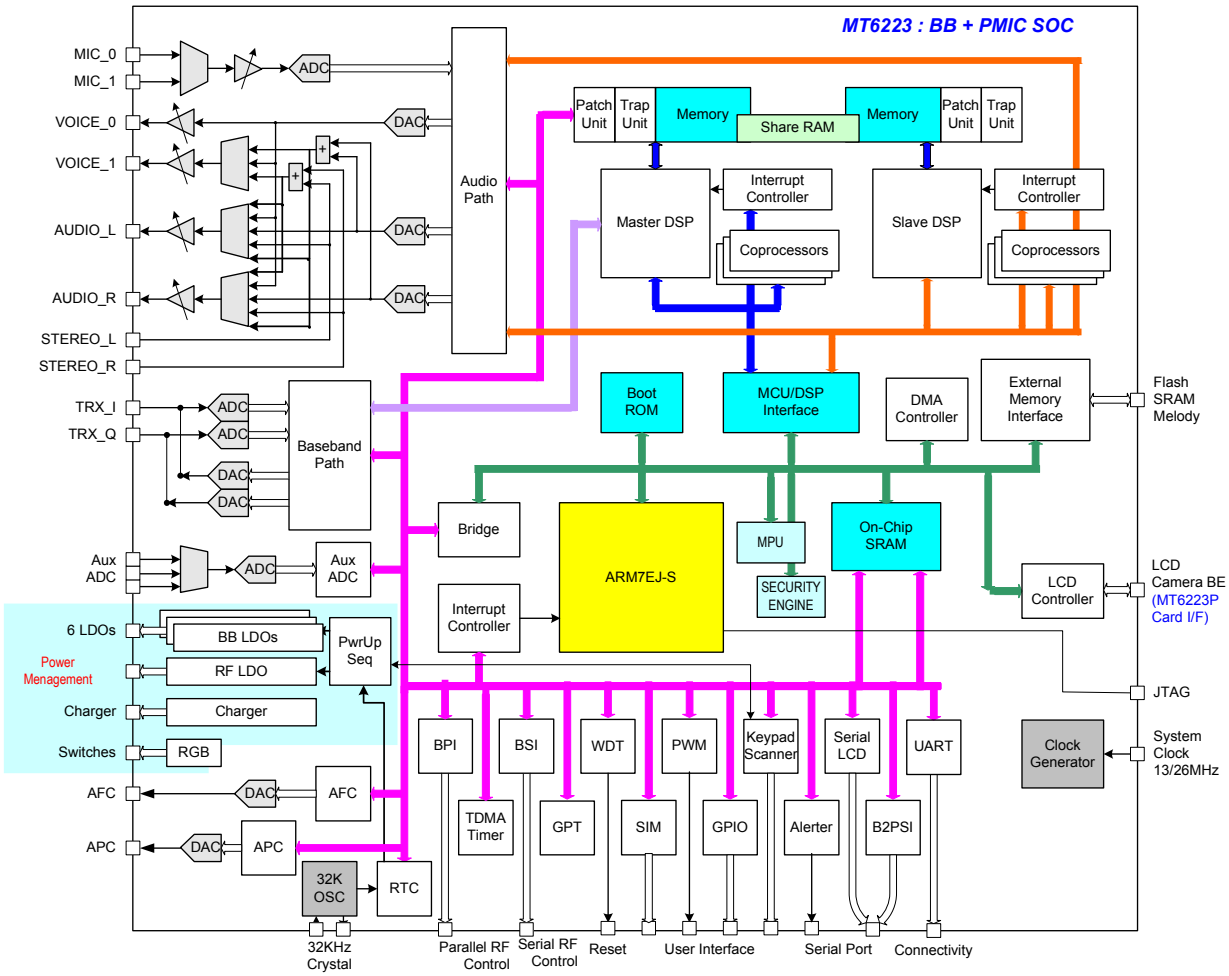


Figure 2 MT6223 block diagram.

2 Product Descriptions

2.1 Pin Outs

One type of package for this product, TFBGA 9mm * 9mm, 224-ball, 0.5mm pitch Package is offered.
Pin-outs and the top view are illustrated in **Figure 3** for this package. Outline and dimension of package is illustrated in **Figure 4**, while the definition of package is shown in **Table 1**.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
C	VA	RESET		GATEDRV	BATDET	SIMRST	URXD1	URXD2	URTS1_B	UTXD1	EINT2	KROW0	KROW3	EA22		EA21	EA20	C
D	AGND	RSTCAP	PWRKEY	LED	CHRIN	SIMCLK	BAT_BACKUP	UTXD2	VDDK	UCTS1_B	EINT3	EINT0	VDD33	EA19	EA18	EA17	EA16	D
E	AVDD_AFE	VCTXO	AU_FMINR	VMSEL										EA15	EA14	EA13	EA12	E
F	AU_MOUTR	AU_MOUTL	AU_FMINL	AVDD_MBUFL										VDD33_EMI	EA11	EA10	EA9	F
G	AU_OUT0_N	AU_OUT0_P	AU_MICBIAS_P	AVSS_MBUFL				VIBRATOR	LED_G	LED_B				VDD33_EMI	EA8	EA7	EA6	G
H	AGND_AFE	AU_MICBIAS_N	AU_VREF_NI	AU_VREF_PO			DGND	LED_R	DGND	DGND	DGND			VDDK	EA5	EA4	EA3	H
J	AU_VIN0_P	AU_VIN0_N	AVSS_AFE	AVDD_GSMRFRX			VSS33	PGND		TESTMODE	VSS33			EA2	EA1	EA0	EUB_B	J
K	AU_VIN1_N	AU_VIN1_P	AGND_RFE	AVDD_RFE			VSS33	VSS33	VSS33_EMI	VSS33_EMI	VSS33_EMI			ELB_B	ECS3_B	ECS2_B	ECS1_B	K
L	BDLAQP	BDLAQN	BDLAIN	BDLAIP				VSS33_LCD	VSS33_EMI	VSS33_EMI				ECS0_B	EWR_B	ERD_B	ED15	L
M	AVSS_GSMRFRX	AUXADIN0	AUXADIN1	AVDD_PLL										VDD33_EMI	ED14	ED13	ED12	M
N	APC	AUXADIN2	AUX_REF	VDDK										VDD33_EMI	ED11	ED10	ED9	N
P	AVSS_RFE	AFC_BYP	BPI_BUS5	VDD33	VDD33	DAISYNC	PWM	JTDI	VDDK	LCD_D6	VDD33_LCD	VDD33_EMI	EA25	ED3	ED8	ED7	ED6	P
R	AFC	BPI_BUS0	BPI_BUS2	BPI_BUS6	BSI_DATA	DAIRST	ALERTER	JTRST_B	JTDO	LCD_D7	LCD_D2	LCD_WR_B	LCD_A0	LCD_CS0_B		ED4	ED5	R
T	AVSS_PLL	BPI_BUS1	BPI_BUS4	BPI_BUS7	BSI_CS0	DAICLK	DAIPCMIN	SYSRST_B	JTMS	LCD_D8	LCD_D3	LCD_RSTB	LCD_D0	WATCHDOG	EWAIT	ED0	ED2	T
U	SYSCLK		BPI_BUS3	BPI_BUS8	BPI_BUS9	BSI_CLK	DAIPCMOUT	JRTCK	JTCK	LCD_D5	LCD_D4	LCD_D1	LCD_RD_B	LCD_CS1_B	EADV_B	ECLK	ED1	U

Figure 3 Top View of MT6223 TFBGA 9mm*9mm 0.5mm pitch package

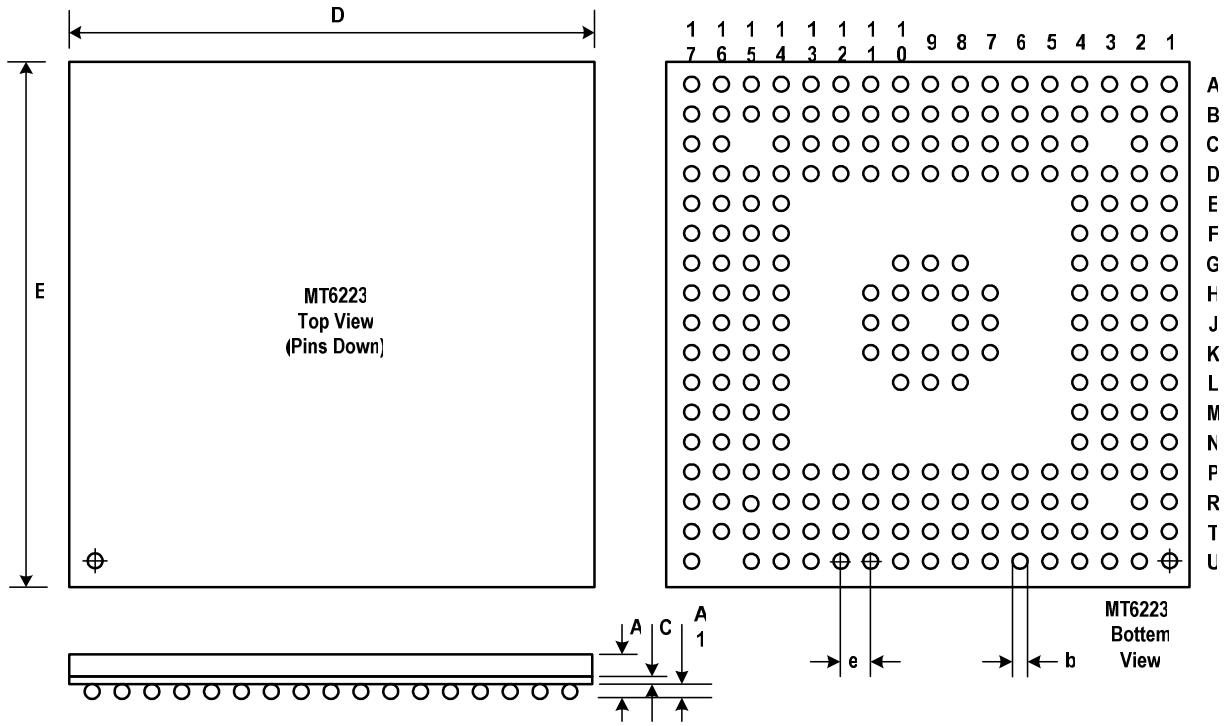


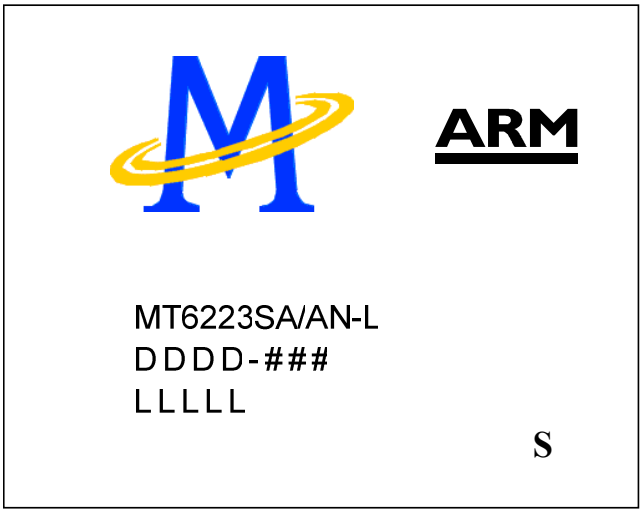
Figure 4 Outlines and Dimension of TFBGA 9mm*9mm, 224-ball, 0. 5 mm pitch Package

Body Size		Ball Count	Ball Pitch	Ball Dia.	Package Thk.	Stand Off	Substrate Thk.
D	E	N	e	b	A (Max.)	A1	C
9.0	9.0	224	0.5	0.275	1.2	0.21	0.36

Table 1 Definition of TFBGA 9mm*9mm, 224-ball, 0.5 mm pitch Package (Unit: mm)

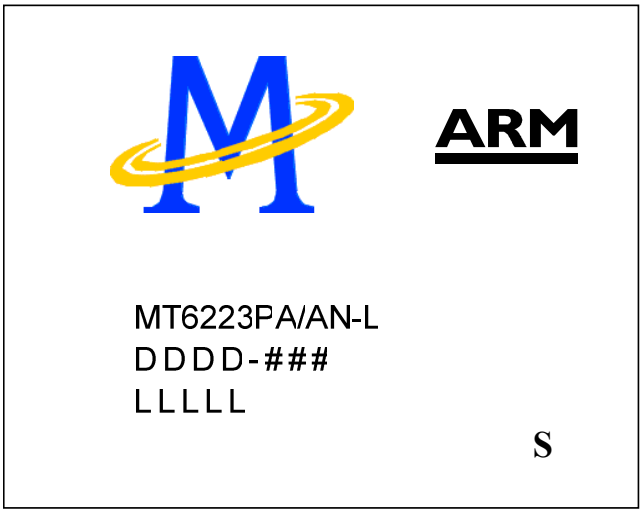
2.2 Top Marking Definition

Security version (MT6223S)



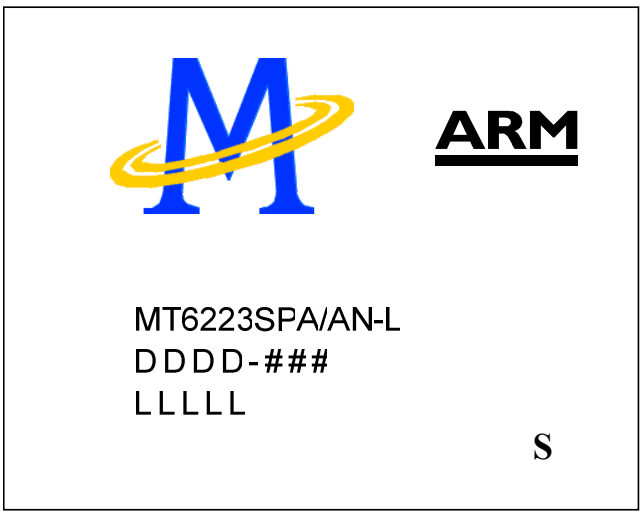
MT6223SA/AN-L: Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: Die Lot No.
S: Special Code

Memory card MP3 version (MT6223P)



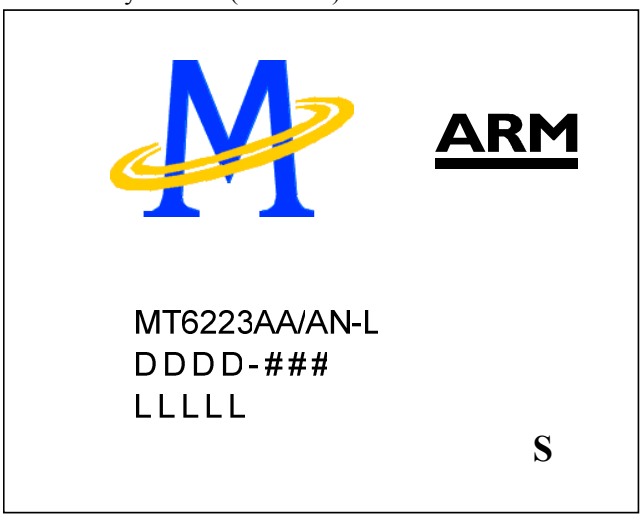
MT6223PA/AN-L: Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: Die Lot No.
S: Special Code

Security, Memory card MP3 version (MT6223SP)



MT6223SPA/AN-L: Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: Die Lot No.
S: Special Code

Non-security version (MT6223)



MT6223AA/AN-L: Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: Die Lot No.
S: Special Code

#

DC Characteristics

2.2.1 Absolute Maximum Ratings

Prolonged exposure to absolute maximum ratings may reduce device reliability. Functional operation at these maximum ratings is not implied.

Item	Symbol	Min	Max	Unit
IO power supply	VDD33	-0.3	VDD33+0.3	V
I/O input voltage	VDD33I	-0.3	VDD33+0.3	V
Operating temperature	Topr	-20	80	Celsius
Storage temperature	Tstg	-55	125	Celsius

2.3 Pin Description

Below pin description is identical for both MT6223.

BGA	NAME	Dir	PIN DESCRIPTION	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	PU/PD	Reset
			Analog Baseband Interface						
F2	AU_MOUTL		Audio analog output left channel						
F1	AU_MOUTR		Audio analog output right channel						
E3	AU_FMINR		FM radio analog input right channel						
F3	AU_FMINL		FM radio analog input left channel						
G1	AU_OUT0_N		Earphone 0 amplifier output (-)						
G2	AU_OUT0_P		Earphone 0 amplifier output (+)						
G3	AU_MICBIAS_P		Microphone bias supply (+)						
H2	AU_MICBIAS_N		Microphone bias supply (-)						
H4	AU_VREF_PO		Audio reference voltage (+)						
H3	AU_VREF_NI		Audio reference voltage (-)						
J1	AU_VIN0_P		Microphone 0 amplifier input (+)						
J2	AU_VIN0_N		Microphone 0 amplifier input (-)						
K1	AU_VIN1_N		Microphone 1 amplifier input (-)						
K2	AU_VIN1_P		Microphone 1 amplifier input (+)						
L1	BDLAQP		Quadrature (Q+) baseband codec						
L2	BDLAQN		Quadrature (Q-) baseband codec						
L3	BDLAIN		Quadrature (I-) baseband codec						
L4	BDLAIP		Quadrature (I+) baseband codec						
N1	APC		Automatic power control DAC output						
M2	AUXADIN0		Auxiliary ADC input 0						
M3	AUXADIN1		Auxiliary ADC input 1						
N2	AUXADIN2		Auxiliary ADC input 2						
N3	AUX_REF		Reference voltage of Auxiliary ADC						
R1	AFC		Automatic frequency control DAC output						
P2	AFC_BYP		Automatic frequency control DAC bypass capacitance						
			RF control circuitry						
R2	BPI_BUS0	O	RF hard-wire control bus bit 0						
T2	BPI_BUS1	O	RF hard-wire control bus bit 1						
R3	BPI_BUS2	O	RF hard-wire control bus bit 2						
U3	BPI_BUS3	O	RF hard-wire control bus bit 3						
T3	BPI_BUS4	O	RF hard-wire control bus bit 4						
P3	BPI_BUS5	O	RF hard-wire control bus bit 5						
R4	BPI_BUS6	IO	RF hard-wire control bus bit 6	BPI_BUS6	GPIO20	XADMUX		PD	
T4	BPI_BUS7	IO	RF hard-wire control bus bit 7	BPI_BUS7	GPIO21	BSI_RFIN	clk_out0	PD	
U4	BPI_BUS8	IO	RF hard-wire control bus bit 8	BPI_BUS8	GPIO22	KCOL5	clk_out1	PU	
U5	BPI_BUS9	IO	RF hard-wire control bus bit 9	BPI_BUS9	GPIO23	BSI_CS1	clk_out2		
T5	BSI_CS0	O	RF 3-wire control interface chip select 0						
R5	BSI_DATA	IO	RF 3-wire control interface data output						
U6	BSI_CLK	O	RF 3-wire control interface clock output						
			Digital Audio Interface (DAI)						
T6	DAICLK	IO	DAI interface clock output	DAICLK	GPIO15	EDICK		PU	
U7	DAIPCMOUT	IO	DAI PCM data output	DAIPCMOUT	GPIO16	EDIDAT		PD	
T7	DAIPCMIN	IO	DAI PCM data input	DAIPCMIN	GPIO17			PU	

R6	DAIRST	IO	DAI reset signal input	DAIRST	GPIO18			PU	
P6	DAISYNC	IO	DAI frame synchronization input	DAISYNC	GPIO19	EDIWS		PU	
			PWM Interface						
R7	ALERTER	IO	Pulse-width modulated signal for buzzer	ALERTER	GPIO24			PD	
P7	PWM	IO	Pulse-width modulated signal	PWM	GPIO25			PD	
			JTAG Interface						
U8	JRTCK	O	JTAG test port returned clock output					PU	
R8	JTRST_B	I	JTAG test port reset input	JTRST_B	GPIO26	EINT4		PU	
U9	JTCK	I	JTAG test port clock input					PU	
P8	JTDI	I	JTAG test port data input	JTDI	GPIO27	EINT5		PU	
T9	JTMS	I	JTAG test port mode switch	JTMS	GPIO28	EINT6		PU	
R9	JTDO	O	JTAG test port data output						
			Parallel LCD Interface						
T10	LCD_D8	IO	Parallel display interface Data 8	LCD_D8	GPIO0			PD	
R10	LCD_D7	IO	Parallel display interface Data 7	LCD_D7	GPIO1			PD	
P10	LCD_D6	IO	Parallel display interface Data 6	LCD_D6	GPIO2			PD	
U10	LCD_D5	IO	Parallel display interface Data 5	LCD_D5	GPIO3			PD	
U11	LCD_D4	IO	Parallel display interface Data 4	LCD_D4	GPIO4			PD	
T11	LCD_D3	IO	Parallel display interface Data 3	LCD_D3	GPIO5			PD	
R11	LCD_D2	IO	Parallel display interface Data 2	LCD_D2	GPIO6			PD	
U12	LCD_D1	IO	Parallel display interface Data 1	LCD_D1	GPIO7			PD	
T12	LCD_RSTB	O	Parallel display interface Reset Signal	LCD_RSTB	GPIO8			PD	
R12	LCD_WR_B	O	Parallel display interface Write Strobe	LCD_WR_B	GPIO9			PU	
U13	LCD_RD_B	O	Parallel display interface Read Strobe	LCD_RD_B	GPIO10	LCD_SCLK		PU	
T13	LCD_D0	IO	Parallel display interface Data 0	LCD_D0	GPIO11	LCD_SDA		PD	
R13	LCD_A0	O	Parallel display interface address output	LCD_A0	GPIO12	LCD_SA0		PU	
R14	LCD_CS0_B	O	Parallel display interface chip select 0 output	LCD_CS0_B	GPIO13	LCD_SCE0_B		PU	
U14	LCD_CS1_B	O	Parallel display interface chip select 1 output	LCD_CS1_B	GPIO14	LCD_SCE1_B	EINT7	PU	
			External Memory Interface						
U15	EADV_B	O	Flash, PSRAM and CellularRAM address valid, active low						
T15	EWAIT	O	Flash, PSRAM and CellularRAM data ready						
U16	ECLK	O	Flash, PSRAM and CellularRAM clock						
P13	EA25	IO	External memory CRE pin						
T16	ED0	IO	External memory data bus 0						
U17	ED1	IO	External memory data bus 1						
T17	ED2	IO	External memory data bus 2						
P14	ED3	IO	External memory data bus 3						
R16	ED4	IO	External memory data bus 4						
R17	ED5	IO	External memory data bus 5						
P17	ED6	IO	External memory data bus 6						
P16	ED7	IO	External memory data bus 7						
P15	ED8	IO	External memory data bus 8						
N17	ED9	IO	External memory data bus 9						
N16	ED10	IO	External memory data bus 10						
N15	ED11	IO	External memory data bus 11						
M17	ED12	IO	External memory data bus 12						
M16	ED13	IO	External memory data bus 13						
M15	ED14	IO	External memory data bus 14						

L17	ED15	IO	External memory data bus 15						
L16	ERD_B	O	External memory read strobe, active low						
L15	EWR_B	O	External memory write strobe, active low						
L14	ECS0_B	O	External memory chip select 0						
K17	ECS1_B	O	External memory chip select 1						
K16	ECS2_B	O	External memory chip select 2					—	
K15	ECS3_B	O	External memory chip select 3		GPIO52	MFIQ		—	
K14	ELB_B	O	External memory lower byte strobe						
J17	EUB_B	O	External memory upper byte strobe						
J16	EA0	O	External memory address bus 0	EA0	GPIO30	EA25		PD	
J15	EA1	O	External memory address bus 1						
J14	EA2	O	External memory address bus 2						
H17	EA3	O	External memory address bus 3						
H16	EA4	O	External memory address bus 4						
H15	EA5	O	External memory address bus 5						
G17	EA6	O	External memory address bus 6						
G16	EA7	O	External memory address bus 7						
G15	EA8	O	External memory address bus 8						
F17	EA9	O	External memory address bus 9						
F16	EA10	O	External memory address bus 10						
F15	EA11	O	External memory address bus 11						
E17	EA12	O	External memory address bus 12						
E16	EA13	O	External memory address bus 13						
E15	EA14	O	External memory address bus 14						
E14	EA15	O	External memory address bus 15						
D17	EA16	O	External memory address bus 16						
D16	EA17	O	External memory address bus 17						
D15	EA18	O	External memory address bus 18						
D14	EA19	O	External memory address bus 19						
C17	EA20	O	External memory address bus 20						
C16	EA21	O	External memory address bus 21						
C14	EA22	O	External memory address bus 22						
B17	EA23	O	External memory address bus 23						
B16	EA24	O	External memory address bus 24						
			System Miscellaneous						
J10	TESTMODE	I	Factory test mode enable input					PD	
T8	SYSRST_B	I	System reset input active low					PU	
T14	WATCHDOG	O	Watchdog reset output, active low	WATCHDOG	GPIO29			PD	
A17	SRCLKENAI	I	External VCTCXO enable input	SRCLKENAI	GPIO31			PD	
A16	SRCLKENA	O	External VCTCXO enable output active high						
			Keypad Interface						
A15	KCOL4	I	Keypad column 4	KCOL4	GPIO32			PU	
B15	KCOL3	I	Keypad column 3	KCOL3	GPIO33			PU	
A14	KCOL2	I	Keypad column 2	KCOL2	GPIO34			PU	
B14	KCOL1	I	Keypad column 1	KCOL1	GPIO35			PU	
A13	KCOL0	I	Keypad column 0	KCOL0	GPIO36			PU	
B13	KROW4	O	Keypad row 4	KROW4	GPIO37				
C13	KROW3	O	Keypad row 3	KROW3	GPIO38				

A12	KROW2	O	Keypad row 2	KROW2	GPIO39				
B12	KROW1	O	Keypad row 1	KROW1	GPIO40				
C12	KROW0	O	Keypad row 0	KROW0	GPIO41				
			External Interrupt Inputs						
D12	EINT0	I	External interrupt 0	EINT0				PU	
B11	EINT1	I	External interrupt 1	EINT1				PU	
C11	EINT2	I	External interrupt 2	EINT2	GPIO42		BT	PU	
D11	EINT3	I	External interrupt 3	EINT3	GPIO43	MIRQ	BE	PU	
			UART						
C10	UTXD1	O	UART 1 transmit data	UTXD1	GPIO44			PU	
D10	UCTS1_B	I	UART 1 clear to send, active low	UCTS1_B	GPIO45		SCL	PU	
C9	URTS1_B	O	UART 1 request to send, active low	URTS1_B	GPIO46		SDA	PU	
A9	UTXD3	IO	UART 3 transmit data	UTXD3	GPIO47	UCTS2_B	clk_out3	PU	
B9	URXD3	IO	UART 3 receive data	URXD3	GPIO48	URTS2_B	clk_out4	PU	
C8	URXD2	IO	UART2 receive data	URXD2	GPIO49	clk_out5		PU	
C7	URXD1	I	UART 1 receive data	URXD1	GPIO50			PU	
D8	UTXD2	IO	UART2 transmit data	UTXD2	GPIO51			PU	
			Crystal and Clock Inputs						
U1	SYSCLK		13MHz or 26MHz system clock input						
A11	XIN		32.768 KHz crystal input						
A10	XOUT		32.768 KHz crystal output						
			SIM Card Interface						
B5	SIMIO	IO	SIM Data Input / Outputs						
C6	SIMRST		SIM card reset output						
D6	SIMCLK		SIM card clock output						
			Charger and LED Driving Interface						
D5	CHRIN		Charger input						
C4	GATEDRV								
G10	LED_B								
G9	LED_G								
H8	LED_R								
D4	LED								
G8	VIBRATOR		Vibrator driving output						
			LDO Outputs						
A5	VSIM		LDO output to SIM card						
A8	VRF		RF LDO output						
B8	VRF_SENSE		RF LDO output sensing input						
A7	VCORE		Digital core voltage LDO output						
B7	VIO		Digital I/O voltage LDO output						
B6	VM		External memory LDO output						
C1	VA		Analog LDO output						
E2	VCTXO		Crystal or VCTCXO LDO output						
			PMIC Miscellaneous						
A3	VBAT_RF		RF used battery voltage input						
B3	VBAT		Battery voltage input						
B2	VBAT		Battery voltage input						
A1	VBAT		Battery voltage input						
A2	AVBAT		Battery voltage input						

D7	BAT_BACKUP								
C5	BATDET		Battery detection input						
A4	BATSENSE		Battery sense input						
B4	ISENSE		Current sense input						
C2	RESET		Powr on reset						
D2	RSTCAP		Reset capacitor connection point						
B1	VREF		Reference voltage for PMIC						
E4	VMSEL		Memory supply voltage level select input						
D3	PWRKEY		Power key press input						
			Digital Power and Grounds						
J8	PGND		PMIC ground						
H7	DGND		PMIC ground						
H11	DGND		PMIC ground						
H10	DGND		PMIC ground						
H9	DGND		PMIC ground						
K7	VSS33		Groud of chip digital part I/O circuitry						
L8	VSS33		Groud of chip digital part I/O circuitry						
K8	VSS33		Groud of chip digital part I/O circuitry						
J11	VSS33		Groud of chip digital part I/O circuitry						
J7	VSS33		Groud of chip digital part I/O circuitry						
L9	VSS33_EMI		Groud of external memory interface						
K9	VSS33_EMI		Groud of external memory interface						
L10	VSS33_EMI		Groud of external memory interface						
K10	VSS33_EMI		Groud of external memory interface						
K11	VSS33_EMI		Groud of external memory interface						
N4	VDDK		Supply voltage of digital core circuitry						
P9	VDDK		Supply voltage of digital core circuitry						
D9	VDDK		Supply voltage of digital core circuitry						
H14	VDDK		Supply voltage of digital core circuitry						
D13	VDD33		Supply voltage of digital part I/O circuitry						
P4	VDD33		Supply voltage of digital part I/O circuitry						
P5	VDD33		Supply voltage of digital part I/O circuitry						
P11	VDD33_LCD		Supply voltage of display interface I/O circuitry						
P12	VDD33_EMI		Supply voltage of external memory interface						
N14	VDD33_EMI		Supply voltage of external memory interface						
M14	VDD33_EMI		Supply voltage of external memory interface						
G14	VDD33_EMI		Supply voltage of external memory interface						
F14	VDD33_EMI		Supply voltage of external memory interface						
			Analog Power and Grounds						
K4	AVDD_RFE								
F4	AVDD_MBUFL								
J4	AVDD_GSMRFRX								
M4	AVDD_PLL								
E1	AVDD_AFE								
G4	AVSS_MBUFL								
T1	AVSS_PLL								
M1	AVSS_GSMRFRX								
P1	AVSS_RFE								

J3	AVSS_AFE								
D1	AGND								
A6	AGND_RF								
H1	AGND_AFE								
K3	AGND_RFE								
B10	AVDD_RTC		Supply voltage of real time clock circuitry						

Table 2 Pin Descriptions (**Bolded** types are functions at reset)

Power Description

NAME	IO Supply	IO GND	Core Supply	Core GND	Remark
AU_MOUTL					
AU_MOUTR					
AU_FMINR					
AU_FMINL					
AU_OUT0_N					
AU_OUT0_P					
AU_MICBIAS_P					
AU_MICBIAS_N					
AU_VREF_PO					
AU_VREF_NI					
AU_VIN0_P					
AU_VIN0_N					
AU_VIN1_N					
AU_VIN1_P					
BDLAQP					
BDLAQN					
BDLAIN					
BDLAIP					
APC					
AUXADIN0					
AUXADIN1					
AUXADIN2					
AUX_REF					
AFC					
AFC_BYP					
BPI_BUS0	VDD33	VSS33	VDDK	VSSK	
BPI_BUS1	VDD33	VSS33	VDDK	VSSK	
BPI_BUS2	VDD33	VSS33	VDDK	VSSK	
BPI_BUS3	VDD33	VSS33	VDDK	VSSK	
BPI_BUS4	VDD33	VSS33	VDDK	VSSK	
BPI_BUS5	VDD33	VSS33	VDDK	VSSK	
BPI_BUS6	VDD33	VSS33	VDDK	VSSK	
BPI_BUS7	VDD33	VSS33	VDDK	VSSK	
BPI_BUS8	VDD33	VSS33	VDDK	VSSK	
BPI_BUS9	VDD33	VSS33	VDDK	VSSK	
BSI_CS0	VDD33	VSS33	VDDK	VSSK	
BSI_DATA	VDD33	VSS33	VDDK	VSSK	
BSI_CLK	VDD33	VSS33	VDDK	VSSK	
DAICLK	VDD33	VSS33	VDDK	VSSK	
DAIPCMOUT	VDD33	VSS33	VDDK	VSSK	
DAIPCMIN	VDD33	VSS33	VDDK	VSSK	
DAIRST	VDD33	VSS33	VDDK	VSSK	
DAISYNC	VDD33	VSS33	VDDK	VSSK	

ALERTER	VDD33	VSS33	VDDK	VSSK	
PWM	VDD33	VSS33	VDDK	VSSK	
JRTCK	VDD33	VSS33	VDDK	VSSK	
JTRST_B	VDD33	VSS33	VDDK	VSSK	
JTCK	VDD33	VSS33	VDDK	VSSK	
JTDI	VDD33	VSS33	VDDK	VSSK	
JTMS	VDD33	VSS33	VDDK	VSSK	
JTDO	VDD33	VSS33	VDDK	VSSK	
LCD_D8	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D7	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D6	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D5	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D4	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D3	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D2	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D1	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_RSTB	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_WR_B	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_RD_B	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D0	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_A0	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_CS0_B	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_CS1_B	VDD33_LCD	VSS33	VDDK	VSSK	
EADV_B	VDD33_EMI	VSS33	VDDK	VSSK	
EWAIT	VDD33_EMI	VSS33	VDDK	VSSK	
ECLK	VDD33_EMI	VSS33	VDDK	VSSK	
EA25	VDD33_EMI	VSS33	VDDK	VSSK	
ED0	VDD33_EMI	VSS33	VDDK	VSSK	
ED1	VDD33_EMI	VSS33	VDDK	VSSK	
ED2	VDD33_EMI	VSS33	VDDK	VSSK	
ED3	VDD33_EMI	VSS33	VDDK	VSSK	
ED4	VDD33_EMI	VSS33	VDDK	VSSK	
ED5	VDD33_EMI	VSS33	VDDK	VSSK	
ED6	VDD33_EMI	VSS33	VDDK	VSSK	
ED7	VDD33_EMI	VSS33	VDDK	VSSK	
ED8	VDD33_EMI	VSS33	VDDK	VSSK	
ED9	VDD33_EMI	VSS33	VDDK	VSSK	
ED10	VDD33_EMI	VSS33	VDDK	VSSK	
ED11	VDD33_EMI	VSS33	VDDK	VSSK	
ED12	VDD33_EMI	VSS33	VDDK	VSSK	
ED13	VDD33_EMI	VSS33	VDDK	VSSK	
ED14	VDD33_EMI	VSS33	VDDK	VSSK	
ED15	VDD33_EMI	VSS33	VDDK	VSSK	
ERD_B	VDD33_EMI	VSS33	VDDK	VSSK	

EWR_B	VDD33_EMI	VSS33	VDDK	VSSK	
ECS0_B	VDD33_EMI	VSS33	VDDK	VSSK	
ECS1_B	VDD33_EMI	VSS33	VDDK	VSSK	
ECS2_B	VDD33_EMI	VSS33	VDDK	VSSK	
ECS3_B	VDD33_EMI	VSS33	VDDK	VSSK	
ELB_B	VDD33_EMI	VSS33	VDDK	VSSK	
EUB_B	VDD33_EMI	VSS33	VDDK	VSSK	
EA0	VDD33_EMI	VSS33	VDDK	VSSK	
EA1	VDD33_EMI	VSS33	VDDK	VSSK	
EA2	VDD33_EMI	VSS33	VDDK	VSSK	
EA3	VDD33_EMI	VSS33	VDDK	VSSK	
EA4	VDD33_EMI	VSS33	VDDK	VSSK	
EA5	VDD33_EMI	VSS33	VDDK	VSSK	
EA6	VDD33_EMI	VSS33	VDDK	VSSK	
EA7	VDD33_EMI	VSS33	VDDK	VSSK	
EA8	VDD33_EMI	VSS33	VDDK	VSSK	
EA9	VDD33_EMI	VSS33	VDDK	VSSK	
EA10	VDD33_EMI	VSS33	VDDK	VSSK	
EA11	VDD33_EMI	VSS33	VDDK	VSSK	
EA12	VDD33_EMI	VSS33	VDDK	VSSK	
EA13	VDD33_EMI	VSS33	VDDK	VSSK	
EA14	VDD33_EMI	VSS33	VDDK	VSSK	
EA15	VDD33_EMI	VSS33	VDDK	VSSK	
EA16	VDD33_EMI	VSS33	VDDK	VSSK	
EA17	VDD33_EMI	VSS33	VDDK	VSSK	
EA18	VDD33_EMI	VSS33	VDDK	VSSK	
EA19	VDD33_EMI	VSS33	VDDK	VSSK	
EA20	VDD33_EMI	VSS33	VDDK	VSSK	
EA21	VDD33_EMI	VSS33	VDDK	VSSK	
EA22	VDD33_EMI	VSS33	VDDK	VSSK	
EA23	VDD33_EMI	VSS33	VDDK	VSSK	
EA24	VDD33_EMI	VSS33	VDDK	VSSK	
TESTMODE	VDD33	VSS33	VDDK	VSSK	
SYSRST_B	VDD33	VSS33	VDDK	VSSK	
WATCHDOG	VDD33_EMI	VSS33	VDDK	VSSK	
SRCLKENAI	VDD33	VSS33	VDDK	VSSK	
SRCLKENA	VDD33	VSS33	VDDK	VSSK	
KCOL4	VDD33	VSS33	VDDK	VSSK	
KCOL3	VDD33	VSS33	VDDK	VSSK	
KCOL2	VDD33	VSS33	VDDK	VSSK	
KCOL1	VDD33	VSS33	VDDK	VSSK	
KCOL0	VDD33	VSS33	VDDK	VSSK	
KROW4	VDD33	VSS33	VDDK	VSSK	
KROW3	VDD33	VSS33	VDDK	VSSK	
KROW2	VDD33	VSS33	VDDK	VSSK	
KROW1	VDD33	VSS33	VDDK	VSSK	

KROW0	VDD33	VSS33	VDDK	VSSK	
EINT0	VDD33	VSS33	VDDK	VSSK	
EINT1	VDD33	VSS33	VDDK	VSSK	
EINT2	VDD33	VSS33	VDDK	VSSK	
EINT3	VDD33	VSS33	VDDK	VSSK	
UTXD1	VDD33	VSS33	VDDK	VSSK	
UCTS1_B	VDD33	VSS33	VDDK	VSSK	
URTS1_B	VDD33	VSS33	VDDK	VSSK	
UTXD3	VDD33	VSS33	VDDK	VSSK	
URXD3	VDD33	VSS33	VDDK	VSSK	
URXD2	VDD33	VSS33	VDDK	VSSK	
URXD1	VDD33	VSS33	VDDK	VSSK	
UTXD2	VDD33	VSS33	VDDK	VSSK	
SYSCLK	AVDD_PLL	AVSS_PLL	AVDD_PLL	AVSS_PLL	
XIN	AVDD_RTC	AVSS_RTC	AVDD_RTC	AVSS_RTC	
XOUT	AVDD_RTC	AVSS_RTC	AVDD_RTC	AVSS_RTC	
SIMIO	VSIM				
SIMRST	VSIM				
SIMCLK	VSIM				
CHRIN					
GATEDRV					
LED_B					
LED_G					
LED_R					
LED					
VIBRATOR					
VSIM					3.3/1.8V
VRF					2.8V
VRF_SENSE					
VCORE					1.8/1.5V
VIO					2.8V
VM					2.8/1.8V
VA					2.8V
VCTXO					2.8V
VBAT_RF					
VBAT					
VBAT					
VBAT					
AVBAT					
BAT_BACKUP					
BATDET					

BATSENSE					
ISENSE					
RESET					
RSTCAP					
VREF					
VMSEL					
PWRKEY					
PGND					
DGND					
DGND					
DGND					
DGND					
VSS33					
VSS33					
VSS33					
VSS33					
VSS33					
VSS33_EMI					
VSS33_EMI					
VSS33_EMI					
VSS33_EMI					
VSS33_EMI					
VDDK					TYP 1.8V
VDDK					TYP 1.8V
VDDK					TYP 1.8V
VDDK					TYP 1.8V
VDD33					TYP 2.8V
VDD33					TYP 2.8V
VDD33					TYP 2.8V
VDD33_LCD					2.8V/1.8V
VDD33_EMI					2.8V/1.8V
VDD33_EMI					2.8V/1.8V
VDD33_EMI					2.8V/1.8V
VDD33_EMI					2.8V/1.8V
VDD33_EMI					2.8V/1.8V
AVDD_RFE					
AVDD_MBUFL					
AVDD_GSMRFRX					
AVDD_PLL					
AVDD_AFE					
AVSS_MBUFL					
AVSS_PLL					
AVSS_GSMRFRX					
AVSS_RFE					
AVSS_AFE					
AGND					

AGND_RF					
AGND_AFE					
AGND_RFE					
AVDD_RTC					

Table 3 Power Descriptions