

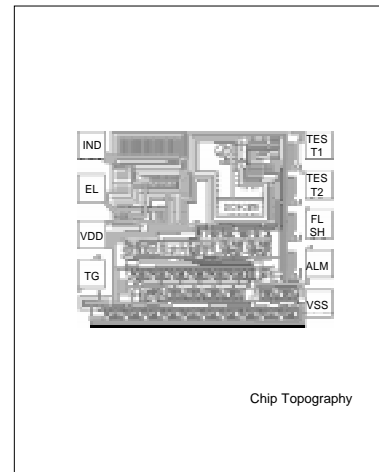
EL LAMP DRIVER IC

DESCRIPTION

The SC6802 is a poly gate CMOS integrated circuit which is designed to drive an Electroluminescence Lamp (EL) to light. It supplies three pins for trigger input: one is active at low (ALM) and other two are active at high (TG & FLSH). 3 seconds display delay function is implemented by internal divider. Only ALM and TG will 3 seconds delay but FLSH not. The switching and EL driving frequency is decided by an internal RC oscillator.

The driving capability for IND output and frequency for EL output are different options, the detail information shown in the OPTION LIST.

The SC6802 can be widely used in the back light of digital watch, analogy watch, calculator etc.



FEATURES

- * Single 3V or 1.5V battery operation
- * DC to AC conversion
- * Built-in RC oscillator
- * Built-in delay function
- * Three independent trigger inputs:
 - ALM (active Low) makes EL display for 3 seconds delay;
 - TG (active High) makes EL display for 3 seconds delay;
 - FLSH (active high) makes EL flash companied with the pulse from FLSH without any delay (See Timing Diagram)
- * Economical solution for EL display
- * CMOS process and low power consumption
- * No external component needed for delay function
- * Minimum external components application

OPTION LIST

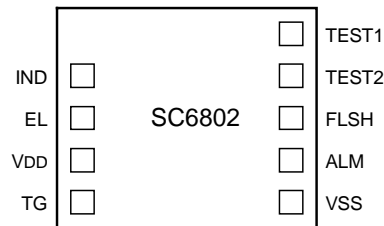
| OPTION | IND Output Current I_{OH1} (mA) | | | Oscillator Frequency F_{osc} (kHz) | | |
|----------|-----------------------------------|------|------|--------------------------------------|------|------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| SC6802-1 | 0.25 | 0.5 | 1.0 | 170 | 240 | 310 |
| SC6802-2 | 1.0 | 1.5 | 2.5 | 400 | 500 | 670 |
| SC6802-3 | 0.2 | 0.4 | 0.8 | 400 | 500 | 670 |

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

| Characteristic | Symbol | Test Conditions | Value | Unit |
|-----------------------|------------------|-----------------|----------------------|------|
| Supply Voltage | VDD - VSS | -- | -0.3 ~ 5.0 | V |
| Input Voltage | V _{IN} | -- | VSS -0.3V ~ VDD+0.3V | V |
| Operating Temperature | T _{opr} | -- | -10 ~ +70 | °C |
| Storage Temperature | T _{stg} | -- | -55 ~ +125 | °C |

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**PAD
ASSIGNMENT**Chip size: 1.11x0.85(mm)²

Note: The IC substrate should be connected to VDD in the PCB layout artwork.

ELECTRICAL CHARACTERISTICS (Ta=25°C, VSS=0V, VDD=3.0V; Unless otherwise specified)

| Parameter | Symbol | Test conditions | Min | Typ | Max | Unit |
|-----------------------------|--------|----------------------------------|-----|-----|-----|------|
| Operating Voltage | VDD | -- | 1.3 | 3.0 | 4.5 | V |
| Stand-by Current | IDD | All input and output are opened. | -- | 0.1 | 1 | μA |
| IND Output Source Current * | IOH1 | VOH = 0.8V | 1.0 | 1.5 | 2.5 | mA |
| EL Output Source Current | IOH2 | VOH = 0.8V | 0.2 | 0.6 | -- | mA |
| IND Output Sink Current | IOL1 | VOL = 0.8V | 10 | 20 | -- | mA |
| EL Output Sink Current | IOL2 | VOL = 0.8V | 0.5 | 2 | -- | mA |
| Oscillator Start Voltage | VOsc | Within 2 sec | 1.3 | -- | -- | V |
| Oscillator Frequency * | Fosc | VDD = 3.0V | 400 | 500 | 670 | KHz |

* The parameters IOH and Fosc in the above table refer to option SC6802-2; Others can be found in the OPTION LIST.

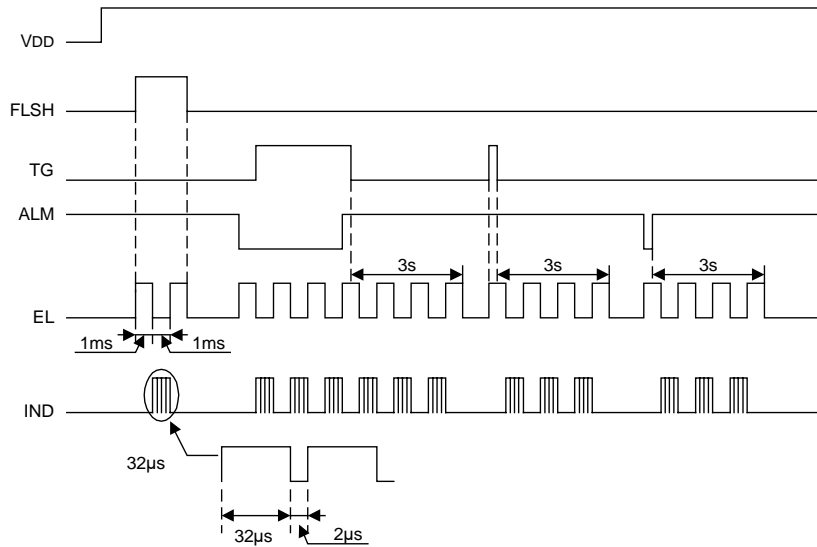
PAD DESCRIPTION

| Pad No. | Symbol | I/O | Description |
|---------|--------|-----|---------------------------------|
| 1 | Vss | -- | Negative power supply |
| 2 | ALM | I | Trigger input pin (active low) |
| 3 | FLSH | I | Trigger input pin (active high) |
| 4 | TEST2 | -- | Test pin |
| 5 | TEST1 | -- | Test pin |
| 6 | IND | O | DC to AC converter output |
| 7 | EL | O | |
| 8 | VDD | -- | Positive power supply |
| 9 | TG | I | Trigger input pin (active high) |

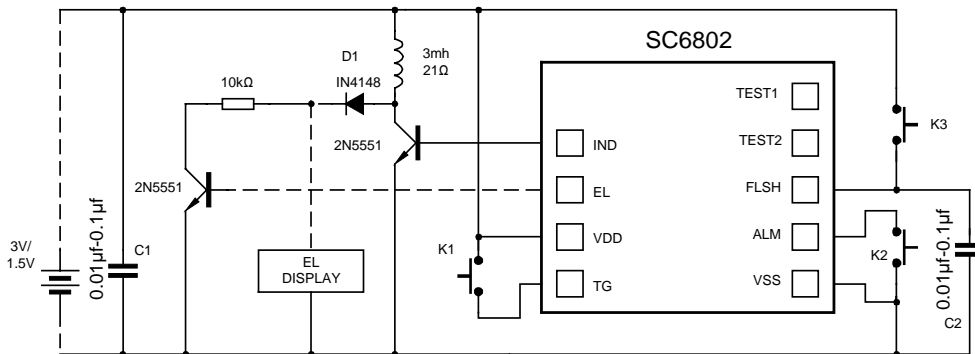
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TIMING DIAGRAM



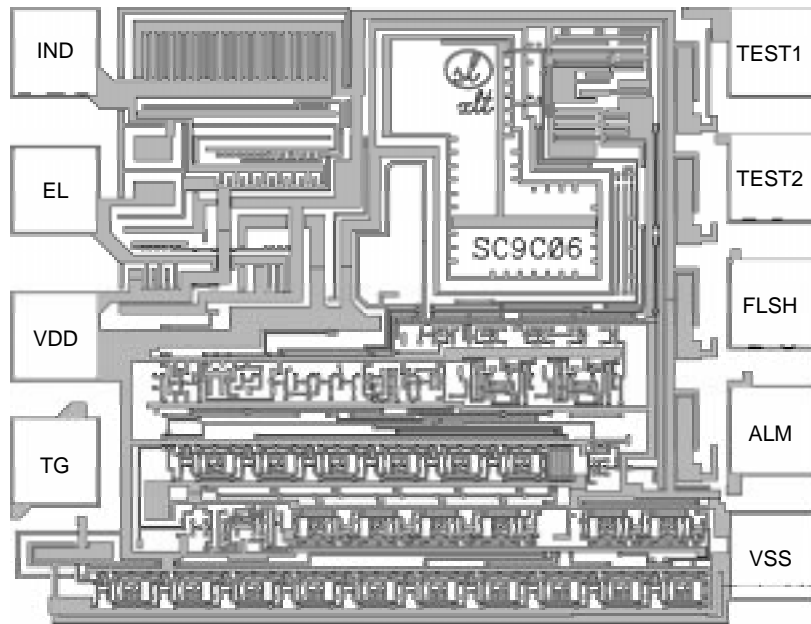
APPLICATION CIRCUIT



- Note: 1. Substrate is connected to VDD.
 2. The wires connected to TG and ALM cannot cross the line inside the black dot line box. Furthermore, these wires should be separated from the lines inside the black dot line box by Vss or VDD.
 3. The capacitor C2 can be connected to Vss or VDD.
 4. During the watch application, the two wires connected to crystal are better to be surrounded by Vss or VDD, and they are the farer the better away from the wire connected to EL.
 5. The items 2,3,4 are very important for PCB layout.

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CHIP TOPOGRAPHY

Chip Size: 1.11mm x 0.85mm

PAD COORDINATES (Unit: μm)

| PAD Name | X | Y | PAD Name | X | Y |
|----------|------|------|----------|------|-----|
| VDD | -470 | -35 | TEST2 | 460 | 170 |
| TG | -470 | 300 | TEST1 | 460 | 340 |
| VSS | 460 | -325 | IND | -470 | 340 |
| ALM | 460 | 160 | EL | -470 | 160 |
| FLSH | 460 | 5 | | | |

Note: The original point of the coordinate is the die center.

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