Upgrading to the 21143-PD and 21143-TD

Application Note

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Order Number: 278232-001

Application Note

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1.0 Introduction

The purpose of this document is to provide customers of the 21143 family with information to upgrade to its newest and most powerful members, the 21143–PD and the 21143–TD.

This document describes how to upgrade your designs from the 21143–PC and 21143–TC, to the 21143–PD and 21143–TD. It also describes register-level differences, and serves as a convenient reference for upgrading customer-developed drivers. For detailed programming information and for register descriptions, consult the *21143 PCI/CardBus 10/100 Mb/s Ethernet LAN Controller Hardware Reference Manual* (order number 278074).

1.1 Advantages of Upgrading to the 21143-xD

The 21143-PD and 21143-TD are pin compatible and are the functional equivalent of the 21143-PC and 21143-TC. However, they offer the following additional features and performance enhancements:

- Support network device class OnNow requirements for Microsoft's PC 97 and PC 98 specifications, including all wake-up events:
  - — Pattern matching
  - — Link change
  - — Magic Packet
- Fully compliant with *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 1.0.
- Fully compliant with *PCI Bus Power Management Interface specification*, Revision 1.0.
- Support PCI/CardBus clock control through clkrun.
- Support CardBus **cstschg** pin and Status Changed registers.
- Support interrupt mitigation on transmit and receive.
- Improve power consumption in sleep and snooze modes.
- Support the electrical requirements of both PCI and CardBus pads.
- Support storage of CardBus Card Information Structure (CIS), also known as tuples, in the serial ROM or the external flash ROM.
- Provide a link indication for the 10BASE-T and the 100BASE-TX symbol interface on the same pin. The LED is On when a valid link is established, and Off when a valid link is not found.
- Implement stretcher circuitry for the activity LED. This enables direct connection of the 21143-xD pin to the LED without the need for an external stretcher circuit.
- Provide link and activity indications on the same pin.
- Implement signal-detection filtering to avoid false detection of a link in the 100BASE-TX symbol interface.
- Provide three new PCI configuration registers.
- Provide two new control status registers.
- Implement fixes to erratas of the 21143-PC and 21143-TC.

1.2 Physical Features of the 21143-PD and 21143-TD

The 21143-PD and 21143-TD have the same body size and pin count as the 21143-PC and 21143-TC, making them drop-in replacements.

2.0 Pinout Changes

Table 1 lists the pins that have changed and includes the descriptions for the 21143-xC pins and the descriptions for the 21143-xD pins.

Table 1. Pin Changes and Descriptions (Sheet 1 of 2)

Pin #	Type	21143-xC Pin Name	21143-xC Pin Description	21143-xD Pin Name	21143-xD Pin Description
86	I/O O/D	clkrun_l	CardBus clock run indicates the clock status. The host system asserts **clkrun_l** to indicate normal operation of the clock. The host system deasserts **clkrun_l** when the clock is going to be slowed down to a nonoperational frequency. The 21143-xC samples **clkrun_l**, and when the signal is found deasserted, the 21143-xC asserts **clkrun_l**, requesting that normal clock operation be maintained.	clkrun_l	PCI/CardBus clock run indication. The host system asserts **clkrun_l** to indicate normal operation of the clock. The host system deasserts **clkrun_l** when the clock is going to be stopped or slowed down to a nonoperational frequency. If the clock is needed by the 21143, the 21143 asserts **clkrun_l**, requesting normal clock operation to be maintained or restored. Otherwise, the 21143 allows the system to stop the clock.
88	O	br_a<0>	Boot ROM address line bit 0. In a 256KB configuration, this pin also carries in two consecutive address cycles, boot ROM address bits 16 and 17.	br_a<0>/cb_pads_l	Boot ROM address line bit 0. In a 256KB configuration, this pin also carries in two consecutive address cycles, boot ROM address bits 16 and 17. This pin also determines the types of signals to use for the PCI/CardBus output pins, either PCI or CardBus. By default, this pin selects PCI signaling. To select CardBus signaling, this pin must be connected to a pull-down resistor.
102	I/O	gep<2>/rcv_match	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. • A status pin that drives an LED to indicate a receive packet has passed address recognition. When the 21143 is in remote wake-up LAN mode, this pin is used as an indicator that a Magic Packet has been successfully detected.	gep<2>/rcv_match/wake	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. • A status pin that drives an LED to indicate a receive packet has passed address recognition. This pin can also be controlled by bit Func0_HwOptions<3> in the serial ROM to be a wake-up event pin that can be connected to pin **pme#** of the PCI connector or pin **ctschg** of the CardBus connector. When this pin is in a wake function, bit MiscHwOptions<1> in the serial ROM determines the polarity. The PME function takes precedence over the Magic Packet indication function. When the 21143 is in remote wake-up-LAN mode, this pin is used as an indicator that a Magic Packet has been successfully detected.

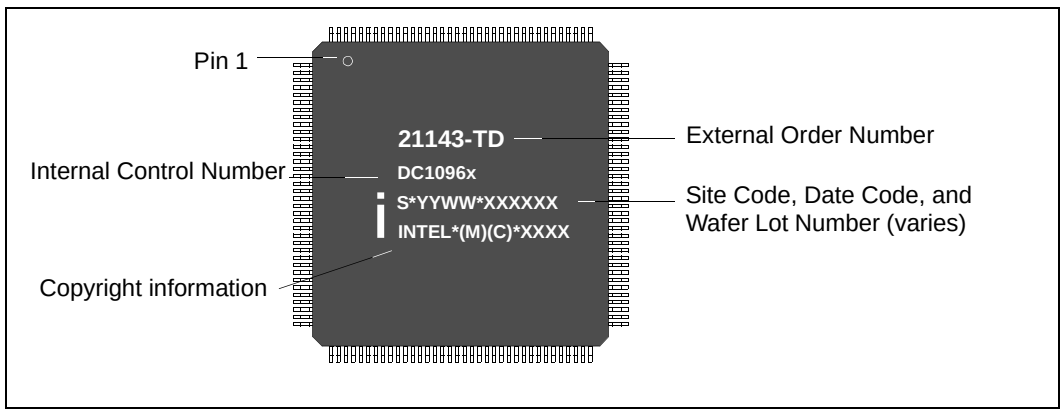
Table 1. Pin Changes and Descriptions (Sheet 2 of 2)

Pin #	Type	21143-xC Pin Name	21143-xC Pin Description	21143-xD Pin Name	21143-xD Pin Description
103	I/O	gep<3>10bt_link	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. • A status pin that drives an LED to indicate that the 10BASE-T link integrity test has completed successfully after the link was down.	gep<3>/link	This pin can be configured by software to be: A general-purpose pin that performs either input or output functions. A status pin that drives an LED to indicate: • Network link integrity state for 10BASE-T. • Network link integrity state for 100BASE-TX. • Both network activity and network link integrity state. • An input link status pin for OnNow support. When used with an MII PHY device, this pin should be connected to the MII PHY link indication pin (the 21143 interprets link-pass when this pin is high). This pin should not be left unconnected.

3.0 Package Marking Conventions

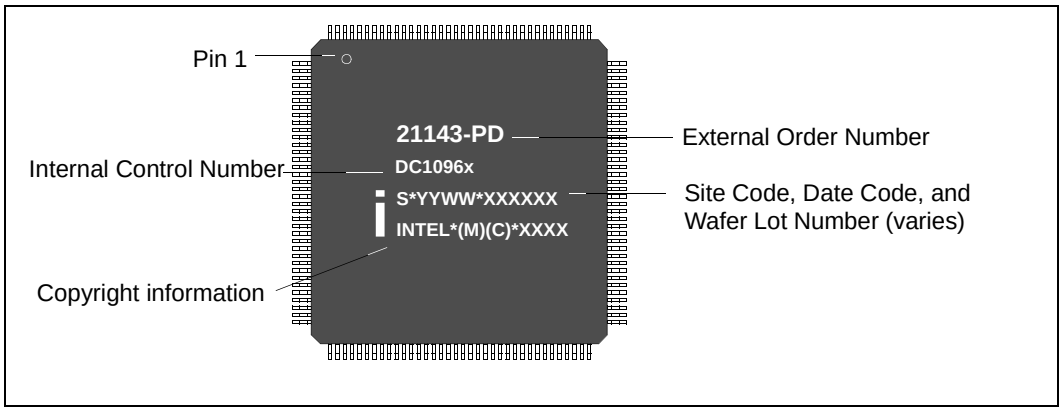
The 21143-TD device uses the following conventions (Figure 1) for package markings.

Figure 1. 21143-TD Package Marking Conventions



The 21143–PD device uses the following conventions (Figure 2) for package markings.

Figure 2. 21143-PD Package Marking Conventions



4.0 Cross-Referencing Package Markings

Use Table 2 to cross-reference the 21143 package markings with the related documentation.

Table 2. 21143 Package Markings and Related Documentation

External Order #	Device	Device Type and Revision	Internal Part #	Package Type[1]	Hardware Reference Manual #	Data Sheet #
21143–PC	21143	DC1071-C	21-44085-12	PQFP	278074	278073
21143–TC	21143	DC1071-C	21-44085-22	TQFP	278074	278073
21143–PD	21143	DC1096-B	—	MQFP	278074	278073
21143–TD	21143	DC1096-B	—	LQFP	278074	278073

1. For the 21143-xD, the PQFP package type has been reidentified as the MQFP, and the TQFP package type has been re-identified as the LQFP. This was done to conform to industry standard. The physical characteristics are the same for both package identifiers.

5.0 Upgrading Drivers

Software compatibility is retained for those customers utilizing Intel's drivers. This allows the same drivers and serial ROM format to be used with the 21143-PD and 21143-TD that were used for the 21143-PC and 21143-TC, providing the same functionality. For those customers who have developed their own drivers and require register-level information, see the section in this upgrade document titled, Register Differences Between 21143-xC and 21143-xD.

Table 3 lists the network and communications software available for the 21143. For the latest driver and communications software information that takes advantage of the new features of the 21143-xD, see the components page available on the Intel World Wide Web Internet site at:

http://developer.intel.com/design/network/new21/download/dsc-software-nc.htm

Table 3. Network and Communications Software Available for the 21143

Drivers	Supports
NDIS4 Unified DC21x4 driver	PC 97 compliant and supports Windows NT 4.0, Windows 95, and Windows 98
Novell Server Unified DC21x4 driver	32-bit ODI drivers for Versions 3.1*x* and 4.*x* Novell servers; Client32 drivers for DOS
Novell Client Unified DC21x4 driver	16-bit ODI drivers for DOS
NDIS2 Unified DC21x4 driver	NDIS2 MAC drivers for DOS, OS/2, Windows 3.1, Windows for Workgroups 3.11, and Windows 95
SCO UNIX Unified DC21x4 driver	SCO UNIX LLI, MDI, and MDI2 drivers

Support Files	Description
SROM Specification for DC21x4 devices	EEPROM data and format requirements for interoperability with DC21x4 drivers
SROM programming toolkit	Serial ROM programming utilities
DVT Design Verification	Manufacturing test utility for verifying DC21x4 adapter functionality
PCITEST diagnostic	Utility to determine whether a PC is Revision 2.0 PCI compliant
EVBDebug diagnostic	Utility for low-level debug and analysis of Intel 21x4 evaluation boards (or similar)
CardBus Enabler	Utility that maps CardBus slots into PCI configuration space for some CardBus laptops
BSDL	Boundary Scan Description Language files for Intel network chips
NDISDBG	Utility for low-level debug under Win 32 (Windows NT, Windows 95, and Windows 98) environment

6.0 Register Differences Between 21143-xC and 21143-xD

Enhancements to the 21143-xD have resulted in changes to existing registers and the addition of new registers.

Table 4. Register Differences Between 21143-xC and 21143-xD (Sheet 1 of 6)

New or Different Items	21143-xC Registers	21143-xD Registers
Configuration Registers		
CFCS<20>	Reserved	**New Capabilities**. Indicates whether or not the 21143-xD implements a list of new capabilities: • When set, this bit indicates the presence of New Capabilities. • When cleared, New Capabilities is not implemented. The value of this bit is loaded from Func0_HwOptions<3> bit (PME_Enable) in the serial ROM.
CFRV<3:0>	**Step Number**. Indicates the 21143-xC step number. The value of this field is set to 0.	**Step Number**. Indicates the 21143-xD step number. The value of this field is set to 1.
CFRV<7:4>	**Revision Number**. Indicates the 21143-xC revision number. The value of this field is set to 3.	**Revision Number**. Indicates the 21143-xD revision number. The value of this field is set to 4.
CCIS<2:0>	**Address Space Indicator**. This field indicates the location of the CIS base address. The 21143-xC supports only the value of 7 for this field, which means that the CIS begins in the expansion ROM space. Any other value causes the CIS register to reset to 0.	**Address Space Indicator**. This field indicates the location of the CIS base address. The 21143-xD supports the value of 2, indicating that the CIS is stored in the serial ROM, and 7, indicating that the CIS is stored in the expansion ROM. Any value other than 2 or 7 may lead to unpredictable behavior.
CCAP	Reserved	Capabilities Pointer Register. Offset 34h.
CCAP<7:0>	Reserved	**Capabilities Pointer**. Points to the location of the power-management register block in the PCI configuration space. The value of this field is determined by Func0_HwOptions<3> bit (PME_Enable) in the serial ROM. If this bit is set, the value of this field is DCh; otherwise, this field is read as 00h.
CWUC<0>	**Remote Wake-Up-LAN Disable**. When set, disables the remote wake-up-LAN mode.	**MBZ**. This bit must not be written with a value of 1.
CCID	Not present	Capability ID Register. Offset DCh.
CCID<7:0>	Not present	**Capabilities ID**. PCI Power Management Registers ID. The value of this field is 01h, indicating that this is the power-management-register block.
CCID<15:8>	Not present	**Next Item Pointer**. Points to the location of the next block of the capability list in the PCI Configuration Space. The value of this field is 00h, indicating that this is the last item of the Capability linked list.
CCID<18:16>	Not present	**Power Management PCI Version**. The value of this field is 001Bh, indicating that the 21143-xD complies with Revision 1 of the *PCI Power Management Specification*.

Table 4. Register Differences Between 21143-xC and 21143-xD (Sheet 2 of 6)

New or Different Items	21143-xC Registers	21143-xD Registers
CCID<19>	Not present	**Power Management Event Clock**. The value of this field is 0, indicating that the 21143-xD does not rely on the presence of the PCI/CardBus clock in order to generate a PME.
CCID<21>	Not present	**Device Specific Initialization**. The value of this field is 0, indicating that the 21143-xD does not require a special initialization code sequence in order to be configured correctly.
CCID<25>	Not present	**D1 Support**. The value of this field is 1, indicating that the 21143-xD supports the D1 power state.
CCID<26>	Not present	**D2 Support**. The value of this field is 1, indicating that the 21143-xD supports the D2 power state.
CCID<27>	Not present	**PME Support D0**. The value of this field is 0, indicating the 21143-xD does not assert PME in D0 power state.
CCID<28>	Not present	**PME Support D1**. The value of this field is 1, indicating that the 21143-xD may assert PME in D1 power state.
CCID<29>	Not present	**PME Support D2**. The value of this field is 1, indicating that the 21143-xD may assert PME in D2 power state.
CCID<30>	Not present	**PME Support $D3_{hot}$**. The value of this field is 1, indicating the 21143-xD may assert PME in $D3_{hot}$ power state.
CCID<31>	Not present	**PME Support $D3_{cold}$**. If this bit is set, the 21143-xD may assert PME in $D3_{cold}$ power state. Otherwise, the 21143-xD may not assert PME in$D3_{cold}$. The value of this bit is loaded from Func0_HwOptions<6> bit in the serial ROM.
CPMC	Not present	Power Management Control and Status Register. Offset E0h.
CPMC<1:0>	Not present	**Power State**. This field is used to set the current power state of the 21143-xD and to determine its power state. The definition of the field values are: 0 - D0 1 - D1 2 - D2 3 - $D3_{hot}$ This field gets a value of 0 after power-up.
CPMC<8>	Not present	**PME_Enable**. If this bit is set the 21143-xD can assert the **gep<2>/rcv_match/wake** pin. Otherwise, the assertion of the **gep<2>/rcv_match/wake** pin by the 21143-xD is disabled. This bit is cleared on power-up reset only, and is not modified by either hardware or software reset.
CPMC<15>	Not present	**PME_Status**. This bit indicates that the 21143-xD has detected a power-management event. If the PME_Enable bit is set, the 21143-xD also asserts the **gep<2>/rcv_match/wake** pin. This bit is cleared on power-up reset or by write 1. It is not modified by either a hardware or software reset. When this bit is cleared the 21143-xD deasserts the **gep<2>/rcv_match/wake** pin. **NOTE:** This bit is also cleared if the General Enable bit of the FER (FER<4>) is cleared.

Table 4. Register Differences Between 21143-xC and 21143-xD (Sheet 3 of 6)

New or Different Items	21143-xC Registers	21143-xD Registers
Control and Status Registers		
CSR0<26>	Reserved	**Enable OnNow Registers**. When set, CSR1-PM and CSR2-PM are accessible. When this bit is cleared, writing to these registers is interpreted as writing to CSR1 and CSR2 (receive/transmit poll demand). This bit is cleared upon hardware or software reset.
CSR1-PM	Not present	**Wake-Up Frame Filter Register**. This register is used for loading the wake-up frame filter register. In order to load the wake-up frame filter register, CSR0<26> must be set and CSR1-PM must be written eight times. Offset **80h**. Value after reset is **undefined**.
CSR1-PM<31:0>	Not present	**Wake-Up Frame Filter**. The first value written to this register, after CSR0<26> was set, is loaded by the 21143-xD to the first longword in the wake-up frame filter register (filter_0_byte_mask). The second value written to this register is loaded to the second longword in the wake-up frame filter register block, and so on. **NOTE:** Complete details about the format of the wake-up frame filter register block are contained in the *Miscellaneous Changes* section of this document.
CSR2-PM	Not present	**Wake-Up Events Control and Status Register**. This register is used for programming the requested wake-up events and the VLAN parameters. In order to program the requested wake-up events and the VLAN parameters, CSR0<26> must be set. Offset **10h**. Value after reset is **undefined**.
CSR2-PM<0>	Not present	**Link Change Enable**. If set, enables generation of a power-management event due to link change.
CSR2-PM<1>	Not present	**Magic Packet Enable**. If set, enables generation of a power-management event due to Magic Packet reception.
CSR2-PM<2>	Not present	**Wake-Up Frame Enable**. If set, enables generation of a power-management event due to reception of a wake-up frame.
CSR2-PM<4>	Not present	**Link Change Detected**. If set, indicates that a power-management event was generated due to a link change. The bit is cleared by a write 1, or upon a power-up reset. It is unaffected by either a hardware or software reset.
CSR2-PM<5>	Not present	**Magic Packet Received**. If set, indicates that a power-management event was generated due to reception of a Magic Packet. The bit is cleared by a write 1, or upon a power-up reset. It is unaffected by either a hardware or software reset.
CSR2-PM<6>	Not present	**Wake-Up Frame Received**. If set, indicates that a power-management event was generated due to reception of a wake-up frame. The bit is cleared by a write 1, or upon a power-up reset. It is unaffected by either a hardware or software reset.
CSR2-PM<8>	Not present	**MBZ**. This bit must be zero.
CSR2-PM<9>	Not present	**Global Unicast**. When set, enables any unicast packet filtered by the 21143-xD address recognition to be a wake-up frame.

Table 4. Register Differences Between 21143-xC and 21143-xD (Sheet 4 of 6)

New or Different Items	21143-xC Registers	21143-xD Registers
CSR2-PM<11>	Not present	**VLAN Enable**. When set, enable the 21143-xD's VLAN support. This field is reset upon hardware and software reset.
CSR2-PM<31:16>	Not present	**VLAN Type**. If the VLAN Enable bit is set (CSR2-PM<11>), this field should be written with the VLAN type defined by the IEEE 802.1 standard.
CSR6<26>	Reserved	**Ignore Destination Address MSB**. When set, bit 47 of the destination address is ignored in the MAC's address filtering. This bit is meaningful only if the 21143-xD is programmed to do perfect address filtering. It is cleared upon hardware and software reset.
CSR11<19:17>	Reserved	**Number of Receive Packets**. Indicates the number of receive packets before issuing a receive interrupt.
CSR11<23:20>	Reserved	**Receive Timer**. Indicates the time in units of "Cycle Size" before issuing a receive interrupt after packet reception.
CSR11<26:24>	Reserved	**Number of Transmit Packets**. Indicates the number of transmit packets before issuing a transmit interrupt.
CSR11<30:27>	Reserved	**Transmit Timer**. Indicates the time in units of "16*Cycle Size" before issuing a transmit interrupt after packet transmission.
CSR11<31>	Reserved	**Cycle Size**. This field controls the units for the transmit and receive timers. When set, the cycle size is: • 10BASE-T/AUI mode–12.8 µs • MII/SYM 100 Mb/s mode–5.12 µs • MII 10 Mb/s mode–51.2 µs When cleared, the cycle size is: • 10BASE-T/AUI mode–204.8 µs • MII/SYM 100 Mb/s mode–81.92 µs • MII 10 Mb/s mode–819.2 µs
CSR15<11>	Reserved	**Link Extend Enable**. When set, the 21143-xD reports link detection on its 100BASE-TX symbol port only if its **sd** pin (pin 117) is asserted for at least 1.2 ms. When cleared, the 21143-xD reports link detection on its 100BASE-TX symbol port if its **sd** pin (pin 117) is asserted for at least 330 µs.
FER	Not present	**Function Event Register**. This register is the CardBus Status Changed function event register, which is used for reporting of interrupt pending and power-management event detection in a CardBus system. Offset **80h**. Value after reset is **undefined** for reserved bits; 0 for bits that are not reserved.
FER<4>	Not present	**General Wake-Up Event**. This bit is set when the 21143-xD has detected a power-management event. This bit is cleared upon power-up reset and by write 1. It is unaffected by either a hardware or software reset. When the PME_Status bit in the PCI configuration is cleared, this bit is automatically cleared as well.
FER<15>	Not present	**Interrupt**. This bit is set when there is an interrupt pending. This bit is cleared by write 1.

Table 4. Register Differences Between 21143-xC and 21143-xD (Sheet 5 of 6)

New or Different Items	21143-xC Registers	21143-xD Registers
FEMR	Not present	**Function Event Mask Register**. This register is the CardBus Status Changed function event mask register, which controls the assertion of the signals **int_l** and **gep<2>/rcv_match/wake** in a CardBus system. Offset **84h**. Value after reset is **undefined** for reserved bits; 0 for bits that are not reserved.
FEMR<4>	Not present	**General Wake-Up Event Enable**. When set together with the Wake-Up Event Summary Enable bit (FEMR<14>), enables the assertion of the **gep<2>/rcv_match/wake** pin. **NOTE:** To disable the assertion of the**gep<2>/rcv_match/wake** pin, the PME_Enable bit in the PCI configuration register (CPMC<8>) must be cleared as well. This bit is cleared upon power-up reset.
FEMR<14>	Not present	**Wake-Up Event Summary Enable**. When set together with the General Wake-Up Event Enable bit (FEMR<4>), enables the assertion of the **gep<2>/rcv_match/wake** pin. **NOTE:** To disable the assertion of the **gep<2>/rcv_match/wake** pin, the PME_Enable bit in the PCI configuration register (CPMC<8>) must be cleared as well. This bit is cleared upon power-up reset.
FEMR<15>	Not present	**Interrupt Enable**. When set, enables assertion of the interrupt pin (**int_l**).
FPSR	Not present	**Function Present State Register**. This register is the CardBus Status Changed function present state register, which is used for reporting the present state of the **int_l** and **gep<2>/rcv_match/wake** pins in a CardBus system. Offset **88h**. Value after reset is **undefined** for reserved bits; 0 for bits that are not reserved.
FPSR<4>	Not present	**General Wake-Up Event**. Reflects the current state of the wake-up event. This bit is cleared when either the General Wake-Up Event in the function event register is cleared, or when the PME_Status bit in the CPMC register is cleared. This bit is cleared upon power-up reset.
FPSR<15>	Not present	**Interrupt**. This bit reflects the state of the interrupt line. It is set when the following conditions exist: CSR5<15> is set together with CSR7<15> or CSR5<16> is set together with CSR7<16>. The 21143-xD is in the D0 power state. FEMR<15> is set or Func0_HwOptions<7> (RealSTSCHG) bit in the serial ROM is cleared.

Table 4. Register Differences Between 21143-xC and 21143-xD (Sheet 6 of 6)

New or Different Items	21143-xC Registers	21143-xD Registers
FFER	Not present	**Function Force Event Register**. This register is the CardBus Status Changed function force event register, which is used to force the value of the interrupt and the general wake-up event bits in the function event register to a 1. Offset **8Ch**. Value after reset is **undefined** for reserved bits; 0 for bits that are not reserved.
FFER<4>	Not present	**Force Wake-Up**. Writing 1 to this bit sets the wake-up event field in FER<4>, but not in FPSR<4>. If the wake-up event is enabled, the 21143-xD also asserts the **gep<2>/rcv_match/wake** pin. Writing 0 has no effect. This bit is cleared upon power-up reset.
FFER<15>	Not present	**Force Interrupt**. Writing 1 to this bit sets the Interrupt field in FER<15>, but not in FPSR<15>. If the interrupt is enabled, the 21143-xD also asserts the **int_l** pin. Writing 0 has no effect.

7.0 Miscellaneous Changes

The following are descriptions of additional changes incorporated into the 21143-xD.

7.1 Wake-Up Frame Filter Register Block

The wake-up frame filter register block is a new set of registers that is used by the 21143-xD to recognize wake-up frames. Figure 3 details the wake-up frame filter register block and Table 5 details the field assignments:

Figure 3. Wake-up Frame Filter Register Block

<table>
<tr><td colspan="8">Filter 0 Byte Mask</td></tr>
<tr><td colspan="8">Filter 1 Byte Mask</td></tr>
<tr><td colspan="8">Filter 2 Byte Mask</td></tr>
<tr><td colspan="8">Filter 3 Byte Mask</td></tr>
<tr><td>Reserved</td><td>Filter 3 Command</td><td>Reserved</td><td>Filter 2 Command</td><td>Reserved</td><td>Filter 1 Command</td><td>Reserved</td><td>Filter 0 Command</td></tr>
<tr><td colspan="2">Filter 3 Offset</td><td colspan="2">Filter 2 Offset</td><td colspan="2">Filter 1 Offset</td><td colspan="2">Filter 0 Offset</td></tr>
<tr><td colspan="4">Filter 1 CRC-16</td><td colspan="4">Filter 0 CRC-16</td></tr>
<tr><td colspan="4">Filter 3 CRC-16</td><td colspan="4">Filter 2 CRC-16</td></tr>
</table>

Table 5. Wake-up Frame Filter Register Block Field Assignments (Sheet 1 of 2)

Name	Field	Description
Filter 0-3 Byte Mask	31	MBZ This bit must be zero.

Table 5. Wake-up Frame Filter Register Block Field Assignments (Sheet 2 of 2)

Name	Field	Description
	30:0	Byte Mask If bit number *j* of the byte mask is set, byte number *pattern-offset + j* of the incoming frame is processed by the CRC machine. Otherwise, byte *pattern-offset + j* is ignored. This field is not affected by either power-up, hardware, or software reset.
Filter 0-3 Command	3	Address Type Defines the destination address type of the pattern. When this bit is set, the pattern applies only to multicast frames. When this bit is cleared, the pattern applies only to unicast frames.
	2	Add Previous When this bit is set, the 21143-xD performs a logical AND between the current filter matching signal and the matching signal of the previous filter. For the first filter, the 21143-xD chains the filter's matching signal with the result of the global unicast filter (CRS2-PM<9>).
	1	Inverse Mode When this bit is set, the 21143-xD uses its match signal as a rejection signal. A frame that does not match this filter causes the 21143-xD to generate a power-management event.
	0	Enable Filter When this bit is set, filter i is enabled, otherwise, filter i is disabled.
Filter 0-3 Offset	7:0	Pattern Offset The offset of the first byte in the frame that is examined by the 21143 in order to check if an incoming frame is a wake-up frame. Offset 0 is the first byte of the incoming frame's destination address. The minimum value allowed for this field is 12. This field is not affected by either power-up, hardware, or software reset.
Filter 0-3 CRC-16	15:0	Pattern CRC16 This field contains the 16-bit CRC value calculated from the pattern and the byte mask programmed to the wake-up filter register block. The 21143-xD compares the result of its CRC machine to this value in order to determine whether the frame is a wake-up frame. This field is not affected by either power-up, hardware, or software reset.

7.2 JTAG Ring Boundary Shift Registers

The 21143-xD provides three new JTAG ring boundary shift registers: INTER3, BR_A0_OE, and MII_MDC_OE.

7.3 Wake-Up LAN Mode

The 21143-xD wake-up-LAN mode operation has been modified so that it now asserts only the WAKE (**gep<2>**) pin when it detects a Magic Packet.

7.4 PCI/CardBus Signaling

The 21143xD PCI pads were modified to support CardBus signaling. The selection of PCI signaling or CardBus signaling is done through the **br_a<0>/cb_pads_l** pin. The 21143-xC supports only PCI signaling. To get CardBus signaling, external resistors are needed.

8.0 Comparing Programming Characteristics

Table 6 compares the programming characteristics of the 21143-xC with the 21143-xD.

Table 6. Programming Characteristics of the 21143-xC with the 21143-xD

Characteristic	21143-xC	21143-xD
Supports 1KB memory space	Unsupported	CMBA<9:7>
Device revision[1]	CFRV<7:0>, 30h	CFRV<7:0>, 41h
VLAN enable	Unsupported	CSR2-PM<11><31:16>
Link LED for 100BASE-TX symbol interface	Unsupported	CSR15<11>
Power-management register block	Unsupported	CCAP<7:0>
Power-management register ID	Unsupported	CCID<7:0>
Power-management specification revision	Unsupported	CCID<18:16>
PCI clock present	Unsupported	CCID<19>
Auxiliary power source supplied	Unsupported	CCID<20>
Device-specific initialization	Unsupported	CCID<21>
Power state	Unsupported	D1=CCID<25> D2=CCID<26>
PME support	Unsupported	D0=CCID<27>, D1=CCID<28>, D2=CCID<29>, $D3_{hot}$=CCID<30>, and $D3_{cold}$=CCID<31>
Power state status (D0-D3)	Unsupported	CPMC<1:0>
Power-management enable	Unsupported	CPMC<8>
Power-management status	Unsupported	CPMC<15>
Generate a power-management event after a wake-up frame	Unsupported	CSR2-PM<4>
Generate a power-management event after a Magic Packet	Unsupported	CSR2-PM<6>
Force a wake-up	Unsupported	FFER<4>
Force an interrupt event	Unsupported	FFER<15>

1. This change can affect the behavior of software drivers.

9.0 Hardware Characteristics

The following table compares the temperature and power characteristics of the 21143-xC with the 21143-xD.

Characteristics	21143-xC	21143-xD
Operating temperature range	0°C to 70°C (32°F to 158°F)	0°C to 70°C (32°F to 158°F)
Package[1]	144-pin PQFP, 144-pin TQFP	144-pin MQFP, 144-pin LQFP
Power supply	**Vdd** = 3.3 V, **Vdd_clamp** = 5 V or 3.3 V	Vdd = 3.3 V, Vdd_clamp = 5 V or 3.3 V
Storage temperature range	–55°C to +125°C (–67°F to +257°F)	–55°C to +125°C (–67°F to +257°F)

1. For the 21143-xD, the PQFP package type has been reidentified as the MQFP, and the TQFP package type has been re-identified as the LQFP. This was done to conform to industry standard. The physical characteristics are the same for both package identifiers.

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