Am7943/44/45 SLIC
Evaluation Board
User's Guide

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AMD

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AMD

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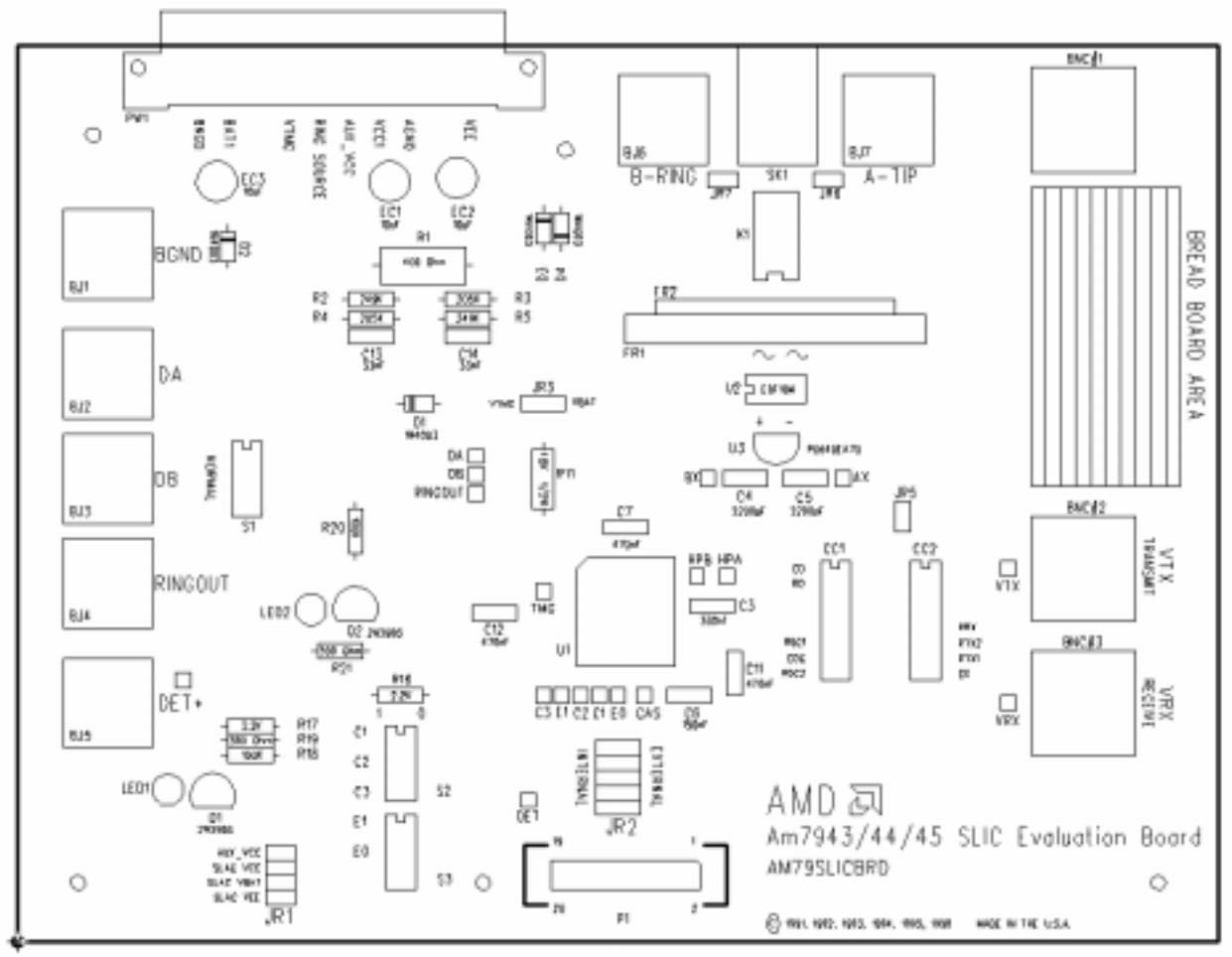
1.0 INTRODUCTION

The Am7943/44/45 SLIC Evaluation Board provides a platform to evaluate the different capabilities of the Am7943/44/45 SLIC devices. The evaluation board's two modes of operation, INTERNAL and EXTERNAL, provide a flexible platform to evaluate each SLIC device. All digital control signals and voice band signals have test points for easy probing. All user selectable components are mounted on component carriers for easy modification where required. A surge protection circuit, robust enough to meet Bellcore GR-1089-CORE specifications, is part of the telephone interface. All power is brought to the board via a single-keyed connector. LEDs are provided to indicate when the loop detect/ground-key (DET) and RINGOUT circuits are active or non-active.

Detailed device explanations, operational circuit descriptions, and required formulas can be found in the Linecard Products Data Book and the individual SLIC device data sheets.

The Am7943/44/45 SLIC evaluation board physical layout is shown in Figure 1.

Figure 1



2.0 BOARD SETUP AND CONNECTION

The SLIC evaluation board operates either standalone or in conjunction with an AMD SLAC™ device evaluation board. Standalone operation is supported using manual switch settings to control operation. When connected to a SLAC device board, control and digital transmission access is provided through the programmable pins of the SLAC device, which is then controlled by AMD's computer interface evaluation software.

2.1 Power Connections

Input power is supplied to the board via the 10-pin connector PW1. The power cables are color coded and labeled at the banana jack. The following chart details all ten cables by color and description.

Pin #	Cable Color	Label	Description
1	Black	BGND	Common ground for VBAT
2	White	VBAT1	Main Battery supply
3	Gray	VBAT2	*Not required*
4	Blue	VTMG	Input Voltage for RTMG (optional)
5	Violet	RING SRC	External ringing signal input
6	Orange	AUX_VCC	Supply for all 5 V requirements except the SLIC
7	Red	VCC1	SLIC supply only
8	Brown	AGND	Common ground
9	Green	VNEG	*Not required*
10	Yellow	VEE	Fixed –5 V supply

The Am7943/44/45 SLIC board does not require the VBAT2 or V_{NEG} cables to be connected as these inputs do not go to or affect the operation of the SLIC device.

2.2 Telephone Line Interface

To interface the Am7943/44/45 evaluation board, to a telephone simply plug the phone connector into the RJ-11 modular jack. The TIP and RING banana jacks are connected in parallel with the RJ-11 jack and allow the evaluation board to also be interfaced to telephony test equipment. JR7 and JR8 route the TIP and RING signals to SK1. Removing the shunts will disconnect SK1.

A tip/ring surge protection circuit is included on the board. The protection circuit is placed in series with the tip and ring leads as they connect to the A and B leads of the SLIC. The circuit is composed of a diode bridge, a Teccor Sidactor protection device, and the thick-film hybrid fusing resistor assembly (FRP1). While this circuit is not the definitive type, it is typical of a circuit that will withstand the rigors of Bellcore testing.

2.3 Analog Signal Connections

Analog four-wire signal connections are provided to the SLIC by shielded BNC connectors on the board. One connector, VRX, is used for connecting an analog input signal to the SLIC, where that signal will appear across the tip/ring two-wire interface. The other connector, VTX, is an analog signal output representing the two-wire signal, which appears across tip and ring.

2.4 Digital Interface

The SLIC is an analog part but may be placed in different operating states through logic control signals, which are presented to the digital control inputs. Five input signals and one output signal comprise the digital interface to the SLIC device. Operation of the SLIC with these control inputs is explained in the SLIC data sheet. The following table gives a general description of the signals.

Name	Type	Description
C1	Input	SLIC control pin. C1 is the LSB.
C2	Input	SLIC control pin.
C3	Input	SLIC control pin. C3 is the MSB.
E1	Input	Ground Key enable control input.
E0	Input	DETECT enable control input.
DET*	Output	Indicates when the selected condition of C1–C3, E1 and E0 is detected.

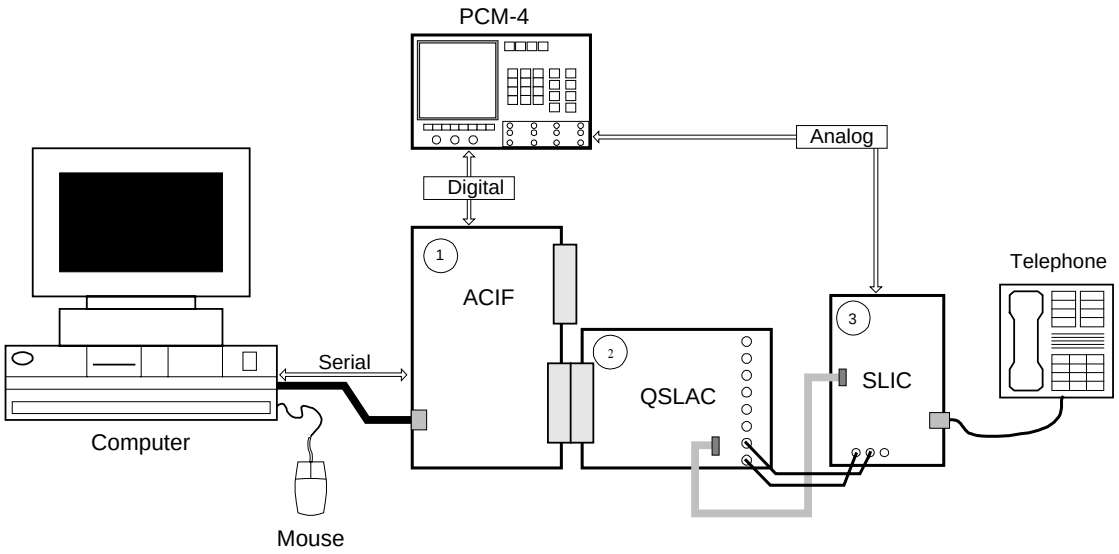
2.5 Interconnecting to SLAC™ Device Evaluation Boards

In addition to operating in a standalone mode, the SLIC board may be connected to an AMD SLAC device evaluation board, utilizing that SLAC device together with the SLIC as the complete front-end system solution of an analog line interface circuit. The SLAC device performs the digital conversion through its connection with the Computer Interface (ACIF) Board and provides companded digital input and output of the line circuit.

The SLAC device boards have a pair of analog input and output BNC connectors, representing the analog input and output of the SLAC device's channel and are wired directly to the SLIC board's corresponding output and input analog connectors. Control of the SLIC is provided through the digital control cable that is wired from the SLAC device board's control header for that channel to the control signal header on the SLIC board. The INTERNAL/EXTERNAL jumpers on the SLIC board must be placed in the external position to enable this control.

A representative connection of the SLIC board to an AMD SLAC device board, along with the other major items and their interconnect, is shown in Figure 2.

Figure 2



1. *ACIF Computer Interface Board.*
2. *QSLAC™ (SLAC) Device Evaluation Board.*
3. *SLIC Device Evaluation Board.*

3.0 BOARD OPERATION AND CONTROL

The SLIC board is controlled through on-board DIP switches (standalone), through an external control interface (in conjunction with an AMD SLAC device board), and by selection of on-board jumpers. Operational performance is programmable by user selection of on-board components. Indicators are also included to provide visual state indication of key functions. User operation and programming selection is described in this section.

3.1 Controlling the SLIC

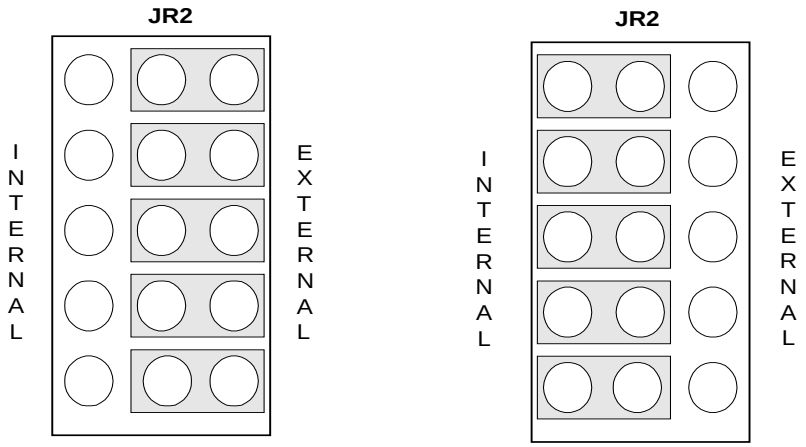
The SLIC Evaluation Board can be operated in either an INTERNAL (standalone) mode or EXTERNAL (controlled via a 20-pin header) mode. The INTERNAL mode can be selected by placing the shunts provided on JR2 between the center and left columns, this allows switches S2 and S3 to control the device. The EXTERNAL mode can be selected by placing the shunts on JR2 between the center and right columns.

3.2 Jumper Settings

3.2.1 JR2 SLIC Control Source

This jumper header allows the SLIC to be controlled by the on-board DIP switches S2 and S3 or by an external AMD SLAC device board via the ribbon cable provided. Each pin and/or switch can be individually selected for internal (DIP switch) or external (DSLAC™/QSLAC) control by changing the JR2 jumpers. The different jumper positions are shown in Figure 3.

Figure 3 JR2 Jumper Options



The default setting of the board as shipped from AMD is the EXTERNAL mode. The functions of each of these jumpers and the corresponding signal pins from the DSLAC and QSLAC device boards is shown in the following table. (Refer to the particular SLAC device data sheet for further explanations of their control pin functions.)

Jumper Row	SLIC Pin	SLAC Device Board Control Pins		P1 Control Header Pin
		QSLAC Device	DSLAC Device	
JR2–1	C1	CD2	C1	1
JR2–2	C2	C3	C2	3
JR2–3	C3	C4	C3	5
JR2–4	E1	MCLK/E1	C4	7
JR2–5	E0	C5	C5 *	9

Note The Am79C02/Am79C031 DSLAC devices have pins C1–C5. The Am79C03 DSLAC device has pins C1–C4 only.

3.2.2 Jumper JR7 and JR8

Two jumpers, JR7 and JR8, are located next to the TIP and RING banana jacks. The two jumpers route the TIP and RING signals to the RJ-11 modular jack (SK1). If these are removed, only the banana jacks will have the output audio signal. The evaluation board is shipped from the factory with these installed.

3.2.3 Jumper JR3

This jumper switches one end of the RTMG resistor from VBAT1 to the VNEG input from the PW1 connector. RTMG helps reduce the on-chip power dissipation in the normal polarity, active state. The default shunt position is from pins 2–3 (VBAT1). However, moving the shunt to pins 1–2 (VTMG) means this requirement must be met from a different source other than the main battery supply. The VTMG source is diode protected.

3.3 DIP Switches S1, S2, and S3

S1 selects between the on board ring trip bridge components and ring relay and external access to the DA, DB, and RINGOUT pins via the corresponding 4 mm banana jack sockets.

S2 controls the operating state of the SLIC inputs (C1, C2, and C3) if internal control is selected via JR2.

S3 controls the E1 and E0 inputs to the SLIC device if internal control is selected via JR2.

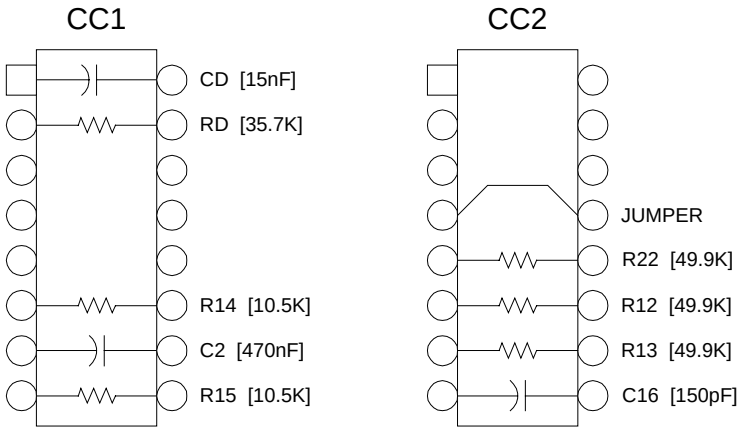
3.4 Component Carriers CC1 and CC2

The two component carriers are designed to accommodate the more commonly changed external components, i.e., the user programmable components.

CC1 carries the DC feed setting components: RDC1 (R15), RDC2 (R14), CDC (C2); and the loop detect threshold setting components: RD (R7) and CD (C1).

CC2 carries the input impedance programming and receive gain-setting components. The header is arranged to allow a variety of configurations to be supported. The default components supplied with the Evaluation Board are designed to provide a nominal 600 Ω two-wire input impedance using a group delay compensated network comprised of RTX1 (R13), RTX2 (R12), CT (C16), and an **open** circuit receive gain of 2.0 via RRX (R22).

Figure 4



3.5 Two-Wire Impedance and Gain Control

Two BNC connectors, V_{TX} and V_{RX}, provide the audio signal I/O paths for the SLIC device. V_{TX} is the direct output of the SLIC pin. V_{RX} is the four-wire input to the impedance circuit between the SLIC and SLAC devices.

Placing the appropriate components on CC2, can program impedance matching. The interface configuration can be as simple as Diagram 1 or as complex as Diagrams 3 and 4. Diagram 2 is the factory default configuration when the board is shipped. The default components supplied with the Evaluation Board are designed to provide a nominal 600 Ω two-wire input impedance using a group delay compensated network and an **open** circuit receive gain of 2.0.

Figure 5 Impedance Matching Network Configuration Diagrams

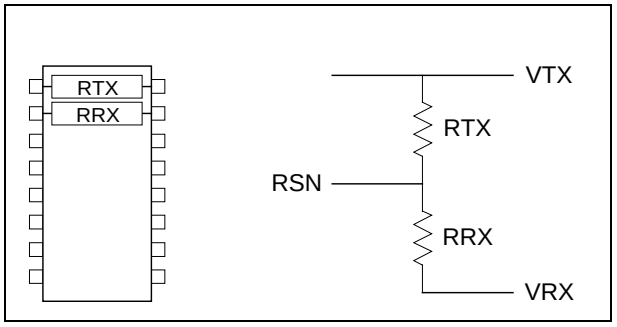


Diagram 1

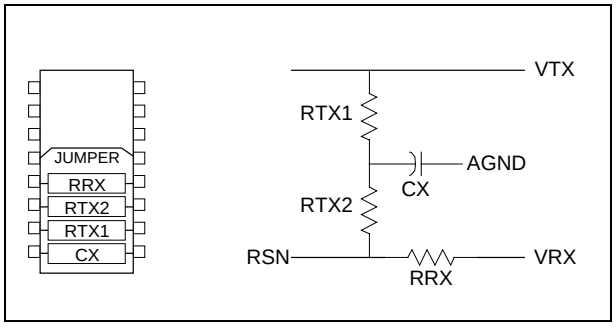


Diagram 2

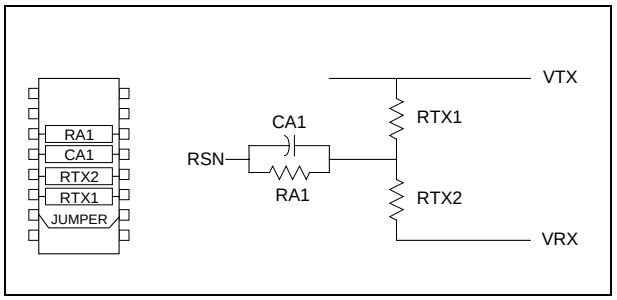


Diagram 3

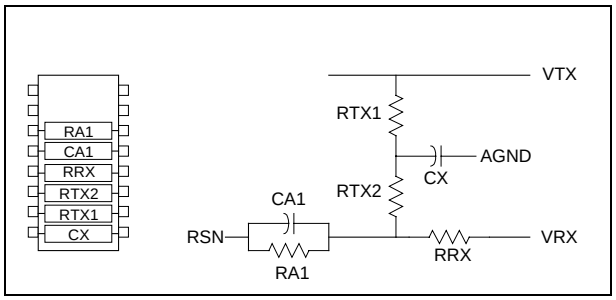


Diagram 4

The component values installed at the factory are calculated using the formulas in the data sheet. The hybrid fuse resistors on the board are 50 Ω each. The G_{42} gain value (i.e., SLIC to phone or four-wire to two-wire) used in the Z_{RX} formula (from the data sheet) is 1.

3.6 Loop Detect Threshold Setting (RD/CD)

The Loop Detect Circuit is a filter composed of a resistor (RD) and capacitor (CD) in parallel with each other and in series with the RD pin. Component values for this circuit are chosen to set the threshold and filter point for the off-hook detector to on-hook transition. Components are mounted on CC1 (refer to Figure 6). The values are derived by the following formula, which is also explained in the device data sheet:

$$C_D = \frac{0.5mS}{R_D}$$

Where: 0.5 mS is the time constant

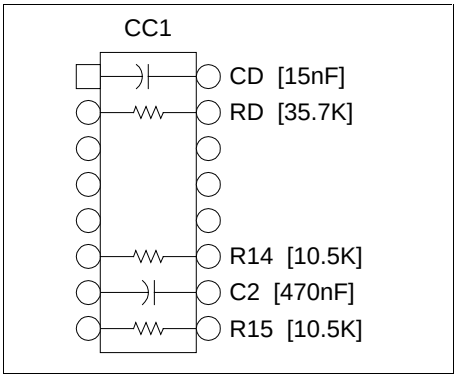
RD is a selected resistance

CD is the calculated capacitive value

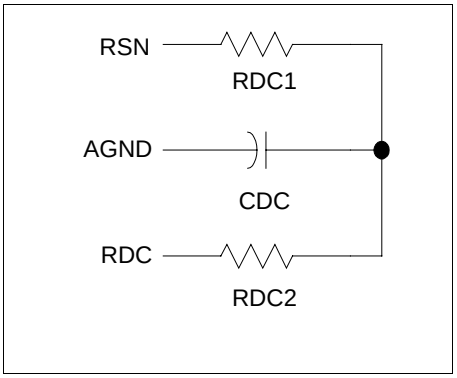
3.7 Battery Feed Control and Setting (RDC1, CDC, RDC2)

The components for the loop current circuit of the evaluation board are set to provide a programmed DC loop current (I_L) of approximately 25 mA. The components for the loop current are located on CC1. The visual placement of components on CC1 and the electrical equivalent circuit are shown in Figure 6. They are shown here to facilitate their identification to the user when being placed on the board.

Figure 6



CC1 Component Carrier



DC Feed Control Circuit

3.8 DA, DB, and RINGOUT Banana Jacks

External DA and DB input signals can be applied to the SLIC via the DA and DB banana jacks when the top two switches of S1 are set to the *switched* position. The banana jacks are incorporated to allow the user to connect to off-board custom-built ringing circuitry. *Please be aware that if the* RINGOUT *signal is switched to this banana jack the user can no longer control the relay K1.*

The Ring Source input from the PW1 connector can be used to supply an off-board ring signal to relay K1. The ring signal is applied to the unbalanced ring circuit composed of resistors R1, R2, R3, R4, R5; and capacitors C12 and C14. The unbalanced ring circuit is used to set the on board DA and DB inputs of the SLIC device.

3.9 LED Indicators

LED indicators are provided to monitor the various SLIC outputs.

LED	On	Off
1	DET Low	DET High
2	RINGOUT Low	RINGOUT High

Each LED indicator resides in parallel with, and is isolated from, the main signal by feeding the signal through a 100 K resistor to the base of an LED drive transistor. Because the transistor requires only a few micro amps to activate or deactivate the LED, it does not present any loading effect.

3.10 Breadboard Area

In order to evaluate the performance of the SLIC device when the application also requires additional circuitry, such as provision for metering (teletax) pulses, a two-square-inch breadboard area and a BNC connector are provided on the evaluation board. The user can use this breadboard area to add whatever external circuitry is desired. For metering applications, the associated BNC connector can be used to directly inject the 12 or 16 kHz teletax pulse signal. The connection can then be closed by shorting across J5, optionally using the breadboard area for any desired control or filtering operation.

As an example of metering: if V_{MG} is the voltage sent into the BNC connector and V_{LM} is the metering voltage required across the subscriber line loaded with Z_{LM}, the equation describing the signal levels is:

$$\frac{V_{LM}}{V_{MG}} = \frac{Z_{LM}}{Z_{LM} + Z_{SLIC}(f) + 2R_F} \times \frac{Zr(f)}{R_M}$$

The value of R_M would depend on the metering signal requirement into the subscriber line, the output voltage of the metering signal source, and the value of the impedance connected across V_{TX} and R_{SN} (Z_T).

In the previous equation, (f) denotes the frequency of the metering signal and Z_{SLIC} is $Z_T/1000$. V_{LM} and Z_{LM} are specified by the PTT or a similar government agency. Z_T is chosen based on the two-wire input impedance requirement and R_F is the fuse resistor. Hence, R_M is directly related to V_{MG}. A suitable notch or low-pass filter to prevent the metering pulses from entering the SLAC can also be installed in the breadboard area.

4.0 SOFTWARE OPERATION

The AMD SLIC evaluation board operates either standalone or in conjunction with an AMD SLAC device evaluation board. The SLIC devices by themselves do not require any software for operation. However, when connected to AMD's SLAC devices, software control is available. Two software families, the WinSLAC™ software and xSLACIFP software, are provided for design and evaluation.

4.1 WinSLAC™ Software

The WinSLAC program is a software tool that aids in the design and development of telephone linecards and related voice band applications. It enables the user to design and generate coefficients for the programmable filters of the AMD SLAC family of devices, and provides the user with predicted performance of system parameters.

The program models the SLAC device, the line conditions and associated linecard SLIC components. It calculates an optimum set of filter coefficients based on the overall system design conditions, and generates the corresponding system responses for each of the programmable functions. It also calculates and plots predicted system responses for Two-Wire Return Loss (2WRL), Four-Wire Return Loss (4WRL), and Receive and Transmit frequency responses.

The WinSLAC program uses gain-phase parameters (G-Parameters) to describe the SLIC circuitry for input to the program. The G-Parameter arrays are typically produced by the program through Spice simulation of the SLIC circuitry. They may also be entered manually, using data obtained by lab measurements on a real SLIC circuit.

In order to generate the G-parameters, the WinSLAC program incorporates and uses an evaluation version of MicroSim Corporation's PSpice and Schematics programs to simulate the analog circuitry of the SLIC. Although the evaluation versions of these programs are sufficient for

most designs, their limitations may impose certain restrictions on more complex designs. In such cases, the full production version of these programs may be purchased directly from MicroSim Corporation, and easily integrated into the WinSLAC program operation.

The WinSLAC software is not required to operate the SLIC evaluation board, but becomes a necessary tool whenever the SLIC board is used in conjunction with an AMD SLAC device in a full evaluation setup.

4.2 SLACIFP Software

The SLACIFP (DSLACIFP, QSLACIFP) software is used to communicate from a user's computer to the SLAC device through the Computer Interface (ACIF) board. It is not necessary for standalone operation of the SLIC board, but like the WinSLAC software, becomes a necessary tool whenever the SLIC board is used in conjunction with an AMD SLAC device in a full evaluation setup.

4.3 SLIC Circuit Simulation Models

As explained above, the WinSLAC software uses gain-phase parameters (G-Parameters) to describe the SLIC circuitry for input to the program. In order to generate the G-parameters, the WinSLAC program incorporates and uses an evaluation version of MicroSim Corporation's PSpice and Schematics programs to simulate the analog circuitry of the SLIC. In order to support this analysis, a simulation model of the SLIC device must be available. The WinSLAC software includes simulation models for each of the AMD SLIC devices. These are very simplified models, intended to produce transmission performance characteristics under limited DC feed conditions. These models are accurate for their intended purpose of transmission band performance representation, but are not intended to accurately represent all SLIC operations.

The text listing of the SLIC model follows.

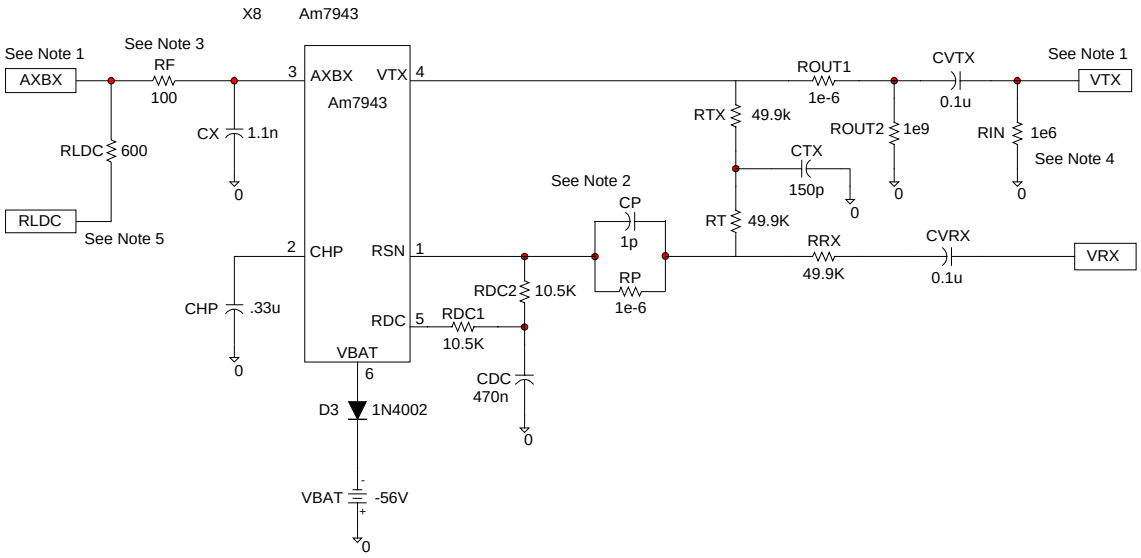
4.4 Am7943 SLIC Device Simulation Model

```
*MODEL FOR AM7943 8/3/95
.SUBCKT AM7943 1 2 3 4 5 6
*DC PATH
EDC 16 0 2 0 1
R11 16 12 20K
VAS 7 0 DC 0 AC 0
HDC 5 0 VAS 10K
IAPP 0 7 .25M
Q1 10 10 0 NPN
Q3 7 9 12 NPN
IASB 0 10 100U
EAS2 9 10 POLY(1) 6 0 9.3 1.0
RB 6 0 2K

VFSENSE 1 0 0
F1 13 0 VFSENSE 205.5
R1 13 3 36
RNOFLT 13 0 100MEG
C0 13 0 11.5N

*AC PATH
ETX 14 0 3 2 1.0
R3 3 2 463K
R2 14 4 1
C2 4 0 455N

D1 3 0 DIODE
D2 6 3 DIODE

.MODEL NPN NPN IS=1E-14
.MODEL DIODE D IS=1E-14
.ENDS AM7943
```

4.5 Example Schematic Circuit

The SLIC device must be included in a top-level analog circuit that represents the entire analog front end of the linecard design. This circuit must include all circuit elements between tip/ring and the analog input/output connections of the connected SLAC device. A basic circuit is included with the WinSLAC software, and the MicroSim Schematics program allows editing of this circuit for updating user-selected component values or adding optional circuitry. The default circuit provided with the program is shown in Figure 7.

Figure 7



Notes:

1. *Do **not** change the names of the offpage connectors (TIP, RING, VTX, and VRX). Doing so will interfere with the creation of G-parameters.*
2. *The default values may or may not be the proper values for a given SLIC. Refer to Note 1 in the datasheet for default values.*
3. *Because this model combines the TIP and RING into one pin, RF should be twice the value of your fuse resistance and CX should be half.*
4. *RIN is internal to the QSLAC device.*
5. *RLDC establishes the DC operating point of the SLIC. This resistor **has no effect** on transmission performance and therefore we recommend it not be changed.*

The PSpice circuit shown previously has the default values (as shipped from the factory) for the impedance matching circuit and the loop current circuit for the Am7943/44/45 SLIC device. The loop current components (RDC1, RDC2, and CDC) are chosen to provide a loop current of approximately 25 mA.

While the drawing above references the Am7943, it is applicable to the Am7944 or the Am7945 when using the “Create Schematic” option from the WinSLAC program.

5.0 REPRESENTATIVE TRANSMISSION PERFORMANCE

Some typical transmission performance measurements have been taken with the Am7943/44/45 SLIC connected to the AMD Am79Q021 QSLAC device.

The conditions for these measurements are:

QSLAC Device	Rev. D1
Am7943 SLIC device	Rev. 6J
Am7943 SLIC model date	08/03/95
BAT	–56 V
SLIC State	ACTIVE

The measured results will be approximately:

VAB(SLIC)	14.09 VDC
IAB	26.08 mA

The default (as shipped) evaluation board component values for the circuit were used. These values are:

Component	Value
RRX	49.9K
RT1	49.9K
RT2	49.9K
CT	150 pF
RF	100 Ω (50 Ω each)
RDC1	10.5K
RDC2	10.5K
CDC	470 nF

Three typical line conditions were used for these measurements. These are common values and one or more of these impedances is typically available in most telecom test instrumentation, making it relatively easy to directly hook up to the evaluation board as a setup verification exercise. These impedance conditions are:

- 600 Ω line
- 900 Ω line
- German complex impedance line

For each of these three conditions, graphs of two-wire return loss, four-wire return loss, and receive and transmit path attenuation distortion are provided. These can be compared to actual lab measurements during verification testing.

5.1 600 Ω Line (Default)

All programmable filters of the QSLAC device, except the Balance Filter, were disabled for this condition. The QSLAC device has the capability of altering the programmed two-wire impedance, frequency response, and path gains. By disabling these functions, the performance measurements represent pure SLIC-only operation. The balance filter was left enabled because it performs the hybrid balance function of the complete solution, and without this, four-wire return loss measurements are meaningless.

When using the WinSLAC coefficient calculation program, the following table shows, by main menu items and sub-menu items, what the required filter settings should be for the generation of coefficients.

Main Menu Item	Sub-menu	Set
System:	Desired Impedance:	ZD = to 600
	Line Impedance:	ZL = to 600
SLAC:	AISN & Z Filter:	AISN to disabled
		Ziir & Zfir to disabled
SLAC:	R & X Filters/Gain Blocks:	X & R to 1
		GX & GR to 0.0
		AX & AR to 0.0
SLAC:	B Filter & Adaptive Balance:	B to calculate

Figure 8 600 Ω Line Two-Wire Return Loss Performance

Figure 9 600 Ω Line Four-Wire Return Loss Performance

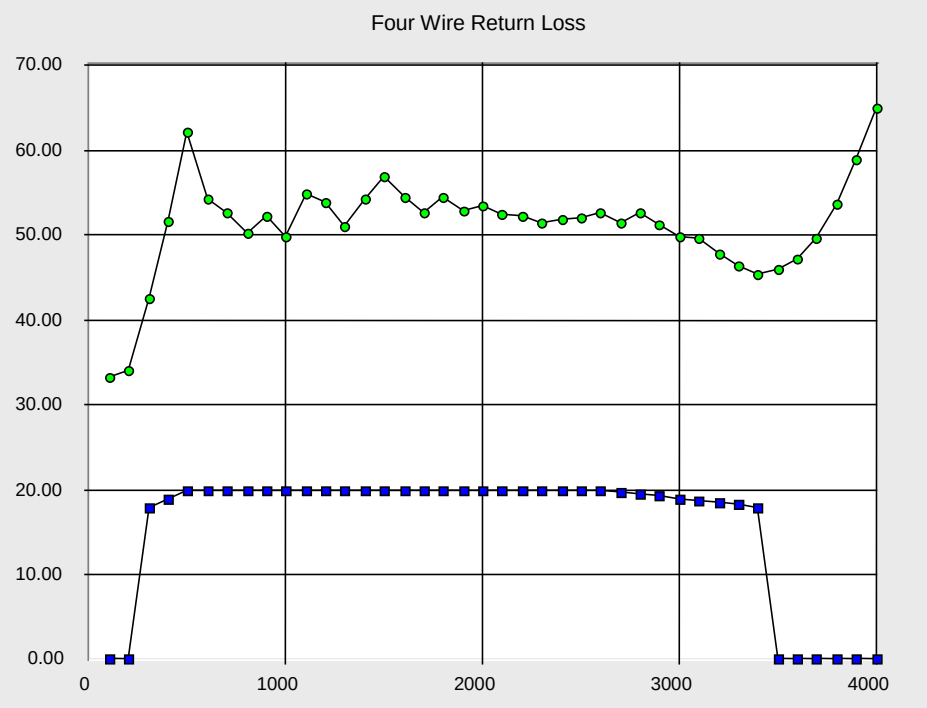


Figure 10 600 Ω Line Receive Path Attenuation Distortion Performance

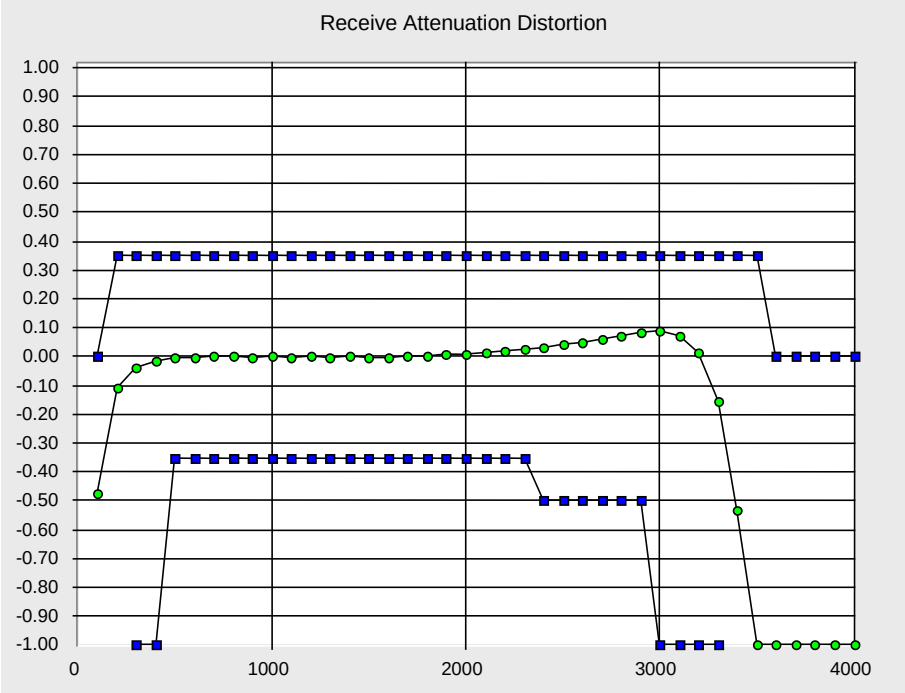
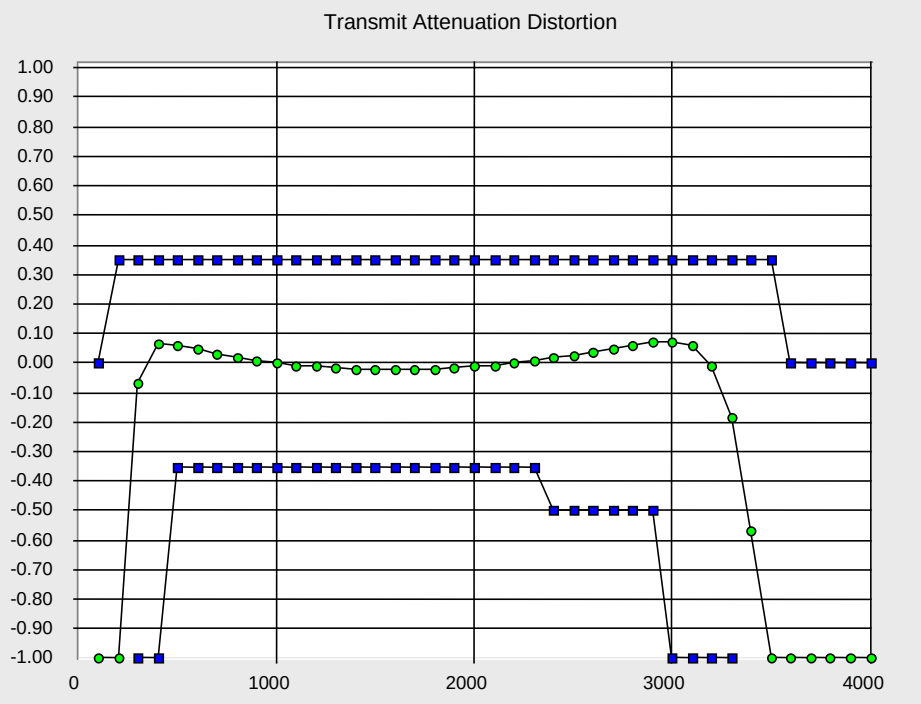


Figure 11 600 Ω Line Transmit Path Attenuation Distortion Performance



5.2 900 Ω Line

All programmable filter blocks of the QSLAC device were enabled, except AX and AR, which were set to 0 dB gain each. The two-wire and balance impedances were specified as 900 Ω and the WinSLAC program computed programmed coefficients to meet this line condition.

When using the WinSLAC coefficient calculation program, the following table shows, by main menu items and sub-menu items, what the required filter settings should be for the generation of coefficients.

Main Menu Item	Sub-menu	Set
System:	Desired Impedance:	ZD = to 900
	Line Impedance:	ZL = to 900
SLAC	AISN & Z Filter:	AISN to calculate
		Ziir & Zfir to calculate
SLAC	R & X Filters/Gain Blocks:	X & R to calculate
		GX & GR to calculate
		AX & AR to 0.0
SLAC	B Filter & Adaptive Balance:	B to calculate

Figure 12 900 Ω Line Two-Wire Return Loss Performance

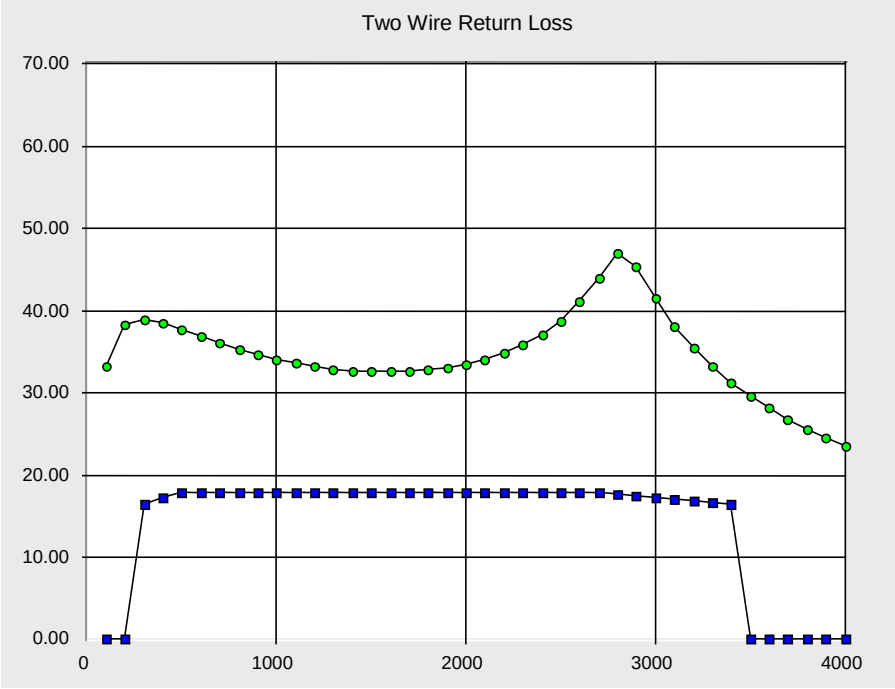


Figure 13 900 Ω Line Four-Wire Return Loss Performance

Figure 14 900 Ω Line Receive Path Attenuation Distortion Performance

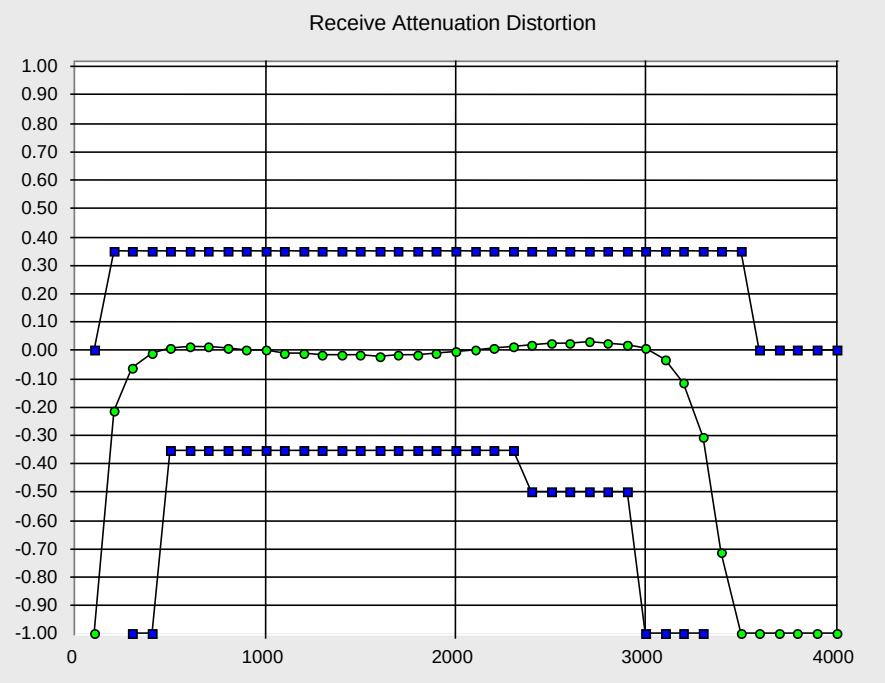
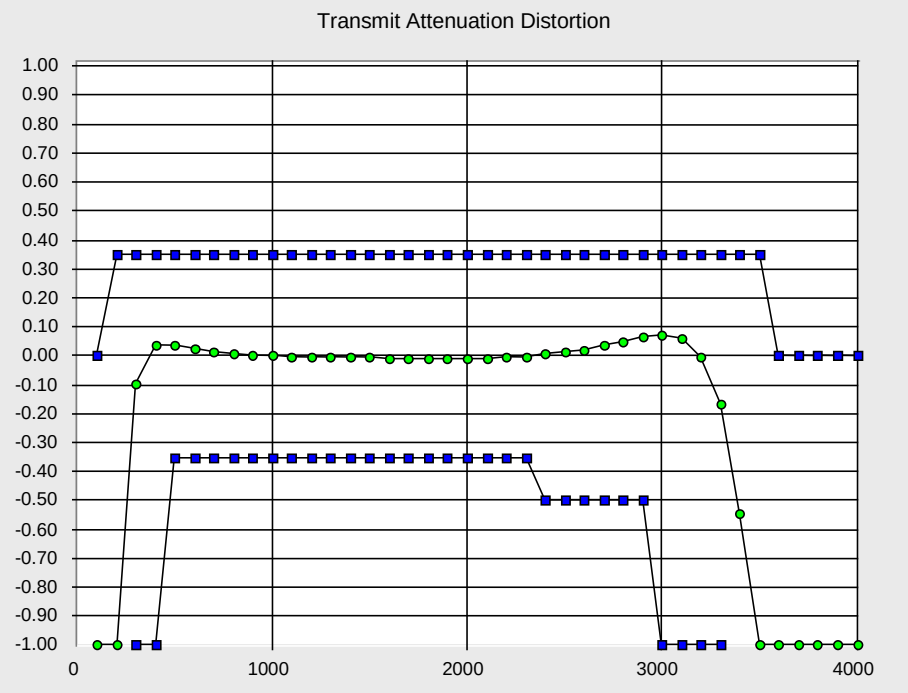


Figure 15 900 Ω Line Transmit Path Attenuation Distortion Performance



5.3 German Line

All programmable filter blocks of the QSLAC device were enabled, except AX and AR, which were set to 0 dB gain each. The two-wire and balance impedances were specified as the German complex impedance (220 Ω in series with a parallel RC network of 820 Ω and 115 nF) and the WinSLAC program computed programmed coefficients to meet this line condition.

When using the WinSLAC coefficient calculation program, the following table shows, by main menu items and sub-menu items, what the required filter settings should be for the generation of coefficients.

Main Menu Item	Sub-menu	Set
System:	Desired Impedance:	ZD = to Complex impedance shown below.
	Line Impedance:	ZL = to Complex impedance
		Shown below
SLAC	AISN & Z Filter:	AISN to calculate
		Ziir & Zfir to calculate
SLAC	R & X Filters/Gain Blocks:	X & R to calculate
		GX & GR to calculate
		AX & AR to 0.0
SLAC	B Filter & Adaptive Balance:	B to calculate

For the complex impedances, the values were entered in S-polynomial format. The formula used is:

$$Z=\frac{1040+(2.0746E^{-2})s}{1+(9.43E^{-5})s}$$

The representative circuit is:

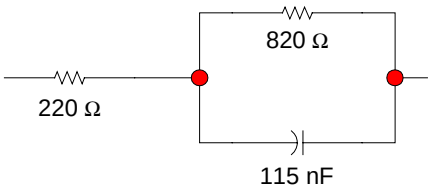


Figure 16 German Complex Line Two-Wire Return Loss Performance

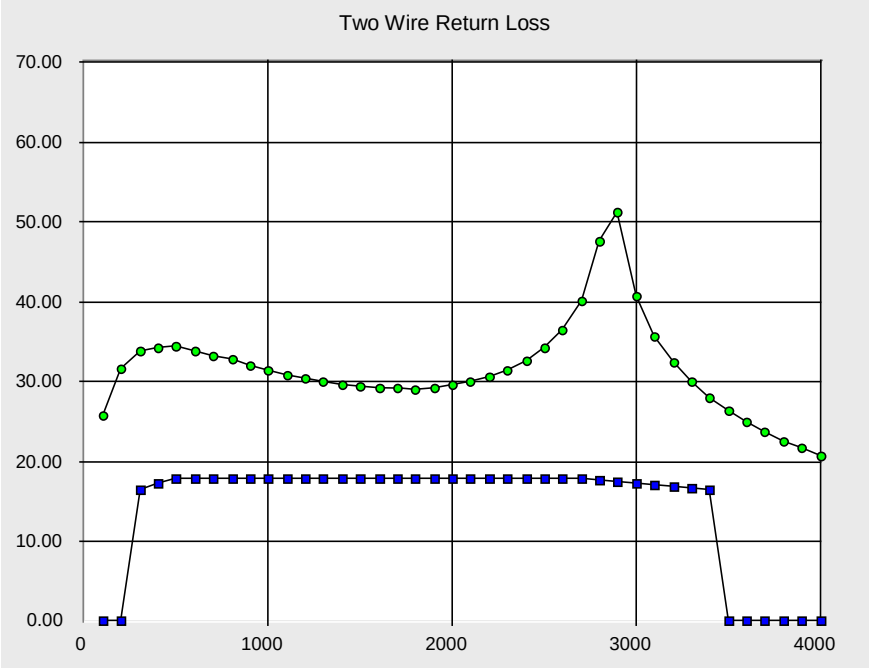


Figure 17 German Complex Line Four-Wire Return Loss Performance

Figure 18 German Complex Line Receive Path Attenuation Distortion Performance

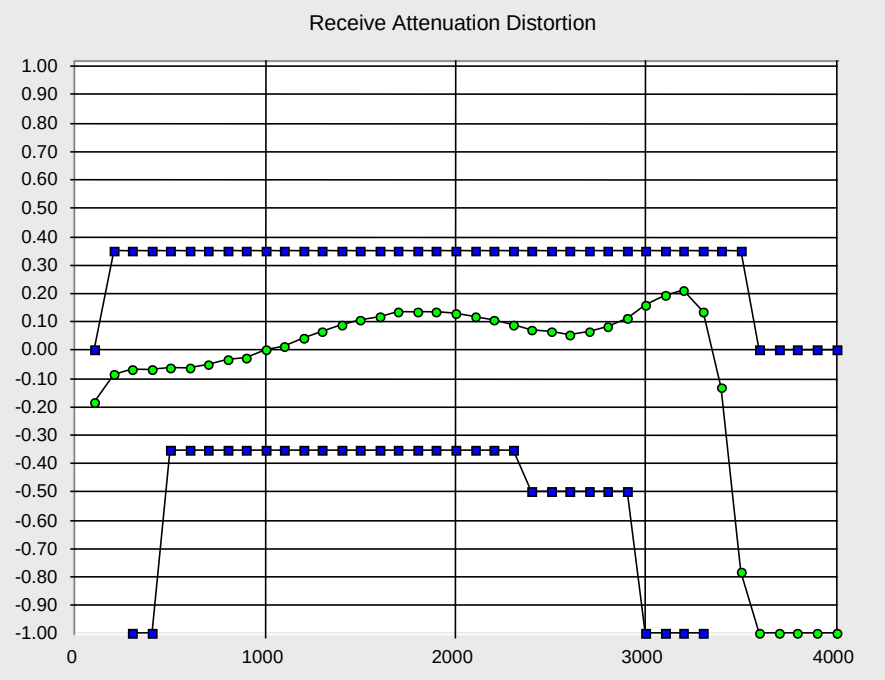
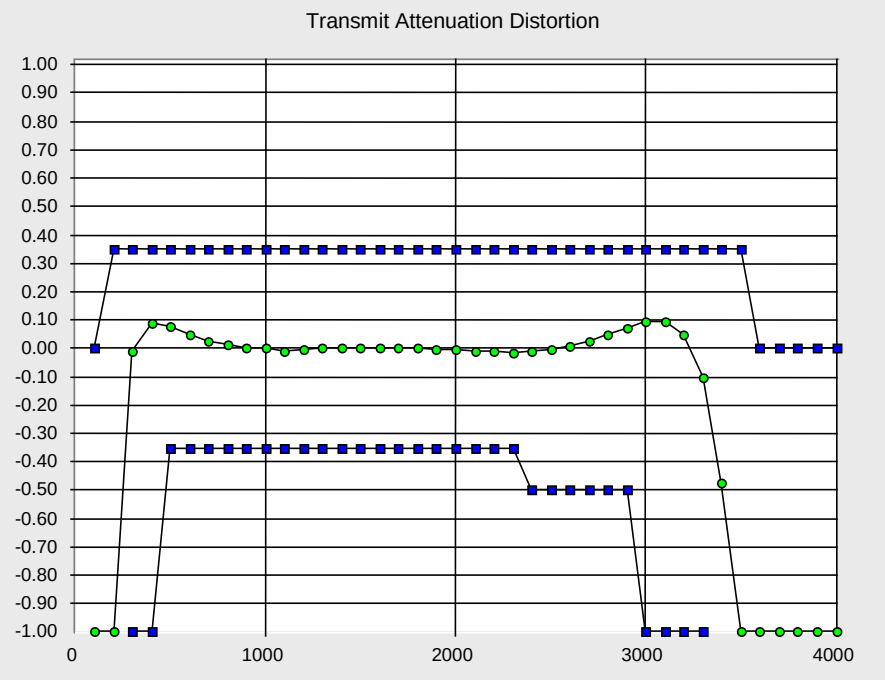


Figure 19 German Complex Line Transmit Path Attenuation Distortion Performance



6.0 EVALUATION BOARD STANDALONE OPERATIONAL TEST

6.1 Am7943/44/45 Standalone Test Procedure

This section explains a simple setup to verify proper functionality of the SLIC Evaluation Board. This procedure uses the default values [refer to the schematic] when the board is shipped. If any modifications have been made to the board, output voltage reading may vary from those described in this document. Equipment needed for this test is:

1. A dual channel oscilloscope.
2. A function Generator.
3. Power supplies: +5, –5, and VBAT supply.

Check that all supplies are turned off while making power supply connections. *Please note that all ground connections must terminate at the power supply.*

1. Connect VCC to +5 Vdc.
2. Connect VEE to –5 Vdc.
3. Connect V_{BAT} to the battery supply [set the supply to a –48 V].
4. Connect the ground/common inputs of all supplies and the evaluation board [AGND and BGND] together. Remember to keep all grounds terminated at one of the power supplies.
5. Set all three switches on S1 to Normal.
6. Move all jumpers on JR2 to the Internal or standalone mode and set the switches on S2 and S3 to [Table 1 lists all decoding states for the SLIC device]:
   - C1 = 0
   - C2 = 1
   - C3 = 0
   - E0 = 1
   - E1 = 1
7. Connect a standard telephone station to SK1.
8. Connect a signal generator to the Receive [V_{RX}] input and one channel of the o'scope. Set the output of the generator to a 1 V p/p sine wave @ 1 kHz.
9. Connect the second channel of the o'scope to the V_{TX} output.
10. Check all connections and turn on the power supplies.

After step 10, there will be 1.1 V p/p sine wave riding on approximately 6 Vdc signal between TIP and RING of the on-hook telephone. The same 1.1 V p/p signal [minus the dc voltage] will be at the Transmit [V_{TX}] output. If a standard telephone is connected to SK1 on the board, an audible tone can be heard when the receiver is lifted. A 180°-phase shift will occur between V_{TX} and V_{RX}.

6.2 Test Setup to Verify Ringing

The ringing on the PLCC Evaluation Board is based on an unbalanced ringing source. The ringing voltage can be supplied via the RING_SOURCE banana jack. To use the ringing circuit:

1. Place the S1 switches in the Normal position.
2. Connect a ringing source to the RA and RB banana jacks.
3. Connect the RING_SOURCE banana jack to the ringing signal source.
4. Set the S2 and S3 switches as follows (JR2 shunted to the left sets the board in the standalone mode):
   - C1 = 1 to activate the ring relay
   - C2 = 0
   - C3 = 0
   - E0 = 1
   - E1 = 1

As C1, C2, and C3 are set to their logic levels [1, 0, 0], an audible click will be heard, indicating the relay is activated. If an on-hook telephone is connected across the TIP and RING leads (or through connector SK1, the RJ-11-type phone connector), the phone will ring. To deactivate the ringing set, switch C1 to 0.

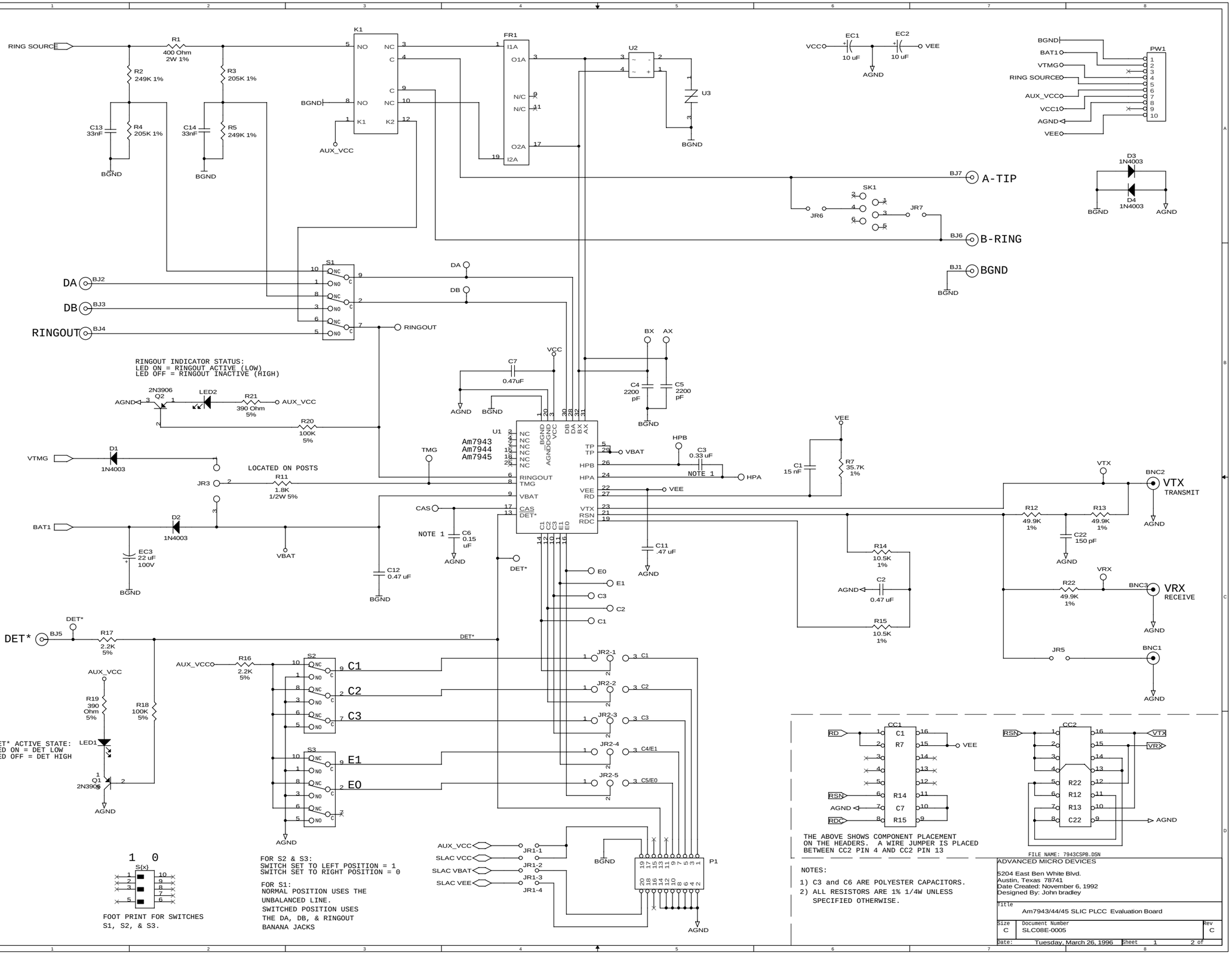
Table 1 Am7943/44/45 SLIC Decoding State

State	C3 C2 C1	2-Wire Status	(DET) Output	
			E1 = 1	E1 = 0
0	0 0 0	Open circuit	Ring Trip	Ring Trip
1	0 0 1	Ringing	Ring Trip	Ring Trip
2	0 1 0	Active	Loop Detector	Ground Key
3	0 1 1	On-hook TX (OHT)	Loop Detector	Ground Key
4	1 0 0	Tip open	Loop Detector	Ground Key
5	1 0 1	Standby	Loop Detector	Ground Key
* 6	1 1 0	Active polarity reversal	Loop Detector	Ground Key
* 7	1 1 1	OHT polarity reversal	Loop Detector	Ground Key

** For the Am7944 and Am7945, decoding states 6 and 7 are reserved. Refer to data sheet for specific part.*

7.0 EVALUATION BOARD SCHEMATIC

See the attached fold-out page.


RING SOURCE
R1 400 Ohm 2W 1%
R2 249K 1%
R3 205K 1%
C13 33nF
R4 205K 1%
C14 33nF
R5 249K 1%
BGND
K1
AUX_VCC
FR1
U2
U3
EC1 10 uF
EC2 10 uF
VCC
VEE
AGND
PW1
BGND
BAT1
VTMG
RING SOURCE
AUX_VCC
VCC1
AGND
VEE
D3 1N4003
D4 1N4003
BJ7 A-TIP
SK1
JR6
JR7
BJ6 B-RING
BJ1 BGND
DA
DB
RINGOUT
BJ2
BJ3
BJ4
S1
RINGOUT INDICATOR STATUS:
LED ON = RINGOUT ACTIVE (LOW)
LED OFF = RINGOUT INACTIVE (HIGH)
2N3906 Q2
LED2
R21 390 Ohm 5%
R20 100K 5%
C7 0.47uF
VCC
BX
AX
C4 2200 pF
C5 2200 pF
U1
Am7943
Am7944
Am7945
D1 1N4003
LOCATED ON POSTS
JR3
R11 1.8K 1/2W 5%
TMG
VBAT
CAS
DET*
NOTE 1
C6 0.15 uF
D2 1N4003
EC3 22 uF 100V
C12 0.47 uF
C11 .47 uF
HPB
HPA
VBAT
C3 0.33 uF
NOTE 1
C1 15 nF
R7 35.7K 1%
R14 10.5K 1%
C2 0.47 uF
R15 10.5K 1%
VTX
BNC2
VTX TRANSMIT
R12 49.9K 1%
R13 49.9K 1%
C22 150 pF
VRX
BNC3
VRX RECEIVE
R22 49.9K 1%
JR5
BNC1
DET*
BJ5
R17 2.2K 5%
R16 2.2K 5%
AUX_VCC
R19 390 Ohm 5%
R18 100K 5%
LED1
Q1 2N3906
DET* ACTIVE STATE:
LED ON = DET LOW
LED OFF = DET HIGH
S2
S3
C1
C2
C3
E1
E0
JR2-1
JR2-2
JR2-3
JR2-4
JR2-5
C4/E1
C5/E0
S{x}
FOOT PRINT FOR SWITCHES S1, S2, & S3.
FOR S2 & S3:
SWITCH SET TO LEFT POSITION = 1
SWITCH SET TO RIGHT POSITION = 0
FOR S1:
NORMAL POSITION USES THE UNBALANCED LINE.
SWITCHED POSITION USES THE DA, DB, & RINGOUT BANANA JACKS
JR1-1
JR1-2
JR1-3
JR1-4
SLAC VCC
SLAC VBAT
SLAC VEE
P1
CC1
CC2
THE ABOVE SHOWS COMPONENT PLACEMENT ON THE HEADERS. A WIRE JUMPER IS PLACED BETWEEN CC2 PIN 4 AND CC2 PIN 13
NOTES:
1) C3 and C6 ARE POLYESTER CAPACITORS.
2) ALL RESISTORS ARE 1% 1/4W UNLESS SPECIFIED OTHERWISE.
FILE NAME: 7943CSPB.DSN
ADVANCED MICRO DEVICES
5204 East Ben White Blvd.
Austin, Texas 78741
Date Created: November 6, 1992
Designed By: John bradley
Title
Am7943/44/45 SLIC PLCC Evaluation Board
Size C
Document Number SLC08E-0005
Rev C
Date: Tuesday, March 26, 1996
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