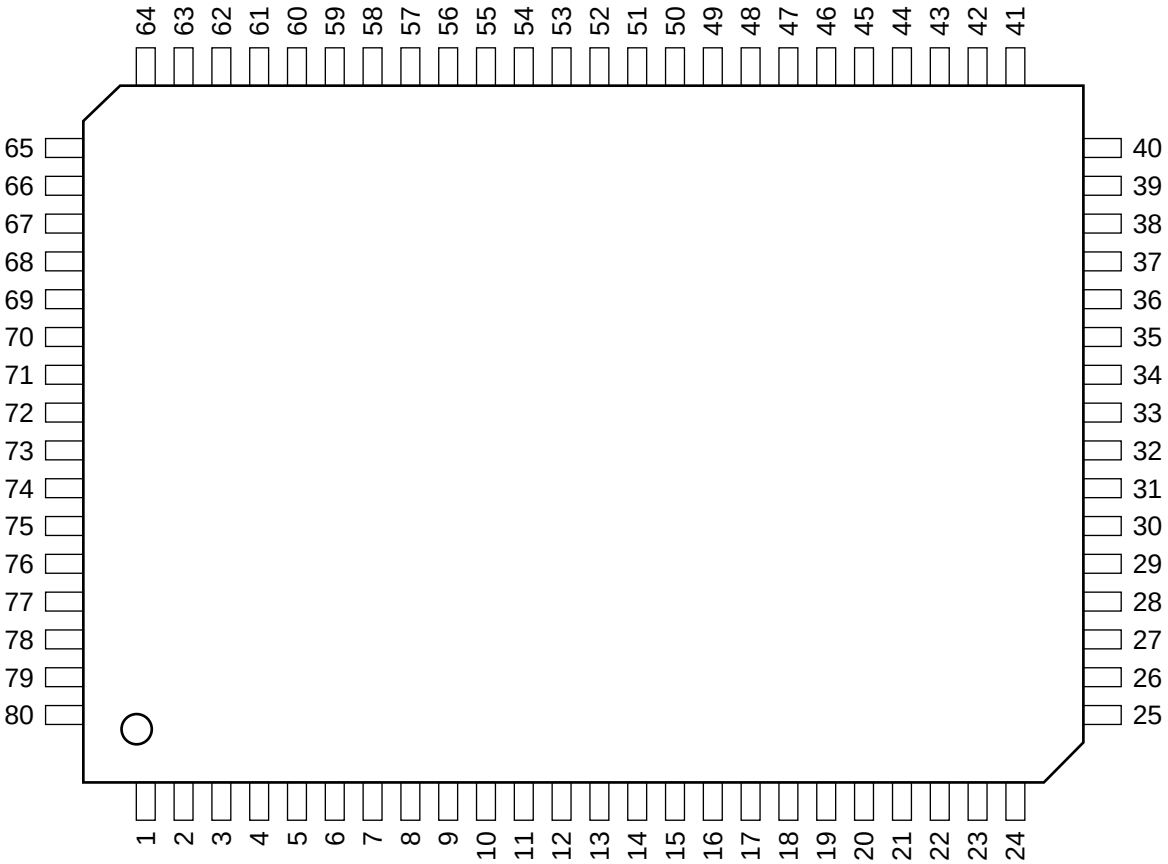
VIDEO SIGNAL PROCESSOR FOR BETACAM

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	RD0	21	I	BD8	41	—	NC	61	—	NC
2	I	RD1	22	—	GND	42	—	GND	62	I	COFF
3	I	RD2	23	O	TM0	43	O	CTD0	63	O	FP1
4	I	RD3	24	O	TM1	44	O	CTD1	64	O	FP2
5	I	RD4	25	O	TM2	45	O	CTD2	65	I	CFFD
6	I	RD5	26	O	TM3	46	O	CTD3	66	I	CFID
7	I	RD6	27	O	TM4	47	O	CTD4	67	I	VO
8	I	RD7	28	O	TM5	48	O	CTD5	68	I	BLK2
9	I	RD8	29	O	TM6	49	O	CTD6	69	O	SH
10	I	TSL2	30	O	TM7	50	O	CTD7	70	I	CLPI
11	I	TSL3	31	O	TM8	51	O	CTD8	71	I	CLPO
12	—	GND	32	O	TM9	52	—	GND	72	I	XRST
13	I	BD0	33	I	V_{DD}	53	—	NC	73	I	V_{DD}
14	I	BD1	34	I	TMOD	54	—	NC	74	I	TST1
15	I	BD2	35	I	TMEN	55	—	NC	75	I	TST2
16	I	BD3	36	I	TSL1	56	—	NC	76	I	ZSHT
17	I	BD4	37	I	BLK1	57	—	NC	77	I	RCK
18	I	BD5	38	I	MODE1	58	—	NC	78	I	WCK
19	I	BD6	39	I	MODE2	59	—	NC	79	I	RZERO
20	I	BD7	40	I	MODE3	60	—	NC	80	I	WZERO

INPUTS

BD0 - BD8 : B-Y DATA
BLK1, BLK2 : BLKG PULSE
CFFD : FIELD SIGNAL INPUT FOR COLOR FRAMING ID MIX
CFID : PULSE INPUT FOR COLOR FRAMING ID MIX
CLPI : CLAMP PULSE INPUT FOR DIGITAL CLAMP
COFF : DIGITAL CLAMP CIRCUIT CONTROL
MODE1 - MODE3 : MODE SELECT
RCK : READ CLOCK
RD0 - RD8 : R-Y DATA
RZERO : READ ZERO
SH : TRIGGER FOR CLPO
TMEN : MEMORY ADD CONTROL INPUT IN TEST MODE
TMOD : TEST MODE CONTROL
TSL1 : MEMORY SELECT INPUT IN TEST MODE
TSL2, TSL3 : TEST
TST1, TST2 : DIGITAL CLAMP CIRCUIT TEST CONTROL
VO : COLOR FRAMING DETECT CIRCUIT RESET PULSE
WCK : WRITE CLOCK
WZERO : WRITE ZERO
XRST : DIGITAL CLAMP CIRCUIT RESET PULSE
ZSHT : INTERNAL/EXTERNAL WZERO SELECT

OUTPUTS

CLPO : CLAMP PULSE
CTD0 - CTD8 : CTDM DATA
FP1, FP2 : COLOR FRAMING DETECT PULSE
TM0 - TM9 : DIGITAL CLAMP CIRCUIT TEST SIGNAL

MODE1	1				1			
MODE2	1		0		1		0	
MODE3	1	0	1	0	1	0	1	0
nfH	910fH	858fH	909fH	×	908fH	864fH	1135fH	TCLR

0 : LOW LEVEL 1 : HIGH LEVEL